

VDD_SOC_IN 0.925 - 1.3V
Power for the core supply

VDD_HIGH_IN 3.0 - 3.6V
VDD_HIGH_IN supply voltage

DCDC_IN 3.0 - 3.6V
Power for the DCDC

VDD_SNVS_IN 2.4 = 3.6V
Power for the SNVS and RTC

USB_OTG1_VBUS 4.4 - 5.5V
Power for the USB VBUS

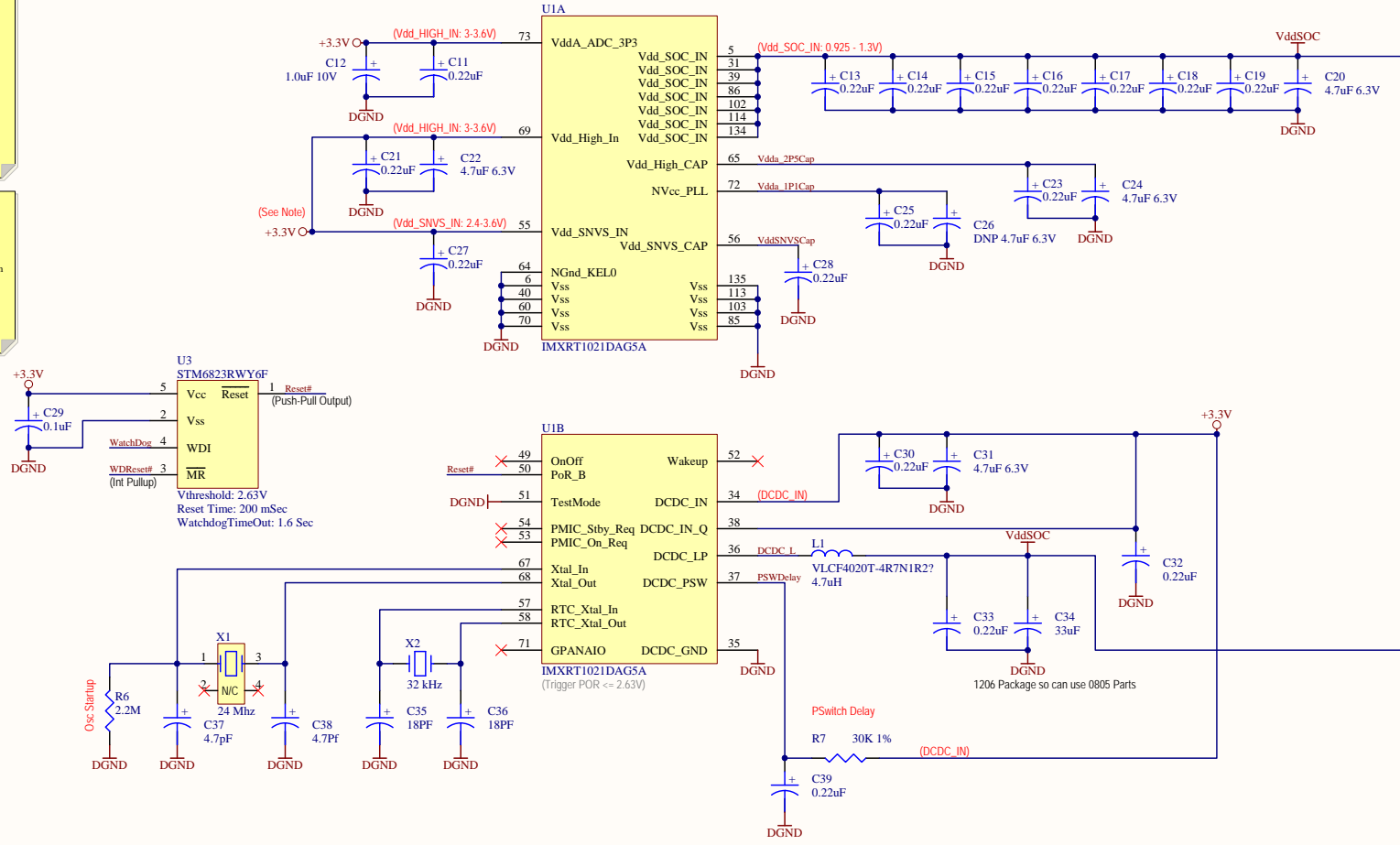
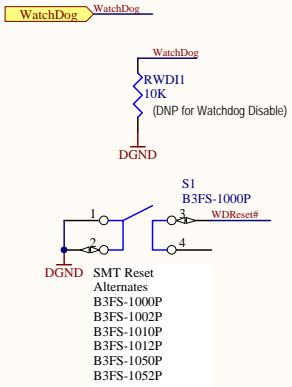
VDDA_ADC_3P3 3.0 - 3.6V
Power for the 12-bit ADC

NVCC_SD0
Power for the GPIO in the SDIO1 bank (3.3 V mode) 3.0 - 3.6V
Power for the GPIO in the SDIO1 bank (1.8 V mode) 1.65 - 1.95V

NVCC_GPIO 3.0 - 3.6V
IO power for the GPIO

Power Up Sequence Requirement

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on
- When internal DCDC is enabled, external delay circuit is required to delay the DCDC_PSWITCH signal at least 1 ms after DCDC_IN is stable
- POR_B must be held low during the entire power up sequence



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