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10	PDM & I2S MIC MAIN-EXT

REVISION HISTORY

REVISION	DESCRIPTION OF CHANGE	DATE	Author	Reviewer
A	Prototype Release	03-June-22	CBC	Vincent FILLATRE
A1	Production X- Release BOM Update: L60 -> 7442335900 U205, U207, U208, U212, U213 -> 74AUP1T34GW,125 J60 -> Default 1:2	16-June-22	CBC	Vincent FILLATRE
A2	Production Pilot Release BOM Update: R322 --> 180K (APN# 470-78122) R323 --> Populated J63 --> Jumper Default Pos: 2-3	10-October-22	CBC	Vincent FILLATRE
A3	Production Pilot Release BOM Update: Default configuration = 3 x I ² S MICs U209, U210 and U211 ACTIVE R228, R368, R222 --> DNP R243, R367, R365 --> 0 Ohm APN# 470-80866	04-Nov-22	CBC	Vincent FILLATRE
A4	U5 --> W25Q256JWEIQ	14-Nov-22	CBC	Vincent FILLATRE
A5	U4 --> 330-77237 / MFG_PN# MIMXRT106VDVL6B	19-Dec-22	CBC	Vincent FILLATRE

Do Not Populate

REF DES	ASSY OPT	PAGE NAME
C22, C221, R13, R317, Y3	DNP	03 Power Section
R215, R216	DNP	04 i.MXRT Section
C277, R14, R30, R264, R273, R274, R275, R276, R277, R286, R382, R383	DNP	05 Memory Section
C61, C62, C63, C66, C67, C68, D1, R72, R74, R75, R218, R302, R330, R331, R332, R333, R334, R335, R346, R347, R348, R349, R357, R361, R376, R378, R380	DNP	06 Wi-Fi & BT/BLE/M2 Section
R22, R23, R32, R40, R41	DNP	07 BOOT & Debug Interfaces
R45, R46	DNP	09 Audio Amplifier EXT
R49, R222, R226, R228, R238, R240, R242, R244, R368	DNP	10 PDM & I2S MIC MAIN-EXT

SLN-SVUI-IOT

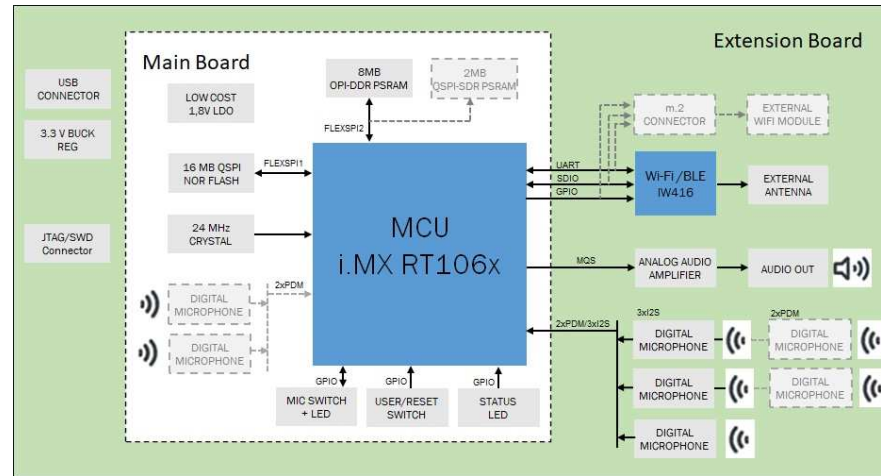
Default Jumpers

REF DES	JUMPER	PAGE NAME
J60	Default 1:2	03 Power Section
J61	Default 1:2	07 BOOT & Debug Interfaces
J63	Default 2:3	07 BOOT & Debug Interfaces

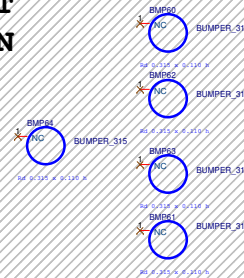


EAP Classification: CP:		IUC:		PUB:	
Drawing Title: SLN-SVUI-IOT					
Page Title: Cover Page					
Size C	Document Number	SPF-55324 SCH-55324	Rev	AS	
Date:	Monday, December 19, 2022	Sheet	1 of 10		

Block Diagram



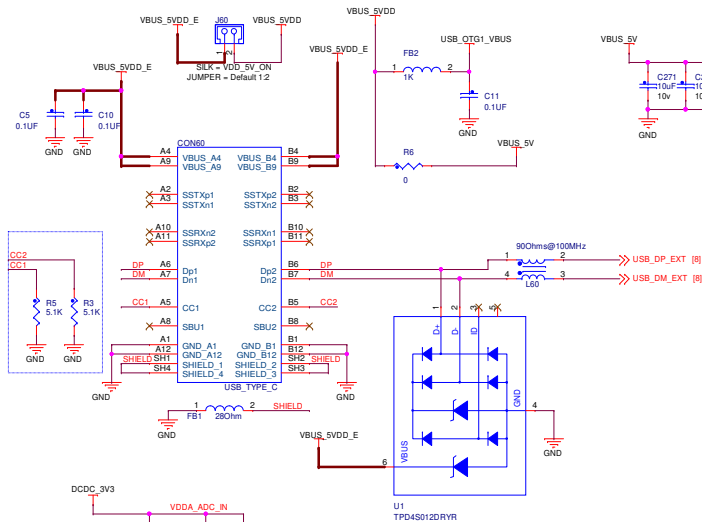
57 mm X 127 mm PCB EXT
57 mm X 38 mm PCB MAIN



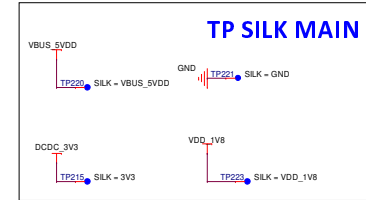
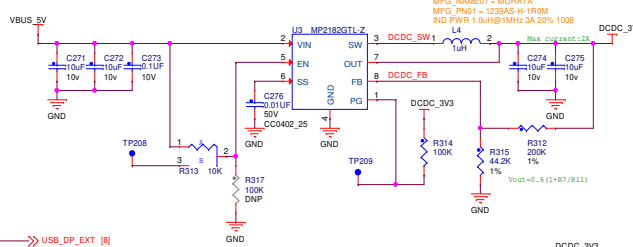
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Drawing Title: SLN-SVUI-HOT			
Page Title: Block Diagram			
Size C	Document Number	SPF-55324 SCH-55324	Rev AS
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iMXRT Connected Module Power Section

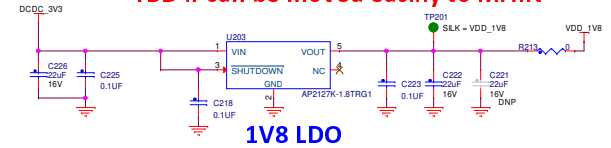
USB Type C Connector



System 3.3V DCDC



TBD if can be moved easily to MAIN



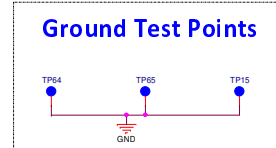
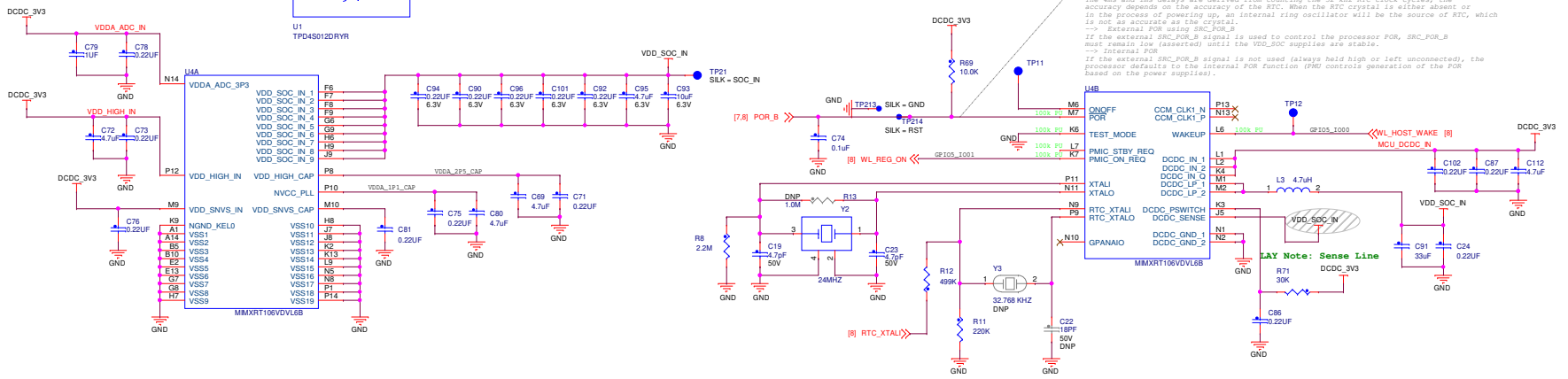
The SRC module generates an internal POR_B signal that is logically AND'ed with any externally applied SRC_POR_B signal. The internal POR_B signal will be held low until all of the following conditions are met:

- +4ms after the external power supply VDDHIGH_IN is valid
- +1ms after the VDD_SNC_IN supply is valid
- The dms and lms delays are derived from counting the 32 kHz RTC clock cycles; the accuracy depends on the accuracy of the RTC. When the RTC crystal is either absent or in the process of powering up, an internal ring oscillator will be the source of RTC, which is not as accurate as the crystal.
- > External POR using SRC_POR_B

If the external SRC_POR_B signal is used to control the processor POR, SRC_POR_B must remain low (asserted) until the VDD_SNC supplies are stable.

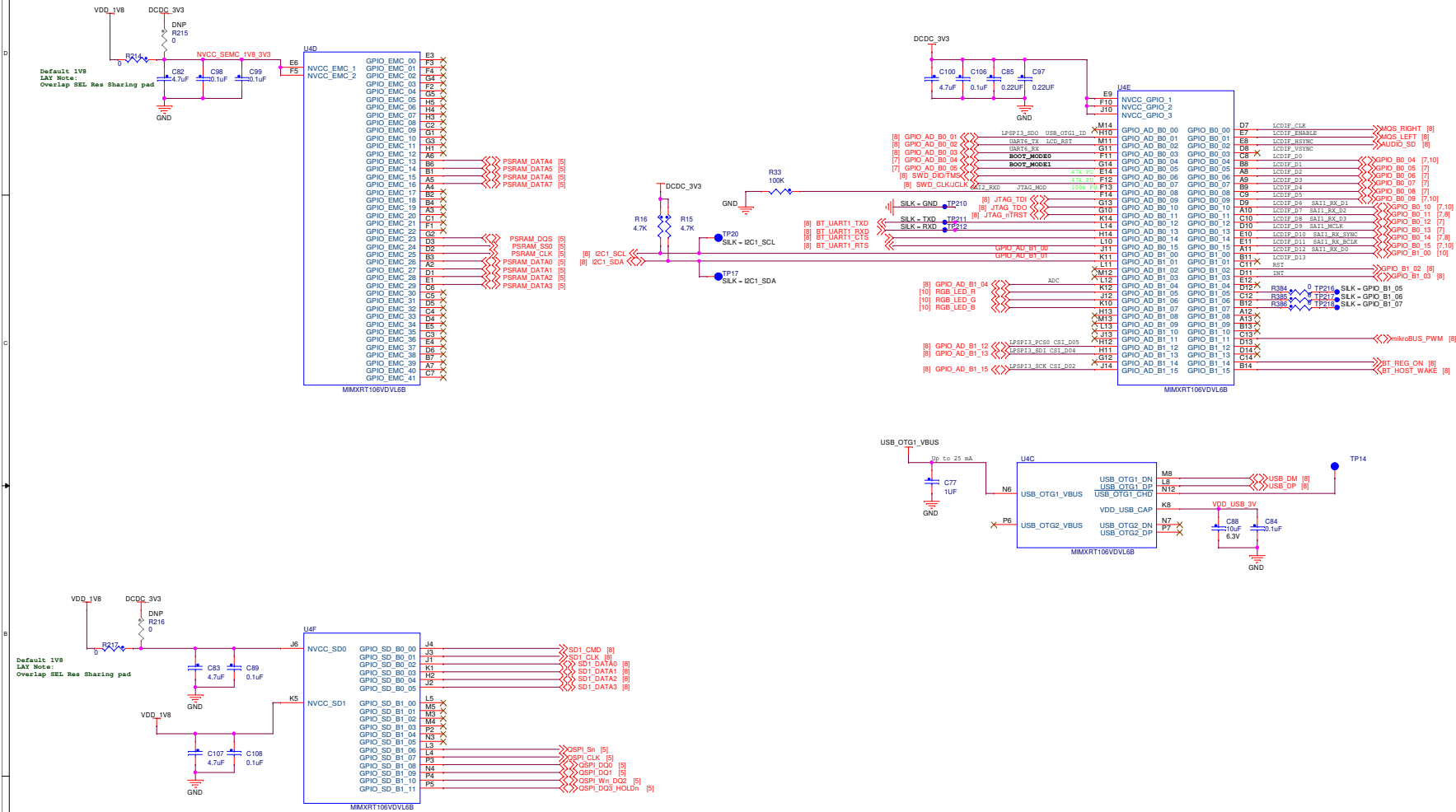
-> Internal POR

If the external SRC_POR_B signal is not used (always held high or left unconnected), the processor defaults to the internal POR (always held high or left unconnected), the processor controls generation of the POR based on the power supplies.



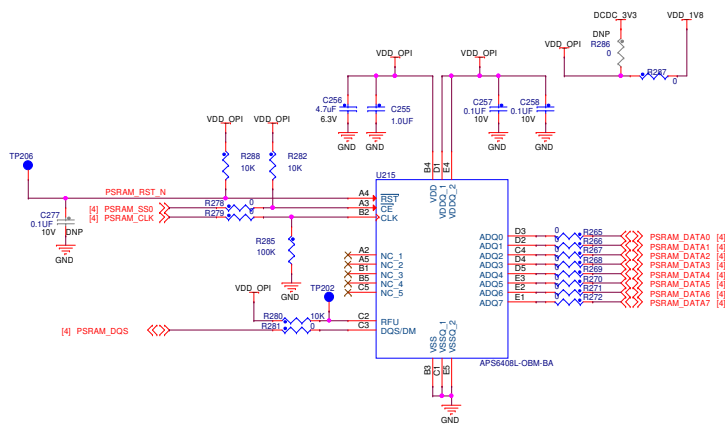
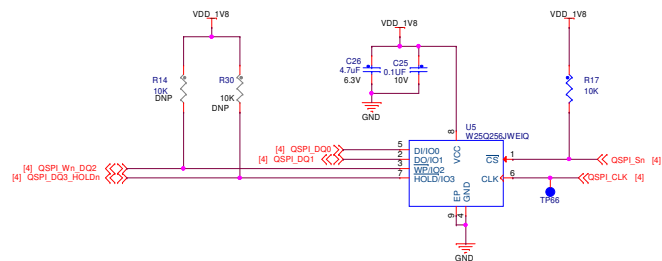
ICAP Classification:	CP:	IUC:	PUB:
SLN-SVUI-HOT			
Page Title: Power Section			
Size C	Document Number	SPF-55334 SCH-55324	Rev A5
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i.MXRT Section

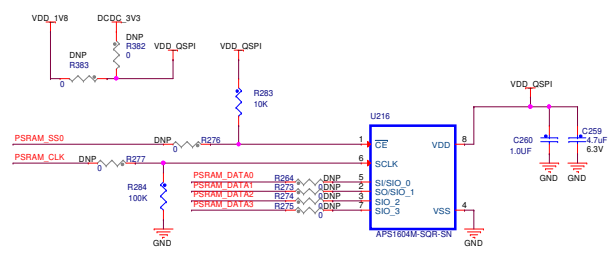


Memory Section

128Mbit QSPI Flash Memory



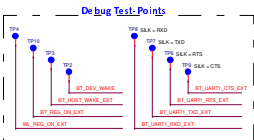
OPI PSRAM



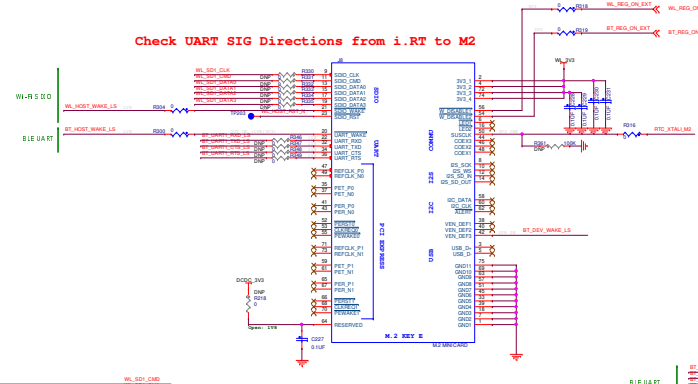
QSPI PSRAM



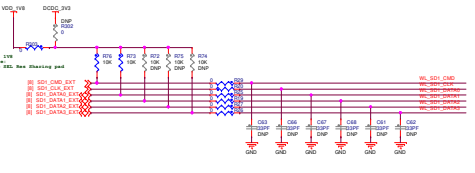
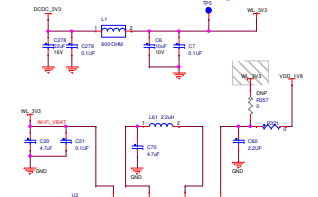
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Drawing Title: SLN-SVU-HOT					
Page Title: Memory Section					
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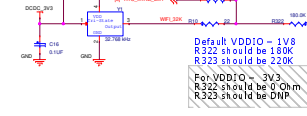
Check UART SIG Directions from i.RT to M2



RF SoC Supply Filter

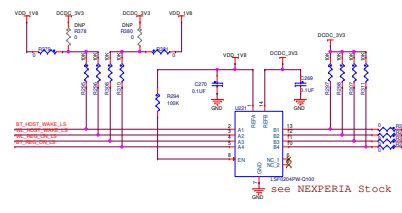


Low Power Mode 32K Clock Source

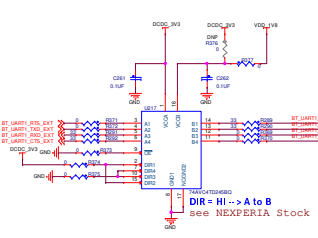


Default VDDIO = 1V8
 R322 should be 180K
 R323 should be 220K
 For VDDIO = 3V3
 R322 should be 1k Ohm
 R323 should be DNP

LAY: KEEEP all the parts close; RF tuning



see NEXPERIA Stock



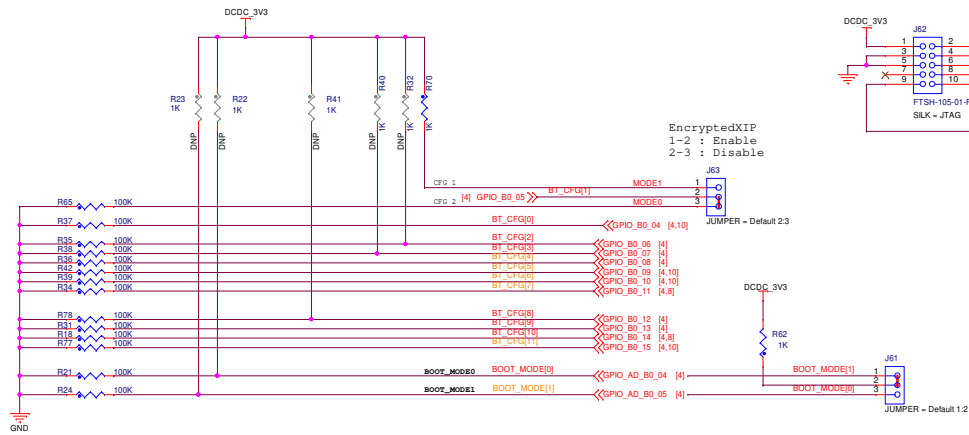
DIR = HI -> A to B
 see NEXPERIA Stock

RF Trace : 50ohm impedance

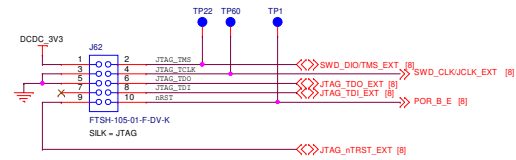
Part Number: SLN-SVUH-KOT	Rev: 1.0
Wi-Fi & BT/BLE Section	
Document Number: SPR-8528	Rev: 1.0
Date: March 14, 2019	

Boot Configuration & Debug Interface

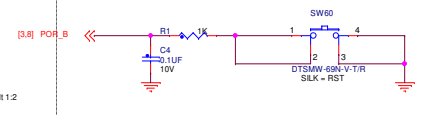
Boot Configuration.



i.MXRT Debug & Programming



i.MXRT Reset Button



Boot Mode selection Header

CHECK RST Timing! Lo --> HI, ~Min 1V for LS to be ON

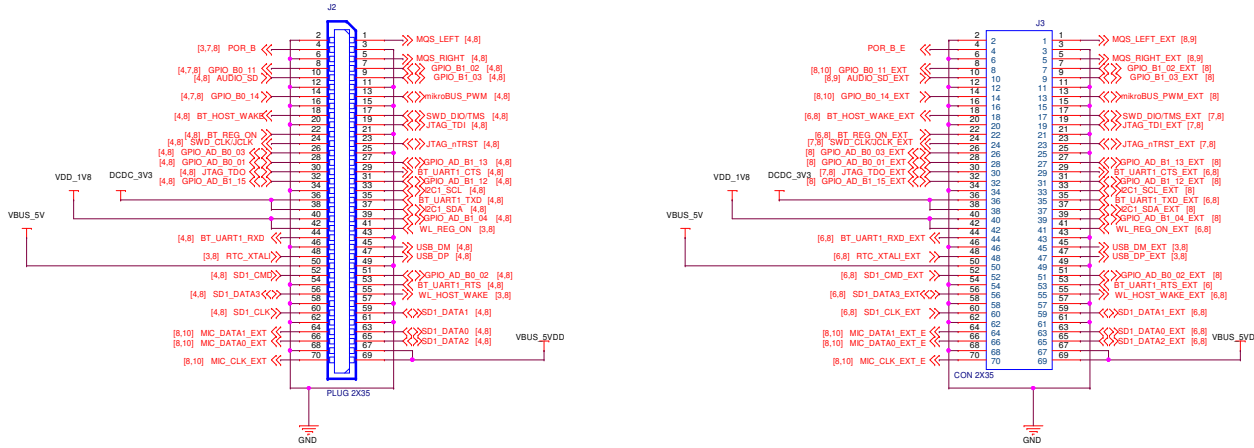
FUSE MAP

TYPE	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
FlexSPI1 - Serial NOR	Infinite-Loop: (Debug USE only) 0 - Disable 1 - Enable	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR			0	0	0	0	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		EncryptedXIP 0 - Disabled 1 - Enabled	Reserved
SD	Infinite-Loop: (Debug USE only) 0 - Disable 1 - Enable	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V	0	1	SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct	Port Select: 0 - esDHC1 1 - esDHC2	Fast Boot: 0 - Regular 1 - Fast Boot

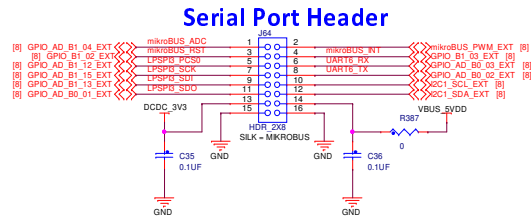


Headers

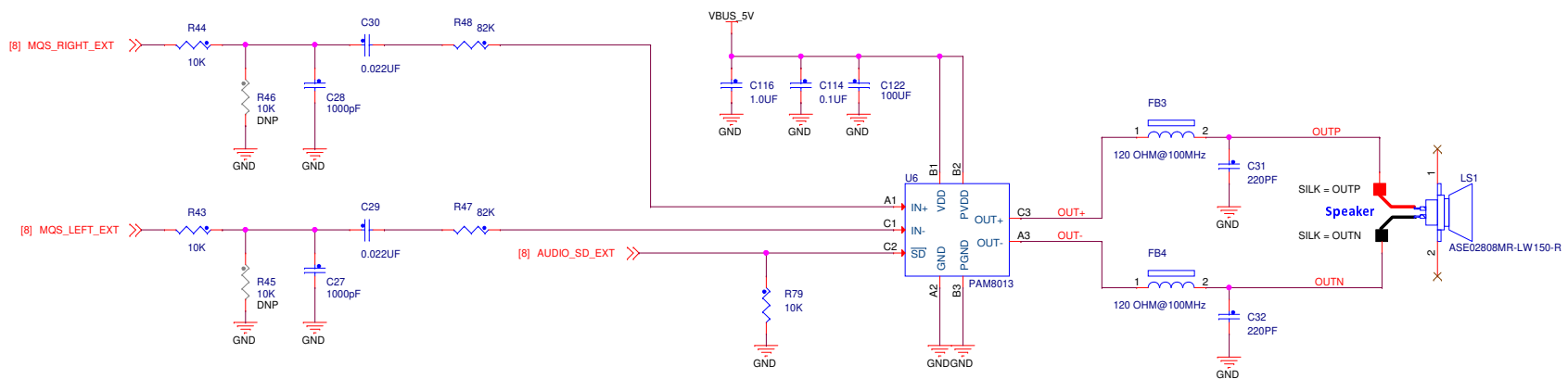
CK Alignment with PE



Serial Port Header

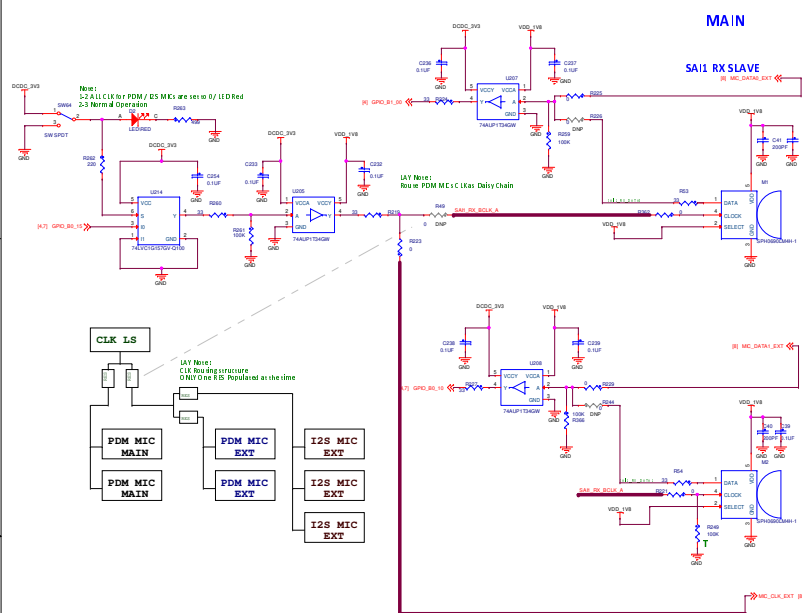


Audio Amplifier Extension Board

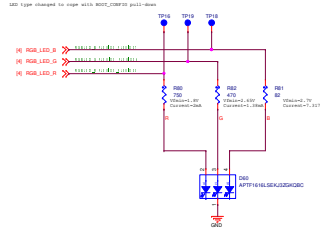


ICAP Classification:		CP:	IUO:	PUBI:
Drawing Title:				
SLN-SVUI-IOT				
Page Title:				
Audio Amplifier				
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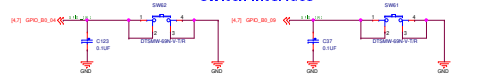
PDM MICROPHONE interface



RGB LED Interface



Switch interface



NXP			
Doc ID: 974818	Doc ID: 974818	Doc ID: 974818	Doc ID: 974818
SLN-SVU1-HOT			
User Interface			
Doc ID: 974818	Doc ID: 974818	Doc ID: 974818	Doc ID: 974818
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