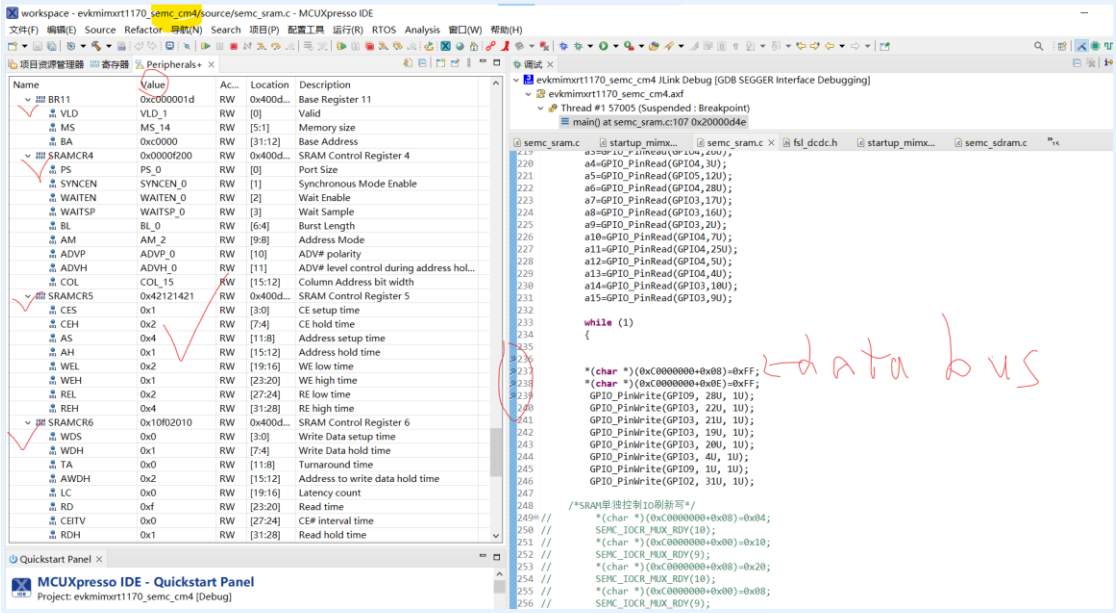
Hello, thank you very much for taking the time to help me with my question, which is related to the previous SEMC SRAM.(Attachment is SEMC CM7 and CM4's own program)

I made changes to the program of the official SEMC SDRAM CM7 core and CM4 core, under the CM7 and CM4 core Source directory, semc_sdram.c has made changes as semc_sram.c， All sram content of the code are all the same for cm7 and cm4 program.

The question is: Why can't the CM7 core run with the same program parameters and content and what's the difference between CM7 and CM4 SRAM for SEMC?

1.The desired SRAM bus refresh results can be achieved on the CM4 core. When debugging the breakpoint to the following statement, the SEMC register section will have values and meet the requirements.

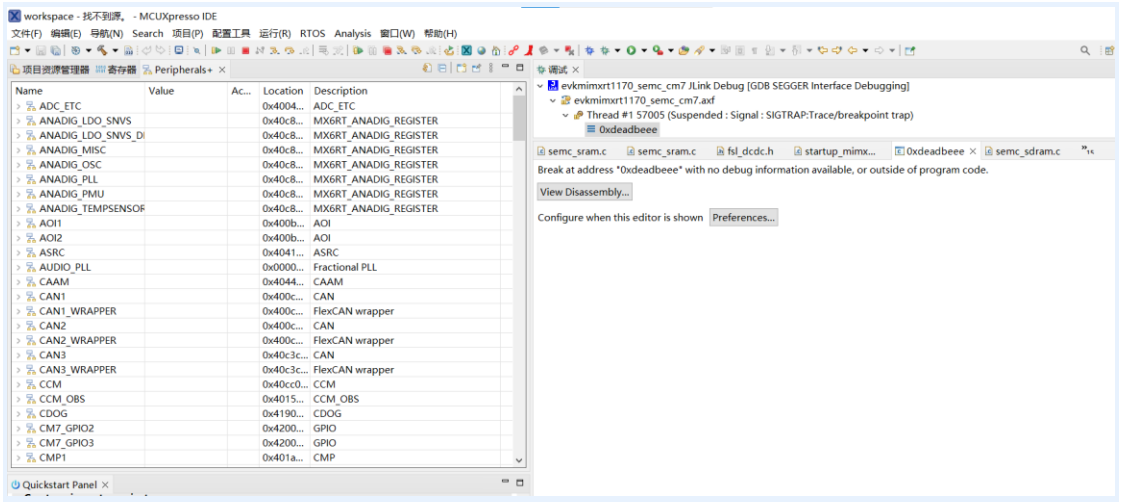
```
*(char *)(0xC0000000+0x08)=0xFF;
```

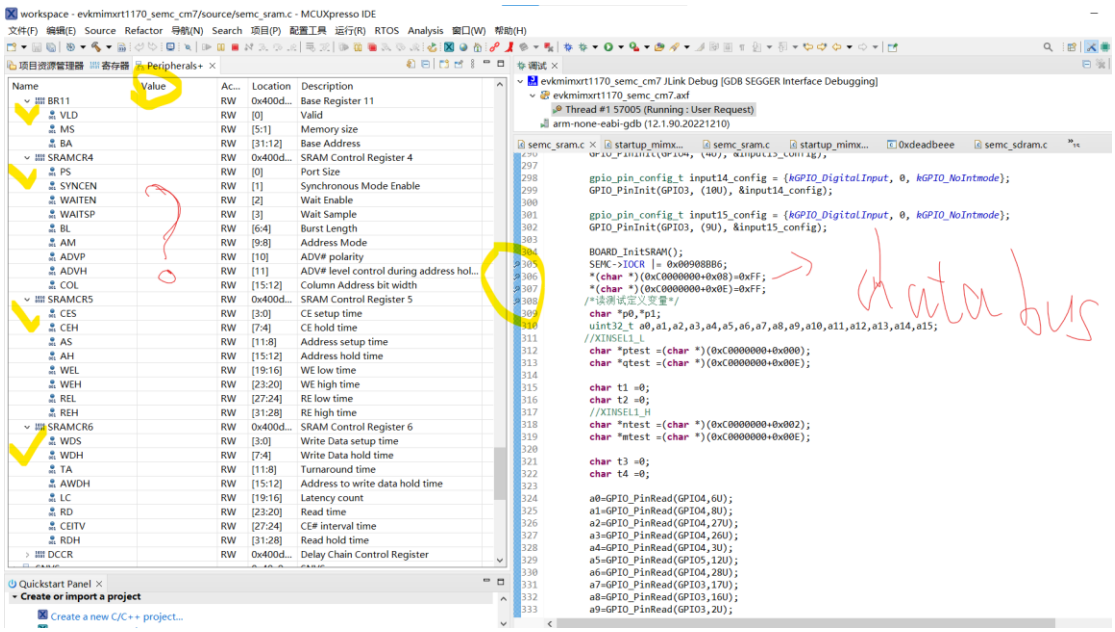


Cm4

2.CM 7 core will occur when debugging begins.：**Break at address "0xdeadbeee" with no debug information available, or outside of program code.** And the breakpoint debugs to the same statement when the register value is 0, can not get the expected result

```
*(char *)(0xC0000000+0x08)=0xFF;
```


workspace - 找不到源。 - MCUXpresso IDE
文件(F) 编辑(E) 导航(N) Search 项目(P) 配置工具 运行(R) RTOS Analysis 窗口(W) 帮助(H)
项目资源管理器 寄存器 Peripherals+
Name Value Ac... Location Description
ADC_ETC 0x4004... ADC_ETC
ANADIG_LDO_SNVS 0x40c8... MX6RT_ANADIG_REGISTER
ANADIG_LDO_SNVS_DI 0x40c8... MX6RT_ANADIG_REGISTER
ANADIG_MISC 0x40c8... MX6RT_ANADIG_REGISTER
ANADIG_OSC 0x40c8... MX6RT_ANADIG_REGISTER
ANADIG_PLL 0x40c8... MX6RT_ANADIG_REGISTER
ANADIG_PMU 0x40c8... MX6RT_ANADIG_REGISTER
ANADIG_TEMPSENSOR 0x40c8... MX6RT_ANADIG_REGISTER
AOI1 0x400b... AOI
AOI2 0x400b... AOI
ASRC 0x4041... ASRC
AUDIO_PLL 0x0000... Fractional PLL
CAAM 0x4044... CAAM
CAN1 0x400c... CAN
CAN1_WRAPPER 0x400c... FlexCAN wrapper
CAN2 0x400c... CAN
CAN2_WRAPPER 0x400c... FlexCAN wrapper
CAN3 0x40c3c... CAN
CAN3_WRAPPER 0x40c3c... FlexCAN wrapper
CCM 0x40cc0... CCM
CCM_OBS 0x4015... CCM_OBS
CDOG 0x4190... CDOG
CM7_GPIO2 0x4200... GPIO
CM7_GPIO3 0x4200... GPIO
CMP1 0x401a... CMP
Quickstart Panel
调试
evkmimxrt1170_semc_cm7 JLink Debug [GDB SEGGER Interface Debugging]
evkmimxrt1170_semc_cm7.axf
Thread #1 57005 (Suspended : Signal : SIGTRAP:Trace/breakpoint trap)
0xdeadbeee
semc_sram.c fsl_dcdc.h startup_mimx... 0xdeadbeee semc_sdram.c
Break at address "0xdeadbeee" with no debug information available, or outside of program code.
View Disassembly...
Configure when this editor is shown Preferences...


workspace - evkmimxrt1170_semc_cm7/source/semc_sram.c - MCUXpresso IDE
文件(F) 编辑(E) Source Refactor 导航(N) Search 项目(P) 配置工具 运行(R) RTOS Analysis 窗口(W) 帮助(H)
项目资源管理器 寄存器 Peripherals+
Name Value Ac... Location Description
BR11 RW 0x400d... Base Register 11
VLD RW [0] Valid
MS RW [5:1] Memory size
BA RW [31:12] Base Address
SRAMCR4 RW 0x400d... SRAM Control Register 4
PS RW [0] Port Size
SYNCEN RW [1] Synchronous Mode Enable
WAITEN RW [2] Wait Enable
WAITSP RW [3] Wait Sample
BL RW [6:4] Burst Length
AM RW [9:8] Address Mode
ADVP RW [10] ADV# polarity
ADVH RW [11] ADV# level control during address hol...
COL RW [15:12] Column Address bit width
SRAMCR5 RW 0x400d... SRAM Control Register 5
CES RW [3:0] CE setup time
CEH RW [7:4] CE hold time
AS RW [11:8] Address setup time
AH RW [15:12] Address hold time
WEL RW [19:16] WE low time
WEH RW [23:20] WE high time
REL RW [27:24] RE low time
REH RW [31:28] RE high time
SRAMCR6 RW 0x400d... SRAM Control Register 6
WDS RW [3:0] Write Data setup time
WDH RW [7:4] Write Data hold time
TA RW [11:8] Turnaround time
AWDH RW [15:12] Address to write data hold time
LC RW [19:16] Latency count
RD RW [23:20] Read time
CEITV RW [27:24] CE# interval time
RDH RW [31:28] Read hold time
DCCR RW 0x400d... Delay Chain Control Register
Quickstart Panel
Create or import a project
Create a new C/C++ project...
调试
evkmimxrt1170_semc_cm7 JLink Debug [GDB SEGGER Interface Debugging]
evkmimxrt1170_semc_cm7.axf
Thread #1 57005 (Running : User Request)
arm-none-eabi-gdb (12.1.90.20221210)
semc_sram.c startup_mimx... semc_sram.c startup_mimx... 0xdeadbeee semc_sdram.c
297
298 gpio_pin_config_t input14_config = {kGPIO_DigitalInput, 0, kGPIO_NoIntmode};
299 GPIO_PinInit(GPIO3, (10U), &input14_config);
300
301 gpio_pin_config_t input15_config = {kGPIO_DigitalInput, 0, kGPIO_NoIntmode};
302 GPIO_PinInit(GPIO3, (9U), &input15_config);
303
304 BOARD_InitSRAM();
305 SEMC->IOCR |= 0x00008BB6;
306 *(char *)(0xC0000000+0x08)=0xFF;
307 *(char *)(0xC0000000+0x0E)=0xFF;
308 /*读测试定义变量*/
309 char *p0,*p1;
310 uint32_t a0,a1,a2,a3,a4,a5,a6,a7,a8,a9,a10,a11,a12,a13,a14,a15;
311 //XINSEL1_L
312 char *ptest =(char *)(0xC0000000+0x000);
313 char *qtest =(char *)(0xC0000000+0x00E);
314
315 char t1 =0;
316 char t2 =0;
317 //XINSEL1_H
318 char *ntest =(char *)(0xC0000000+0x002);
319 char *mtest =(char *)(0xC0000000+0x00E);
320
321 char t3 =0;
322 char t4 =0;
323
324 a0=GPIO_PinRead(GPIO4,6U);
325 a1=GPIO_PinRead(GPIO4,8U);
326 a2=GPIO_PinRead(GPIO4,27U);
327 a3=GPIO_PinRead(GPIO4,26U);
328 a4=GPIO_PinRead(GPIO4,3U);
329 a5=GPIO_PinRead(GPIO5,12U);
330 a6=GPIO_PinRead(GPIO4,28U);
331 a7=GPIO_PinRead(GPIO3,17U);
332 a8=GPIO_PinRead(GPIO3,16U);
333 a9=GPIO_PinRead(GPIO3,2U);

Cm7