Coral Dev Board Micro: Mainboard Cover Page

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Project: *Coral Dev Board Micro*		Google LLC 1600 Amphitheatre Parkway Mountain View, CA 94043
Engineer: Stefan	Revision: PVT	
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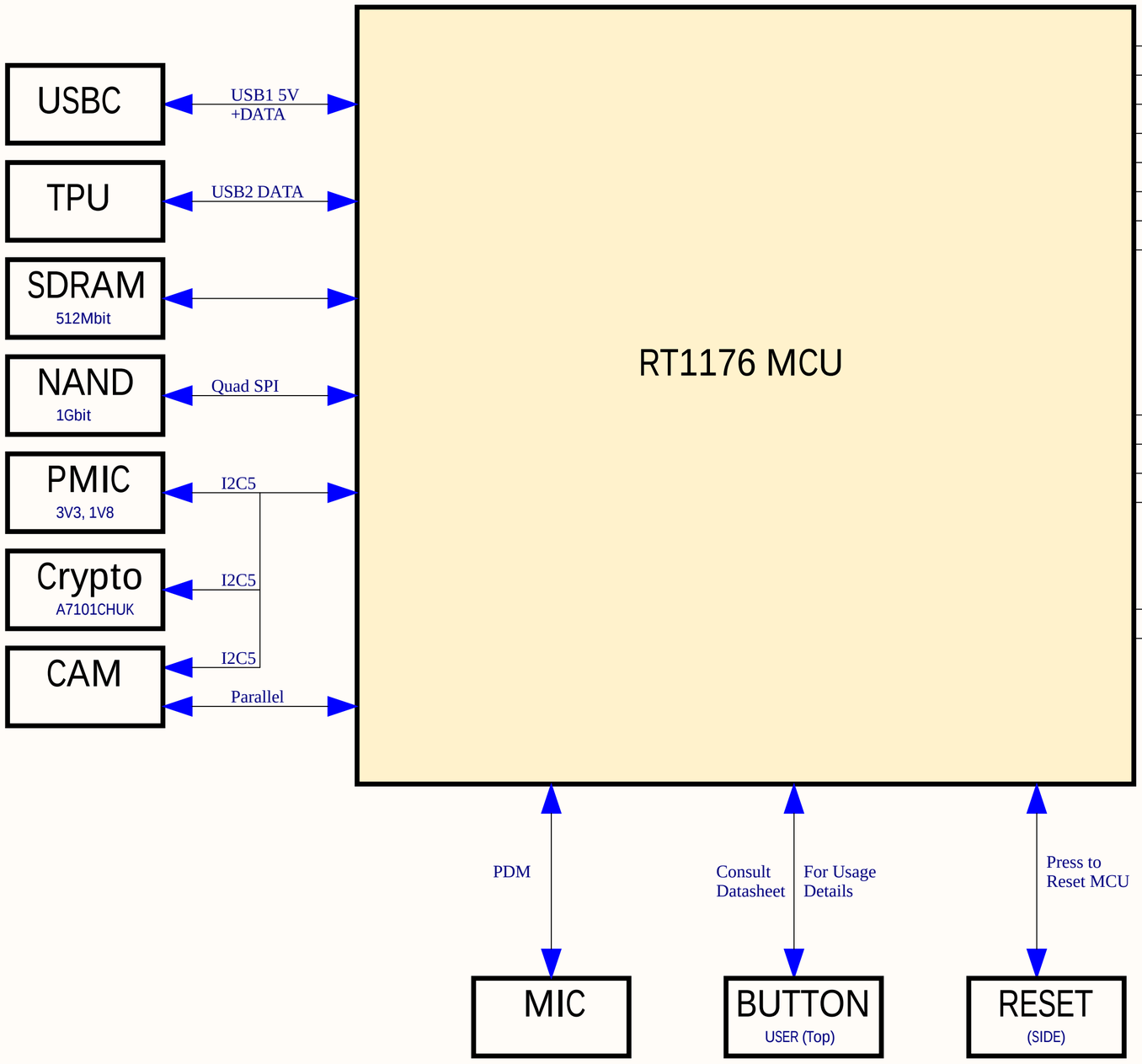
Coral Dev Board Micro: Mainboard Block Diagram

Refer to schematic for pins routed to B2B and default pin MUX



Default Pin Mappings to Header

- ADC (2x)
- PWM (2x)
- DAC (1x)
- I2C (2x)
- SPI (1x)
- UART (1x)
- POWER: 1V8 (2x), 3V3 (1x), VSYS 5V (1x)
- POWER: Coin Cell LP BAK (1x)

Signals used on Add-on boards at Release Time

WIFI

- POWER: 3V3
- WIFI: SDIO (1x) + Control IO
- BT: UART (1x) + Control IO
- DEBUG: JTAG Header Pads

PoE

- POWER: VSYS (I), 3V3 (O)
- ETHERNET: RGMII(IO) + Control IO

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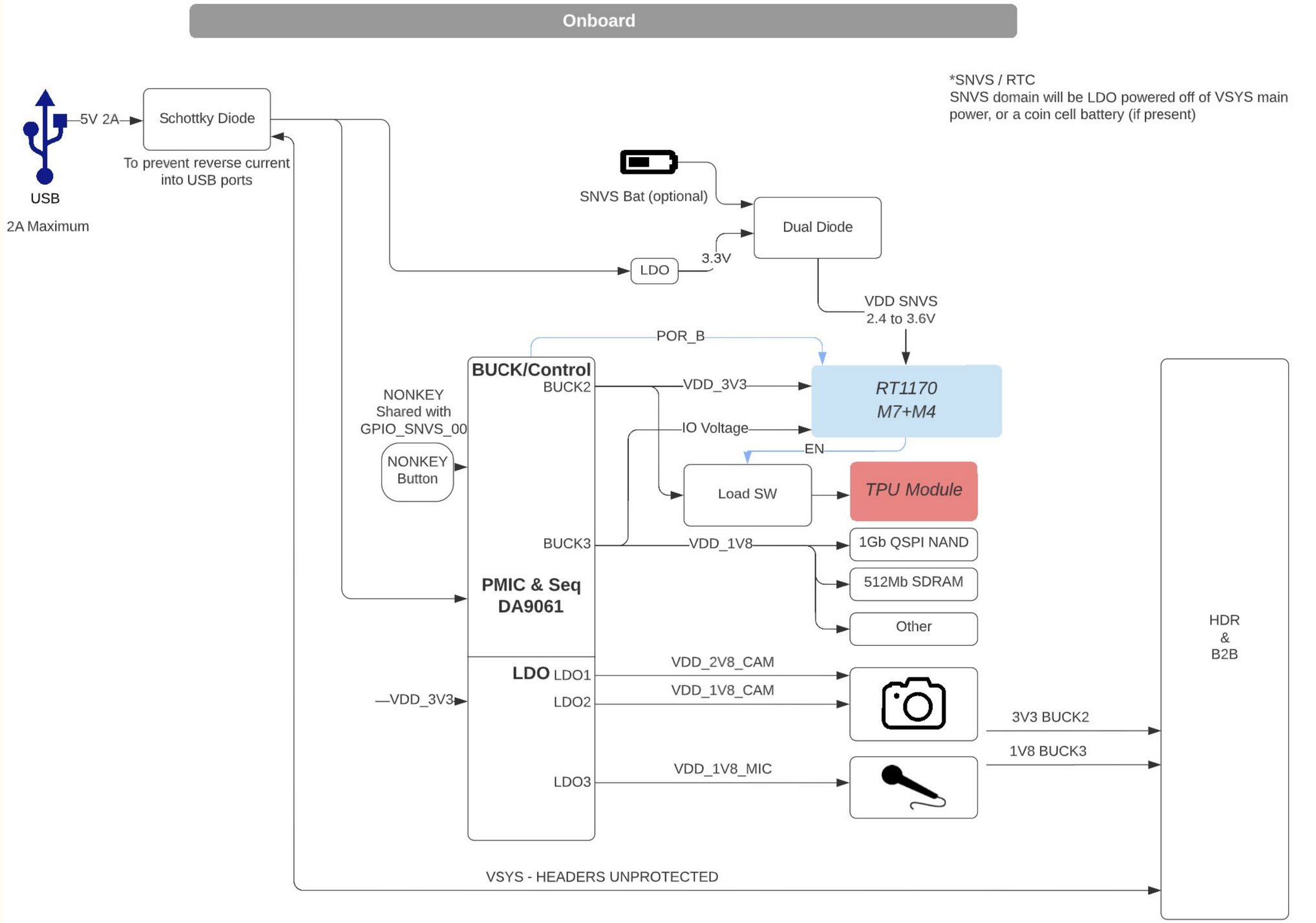
File: 02 BLOCK DIAGRAM.SchDoc		

Coral Dev Board Micro: Mainboard Power Diagram



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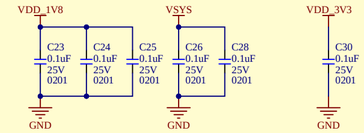
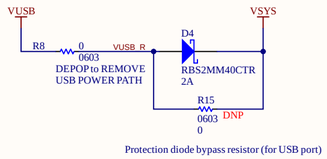
File: 03 POWER DIAGRAM.SchDoc			

Coral Dev Board Micro: Main Power

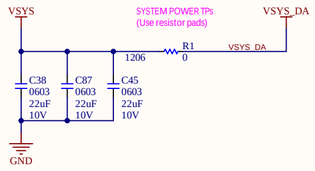
VBAT Power
VSYS Power
VSYS_DA Power

Dispersed Caps

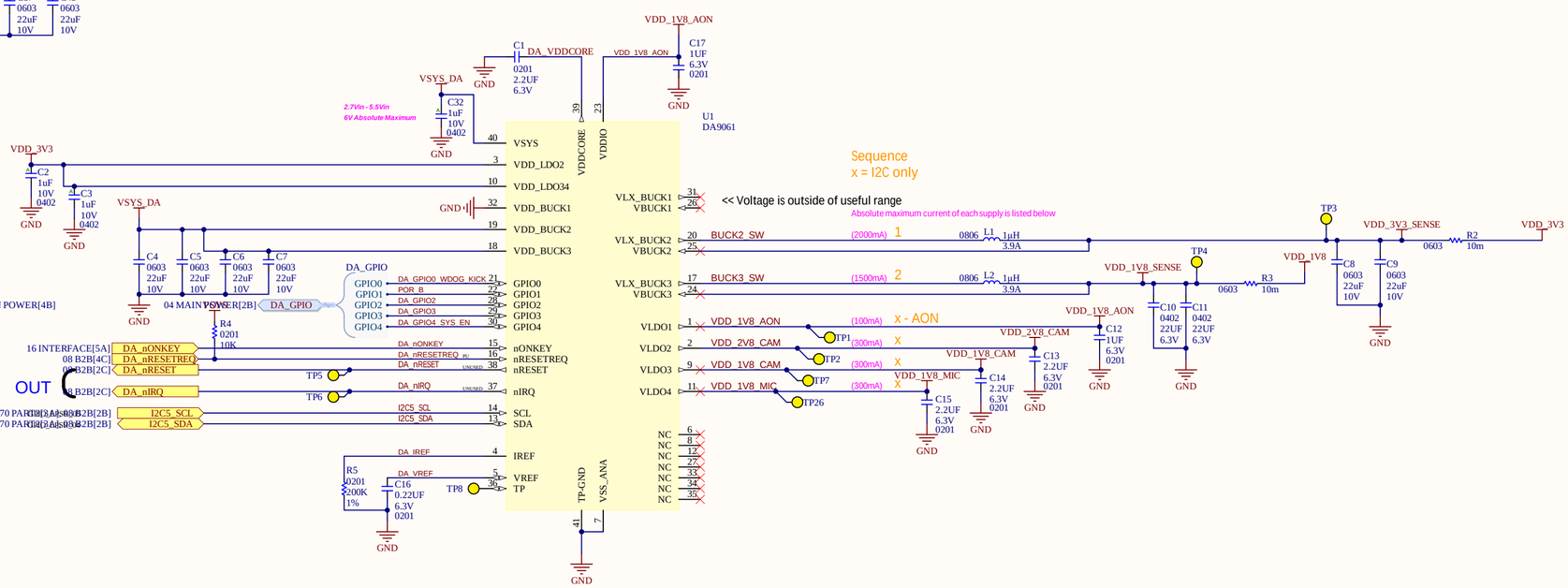




Protection diode bypass resistor (for USB port)



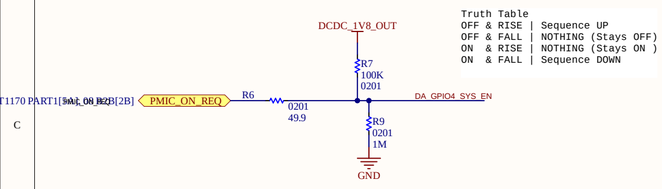
VSYS TO ALL PRIMARY SYSTEM VOLTAGES



WDOG_KICK Optional by customer
DA_GPIO0 can be programmed for watchdog use. Consult the DA9061 Datasheet

Power Control Via Enable (PMIC)

Any TRANSITION on SYS_EN (GPIO4) up or down will cause the DA9061 to smoothly sequence the rails up or down to enter the associated state if it's not already there




```
Truth Table
OFF & RISE | Sequence UP
OFF & FALL | NOTHING (Stays OFF)
ON  & RISE | NOTHING (Stays ON )
ON  & FALL | Sequence DOWN
```

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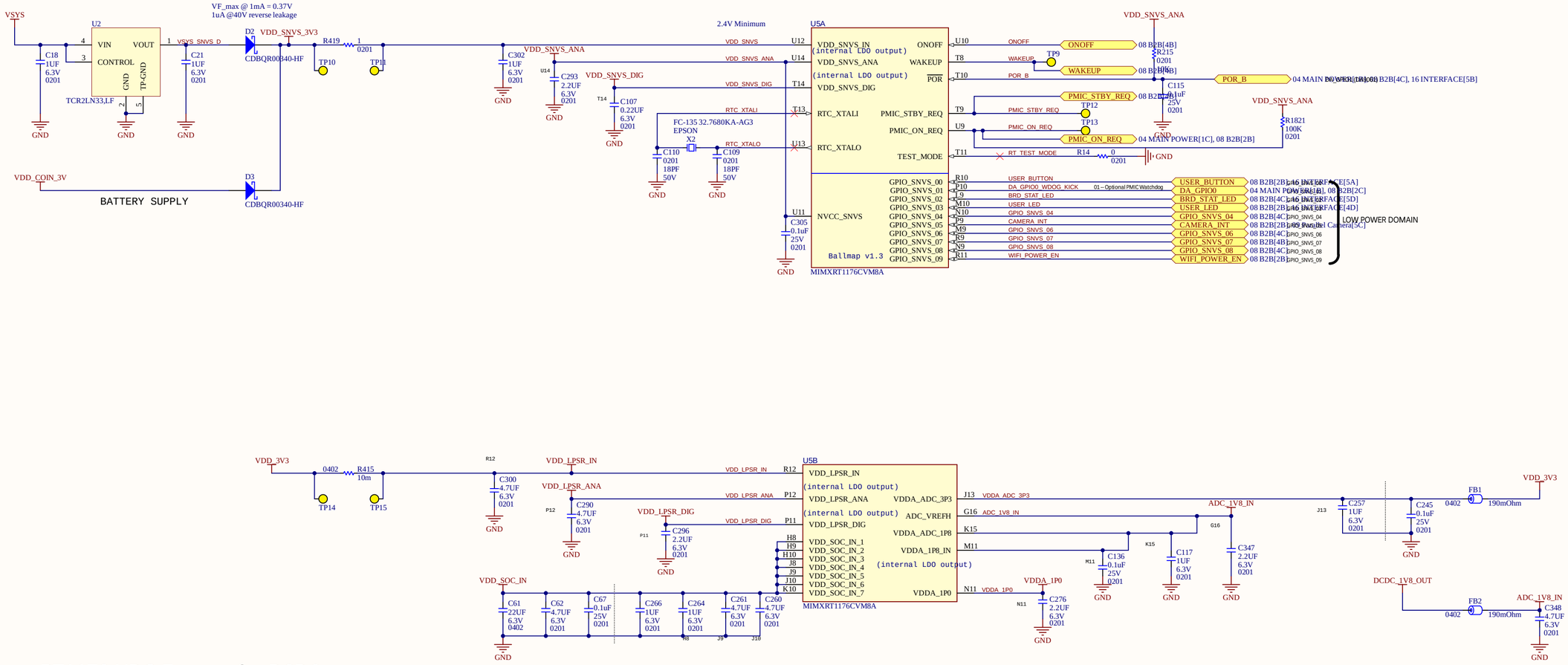
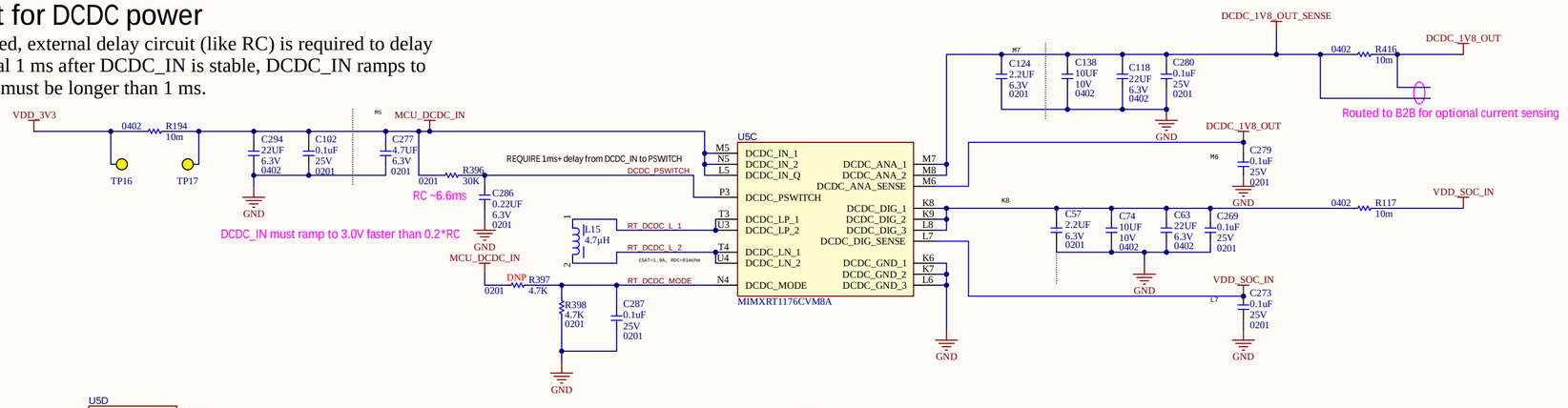
Coral Dev Board Micro: RT1176 PART1



RT1170 HDG Excerpt for DCDC power

When internal DCDC is enabled, external delay circuit (like RC) is required to delay the “DCDC_PSWITCH” signal 1 ms after DCDC_IN is stable, DCDC_IN ramps to 3.0 V within 0.2*RC, and RC must be longer than 1 ms.



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File:	05 MIMXRT1170 PART1.SchDoc		

Coral Dev Board Micro: RT1176 PART2

U5F
MIMXRT1176CVM8A
NVCC_LPSR
VDD_1V8
C256 2.2UF 6.3V 0201
GND
GPIO_LPSR_00 … GPIO_LPSR_15
MIC_CLK, DMIC_DATA0, BOOT_MODE0, BOOT_MODE1, I2C5_SDA, I2C5_SCL, I2C6_SDA, I2C6_SCL, CRYPTO_RST_N, LPSPI6_CS0, LPSPI6_SCK, LPSPI6_SDI, DMIC_DATA1, DMIC_DATA2_JTAG_TCK, DMIC_DATA3_JTAG_TMS
TP18 TP19 TP20 TP21 TP24
SWD_DIO = JTAG_TMS
SWD_CLK = JTAG_CLK
DMIC
BOOT MODE
LPSPI6
JTAG_MOD
R37 0201 DNP
R38 0201 4.7K
VDD_1V8
GND

JTAG Notes
-JTAG_TDO internally controlled - Do not pull
-JTAG_TCK :: On chip 20-50k PD
-JTAG_TMS :: On chip 20-50k PU
-JTAG_TDI :: On chip 20-50k PU
-JTAG_TRSTB :: On chip 20-50k PU
-JTAG_MOD :: On chip 20-50k PD

JTAG_MOD
High= IEEE 1149.1 standard
Low= Standard Debug Mode

VSYS MEASUREMENT
6V*R2/(R1+R2)=1.8V
VSYS
R40 0201 1M
R41 430K 0201
C33 4.7UF 6.3V 0201
ADC1_CH2A
GPIO_AD_10
GND

U5H
MIMXRT1176CVM8A
NVCC_GPIO
VDD_1V8
C345 4.7UF 6.3V 0201
C258 2.2UF 6.3V 0201
GND
GPIO_AD_00 … GPIO_AD_35
FLEXPWM1_PWM0_A, FLEXPWM1_PWM0_B, FLEXPWM1_PWM1_A, FLEXPWM1_PWM1_B
BT_CFG_IO_EN
DRIVE HIGH TO ENABLE IO FUNCTION FROM BOOT PINS
ADC1_CH0A, ADC1_CH0B, USB_PORT_RT, USB_OTG1_ID_RT
R43 0 0201 USB_OTG1_ID
ADC1_CH2A, ADC1_CH2B, CSI_PIXCLK, CSI_MCLK_RT
R44 0 0201 CSI_MCLK
CSI_VSYNC, CSI_HSYNC, CSI_DATA09, CSI_DATA08, CSI_DATA07, CSI_DATA06, CSI_DATA05, CSI_DATA04, CSI_DATA03, CSI_DATA02
LPUART1_TXD_BT
USE ISOLATED BELOW (LPUART1 can interrupt serial boot)
LPUART1_RXD_BT
USE ISOLATED BELOW (LPUART1 can interrupt serial boot)
FLEXPWM2_PWM1_A, FLEXPWM2_PWM1_B, LPSPI1_SCK, LPSPI1_PCS0, LPSPI1_SDO, LPSPI1_SDI, I2C1_SCL, I2C1_SDA, WL_REG_ON, BT_REG_ON
FLEXPWM1_PWM0_A … FLEXPWM1_PWM1_B complimentary or independent
ADC1_CH0A … ADC1_CH0B (CAN also here)
USB_PORT_RT … USB_OTG1_ID
O2C ID
USB-C DRD
ADC1_CH2B … CSI_MCLK
ADC part 1
CSI_VSYNC … CSI_DATA02
CSI PARALLEL
NOTE: [D0:D1] Cannot be used for 8-bit cam
(VIDEO_MUX_CSI_XXXX)
LPUART1 - isolated at boot
FLEXPWM2_PWM1_A … FLEXPWM2_PWM1_B
PWM2
LPSPI1_SCK … LPSPI1_PCS0
LPSPI1
LPSPI1_SDO … I2C1_SDA
LPUART1
WL_REG_ON … BT_REG_ON
WiFi/BT Other

DCDC_1V8_OUT
R373 0201 10K
R374 0201 10K
R23 0201 10K
R24 0201 10K

U5G
MIMXRT1176CVM8A
NVCC_SD1
NVCC_SD2
VDD_1V8
R375 0 0201
D14
C242 2.2UF 6.3V 0201
G13
C254 2.2UF 6.3V 0201
GND
GPIO_SD_B1_00 … GPIO_SD_B1_05
WIFI_SDIO_CMD_R, WIFI_SDIO_CLK, WIFI_SDIO_D0_R, WIFI_SDIO_D1_R, WIFI_SDIO_D2_R, WIFI_SDIO_D3_R
R32 0 WIFI_SDIO_CMD
R33 0 WIFI_SDIO_D0
R34 0 WIFI_SDIO_D1
R35 0 WIFI_SDIO_D2
R36 0 WIFI_SDIO_D3
WIFI_SDIO_CMD … WIFI_SDIO_D3
WIFI/BT SDIO
GPIO_SD_B2_00 … GPIO_SD_B2_11
USDHC2_DATA3 … USDHC2_CMD
FlexSPI_A_SS0 … FlexSPI_A_D3
USDHC2_DATA3 … USDHC2_DATA0, USDHC2_CLK, USDHC2_CMD
USER SD CARD
FlexSPI_A_SS0 … FlexSPI_A_D3
QSPI_BOOT

U5I
MIMXRT1176CVM8A
NVCC_DISP1
NVCC_DISP2
VDD_1V8
D12
C285 2.2UF 6.3V 0201
E7
C327 2.2UF 6.3V 0201
GND
50OHM
GPIO_DISP_B1_00 … GPIO_DISP_B1_11
ENET_RGMII_RX_EN, ENET_RGMII_RXC, ENET_RGMII_RXD0, ENET_RGMII_RXD1, ENET_RGMII_RXD2, ENET_RGMII_RXD3, BT_CFG1_0_ENET_RGMII_TXD3, BT_CFG1_1_ENET_RGMII_TXD2, BT_CFG1_2_ENET_RGMII_TXD1, BT_CFG1_3_ENET_RGMII_TXD0, BT_CFG1_4_ENET_RGMII_TX_EN, BT_CFG1_5_ENET_RGMII_TXC
BT_CFG1[0]=ENET_RGMII_TXD3 … BT_CFG1[5]=ENET_RGMII_TXC
ENET_RGMII_RX_EN … ENET_RGMII_TXC_BT
ETHERNET
GPIO_DISP_B2_00 … GPIO_DISP_B2_15
BT_CFG1_6, BT_CFG1_7, BT_CFG2_0, BT_CFG2_1, BT_CFG2_2, BT_CFG2_3, WL_ANT_SEL, WL_HOST_WAKE, LPUART8_TXD, LPUART8_RXD, LPUART2_TXD, LPUART2_RXD, LPUART2_CTS_B_R, LPUART2_RTS_B, BT_DEV_WAKE, BT_HOST_WAKE
R45 0 LPUART2_CTS_B
BT_CFG1_6 … BT_HOST_WAKE
BOOT_CFG1 6-7
BOOT_CFG2 0-3
WiFi/BT Other
LPUART8 Part 1 of 2
WiFi/BT LPUART2
WiFi/BT Other More on Part 3

I2C Pullups

VDD_1V8
R46 R47 R48 R49 R50 R51 0201 2.2K
I2C1_SCL, I2C1_SDA, I2C5_SDA, I2C5_SCL, I2C6_SDA, I2C6_SCL

Crypto Chip

U6 A7101CHUK
Address: 0x92
VDD_1V8
C4 B4 C2 A1 B1 B3 C1 A2
I2C5_SCL A3
I2C5_SDA A4
CRYPTO_RST_N C3
GPIO_LPSR_08
GND
Explicitly connect A1,B3 no connects for easier routing.
(confirmed with NXP)

MCM/CAM I2C ISOLATION WHEN OFF

VDD_1V8
74LVC2G66GT
I2C5_SDA, I2C5_SCL
I2C5_SDA_MCM … I2C5_SCL_MCM
14 TPU[3C]
MCM I2C ISOLATION
MCM_1V8
U10
I2C5_SDA_CAM … I2C5_SCL_CAM
09 Parallel Camera[5B]
VDD_1V8_CAM
U13

BOOT SIGNAL ISOLATION

ETHERNET
ENET_RGMII_TXD3 … ENET_RGMII_TXC
DO NOT PULL (shared with BT_CFG1[0:5])
R10 R16 R18 R19 R20 R26 0 0201
BT_CFG1_0_ENET_RGMII_TXD3 … BT_CFG1_5_ENET_RGMII_TXC
ENET_RGMII_TXD3_BT … ENET_RGMII_TXC_BT
06 MIMXRT1170 PART2[7B], 15 BOOT[4B]

UART cannot be driven at boot time or USB boot mode will never be reached
Isolation switch added. Drive BT_CFG_IO_EN high to use these pins.

VDD_1V8
DNP R53 100K 0201
DNP R21 100K 0201
74LVC2G66GT
LPUART1_TXD, LPUART1_RXD
LPUART1_TXD_BT, LPUART1_RXD_BT
GPIO_AD_24, GPIO_AD_25
BT_CFG_IO_EN
R27 100K 0201
U14
GND

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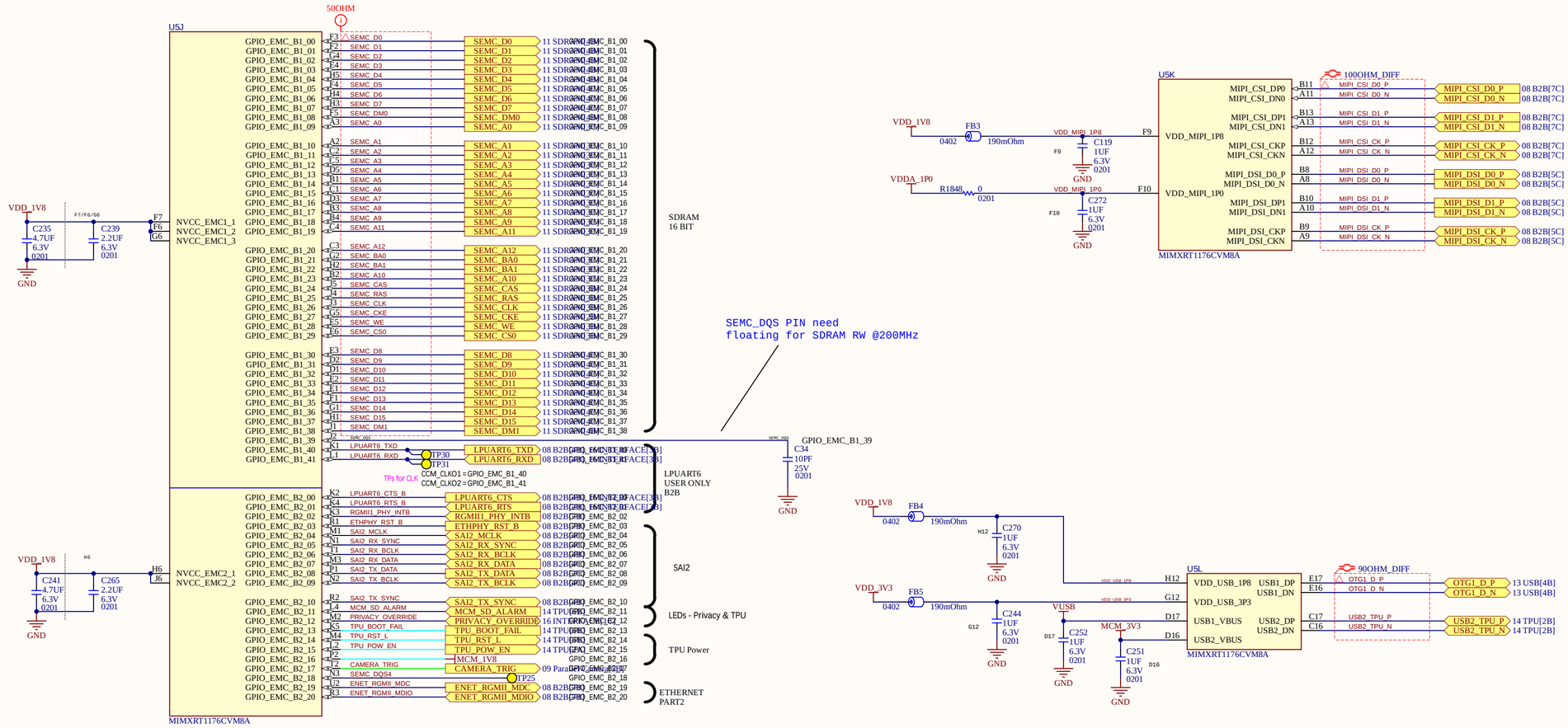
Coral Dev Board Micro: RT1176 PART3



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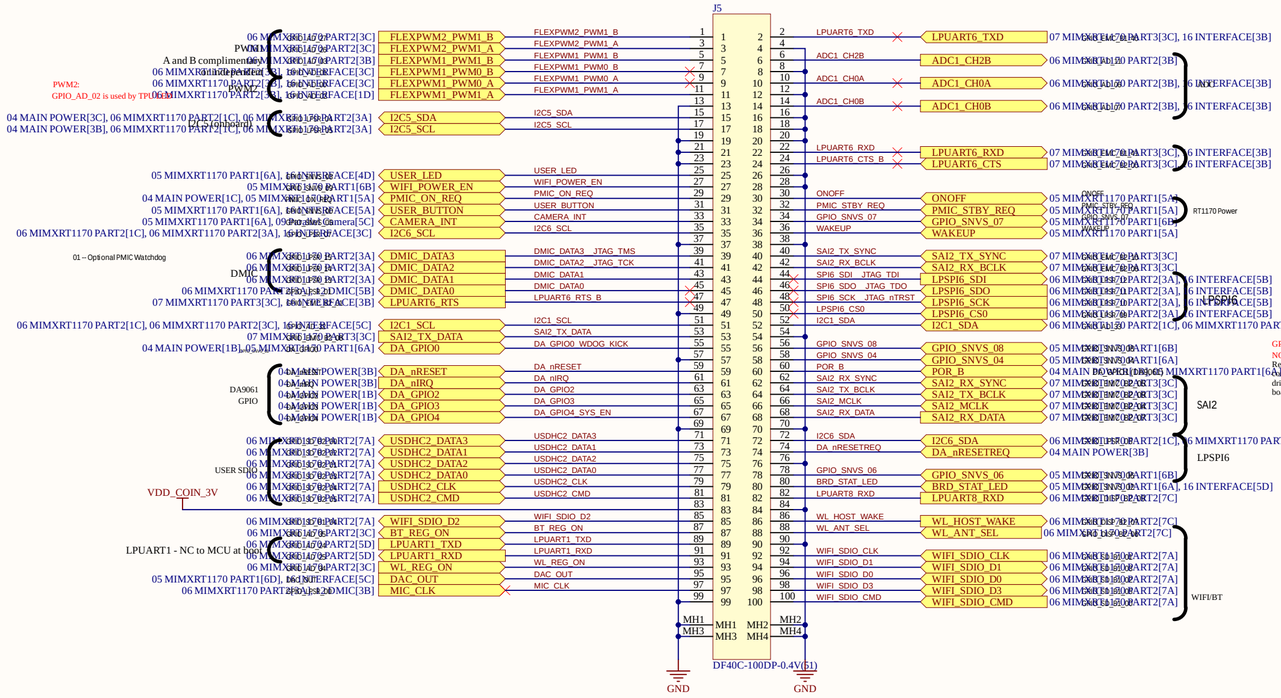
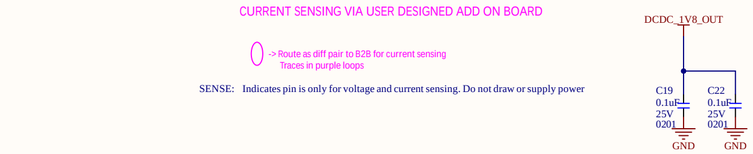
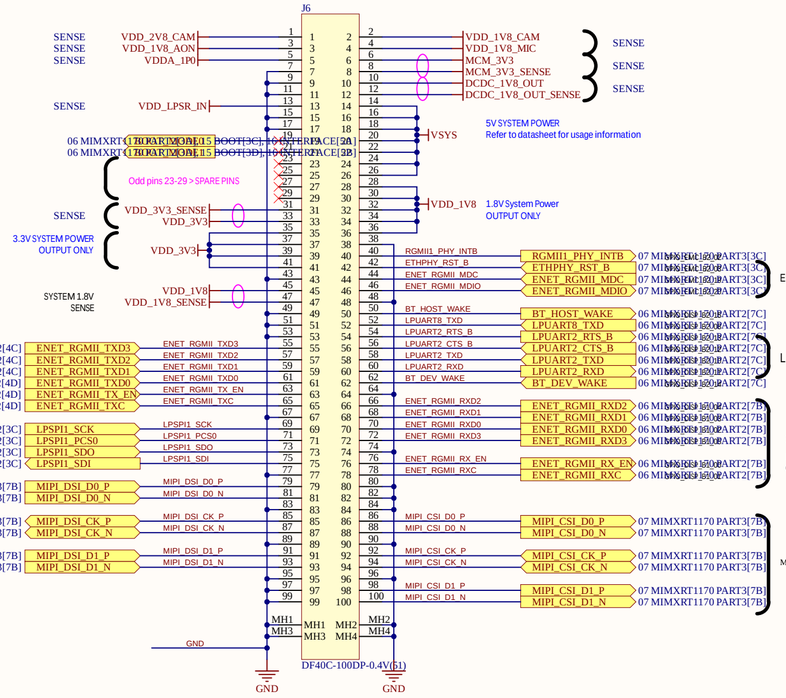
Coral Dev Board Micro: Board to Board Connector

B2B Pinout







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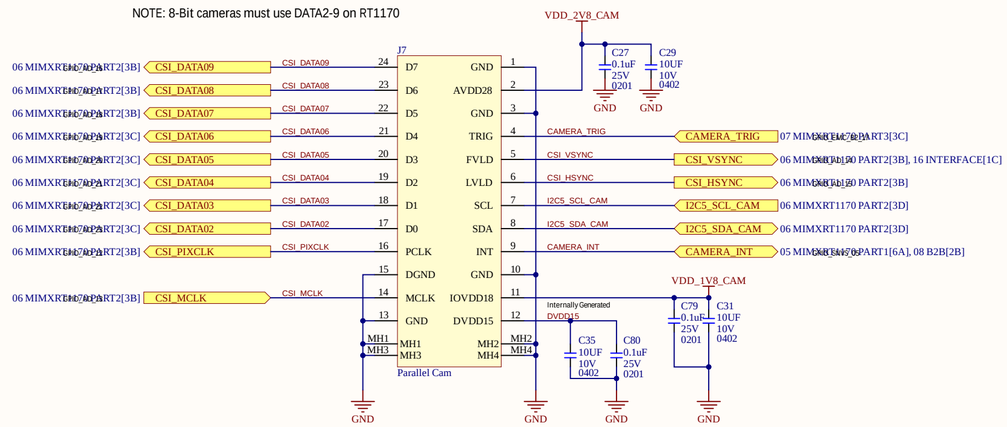
Coral Dev Board Micro: Camera Module

Camera Module Connector



Connector Part Numbers

Molex 5055502420 (receptacle on board) 30 cycles rated
Molex 5055512420 (plug on camera) 30 cycles rated

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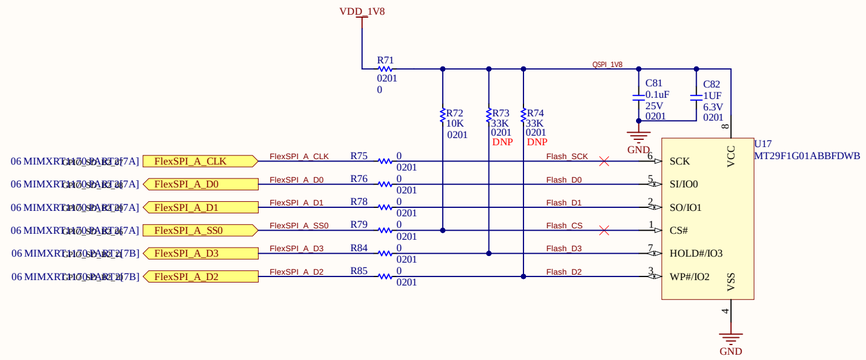
File: 09 Parallel Camera.SchDoc		

Coral Dev Board Micro: Flash Boot

1V8 QSPI Flash



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File: 10 FLASH_BOOT.SchDoc	

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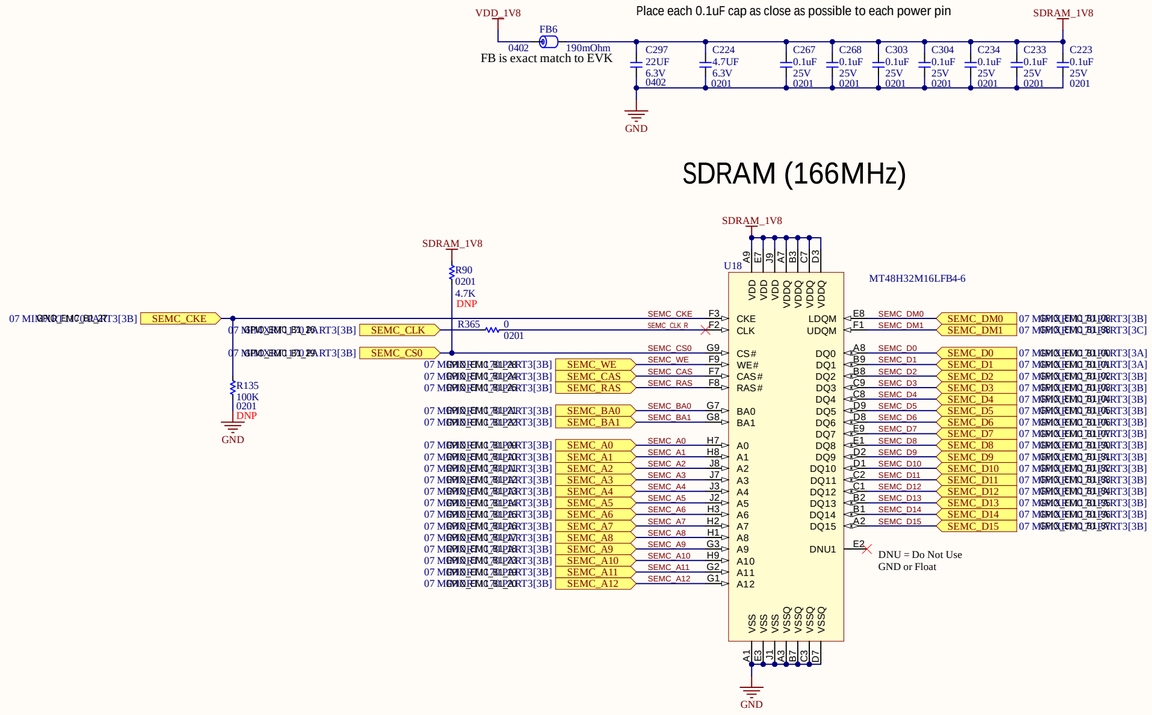
Coral Dev Board Micro: SDRAM



SDRAM (166MHz)

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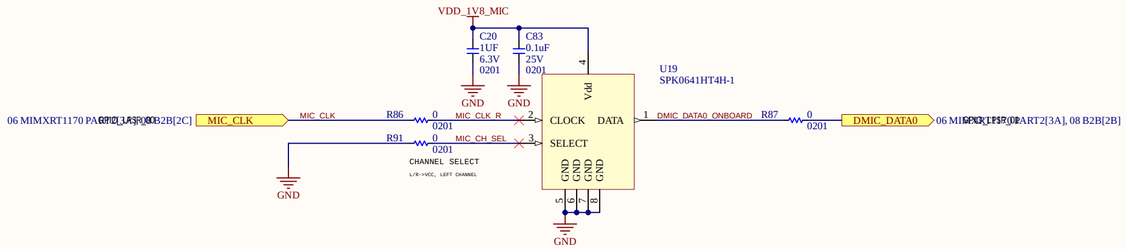
Coral Dev Board Micro: DMIC

DMIC Interface



PDM Channel Info for Microphone

SELECT = GND
-Asserts data on falling edge (MCU samples on CLOCK rising edge)
-By default this is left channel when two mics present on a single data line but can be swapped in the MCU

SELECT = VDD
-Asserts data on the rising edge (MCU samples on CLOCK falling edge)
-By default this is left channel when two mics present on a single data line but can be swapped in the MCU

DMIC 2, 3, 4 SIGNALS sent to B2B

DMIC 1 also sent to B2B. Depop R87 at minimum to use offboard MIC1 left channel.

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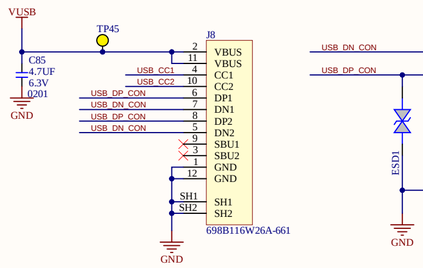
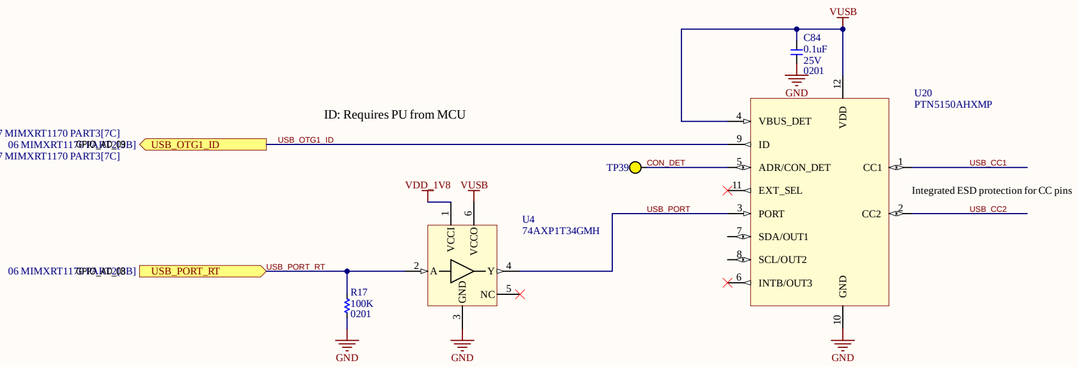
Coral Dev Board Micro: USB

USB-C 2.0 Connector



USB CC Controller



PORT (PTN5150A)
-LOW is UFP
-HIGH is DFP
*DEFAULT: PD for UFP operation

DFP mode is not implemented

```
Host --> ID = GND
Device --> ID = Floating
```

Additional Clarification
- UFP: Upward facing port for USBC. This is sumilar to DEVICE for USB OTG
- DFP: Downward facing port for USBC. Similar to HOST for USB OTG

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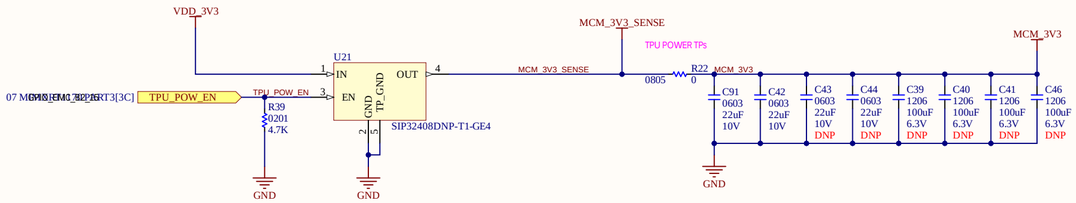
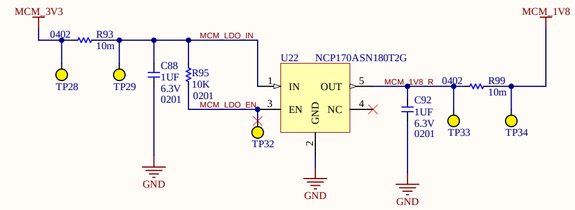
Coral Dev Board Micro: TPU

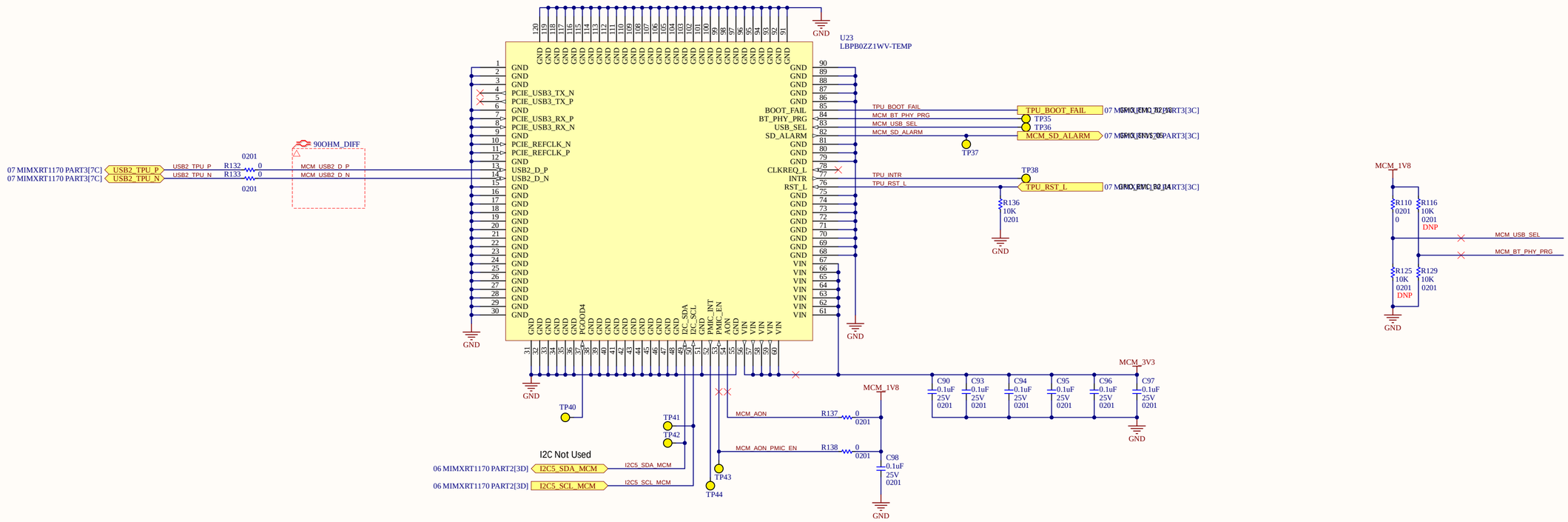
TPU Power Enable Load Switch



TPU 1V8 LDO



Accelerator Module Edge TPU



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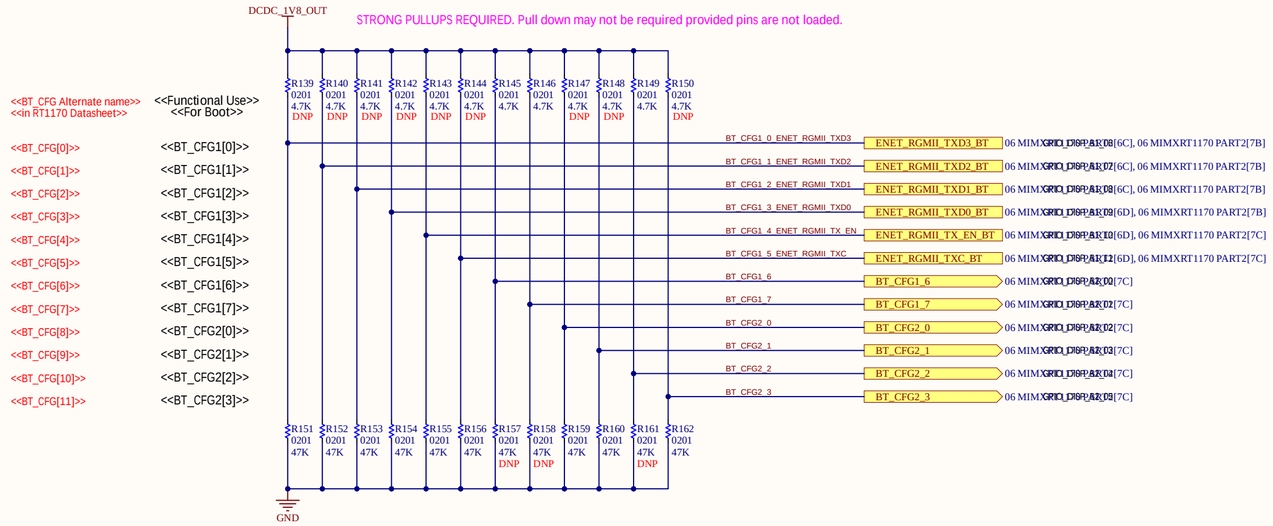
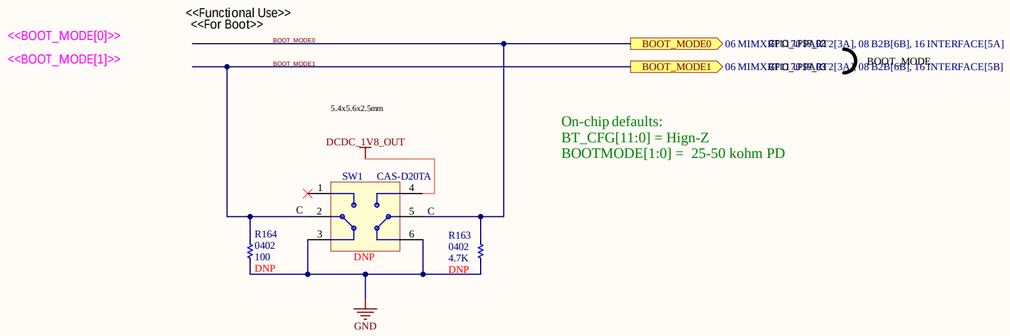
Coral Dev Board Micro: Boot

Boot Configuration

TYPE	BOOT_CFG[11] BT_CFG2[3]	BOOT_CFG[10] BT_CFG2[2]	BOOT_CFG[9] BT_CFG2[1]	BOOT_CFG[8] BT_CFG2[0]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
FlexSPI1 - QSPI NAND	*FLEXSPI_INSTANCE* *0 - FLEXSPI1* *1 - FLEXSPI2*	*CS de-asserted interval between two commands* *0 – 100ns* *1 – 200ns* *2 – 400ns* *3 – 50ns*		*Boot Search Count of FCB and DBBT* *0 - 1* *1 - 2*	*Primary boot device selection* *00 – Serial NOR* *11 – Serial NAND*		*Default safe communication frequency* *0 – High Speed (50MHz)* *1 – Low Speed (30MHz)*	*Column address width* *0 - 12 bits* *1 - 13 bits*	*Hold Time before access to Serial NAND* *0 - Hold time determined by Read Status command* *1 - 500us* *2 - 1ms* *3 - 3ms*		*BOOT_CFG1[1:0]* *0 - 64* *1 - 128* *2 - 256* *3 - 32*	
DEFAULT CONFIGURATION>	RESISTORS : 0 :: FlexSPI1	RESISTORS : 10 :: 400ns		RESISTORS : 0 FCB/DBBT =1	RESISTORS : 11 :: Serial NAND		RESISTORS : 0	RESISTORS : 0 :: 12bit	RESISTORS : 00 :: Hold time by Read Status command		RESISTORS : 00 :: (64)	



External Boot Switch



Boot MODE pin settings

BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

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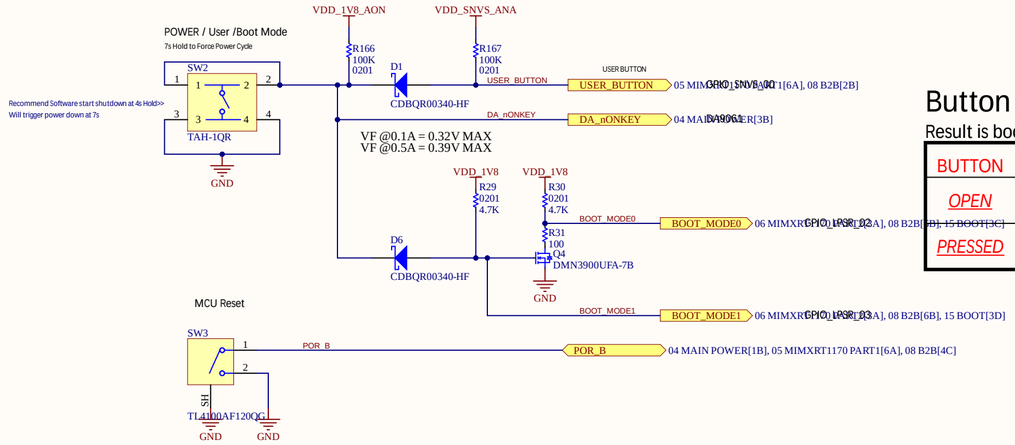
Coral Dev Board Micro: Interface

Buttons

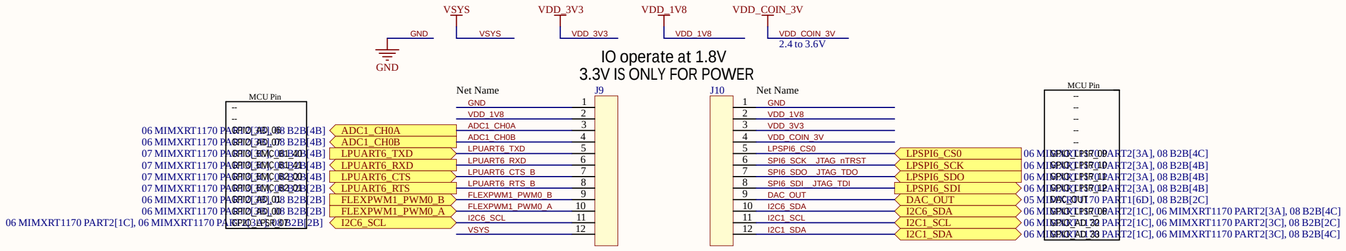


Button usage for entering serial downloader mode

Result is boot mode after soft or hard reset for given button press state

BUTTON	BOOT_MODE1	BOOT_MODE0	Result
OPEN	1	0	*Internal Boot*
PRESSED	0	1	*Serial Downloader Mode*

Header Pinout



Header Pinout Information

Only one possible pin configuration/ muxing solution is shown for the IMXRT1170 in schematic.

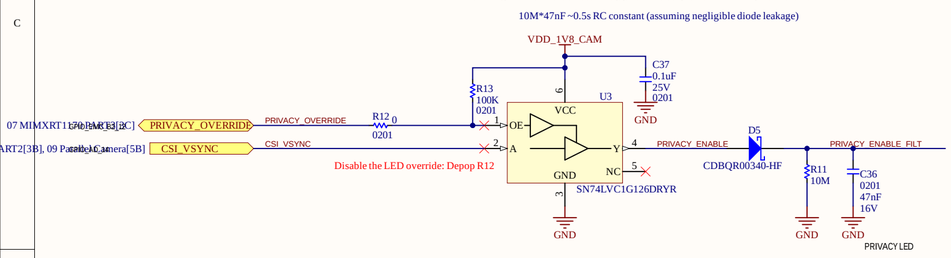
Should the user chooseto MUX pins differently, net names and function may not match schematic.

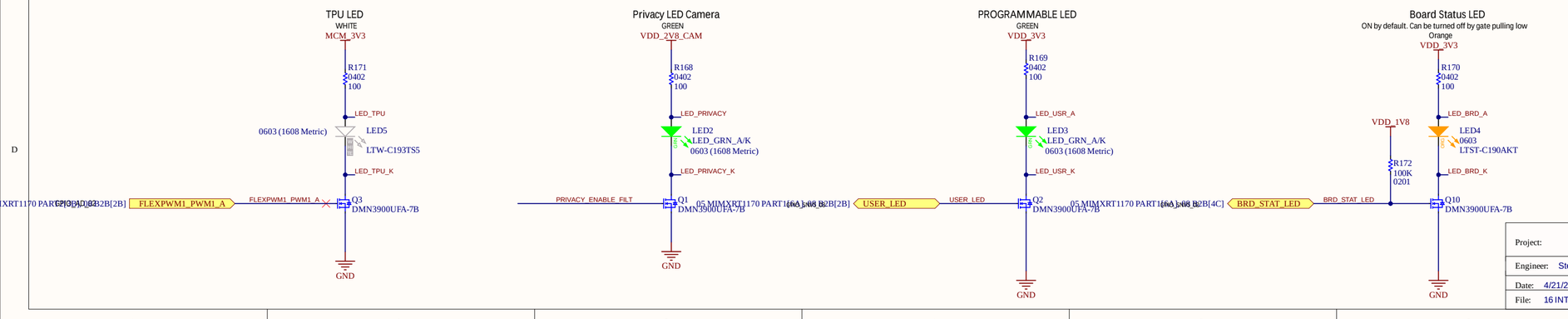
PRIVACY LED

Power Save Circuit

Use CSI VSYNC to trigger privacy LED.

Discharge RC time constant approximately 500ms. Likely to be shorter due to





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Coral

Coral Dev Board Micro: Revision History

Revision History

Rev. Code	Date	By	Description
1.0	2022-08-12	Stefan	Schematics prepared for release

Revision History

Rev. Code	Date	By	Description

Project:	*Coral Dev Board Micro*	*Proprietary and Confidential*	
Engineer: Stefan	Revision: PVT		
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