NXP Semiconductors
User's Guide

Document identifier: UM11159
Rev. 2, 06/2021

i.MX RT685 Evaluation Board User Manual

Contents

Chapter 1
Introduction

The i.MX RT685 Evaluation Board (part number MIMXRT685-EVK) is designed for customers to evaluate the i.MX RT685 MCU. It can be used with a range of development tools, including NXP MCUXpresso IDE. This User Manual describes Revision E of the board with B0 silicon.

NOTE

The EVK is subject to changes in future revisions.

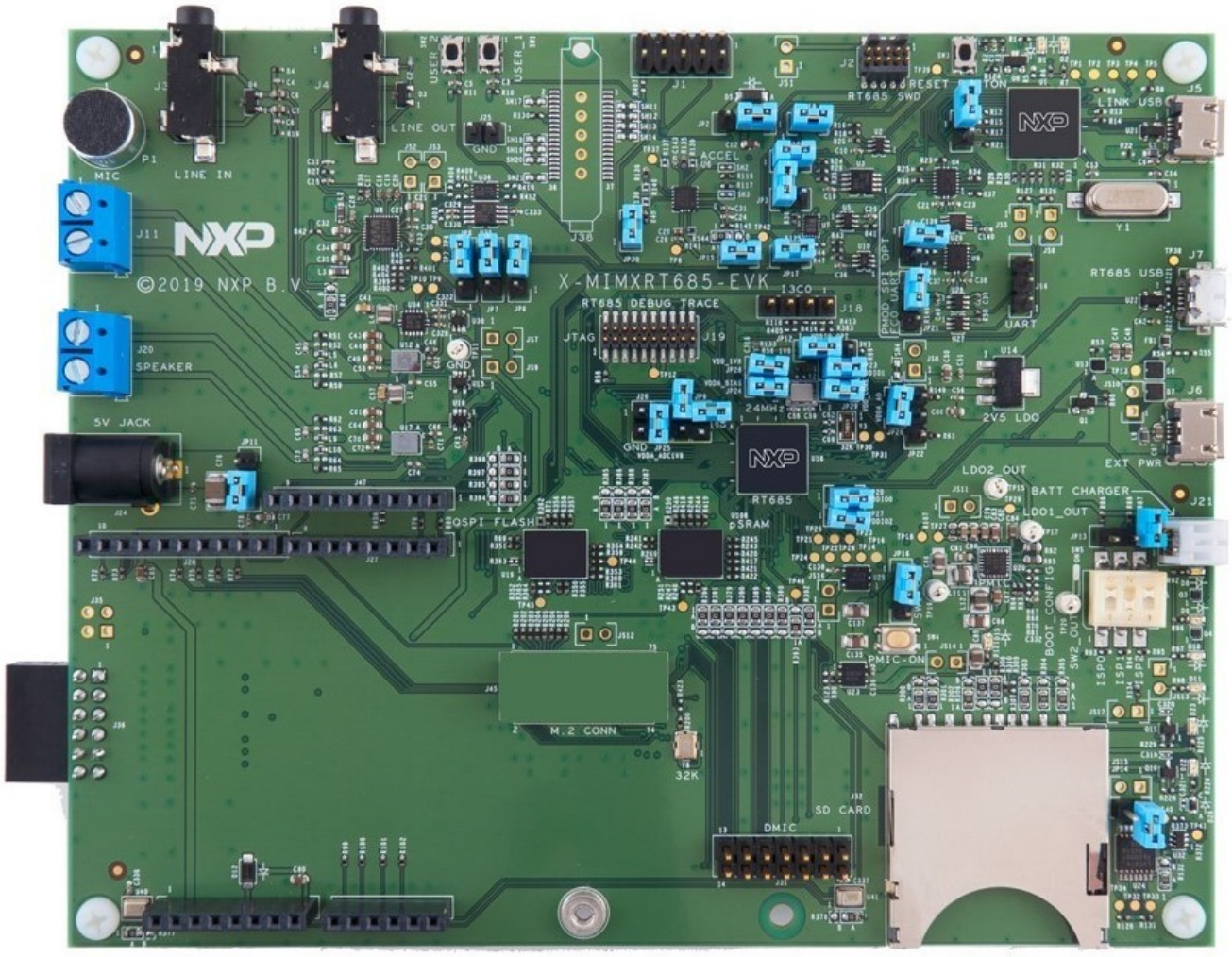

Figure 1. i.MX RT685 board

The i.MX RT685 EVK includes the following features:

- i.MX RT685 Cortex-M33 core processor with Cadence Xtensa HiFi4 DSP
- Onboard, high-speed USB, Link2 debug probe with CMSIS-DAP protocol (supporting Cortex M33 debug only)
- High-speed USB port with micro A/B connector for the host or device functionality
- UART, I2C, and SPI port bridging from i.MX RT685 target to USB via the onboard debug probe
- Optional external debug probe connections with trace option (10-or 20-pin Cortex-M connectors, later required for trace)

- 64 MB Macronix Octal SPI Flash operating at 1.8 V
- 8 MB AP memory PSRAM
- Full-size SD card slot (SDIO)
- NXP PCA9420UK PMIC
- User LEDs
- Reset and User buttons
- Arduino and Pmod/Host expansion connectors
- NXP FXOS8700CQ accelerometer
- Stereo audio codec with line in/out and electret microphone
- Stereo NXP TFA9894 digital amplifiers, with option for external +5 V power for higher performance speakers
- Support for up to eight off-board digital microphones via 12-pin header
- Two onboard DMICs

Chapter 2
Board Layout and Settings

Figure 2 shows the layout of the board (top side), indicating location of the connectors and buttons.

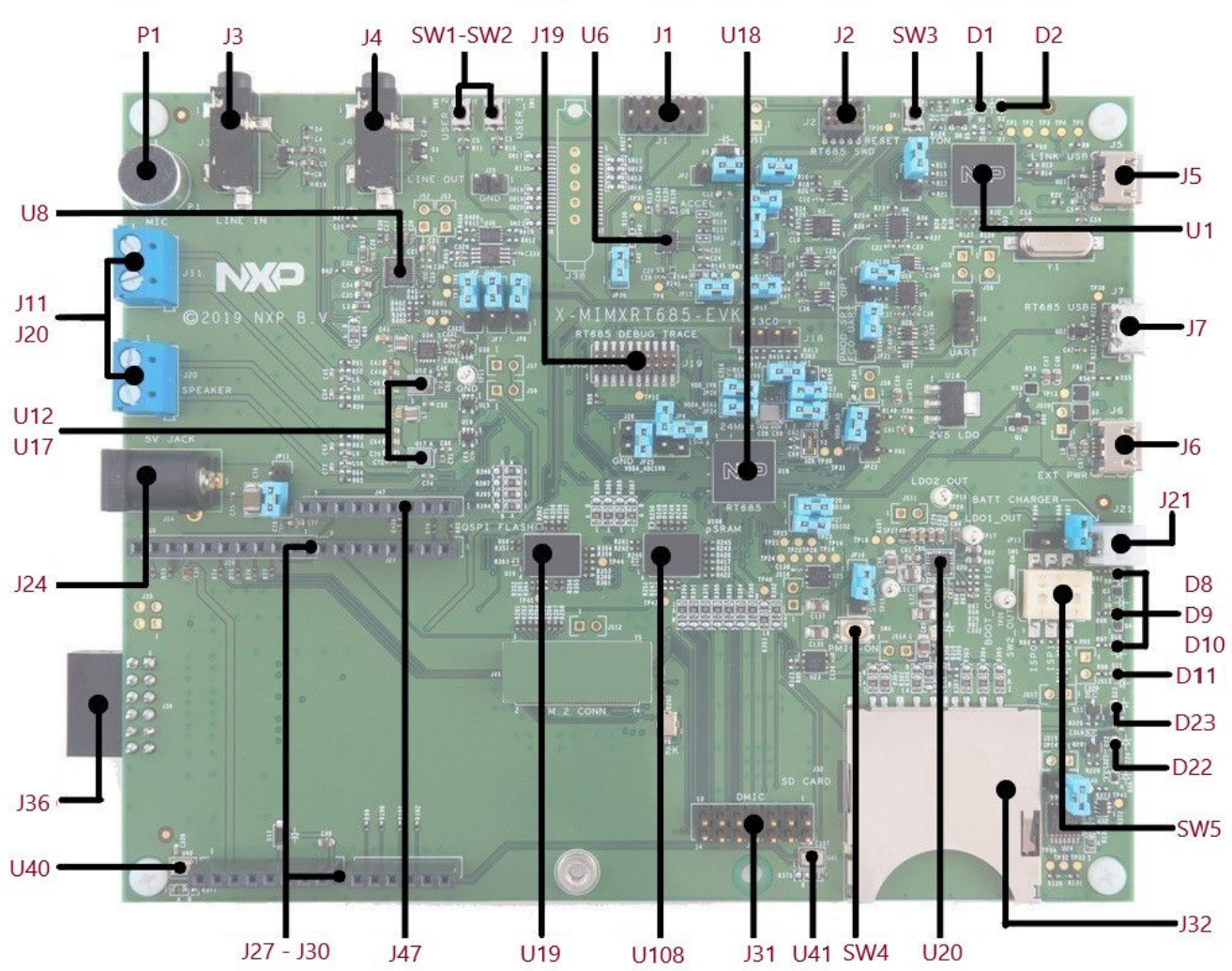

Figure 2. i.MX RT685 EVK connectors, LEDs, buttons, and headers

Table 1 provides a description of connectors, LEDs, and buttons.

Table 1. Connectors, LEDs, buttons, and headers

Circuit ref (Rev E)	Description	Default	Reference
D1	Reset LED	N/A	Schematic
D2	Link2 boot LED	N/A	Schematic
D8 - D10	User LEDs.	N/A	User LEDs

Table continues on the next page...

Table 1. Connectors, LEDs, buttons, and headers (continued)

Circuit ref (Rev E)	Description	Default	Reference
D11	3.3 V power-on LED (`LD2_OUT` when JS11 shunted)	N/A	Schematic
D15	SD card power LED (JS14 shunted)	N/A	Schematic
J2	10-pin Cortex-M target debug header.	N/A	Schematic
J3	Audio codec line input jack	N/A	Schematic
J4	Audio codec line output jack	N/A	Schematic
J5	On board debug probe (**LINK USB**) micro B USB connector	N/A	Schematic
J6	External +5 V power Micro USB connection for power to the i.MX RT685 target and peripheral circuitry (excluding Link2 Debug Probe).	N/A	Schematic
J7	Micro AB high-speed USB connector device/Host.	N/A	USB high-speed port
J19	Debug Trace Connector. 20-pin Cortex-M debug connector for i.MX RT685 target, including trace pins.	N/A	Schematic
J11, J20	Screw terminal connections for external speakers. When attaching a speaker, ensure that the appropriate driver settings are used in the TFA9894 devices to avoid damage to the speaker.	N/A	Schematic
J21	Batt charger.	N/A	Schematic
J24	Additional +5 V power connector. This barrel type connector may be used to supply additional power to the digital amplifiers, if needed. It does not power any of the other circuitries on the board.	N/A	Schematic
J27 – J30	J27, J28, J29, J30 Arduino expansion connectors.	N/A	Arduino connector
J31	External DMIC header. Provides access to all DMIC (PDM) clock and data lines, along with 1.8 V (default SW2_OUT)	N/A	External DMIC
J32	SD/eMMC Card socket.	N/A	SD/eMMC card slot
J36	Pmod/Host connector. This connector provides access to the	N/A	Pmod connector

Table continues on the next page...

Table 1. Connectors, LEDs, buttons, and headers (continued)

Circuit ref (Rev E)	Description	Default	Reference
	SPI and I^2C ports of the i.MX RT685 that are also designated for ISP boot. This connector can be used to work with a remote host, or as an interface to off-the-shelf Pmod expansion boards.		
J47	Flexcomm interface.	N/A	Flexcomm header
P1	Electret mic.	N/A	Schematic
SW1, SW2	User buttons. These buttons, when pressed, pulls the connected i.MX RT685 pin (`P1_1` for SW1 and `P0_10` for SW2) to ground. A 100 K ohm pull up to `VDDIO_1` is connected to the pin.	N/A	User buttons (SW1 and SW2)
SW3	Reset button. When pressed, reset is applied to the i.MX RT685, TFA9894 amplifiers, Octal SPI flash, pSRAM, expansion connector (Arduino reset, if JP14 is installed).	N/A	Reset
SW4	PMIC on button.	N/A	PMIC-ON
SW5	Boot Config switch. ISP boot mode selection. Switch the DIP switch for ISP port signal to **ON** to pull that pin low via a 1 K ohm resistor. Switch 1 is for ISP0, 2 for ISP1 and 3 for ISP2.	ISP0 ON ISP1 OFF ISP2 ON	ISP boot config
U1	LPC4322.	N/A	Schematic
U6	Accelerometer FXOS8700CQ.	N/A	Accelerometer
U8	Audio codec.	N/A	Audio codec
U12, U17	Digital Audio Amplifiers	N/A	Audio digital amplifiers
U18	MIMXRT685.	N/A	Schematic
U19	Octal SPI Flash.	N/A	Schematic
U20	PMIC. Programmable output voltage regulator with four different outputs: SW1, SW2, LDO1, and LDO2.	N/A	PMIC (PCA9420)
U40, U41	Onboard DMICs.	N/A	Onboard DMIC
U108	pSRAM	N/A	Schematic

Figure 3 shows location of jumpers and headers.

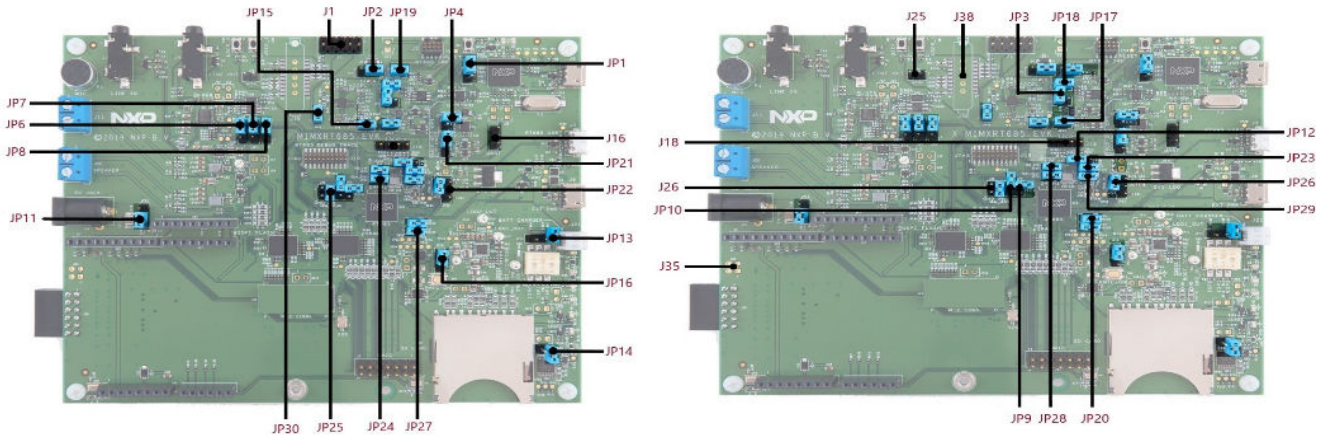

Figure 3. i.MX RT685 EVK jumpers and headers

Table 2 provides a description of jumpers and indicators.

Table 2. Indicators and jumpers

Circuit ref (Rev E)	Description	Default	Reference
JP1	Link2 (LPC43xx) force DFU boot. Leave this jumper open (default) for Link2 to follow the normal boot sequence. The Link2 boots from flash if image is found there. With the flash erased the Link2 normal boot sequence will fall through to DFU boot. Install this jumper to force the Link2 to DFU boot mode. Use this setting to reprogram the Link2 internal flash with a new image (using the LPCScrypt utility) or to use the MCUXpresso IDE with CMSIS-DAP protocol. The Link2 flash is pre-programmed with a version of CMSIS-DAP firmware by default.	Open	Schematic
JP2	Buffer Power Selection For onboard Target, place in position 1-2 (default) For Off-board Target, place in position 2-3	1-2	Schematic
JP3	Target processor selection for the onboard Debug Probe. If jumper is open (default), the i.MX RT685 Target SWD interface is enabled. Normal operating mode	Open	Schematic

Table continues on the next page...

Table 2. Indicators and jumpers (continued)

Circuit ref (Rev E)	Description	Default	Reference
	where the Target SWD is connected to either the onboard Link2 Debug Probe or an external Debug Probe. If jumper is shunted, the i.MX RT685 Target SWD interface is disabled. Use this setting only when the onboard Link2 Debug Probe is used to debug an off-board target MCU.		
JP4	When open (default), the **Bridge** UART and SPI connections from the Link2 probe are driven to the i.MX RT685 target. Install JP4 when using the SPI interface at connector J36 and/or FC0 UART at J16. Note: It disables the Link2 SPI and UART (VCOM/ bridge) connections.	Open	Schematic
JP6	Interrupt source select for audio devices, controlling which audio device drives the interrupt to i.MX RT685 Port 0 pin 0. Insert in position 1-2 for the audio codec or 2-3 for the TFA9894 amplifiers.	2-3 (digital amplifiers)	Audio codec and Audio digital amplifiers
JP7, JP8	I2S data select for audio devices, controlling which audio device drives the I2S connections to the i.MX RT685 I2S port. Insert in position 1-2 for the audio codec or 2-3 for the TFA9894 amplifiers. i.MX RT685 `PIO0_9` used for data transmit and `PIO0_23` for data receive.	2-3 (digital amplifiers)	Audio codec and Audio digital amplifiers
JP9, JP10	ADC reference connector This header provides an access point to inject positive and negative voltage references for the i.MX RT685 ADC. An external positive reference may be connected to JP10 pin 2. An external negative reference may be connected to JP9 pin 1.	Open	MIMXRT685-EVK ADC references and inputs
JP11	Selection jumper for digital amplifier +5 V supply. Install in position 1-2 to draw digital amplifier supply from J6 (Rev E) power connector, or in	1-2	Schematic

Table continues on the next page...

Table 2. Indicators and jumpers (continued)

Circuit ref (Rev E)	Description	Default	Reference
	position 2-3 when external power supply (J24) is used.		
JP12	Voltage/supply selector for i.MX RT685 VDDIO_1 power domain. Selects between PMIC output LDO2_OUT (position 2-3) or SW2_OUT (position 1-2). The PMIC is programmed to default to SW2_OUT at 1.8 V and LDO2_OUT at 3.3 V, but can be reprogrammed on-the-fly by the i.MX RT685.	1-2 SW2_OUT 1.8 V	Schematic
JP13	Host ISP control selection. This header/jumper can be used to select which of the Port 1 pin 15 (ISP0) or pin 16 (ISP1) signals is routed to the Interrupt/ISP pin on the Pmod/Host connector. These signals from can be used as GPIO/interrupts to/from the i.MX RT685, and may be used to determine its boot mode following reset.	Header is not installed by default, but position 1-2 is shorted to select ISP1/P1-16.	Schematic
JP14	Reset enable/disable to Arduino. Install jumper to route the i.MX RT685 reset control signal to the standard Arduino reset pin.	Open	Schematic
JP15	Power supply to FXOS8700CQ accelerometer. Connects 3.3 V from linear regulator U25 to the accelerometer 3.3 V supply input. The I/O voltage for this device is connected to the VDDIO_1 supply rail of the i.MX RT685.	Closed	Schematic
JP16	On button control to PMIC. Set as directed by NXP.	1-2	Schematic
JP17, JP18, JP19	SWD port isolation jumpers. When using the VCOM port and an external debug probe, remove these jumpers to prevent contention with the onboard debug probe (LPC432x device).	All closed	Schematic
JP20	VDDIO_0 supply connection to PMIC / external supply injection. This jumper is provided for optional insertion of an ammeter to measure supply current	Closed	Measuring MIMXRT685-EVK device supply current

Table continues on the next page...

Table 2. Indicators and jumpers (continued)

Circuit ref (Rev E)	Description	Default	Reference
	to the i.MX RT685 VDDIO_0 supply pins.		
JP22	Selects the value of LDO_ENABLE. High (1-2) or Low (2-3).	2-3	Schematic
JP23	This jumper is provided for optional insertion of an ammeter to measure supply current to the i.MX RT685 VDDIO_1 supply pins.	Closed	Measuring MIMXRT685-EVK device supply current and Schematic
JP24	This jumper is provided for optional insertion of an ammeter to measure supply current to the i.MX RT685 VDDA_BIAS supply pins.	Closed	Measuring MIMXRT685-EVK device supply current and Schematic
JP25	This jumper is provided for optional insertion of an ammeter to measure supply current to the i.MX RT685 VDDA_ADC1V8 supply pins.	Closed	Measuring MIMXRT685-EVK device supply current and Schematic
JP26	This jumper is provided for optional insertion of an ammeter to measure supply current to the i.MX RT685 VDDA_AO supply pins.	Closed	Measuring MIMXRT685-EVK device supply current and Schematic
JP27	This jumper is provided for optional insertion of an ammeter to measure supply current to the i.MX RT685 VDDIO_2 supply pins.	Closed	Measuring MIMXRT685-EVK device supply current and Schematic
JP28	This jumper is provided for optional insertion of an ammeter to measure supply current to the i.MX RT685 RT685 VDD1V8 supply pins.	Closed	Measuring MIMXRT685-EVK device supply current and Schematic
JP29	This jumper is provided for optional insertion of an ammeter to measure supply current to the i.MX RT685 Core.	Closed	Measuring MIMXRT685-EVK device supply current and Schematic
JP30	This jumpers routes P1_5 to the accelerometer interrupt pin.	Closed	Schematic
J1	Additional / spare signal expansion header.	N/A	Additional expansion header
J16	UART header for i.MX RT685 Flexcom 0 UART. Note: JP4 must be installed when using this UART to avoid conflicts with the onboard debug probe.	N/A	USART header
J18	Header for access to I3C port. Note that this port is also shared with the	N/A	I3C header

Table continues on the next page...

Table 2. Indicators and jumpers (continued)

Circuit ref (Rev E)	Description	Default	Reference
	audio devices on the board (codec and amplifiers).		
J25, J26	Ground headers, provided for convenient connection to ground.	N/A	Schematic
J35	Host reset control header. Provides a connection point for an external host to drive the reset of the i.MX RT685 (and other devices sharing this reset).	Open	Schematic
J38	Footprint-only for Trace Mictor 38 Adapter gives you the ability to perform trace.	N/A	Schematic

Chapter 3
Getting Started

This section describes how to first power up the board and then how to start a first debug session using the MCUXpresso SDK. The board is pre-programmed with a simple program indicating that the target MCU is running. Connect a micro USB cable from connector J5 (**LINK USB**) to a host computer or power supply to power up the board and run this program.

The following debug probes can be used with the board:

- Onboard debug probe (LPC4322 **Link2**), Cortex® M33 only.
- SEGGER J-link probes (version 9 or newer)

Other debug probes may also be supported by IAR and Keil tools and by other IDEs/debug tools. Refer to the websites of these companies for further information.

3.1 Starting a debug session using the onboard (Link2) Debug Probe

By default, the i.MX RT685 EVK is configured to use the onboard Debug Probe (**Link2**) to debug the onboard target (i.MX RT685), using the CMSIS-DAP debug protocol pre-programmed into the Link2 Flash memory. The MCUXpresso IDE or other development tools that support the CMSIS-DAP protocol can be used in the default configuration (once support is released for those tools). Check with your toolchain vendor for availability of specific device support packs for the i.MX RT685 series devices.

When using the MCUXpresso IDE, the onboard Link2 can also be booted in the DFU mode (see jumper settings). If this is done, MCUXpresso IDE downloads the CMSIS-DAP protocol to the probe as needed. Using the DFU boot mode ensures that the most up-to-date/compatible firmware image is used with the MCUXpresso IDE.

NOTE

If the Debug Probe is set up to boot in DFU mode, the USB bridge functions (virtual COM port) and Debug Probe features will not be available if the board is not first initialized by the MCUXpresso IDE.

3.1.1 Installation steps to use with MCUXpresso IDE

1. Download and install the MCUXpresso IDE v11.1.1 or above.
2. Configure and download an SDK package (with the MCUXpresso IDE tool chain option selected) from the MCUXpresso SDK Builder utility (http://mcuxpresso.nxp.com).

   Install JP1 to force the Link2 Debug Probe to boot in DFU mode (see Note in Starting a debug session using the onboard (Link2) Debug Probe).
3. Ensure that:
   - The jumper JP2 is fitted in position 1-2, local target powered.
   - The jumper JP3 is not installed, target SWD enabled.

   These are the default positions set during board manufacture.
4. Connect the board to the USB port of your host computer, connecting a micro USB cable to connector J5.
5. Allow about 10 seconds for the i.MX RT685 EVK device to enumerate for the first time. The device appears as **LPC-Link2 UCom Port**.

If the first attempt to debug a project fails in the IDE, cancel the debug session and repower the board. On some machines the drivers take longer to enumerate for the first time, so these steps should correct this issue.

3.1.2 Installation steps to use Keil and IAR tools

1. Download and install LPCScrypt or the Windows drivers for LPCXpresso boards (http://www.nxp.com/lpcutilities). This will install required drivers for the board.

NOTE

The Link2 (LPC4322 device) is pre-programmed with CMSIS-DAP firmware during manufacture, so you do not need to program it.

2. Ensure that jumper JP1 is open to force the Link2 Debug Probe to boot from internal flash.
3. Ensure that jumper JP2 is fitted in position 1-2, and JP3 is not installed. These are the default positions set during board manufacture.
4. Connect the i.MX RT685 board to the USB port of your host computer, connecting a micro USB cable to connector J5 (**Link USB**). Allow about 30 seconds for the Link2 devices to enumerate for the first time. It is not necessary to check the Hardware Manager. If this is done, there will be:
   - five devices (if using CMSIS-DAP protocol).
   - four under Human Interface Devices (CMSIS-DAP, LPC-SIO, two HID Compliant Devices, and a USB Input Device).
   - one under Ports (LPC-LinkII UCom.).

Your board is now ready to use with your 3rd-party tool. Follow the instructions for those tools for using a CMSIS-DAP probe. MCUXpresso IDE can also be used with the board after setting up the board this way.

NOTE

If you use IAR, use IAR v8.40 or above.

3.1.3 Starting a debug session using an external Debug Probe

Code running on the i.MX RT685 target can be debugged using an external Debug Probe that conforms to the standard Arm® Cortex-M debug connectors (either 10 or 20 pin). To use an external Debug Probe connect the probe to one of the SWD connectors (J2 or J19) and connect power via the micro USB connector J6.

When using a Revision E board, the Debug link connector (J5) can still be used to power the board, and the VCOM function of the LPC432x can also be used, but JP17, JP18 and JP19 must be removed to prevent contention between the external and onboard debug probes on the SWD port of the i.MX RT685.

Chapter 4
Onboard (Link2) Debug Probe

This section describes the features provided by the onboard Link2 Debug Probe, including how to use this to debug an external target.

The Link2 Debug Probe is implemented using an LPC43xx MCU, which provides a high-speed USB port interface to the host computer that runs the development tools. This device is not intended for developer use and should only be used with approved firmware images from NXP. The Link2 on-chip flash memory is factory programmed with a firmware image that supports CMSIS-DAP debug protocol, but also includes other USB end-point functions.

- Virtual COM (VCOM) port: a serial device that can be used with any host computer application design for serial port communication (for example, Teraterm, puTTY, and s on). Set the terminal program for baud rate to 115200, no parity, 8-bit data, 1 stop bit, no flow control.
- SWO trace end point: this virtual device is used by MCUXpresso to retrieve SWO trace data. See the MCUXpresso IDE documentation for more information.

All of these devices are independent of each other and of the CMSIS-DAP debug device that is enumerated when the board is connected to a host computer; for example, the VCOM port can be used if the board is running an application when no debugger is running.

In order to correctly install and use the Link2 device on the i.MX RT685 EVK (required for any debugging purpose) for Windows 7 (or later) host computers, install the drivers first. These drivers will automatically be installed when MCUXpresso IDE has already been installed. If these IDEs are not being used, it is recommended LPCScrypt be installed as this also includes the required drivers. All these tools and utilities are available for free download at https://www.nxp.com/lpcscrypt.

The CMSIS-DAP firmware image installed at the factory (and by LPCScrypt) will uniquely identify itself to the host computer so that more than one board can be connected to that host computer at any time. Some toolchains cannot discern between multiple debug devices. Refer to your toolchain documentation for more information.

The MCUXpresso does support multiple LPCXpresso board targets. It is recommended to use LPCScrypt to update the Debug Probe firmware to ensure that the latest version is being used.

NOTE

The Link2 only boots when the board is power cycled. The reset button on the board does not reset the Link2.

When using MCUXpresso IDE, the Link2 can be automatically booted with the latest/most appropriate firmware for that IDE version by installing JP1 DFU jumper before powering up the board. It is the recommended approach for the MCUXpresso IDE.

If JP1 is installed when powering the board, the VCOM port (and other devices mentioned above) device will not appear until the MCUXpresso IDE boots the Debug Probe. The Debug Probe is booted once a debug session is started (that is, the IDE attempts to download code to the target).

4.1 Programming the Link2 firmware

As mentioned earlier in this section, it is not normally necessary to program the Link2 firmware. However, this can easily be accomplished using the supporting utility, LPCScrypt.

To program the Link2 Flash, the Link2 device (LPC432x) must be in DFU mode. If the Link2 already has a valid image in the flash, it will need to be forced into DFU mode by placing a jumper shunt on JP1, and power cycling (disconnecting then reconnecting power). Link2 MCU programming is performed using the LPCScrypt utility (see http://www.nxp.com/lpcscrypt). Instructions for using the tool are located at the same webpage.

4.2 VCOM port

The identifier of the VCOM port will vary between boards and hosts as each board will enumerate with a unique identifier. On Windows, to determine the COM port, open the Windows operating system Device Manager. This can be achieved by going to

the Windows operating system Start menu and typing **Device Manager** in the search bar. In the **Device Manager** under **Ports**; the LPC-LinkII UCom Port device and its name should be visible.

NOTE

This VCOM port appears:

- If the Debug Probe has been programmed with the CMSIS-DAP firmware and the Debug Probe DFU link (JP1) is removed at power-up.
- If the Debug Probe has been configured for DFU boot (JP1) installed at power-up and MCUXpresso IDE has booted it (by starting a debug session).

Chapter 5
Board Power

The MIMXRT685-EVK requires +5 V input to power the onboard voltage low dropout linear regulators, of which there are 3.

Link2 Debug probe has a 2.5 V regulator (U14) which draws power from USB connector J5 (**LINK USB**) only. The debug probe is unpowered if J5 is unconnected.

There are two other regulators, both providing the option of 3.3 V, one (U25) for Arduino Interface (DCDC_3V3), Accelerometer sensor (VDD_ACCEL) and USART (VDD_LDO_3V3) the other for SD Card supply (U23); these regulators can be powered by any of the following (+5 V) sources:

- USB Debug Link connector (J5)
- USB External +5 V only connector (J6)
- USB high-speed connector (J7)

The +5 V sources above are connected via protection diodes to prevent reverse powering of any of them by another source. Note that if J7 is configured as USB host port then that connector will not supply power to the board and another source must be provided.

For further details on the power sequence needed by the RT600, refer to **Power Sequencing** in the device data sheet.

5.1 Measuring MIMXRT685-EVK device supply current

Current supply to the RT685 Core can be measured via JP29 (VDDCORE). The voltage supplied can be measured on TP19 (SW1_OUT output voltage from PMIC).

GPIO current supplies can be measured via JP20 (VDDIO_0), JP23 (VDDIO_1) and JP27 (VDDIO_2).

Other headers to measure power are JP24 (VDDA_BIAS), JP25 (VDDA_ADC1V8), JP26 (VDDA_AO) and JP28 (VDD1V8).

For further details, refer to boards schematics.

5.2 PMIC (PCA9420)

The MIMXRT685-EVK has a Power Management Integrated Circuit. Using the PMIC adds flexibility to configure the power supply rails according to the needs of the application. PMIC has four output voltages, SW1_OUT, SW2_OUT, LDO1_OUT, and LDO1_OUT.

Table 3. PMIC Output voltages

PMIC output voltage	RT00 input voltage	Output voltage ranges	Default value
SW1_OUT	VDDCORE	0.5 - 1.5 V	1.0 V
SW2_OUT	VDDIO_0 VDD1V8 VDDA_ADC1V8 VDDIO_1 (JP12, 1-2)	1.5 - 2.1 V/2.7 - 3.3 V	1.8 V
LDO1_OUT	VDD_A0	1.7 - 1.9 V	1.8 V
LDO2_OUT	VDDIO_2 VDDIO_1 (JP12, 2-3)	1.5 - 2.1 V/2.7 - 3.3 V	3.3 V

PMIC is configured via I^2C and external pins.

Table 4. PMIC pins

PMIC	IMXRT685
SCL	PMIC_I2C_SCL
SDA	PMIC_I2C_SDA
MODESEL0	PMIC_MODE0
MODESEL1	PMIC_MODE1
INT	PMIC_IRQ_N
SYSREST	RESET
ON	SW4 (JP16, 1-2)

For further information, refer to the board schematic.

Chapter 6
Board Serial Connections

This section describes connections between MIMXRT685-EVK onboard serial peripherals and connectors for use with off-board devices.

6.1 USB high-speed port

The board incorporates micro AB connector for of USB0 (High Speed, connector J7) port of the MIMXRT685-EVK. USB0 port can operate as a device or a host.

The resistor divider on the VBUS pin (R54 and R55) should be depopulated if user chooses to use the VBUS_VALID comparator to monitor the VBUS supply for a host mode application.

NOTE

The power must be supplied to the board via the external power-only USB connector (J6) when this USB port is configured for host operation.

For further details, refer to the High-speed Device/Host Controller on the User Manual.

6.2 USART header

Header J16 is provided as a convenient way to use the USART with a serial to USB cable. Flexcom 0 ports (`P0_1` and `P0_2`) are used for this feature, since these ports are assigned for USART ISP mode.

These ports are shared with the Link2 debug probe (LPC4322) and Pmod connector. When using this header, ensure that there is no conflicting device connected to the Pmod connector and that jumper JP21 [2-3] is set to disable the connection to the Link2.

6.3 I3C header

The MIMXRT685-EVK provides a header (J18) to easily interface with an I3C serial interface.

6.4 Flexcomm header

The MIMXRT685-EVK provides a Flexcomm interface (J47) with up to eight configurable universal serial interface modules. Each module can be configured as: USART, I^2C Bus, SPI Interface or I2S interface for digital audio.

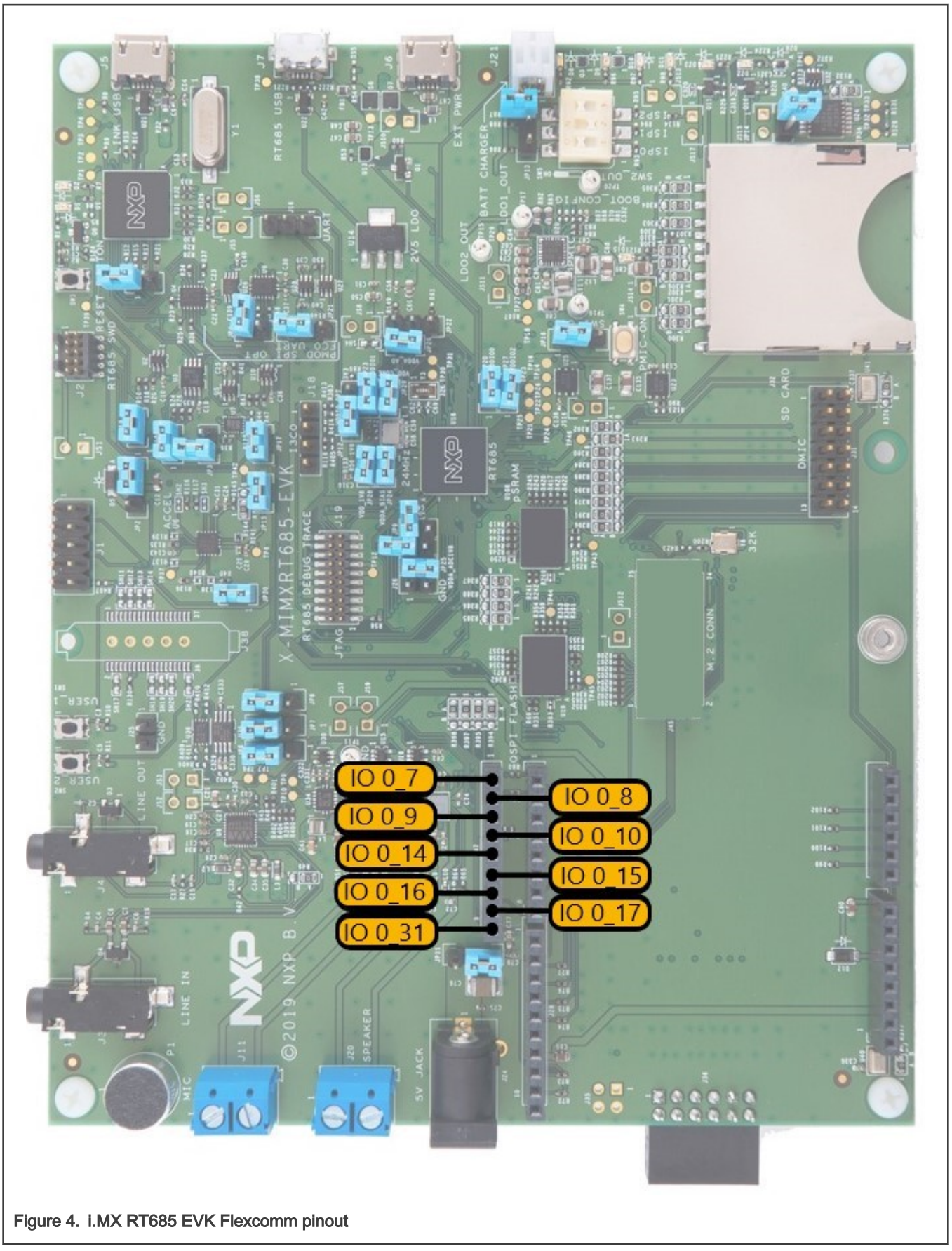

Figure 4. i.MX RT685 EVK Flexcomm pinout

6.5 Additional expansion header

This section shows the pinout for the additional header J1.

Table 5. Additional header port pinout

Header pin	Port
Pin 1	P2_11
Pin 2	P2_13
Pin 3	P0_3
Pin 4	P2_12
Pin 5	P0_4
Pin 6	P0_13
Pin 7	P0_12
Pin 8	P2_15
Pin 9	P2_14
Pin 10	P0_11

Chapter 7
Onboard Peripherals

This section describes how the onboard peripheral devices of the board are connected to the IMXRT685 and relevant configuration options. For details of these devices, refer to the individual device datasheets. For further details on the circuit, refer to the board schematics.

7.1 Audio codec

The MIMXRT685-EVK board incorporates a Cirrus Logic WM8904 audio codec. This codec has both I^2C (for control) and I^2S (for data) interfaces. The I^2C interface of the codec is routed to Port 2 of the IMXRT685, with the same connection for the audio amplifiers and the I3C header on the board. The codec has an address of `0b0011010`.

The I^2S interface of the codec is routed to Port 0 of the IMXRT685, the same connection as used for the audio amplifiers.

Depending on the voltage of `VDDIO_1`, the audio codec is designed to operate with two options, with level shifter (U35 and U36) and without level shifter.

Table 6. Audio codec port connections

Circuit reference	Port
I2C SDA	`P2_30`
I2C SCL	`P2_29`
I2S BLCK	`P0_7`
I2S DAI	`P0_9`
I2S DAO	`P0_23`
I2S WS	`P0_8`
CODEC MCLK	`P1_10`

There are three jumpers (JP6, JP7, and JP8) to select IMXRT685 I2S connections lines between codec and amplifier. To select the codec, jumpers must be (1-2). See schematic for further information.

Line input (J3) and line output (J4) ¼” stereo jack sockets provide analog I/O connections to the codec. See schematic for further information.

7.2 Audio digital amplifiers

A pair of audio amplifiers is included on the MIMXRT685-EVK. Select the external supply between JP24 5 V Jack (JP11, 2-3) or J6 USB (JP11, 1-2). The I^2C interface of the amplifiers is routed to Port 2 of the IMXRT685, the same connection as used for the codec and the I3C header on the board.

The I^2S interface of the amplifiers is routed to Port 0 of the IMXRT685, with the same connection for the codec.

Depending on the voltage of `SW2_OUT`, the audio AMP operates at either 1.8 V or 3.3 V. A level shifter (U34) is added.

Table 7. Digital audio amplifier port connections

Circuit reference	Port
I2C SDA	`P2_30`
I2C SCL	`P2_29`

Table continues on the next page...

Table 7. Digital audio amplifier port connections (continued)

Circuit reference	Port
I2S BLCK	P0_7
I2S DAI	P0_9
I2S DAO	P0_23
I2S WS	P0_8

7.3 SD/eMMC card slot

The SD card (J32) included in the MIMXRT685-EVK board provides a 4-bit SDIO interface to support memory cards, plug-in WiFi modules, and so on. Power enable to the socket is provided via P2_4.

Software drivers and related examples for the SD card are provided as part of the MCUXpresso SDK.

Table 8. Micro SD card connections

SDIO interface signals	Circuit reference	Port	Notes
SDIO Clock	SD_CLK	P1_30	ICON function 2
SDIO Command	SD_CMD	P1_31	ICON function 2
D0	SD_DAT0	P2_0	ICON function 2
D1	SD_DAT1	P2_1	ICON function 2
D2	SD_DAT2	P2_2	ICON function 2
D3	SD_DAT3	P2_3	ICON function 2
Card detect	SD_CD	P2_9	ICON function 2
Power enable	SD_WR_PRT	P2_4	ICON function 2

For further details, refer to the boards schematics and SD/MMC chapter on the User Manual.

7.4 Accelerometer

The board includes an NXP FXOS8700CQ accelerometer, interfaced to port 0 (P0_17 and P0_18) with its interrupt output connected to P1_5 (JP30 has to be populated). The accelerometer has an I^2C address of 0b00011110 (0x1E). See schematic for further information. JP15 must be installed to provide voltage supply to the accelerometer.

I^2C software drivers are provided as part of the MCUXpresso SDK, and example code is provided to illustrate how to read values from the accelerometer.

7.5 User LEDs

Three user LEDs are provided on the board. The LEDs in this device are controlled by with the LEDs being illuminated when the respective LED is pulled low.

7.6 Buttons

Four buttons are provided on the MIMXRT685-EVK, as described in this section.

7.6.1 User buttons (SW1 and SW2)

SW1 (P1_1) and SW2 (P0_10) buttons are intended for user application use. These buttons pull ports low when the button is pressed. 100 kΩ resistors are used to pull these two ports to VDDIO1 when the buttons are not pressed.

7.6.2 Reset

Pressing this button (SW3) will assert reset to the MIMXRT685-EVK, TFA9894 amplifiers, pSRAM and OctalSPI Flash. If you want to route the i.MX RT685 reset control signal to the standard Arduino reset pin, install JP14.

NOTE

The Debug Probe (LPC4322) is not reset when this button is pressed.

7.6.3 PMIC-ON

Press and release to turn on the PMIC. Do not press down for more than three seconds.

7.7 ISP boot config

The ISP pins (`PIO1_15`, `PIO1_16`, and `PIO1_17`) select the boot source.

Table 9. Boot config

Boot mode	ISP2 pin `PIO1_17`	ISP1 pin `PIO1_16`	ISP0 pin `PIO1_15`	Description
—	Low	Low	Low	Reserved
SDIO0 (SD Card)	Low	Low	High	Boot from an SD card device connected to SDIO 1 interface. The RT6xx looks for a valid image in the SD card device. If there is no valid image found, the RT6xx enters the ISP boot mode based on OTP `DEFAULT_ISP_MODE` bits (6:4, `BOOT_CFG[0]`).
FlexSPI Boot from Port B	Low	High	Low	Boot from Quad/Octal SPI Flash devices connected to the FlexSPI interface 0 Port B. The RT6xx looks for a valid image in the external Quad/Octal SPI Flash device. If there is no valid image found, the RT6xx enters recovery boot or ISP boot mode.
FlexSPI Boot from Port A	Low	High	High	Boot from Quad/Octal SPI Flash devices connected to the FlexSPI interface 0 Port A. The RT6xx looks for a valid image in

Table continues on the next page...

Table 9. Boot config (continued)

Boot mode	ISP2 pin PIO1_17	ISP1 pin PIO1_16	ISP0 pin PIO1_15	Description
				the external Quad/Octal SPI Flash device. If there is no valid image found, the RT6xx enters recovery boot or ISP boot mode.
SDIO0 (eMMC)	High	Low	Low	Boot from a eMMC device connected to SDIO 0 interface. The RT6xx looks for a valid image in the SD card device. If there is no valid image found, the RT6xx enters the ISP boot mode based on OTP DEFAULT_ISP_MODE bits (6:4, BOOT_CFG[0]).
—	High	Low	High	Reserved
Serial ISP (UART, SPI, I^2C, USB-HID)	High	High	Low	The Serial Interface (UART, SPI, and I2C, USB-HID) is used to program OTP, external Flash, SD, or eMMC device.
111	High	High	High	Serial Master boot (SPI Slave, I^2C Slave, or UART, USB-HID) is used to download a boot image over the serial interface (SPI Slave, I^2C Slave, or UART, USB-HID)

For further details, refer to RT6xx Non-Secure Boot ROM in *RT6xx User Manual* (document UM11147).

7.8 DMIC

MIMXRT685-EVK provides two DMIC interfaces described below.

7.8.1 Onboard DMIC

The MIMXRT685-EVK incorporates a couple of DMICs on the board. Both DMICs share the data and clock signals and are directly routed to the Port 2 of the MIMXRT685.

NOTE

These pins are shared with the External DMIC. By default, onboard DMICs are selected (see R379 and R380). For further details, refer to the board schematics.

Table 10. Onboard DMIC connections

Circuit reference	Port
PDM_CLK01_OnBoard	P2_16
PDM_DATA01_OnBoard	P2_20

7.8.2 External DMIC

The external DMIC it is a 14-pin adapter that supports up to eight DMIC channels. The clock and data pins are shared with the onboard DMIC. By default, onboard DMICs are selected. You must move R379 (2-3) and R380 (2-3) to use this header. For further details, refer to the board schematics.

Table 11. External DMIC connections

Circuit reference	Port
PDM_CLK01_Ext (Not connected by default)	P2_16
PDM_DATA01_Ext (Not connected by default)	P2_20
PDM_CLK23_A	P2_17
PDM_DATA23_A	P2_21
PDM_CLK45_A	P2_18
PDM_DATA45_A	P2_22
PDM_CLK67_A	P2_19
PDM_DATA67_A	P2_23
I2C SCL	P0_11
I2C SDA	P0_10

Chapter 8
Expansion Connectors

The MIMXRT685-EVK includes two expansion connector sets, incorporating support for Arduino and Pmod standards. Pinout diagrams are provided in Figure 5 and Figure 6.

For further details, refer to the board schematics.

8.1 Pmod connector

Connector J36 is an optional connector which can provide access for a remote host to the SPI and I^2C ports for the RT6xx that support ISP mode.

Table 12. Pmod connections

Pmod pin	Circuit reference	Port
Pin 1	P1_14_SPI_SS0_A	P1_14
Pin 2	BRIDGE_INTR_ISP	P1_16 (JP13)
Pin 3	P1_13_SPI_MOSI_A	P1_13
Pin 4	P0_3	P0_3
Pin 5	P1_12_SPI_MISO_A	P1_12
Pin 6	P0_15_FC2_SCL	P0_15
Pin 7	P1_11_SPI_CLK_A	P1_11
Pin 8	P0_16_FC2_SDA	P0_16
Pins 9, 10	GND	N/A
Pins 11, 12	VDD_PMOD	VDDIO1 (JS9)

8.2 Arduino connector

The connectors J27-J30 provide Arduino compatibility and access to several other signals for use in prototyping. Some ports used on these connectors are shared with other devices/connectors on the board. Refer to the schematic for further information.

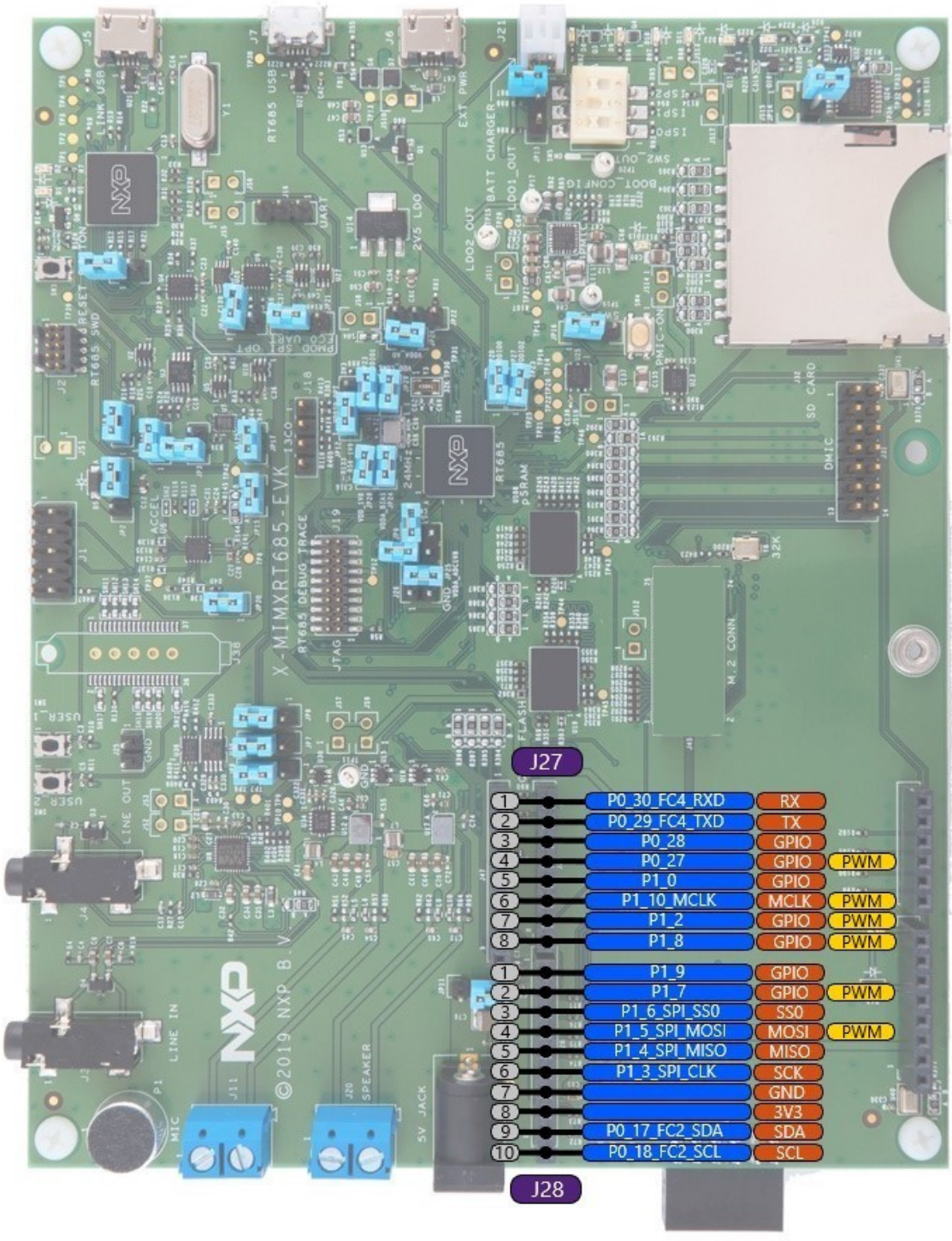

Figure 5. i.MX RT685 EVK Arduino J27 and J28 headers pinout

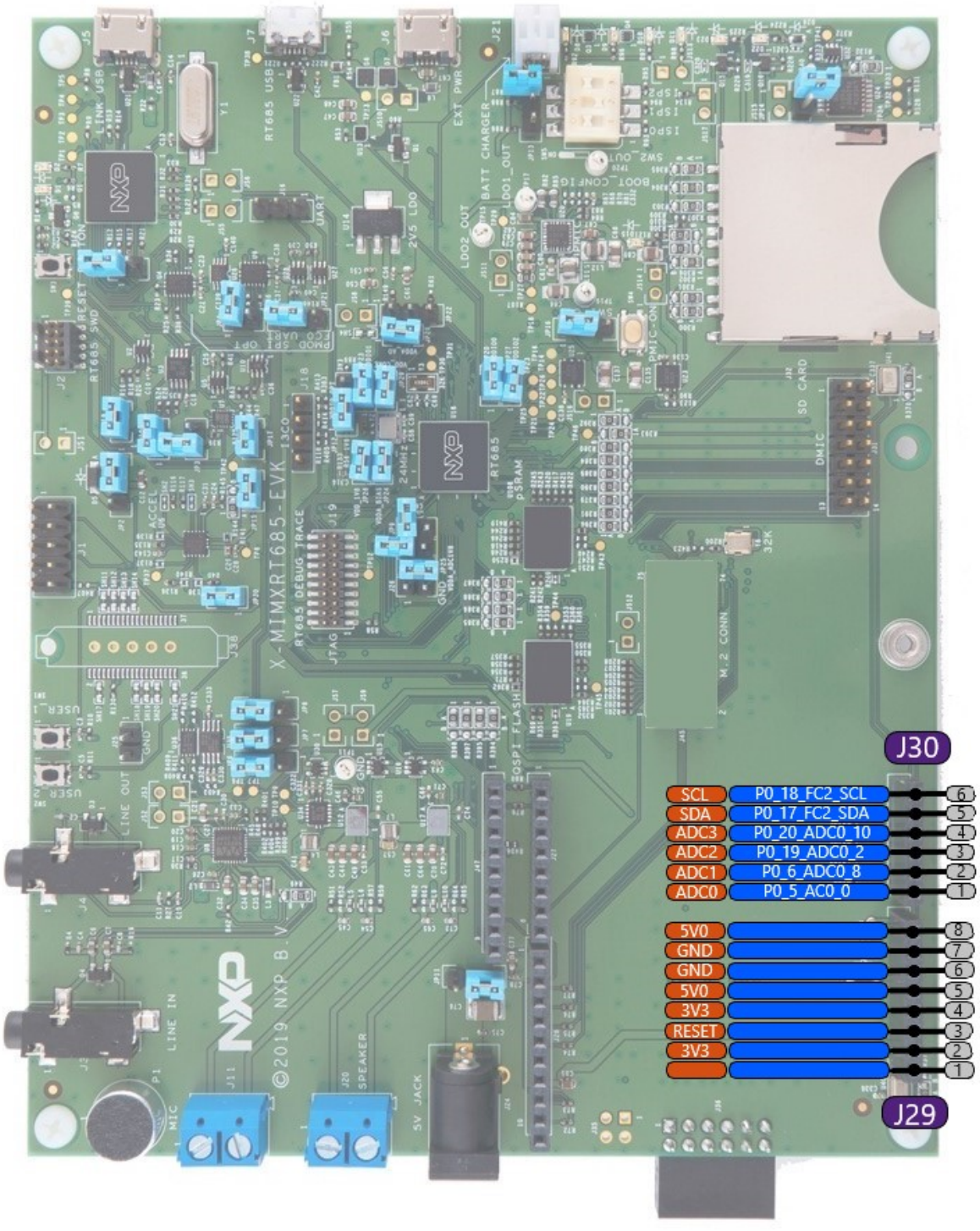

Figure 6. i.MX RT685 EVK Arduino J29 and J30 headers pinout

Chapter 9
Other Board Features

This section describes miscellaneous board features not covered in this manual.

9.1 MIMXRT685-EVK ADC references and inputs

An external ADC voltage reference can be applied at JP9 (pin 1) for the negative reference and JP10 (pin 2) for the positive reference.

If jumpers are populated on both connectors, the positive reference will be connected to `SW2_OUT` (1.8 by default and it can be regulated by the PMIC) and the negative reference to the ground.

NOTE

By default, both expansions (JP9 and JP10) are not populated.

Chapter 10
Known Issues/Errata for Revision E

This section lists known issues with Revision E.

10.1 External PMIC to drive VDDCORE

LDO_ENABLE pin has to be grounded when using external PMIC component when driving the VDDCORE pin externally.

Workaround. Install a jumper on JP22 (2-3) in order to enable PMIC usage.

10.2 Capacitor values for the 24 MHz crystal

Capacitor values of 6.0 pF for the 24 MHz crystal are not optimal values for the EVK board. For the EVK board, 10 pF capacitors, for C58 and C59, are appropriate values to achieve best ppm. For details, see the Application Information section in *RT600 Product data sheet* (document RT600). The actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine-tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine-tuning, measure the clock on the CLOCKOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

10.3 PCA9420 SW2_OUT to power an analog input

EVK board design uses PCA9420 SW2_OUT as the power supply for VDD1V8 pins where the PCA9420 SW2_OUT has more than 20 mV of low frequency ripple ranging from 4 kHz to 30 kHz depending on the load. Due to the multiple options available for configuring and connecting the PMIC to RT device, if the switching output SW2 is used to power an analog input of the RT device, the low frequency ripple can propagate through the crystal circuit and unwanted jitter is observed on the clock using CLKOUT pin where in some applications, this could be an issue. For further details regarding jitter observed and available workarounds, see *Hardware Development Guide for the RT600 Processor* (document RT600HDUG).

Appendix A
Revision History

The table below summarizes the revisions to this document.

Table 13. Revision history

Revision	Date	Description
0	04/2020	Initial release.
1	08/2020	Added Capacitor values for the 24 MHz crystal and PCA9420 SW2_OUT to power an analog input.
2	06/2021	Updated default setting of JP22 jumper in Table 2.

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Date of release: 06/2021
Document identifier: UM11159

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