

MIMXRT1064 EVK Board Hardware User's Guide

Contents

1. Introduction

This document is a Hardware User's Guide for the MIMXRT1064 Evaluation Kit (EVK) based on the NXP Semiconductor i.MX RT1064 Processor. This board is fully supported by NXP Semiconductor. This manual includes system setup and debugging, and provides detailed information on the overall design and usage of the EVK board from a hardware systems perspective.

1.1. Board overview

This EVK board is a platform designed to showcase the most commonly used features of the i.MX RT1064 Processor in a small, low cost package. The MIMXRT1064 EVK board is an entry level development board, which gives the developer the option of becoming familiar with the processor before investing a large amount of resources in more specific designs.

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Features of the MIMXRT1064 EVK board are shown in [Table 1](#)

Table 1. Board features

Processor	NXP Processor	MIMXRT1064DVL6A
DRAM Memory	SDRAM 256 Mb, 166MHz	IS42S16160J-6BLI
DCDC	MPS	MP2144GJ
LDO	UNION	UM1550S-18 UM1750S-00
Mass Storage	TF Card Slot	
	64 Mbit Quad SPI Flash	
	512 Mbit Hyper Flash	
Display Interface	LCD Connector	
Ethernet	10/100 Mbit/s Ethernet Connector. PHY Chip: KSZ8081RNB	
USB	USB 2.0 OTG Connector	
	USB 2.0 Host Connector	
Audio Connector	3.5 mm Audio Stereo Headphone Jack	
	Board-Mounted Microphone	
	Left & Right Speaker Out Connectors	
	SPDIF Interface(unpopulated)	
Power Connector	5V DC-Jack	
Debug Connector	JTAG 20-pin Connector (SWD by default)	
	OpenSDA with DAP-Link	
Sensor	FXOS8700CQ: 6-Axis Ecompass (3-Axis Mag, 3-Axis Accel) (Some boards are unpopulated)	
Camera	CMOS Sensor Interface	
CAN	CAN Bus Connector	
User Interface Button	ON/OFF, POR Reset, Reset, USER Button	
Led Indicator	Power Status, Reset, OpenSDA, USER LED	
Expansion Port	Arduino Interface	
PCB	3.937-inch x 5.9055-inch (10cm x 15cm), 4-layer board	

1.2. MIMXRT1064 EVK contents

The MIMXRT1064 EVK contains the following items:

- MIMXRT1064 EVK Board
- USB Cable (Micro B)
- Camera

1.3. MIMXRT1064 EVK board revision history

- EVK: Mass Product.

2. Specifications

This chapter provides detailed information about the electrical design and practical considerations of the EVK Board, and is organized to discuss each block in the following block diagram of the EVK board.

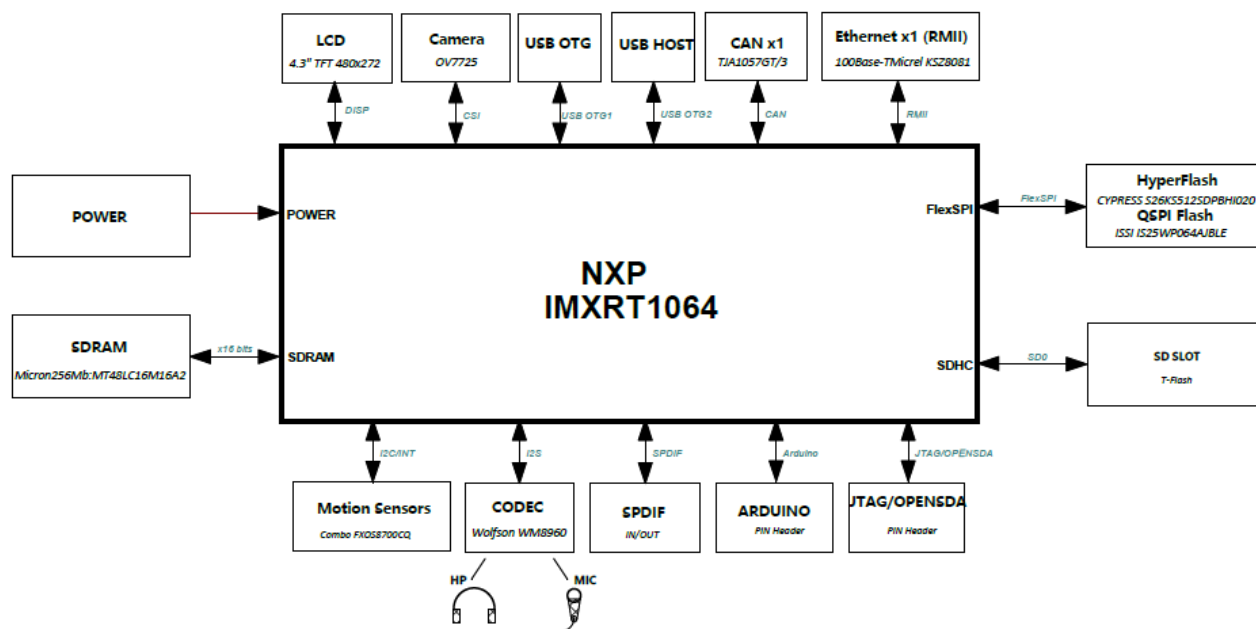


Figure 1. Block diagram

The overview of the MIMXRT1064 EVK Board is shown in [Figure 1](#) & [Figure 2](#).

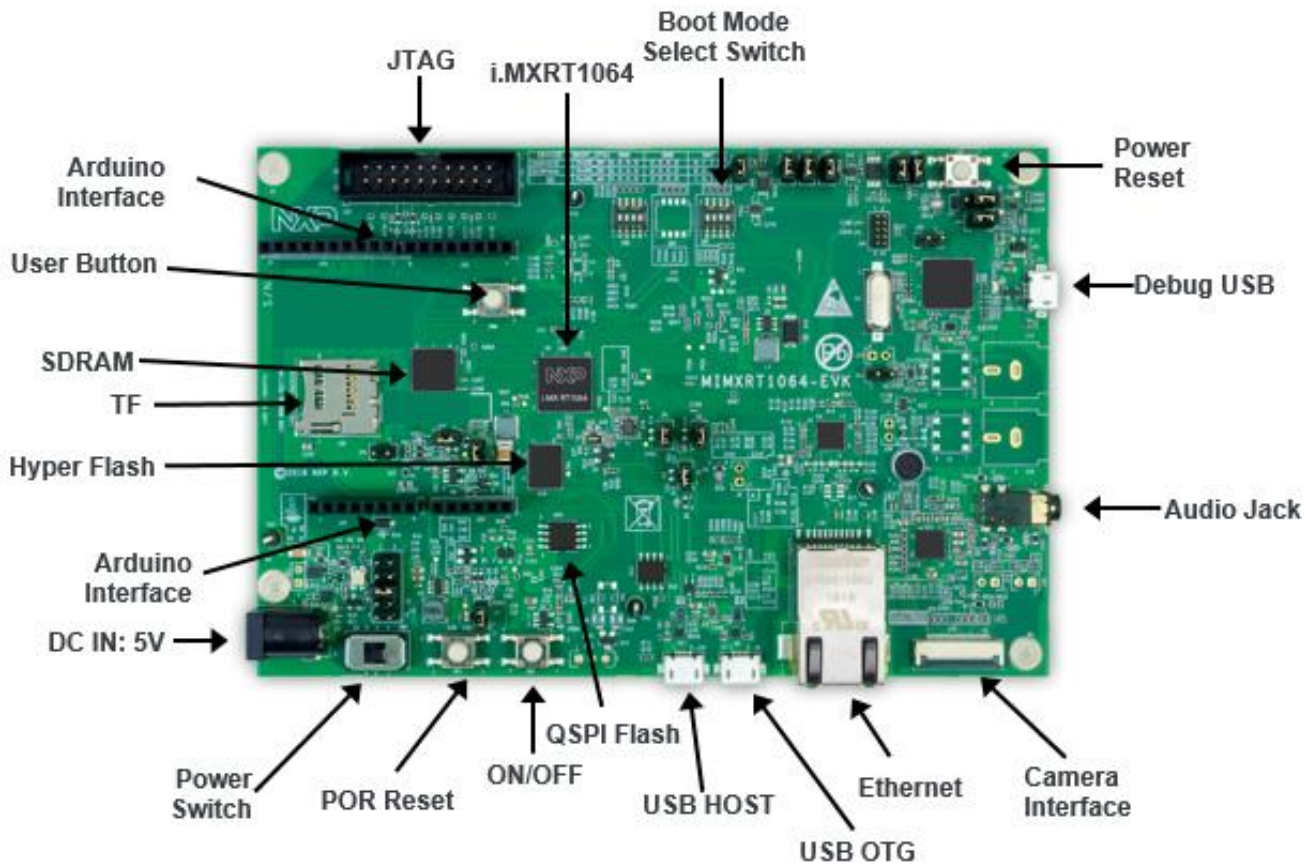


Figure 2. Overview of the MIMXRT1064 EVK Board (Front side)

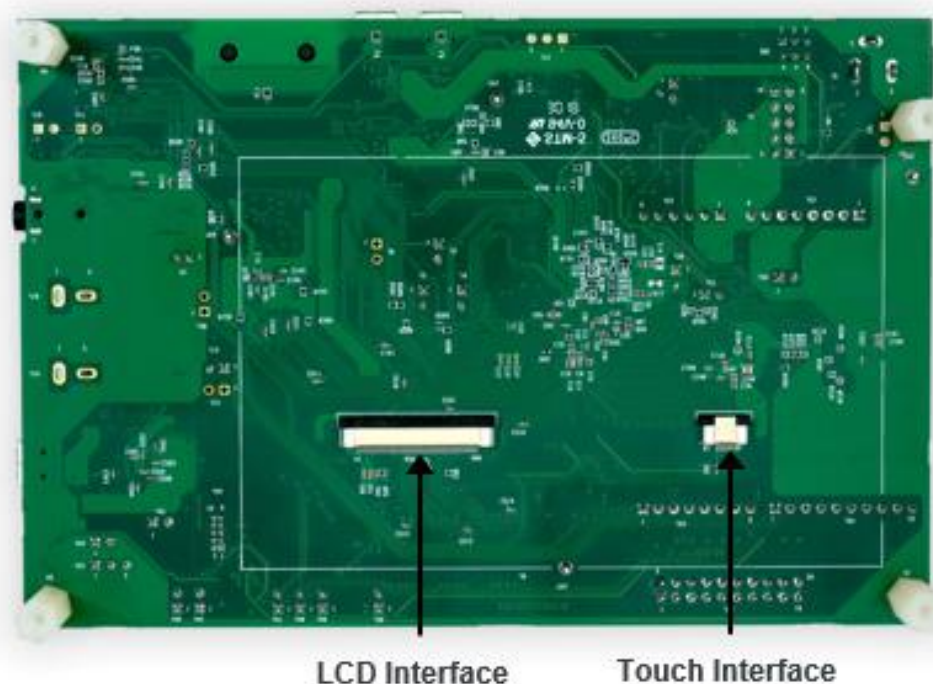


Figure 3. Overview of the MIMXRT1064 EVK Board (Back side)

2.1. i.MX RT1064 processor

The i.MX RT1064 is a new processor family featuring NXP's advanced implementation of the ARM Cortex-M7 Core. It provides high CPU performance and best real-time response. The i.MX RT1064 provides various memory interfaces, including SDRAM, Raw NAND FLASH, NOR FLASH, SD/eMMC, Quad SPI, HyperBus and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors. Same as other i.MX processors, i.MX RT1064 also has rich audio and video features, including LCD display, basic 2D graphics, camera interface, SPDIF and I2S audio interface.

The i.MX RT1064 applications processor can be used in areas such as industrial HMI, IoT, motor control and home appliances. The architecture's flexibility enables it to be used in a wide variety of other general embedded applications too. The i.MX processor provides all interfaces necessary to connect peripherals such as WLAN, Bluetooth™, GPS, camera sensors, and multiple displays.

The more detail information about i.MX RT1064 can be found in the Datasheet and Reference Manual documents.

2.2. Boot mode configurations

The device has four boot modes (one is reserved for NXP use). The boot mode is selected based on the binary value stored in the internal BOOT_MODE register. Switch (SW7-3 & SW7-4) is used to select the boot mode on the MIMXRT1064 EVK Board.

Table 2. Boot Mode pin settings

BOOT_MODE[1:0] (SW7-3 SW7-4)	BOOT Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

Typically, the internal boot is selected for normal boot, which is configured by external BOOT_CFG GPIOs. The following [Table 3](#) shows the typical Boot Mode and Boot Device settings.

Table 3. Typical Boot Mode and Boot Device settings

SW7-1	SW7-2	SW7-3	SW7-4	Boot Device
OFF	OFF	ON	OFF	Internal QSPI Flash

NOTE

For more information about boot mode configuration, see the System Boot chapter of the MIMXRT1064 Reference Manual.

For more information about MIMXRT1064 EVK boot device selection and configuration, see the respective main board schematic on www.nxp.com.

2.3. Power tree

A DC 5V external power supply is used to supply the MIMXRT1064 EVK Board at J2, and a slide switch SW1 is used to turn the Power ON/OFF. J41 and J9 also can be used to supply the EVK Board. Different power supply need to configure different Jumper setting of J1. [Table 4](#) shows the details:

Table 4. Jumper settings of Power Supply

Power Supply	J1 Setting
J2	1-2
J9	3-4
J41	5-6

The power tree is shown in the following figure.

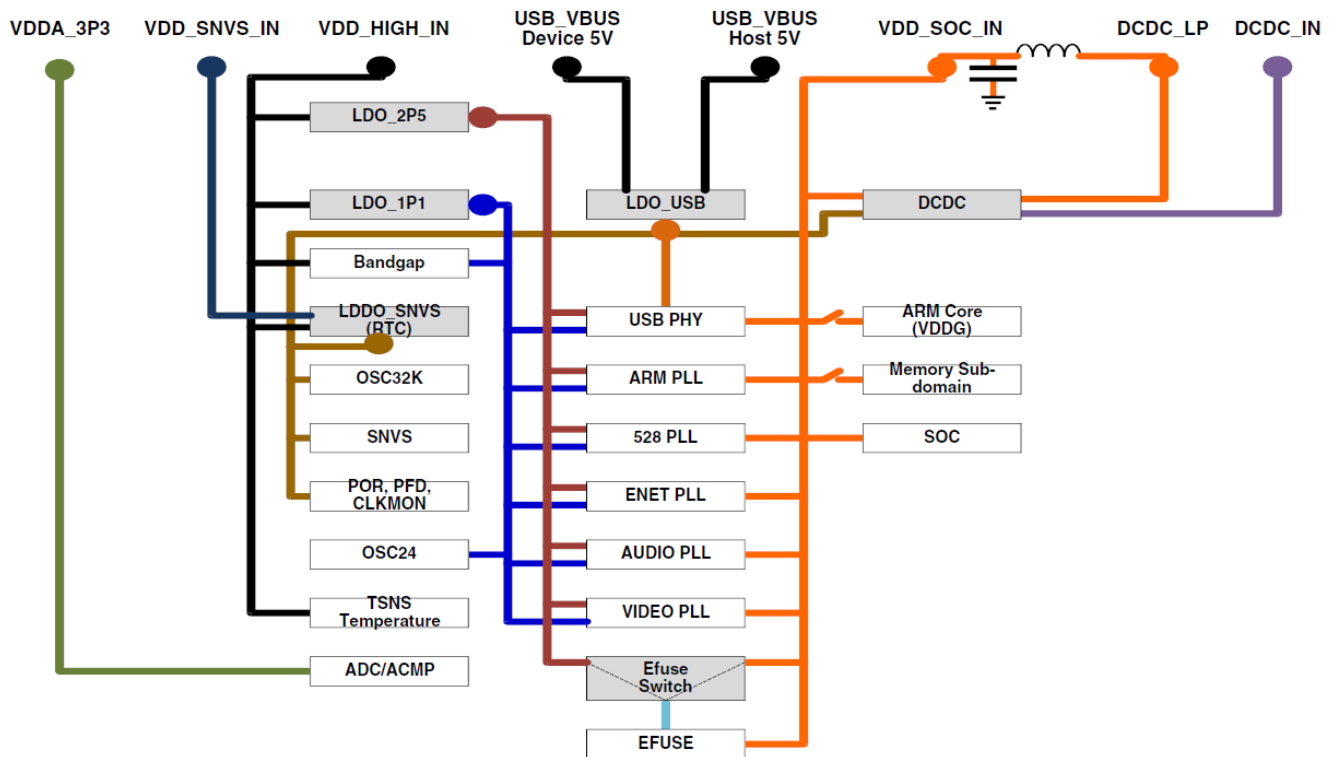


Figure 4. Power Tree

The power control logic of the MIMXRT1064 EVK board is shown in the following figure:

- It will power up SNVS firstly, then PMIC_REQ_ON will be switched on to enable external DC/DC to power up other power domains.
- ON/OFF button is used to switch ON/OFF PMIC_REQ_ON to control power modes.
- RESET button and WDOG output are used to reset the system power.

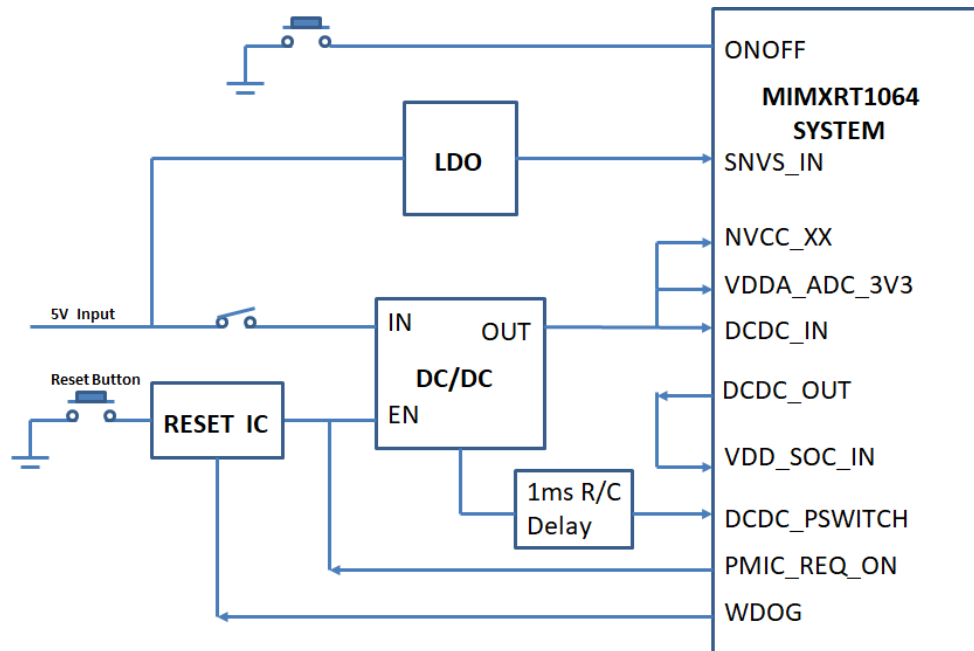


Figure 5. Power Control Diagram

The power rails on the board are shown in Table 5.

Table 5. Power Rails

Power Rail	MIN (V)	TYP (V)	MAX (V)	Description
VDD_SOC_IN	0.925	--	1.26	Core supplies input voltage
VDD_HIGH_IN	3	3.3	3.6	VDD_HIGH_IN supply voltage
DCDC_IN	3	3.3	3.6	Power for DCDC
VDD_SNVS_IN	2.4	3	3.6	Power for SNVS and RTC
USB_OTG1_VBUS USB_OTG2_VBUS	4.4	5	5.5	Power for USB VBUS
VDDA_ADC	3	3.3	3.6	Power for 12-bit ADC
NVCC_SD0	3	3.3	3.6	Power for GPIO in SDIO1 bank (3.3V mode)
	1.65	1.8	1.95	Power for GPIO in SDIO1 bank (1.8V mode)

NVCC_SD1	3	3.3	3.6	Power for GPIO in SDIO2 bank (3.3V mode)
	1.65	1.8	1.95	Power for GPIO in SDIO2 bank (1.8V mode)
NVCC_EMCC	3	3.3	3.6	IO supply for GPIO in EMC bank (3.3 V mode)
	1.65	1.8	1.95	IO supply for GPIO in EMC bank (1.8 V mode)
NVCC_GPIO	3	3.3	3.6	IO power for GPIO

2.4. SDRAM memory

One 256 MB, 166 MHz SDRAM (IS42S16160J-6BLI) is used on the EVK Board.

2.5. SD card slot

There is a SD card slot(J39) on the MIMXRT1064 EVK Board.J39 is the Micro SD slot for USDHC1 interface. If the developer wants to boot from the SD Card, the boot device switch (SW7) settings should be: ON, OFF, ON, OFF, as shown in Table 3.

2.6. Hyper flash

On the MIMXRT1064 EVK Board, there is one 512Mbit Hyper Flash device for developer to rework MIMXRT1064 EVK Board and use the onboard Hyper Flash.

By default, this Hyper Flash is disabled on the EVK. To enable the onboard Hyper Flash, the settings need to be changed.

Step 1:

Weld resistors: R356, R361 - R366.

Step 2:

Removed 0 Ω resistors: R153 - R158.

2.7. QSPI flash

A 64 Mbit QSPI Flash is used on the MIMXRT1064 EVK Board for developer to rework MIMXRT1064 EVK Board and use the onboard QSPI Flash.

2.8. Ethernet connector

There is one Ethernet Mac controller in the MIMXRT1064 processor. The Ethernet subsystem of the MIMXRT1064 EVK Board is provided by the KSZ8081RNB 10/100M Ethernet Transceiver (U16) and a RJ45 (J19) with integrated Magnetic.

2.9. USB PHY connector

The MIMXRT1064 contains 2 integrated USB 2.0 PHYs capable of connecting to USB host/device systems at the USB low-speed (LS) rate of 1.5 Mbits/s, full-speed (FS) rate of 12 Mbits/s or at the USB 2.0 high-speed (HS) rate of 480 Mbits/s.

2.10. Audio input / output connector

The Audio CODEC used on the MIMXRT1064 EVK Board is Wolfson's Low Power, high quality Stereo Codec, WM8960. The MIMXRT1064 EVK Board include one headphone interface (J12), one onboard MIC (P1), two speaker interfaces (J16, J17), and the SPDIF interface (J14 & J18, DNP). J12 is a 3.5mm audio stereo headphone jack, which supports jack detect.

2.11. OpenSDA circuit (DAP-link)

The OpenSDA circuit (CMSIS–DAP) is an open-standard serial and debug adapter. It bridges serial and debug communications between a USB host and an embedded target processor.

CMSIS-DAP features a mass storage device (MSD) bootloader, which provides a quick and easy mechanism for loading different CMSIS-DAP Applications such as flash programmers, run-control debug interfaces, serial-to-USB converters, and more. Two or more CMSIS-DAP applications can run simultaneously. For example, run-control debug application and serial-to-USB converter runs in parallel to provide a virtual COM communication interface while allowing code debugging via CMSIS-DAP with just single USB connection.

For the MIMXRT1064 EVK Board, J41 is the connector between the USB host and the target processor. Jumper to serial downloader mode to use stable DAP-Link debugger function. If developer wants to make OpenSDA going to the bootloader mode, J43 should jumper to 1-2, and press SW4 when power on. Meanwhile, the OpenSDA supports drag/drop feature for U-Disk. First, use the serial downloader mode and drag/drop the image file to U-Disk. Then select QSPI Flash as boot device and reset the Board, the image will run.

2.12. JTAG connector

J21 is a standard 20-pin/2.54 mm Box Header Connector for JTAG. The pin definitions are shown in the following figure. Support SWD by default.

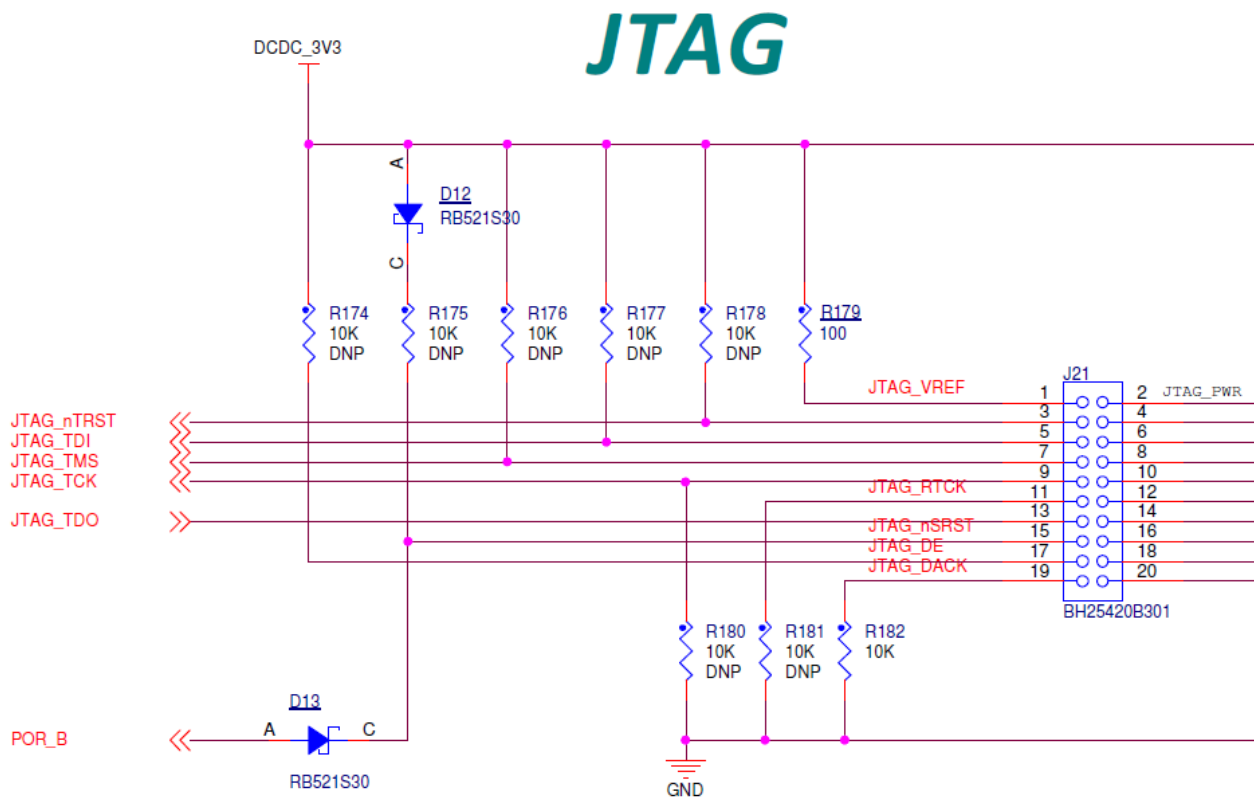


Figure 6. JTAG pin definitions

NOTE

If developer wants to use JTAG, J47 and J48 should be removed.

2.13. Arduino expansion port

J22 – J25 is defined as Arduino Interface. The pin definitions of Arduino Interface are shown in Table 6.

Table 6. Arduino Interface pin definitions

J22	J23
UART_RX/D0	A0/ADC0
UART_TX/D1	A1/ADC1
D2/INT0	A2/ADC2
D3/INT1/PWM/OC2B	A3/ADC3
D4/T0/XCK	A4/ADC4/SDA
D5/TI/PWM	A5/ADC5/SCL

D6/AIN0/PWM/OC0A
D7/AIN1/PWM

J24	J25
D8/CLKO/ICP1	NC
D9/OC1A/PWM	IOREF
D10/SPI_CS	RESET
D11/OC2A/PWM/SPI_MOSI	3.3V
D12/SPI_MISO	5V
D13/SPI_CLK	GND
GND	GND
AREF	VIN
D14/I2C_SDA	
D15/I2C_SCL	

2.14. Camera module connector

One parallel CSI (Camera Sensor Interface) is supported by the i.MX RT1064. There is a Camera Module Connector (J35) on the MIMXRT1064 EVK Board. The CA031C based on OV7725 and CA111C based on MT9M114 can be used directly.

NOTE

J35 supports both MT9M114 and OV7725 camera module, but 3.3 V is a violation to MT9M114 spec 3.1 V. It proved fine for evaluation/demo with 3.3 V supply, but in product design, it is recommended to adjust DCDC output or add level shifter.

2.15. User interface switch

There are four user interface switches on the MIMXRT1064 EVK Board. Their functionality is as below.

2.16. Power switch

SW1 is a slide switch to control the power of the MIMXRT1064 EVK Board when the power supply is from J2. The function of this switch is listed below:

- Sliding the switch to the ON position connects the 5V power supply to the Evaluation board main power system.
- Sliding the switch to OFF position immediately removes all power from the board.

2.17. ON/OFF button

SW2 is the ON/OFF button for MIMXRT1064 EVK Board. A short pressing in OFF mode causes the internal power management state machine to change state to ON. In ON mode, a short pressing generates an interrupt (intended to be a software-controllable(power-down)). An approximate 5 seconds or more pressing causes a forced OFF. Both boot mode inputs can be disconnected.

2.18. Reset button

There are two Reset Button on the EVK Board. SW3 is the Power On Reset Button. Pressing the SW3 in the Power On state will force to reset the system power except SNVS domain. The Processor will be immediately turn off and reinitiate a boot cycle from the Processor Power Off state. SW4 is Reset Button.

2.19. USER button

SW8 is the USER Button(GPIO5-00) for developers using. Pressing can produce changes in high and low levels.

2.20. Sensor

U32 on the EVK Board is a 6-Axis Ecompass (3-Axis Mag, 3-Axis Accel) sensor FXOS8700CQ. The Ecompass is connected to i.MX RT1064 I2C1 port.

NOTE

The sensor on some boards are unpopulated.

2.21. User interface LED indicator

There are four LED status indicators located on the EVK Board. The functions of these LEDs include:

- Main Power Supply (D3)
Green: DC 5 V main supply is normal.
Red: J2 input voltage is over 5.6 V.
Off: the board is not powered.

- Reset RED LED(D21)
- OpenSDA LED(D20)
- USER LED(D18)

2.22. LCD interface

The enhanced Liquid Crystal Display Interface (eLCDIF) is a general purpose display controller.

The eLCDIF block supports the following:

- Displays that support moving pictures and require the RGB interface mode (DOTCLK interface).

The eLCDIF provides fully programmable functionality to supported interfaces:

- Bus master interface to source frame buffer data for display refresh.
- 8/16/18/24/32 -bit LCD data bus support available depending on I/O mux options.
- Programmable timing and parameters for DOTCLK LCD interfaces.

If developers want to use LCD, NXP provides an optional LCD module RK043FN02H-CT which has a 4.3 inches touch-screen and supports a resolution of up to 480*3(RGB)*272. This module contains two FPC cables. The LCD interface can be connected to J8(A1-A40) and the CPT interface can be connected to J8(B1-B6). LCD modules can be purchased from the NXP website.

3. PCB information

The MIMXRT1064 EVK Board is made using standard 4-layer technology. The material used was FR-4. The PCB stack-up information is shown in [Table 7](#).

Table 7. Board stack-up information

Layer	Description	Copper(Oz)	Dielectric Thickness(mil)
1	Signal	1	—
	Dielectric	—	3
2	GND	1	—
	Dielectric	—	52
3	Power	1	—
	Dielectric	—	3
4	Signal	1	—

4. EVK design files

The schematics, layout files, and gerber files (including Silkscreen) can be downloaded from nxp.com/MIMXRT1064-EVK.

5. Contents of the evaluation kit

Table 8. EVK contents

Item	Description
EVK Board	EVK Board with processor, memory, interfaces, etc
USB Cable	USB cable (Micro-B to Standard-A)
Camera	CA111C based on MT9M114

NOTE

Power adaptor, Micro SD Card and LCD Module are not standard parts of the evaluation kit.

6. Revision history

[Table 9](#) summarizes the changes made to this document since the initial release.

Table 9. Revision history

Revision number	Date	Substantive changes
0	10/2018	Initial release

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Document Number: MIMXRT1064EVKHUG
Rev. 0
10/2018

