Jabil VRC SCHEMATICS

Change Note:

06/07:
-remove R209,R210,R130,R131,R132,R133,R134,R135 (unnecessary 0R Jumper)
-Separate PDM CLK (U20/21/23) to avoid hardware conflicts
-Adjust the "WiFi" Antenna Matching Circuit (C128,C128,R120,R262,R263,C241,R240,R119)
-Adjust the "Thread" Antenna Matching Circuit (C141,C142,L15)
-replace U15 QSPI Flash from 64Mbit to 512Mbit (IS25LP512M-JLLE)
-Power Net correction (C121,C214,C213)
-replace U4 DC/DC solution to increase capacity 2A-> 3A
-U12 EN Pin-8 assign correction -> pull high
-added 47uF(C242,C243,C244) on power in to compensate short time power surges.
-U7/U6 Correction DCDC_3V3 powre up control flow, to meet Main Control Power-up sequence
-Replace R47 0R (0402) to FB20 for Optimize power layout
-Reset IC U6/U2 part Correction (Active Low, Open Drain) type
5/31:
-remove R6,R7 (unnecessary resistor)

5/30
-Replace C132 from 1uF to 10uF (base on Murata feedback)
5/27 (base on NXP feedback)
-Remove R37/R42 (fix SNVS/DCDC_IN)power supply
-Replace QSPI FLASH by IS25LP064D-JBLE (1.8V TTL to 3.3V TTL),and also remove
U10 (Flash 1.8V LDO)
-Add 0.1uF C239 on Thread Chip Reset Pull high pin
-JTAG_MOD multi-function assign already remove.

REVISION HISTORY			
REV	DATE	UPDATED BY	Note
--	2022/05/26	Eechaw Ng/ Ethan Cheng	Draft edition

Change Note:

07/02:
1.swap UART Tx/Rx K32_USART0_RXD/TXD , WIFI_UART_TXD/RXD

06/28:
1.remove duplicate connection"DCDC_3V3_PG" (correction)
06/17:
1.added Thread K32_ISP_EN/K32_PIO0_4 GPIO control (K32 Boot modes selaction)
2.adding PU/PD Resistor (R272,273) for SW Master/Slave define "GPIO_B1_06"
3.added Thread K32 SWDIO/CLK/K32I_RSTN interface J12 to 5pin 1.27mmx5 CONN
06/16:
1.remove H1-H6 (screw positioning hole define by E-DAD drawing)
2.added Thread K32_ISP_EN GPIO control
3.added Thread K32 SWDIO/CLK interface J12
06/15:
1.J3 Speaker +- swap for layout consider
2.remove unnecessary 0.1uF
C152,C153,C154,C155,C156,C157,C158,C159,C149,C161,C163,C160,C164,C165,C166,C167,C168,
C169,C162,C148,C150,C151,C170,C171,C172,C173,C174,C175,C176,,C177,C178,C179,C180,C181,C182,
C183,C184,C185,C186,C187,C188,C191,C190,C189)
3.remove SH1 Audio DSP shield (we not use the DSP on this project)
06/10:
1.U14 "PIn17/PIn18/Pin19" PTA based coexistence (correction)
2.reserved 3V3 suppry R270(DNP)
3.U12 (VCCA<VCCB) correction
4.replace RGB LED from "WS2812 (5050)" to IN-PI22TAT5R5G5B (2427) reduced to small size and
Increase the number to 20pcs/PCBA
06/08:
1.Separate Audio interface AMP ->SAI3_MCLK/SAI3_TX_BCLK/SAI3_TX_SYNC/SAI3_TX_DATA
2.Separate Audio interface
MIC's->SAI1_RX_DATA1/SAI1_RX_DATA2/SAI1_RX_SYNC/SAI1_RX_BCLK/SAI1_RX_DATA0
3.U17 pin re-assigned based on NXP feedback and also followed the datasheet (NC assignment)
4.added R269 0R Jumper for debug purpose

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Jabil VRC
01 COVER

DATE:	DWG NO:	REV:
Friday, July 29, 2022		A
DRAWN BY: Eechaw Ng / Ethan Cheng	SHEET: 1 of 15	

VRC EE System Block Diagram (Temp) 26-May-2022

5~9Vbat
9V DCIN
P-ch MosFET Power SW
5~9V
9V to 5V DC / DC MP2332HGTL (MPS)
5V
9V to 3.3V DC / DC MP2332HGTL (MPS)
3.3V
HW Reset
3V3 LDO for FLASH VCC NCP163ASN180T1G (onsemi)
1.8V
3V3 LDO for AMP VCC NCP163ASN180T1G (onsemi)
1.8V
3V3 LDO for SNVS NCP161ASN330T1G (onsemi)
3.3V
3V3 LDO for NVCC SD NCP161ASN330T1G (onsemi)
3.3V
5V
3.3V
1.8V
5V
3.3 to 5V TTL
Serial Data In

CJASB190141

CONN.
5.1W Mono Class D Audio Amp MAX98390CEWX (Maxim)
LPI2C1(1.8V)
1.8/3.3V
GPIOs
SAI1(I2S)

MIMXRT1062DVL6B
ARM MCU -M7 core
MAPBGA-196
(NXP)

GPIO
LPUART1
SDIO
LPUART3

Thread
K32W061Y
Thread RF System on a Chip
(HVQFN40)
3.3V
CONN.
PTA
WiFi IW416
LBEE5CJ1XK-687
dual bandWi-Fi 11a/b/g/n/ac
Bluetooth 5.2
(Murata)
3.3V
CONN.

FPC CONN.
PDM
3.3V
PDM-to-I2S ADAU7002
PDM-to-I2S ADAU7002
PDM-to-I2S ADAU7002
SAI1(I2S)
3.3V

CJPBA185082

QSPI(1.8V)
NOR Flash 64Mb
QPI/QPI/QSPI, 8-pin SOP
S25WP064AJBLE
(ISSI)
1.8V

Data Bus

baud band
PCB Antenna (optional)

GPIOs
LPI2C3(3.3V)
3.3V
2.54mm x5
3.3V
SE051
EdgeLock
(NXP)

256M, 3.3V, SDRAM,
16Mx16, 166Mhz, 54 ball BGA
IS42S16160J-6BLI
(ISSI)
3.3V

JTAG

Uer LED
CPU ON-OFF / Uer Button

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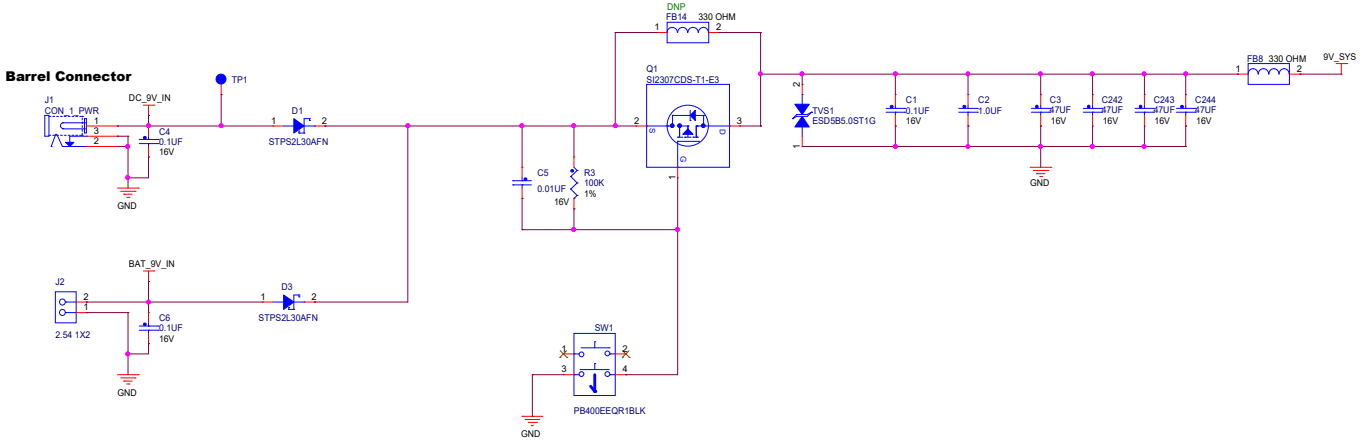
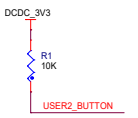
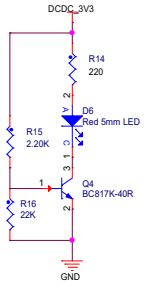
	Jabil VRC **02 BLOCK DIAGRAM**	
This schematic and its contents are proprietary and comprise legally protected subject matter belonging to Jabil Circuit, Inc. Reproduction and use is controlled.	DATE: Sunday, July 03, 2022	DWG NO: / REV: A
	DRAWN BY: Eechaw Ng / Ethan Cheng	SHEET: 2 of 15

Main Power

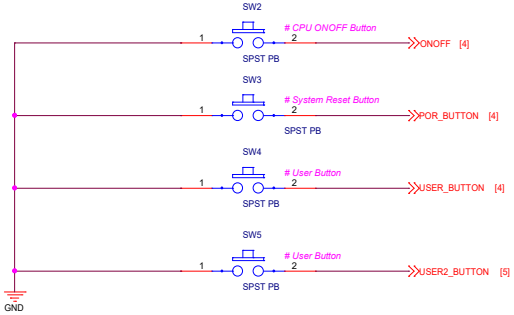


BUTTON GPIO Pull high

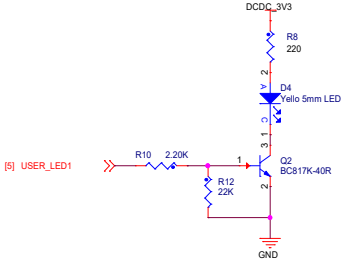


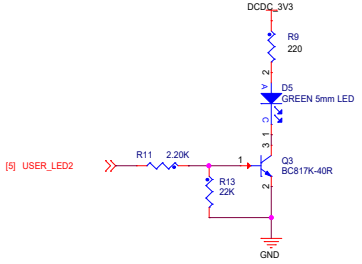


BUTTONS



USER LED

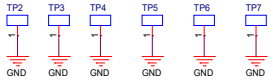




Board Mounting Holes

1.remove H1-H6 (screw positioning hole define by E-DAD drawing)

Ground TPs



Layout Note: Place Ground TPs to assist signal measurement.

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03 MAIN POWER

DATE: Sunday, July 03, 2022
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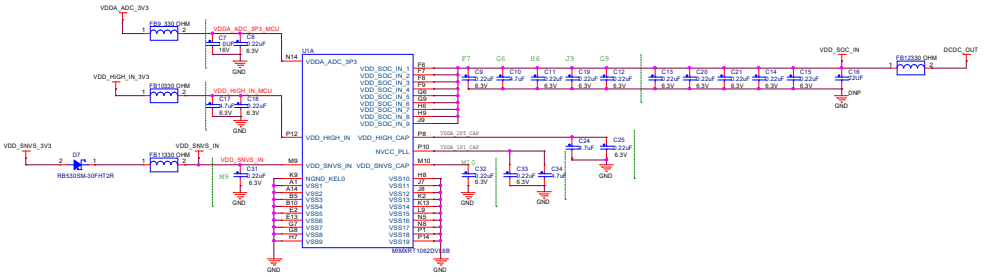
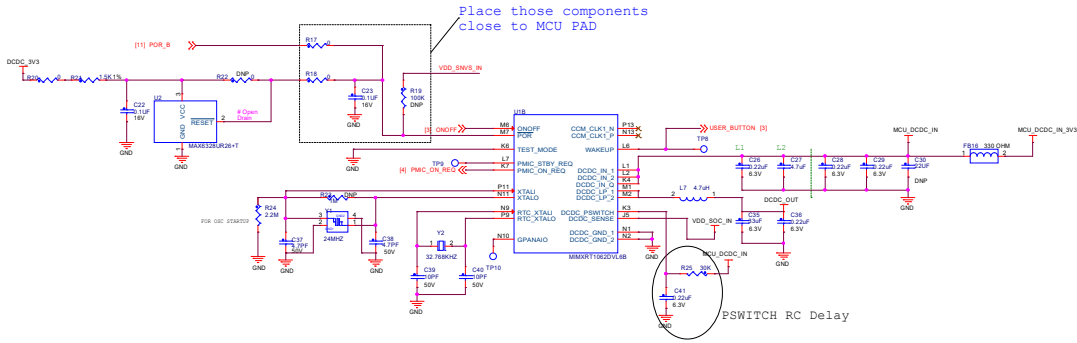
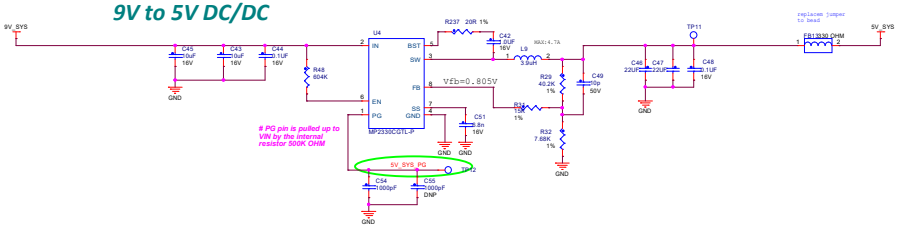
SHEET: 3 of 15



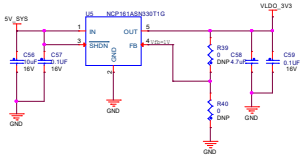


9V to 5V DC/DC

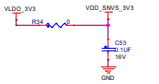


3V3 LDO for SNVS

Fix 3.3V MAX 450 mA

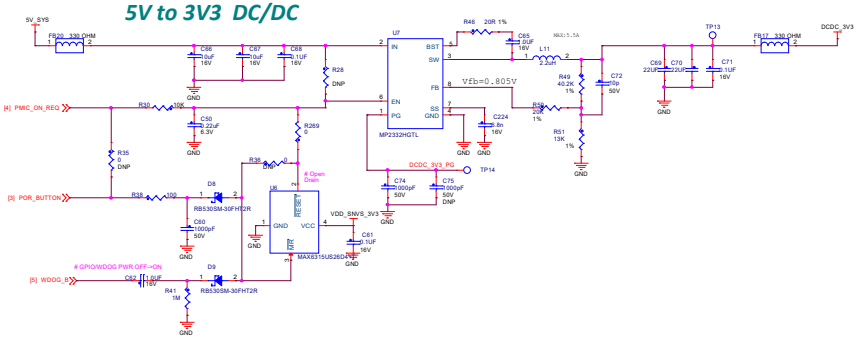


SNVS

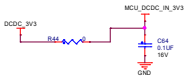


ADC

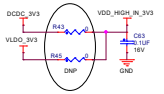
5V to 3V3 DC/DC



DCDC_IN

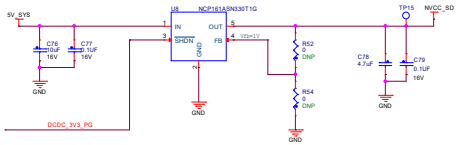


VDD_HIGH_IN



NVCC_SD <SD3.0>

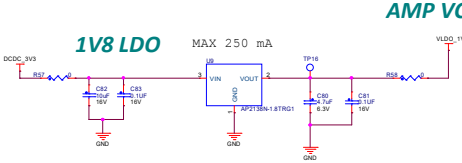
Fix 3.3V MAX 450 mA



FLASH VCC

1V8 LDO

MAX 250 mA



AMP VCC

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04 POWER DOMAIN

DATE:	DWG NO:	REV:
Sunday, July 03, 2022		A
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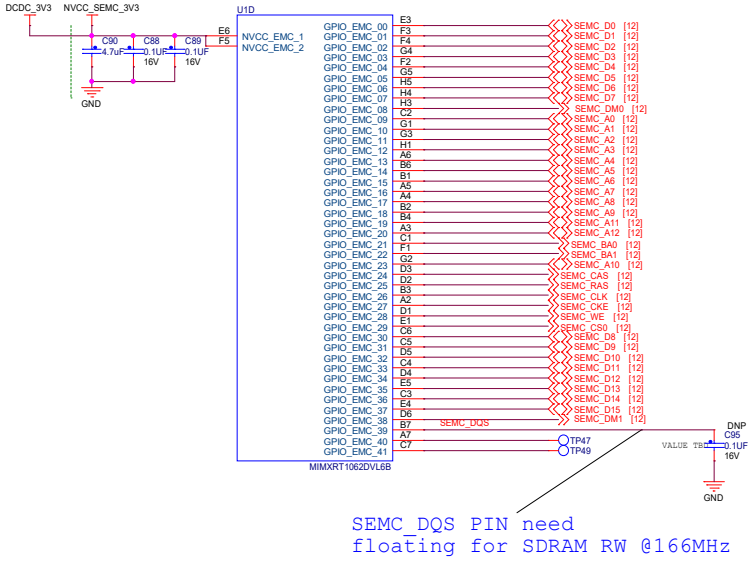
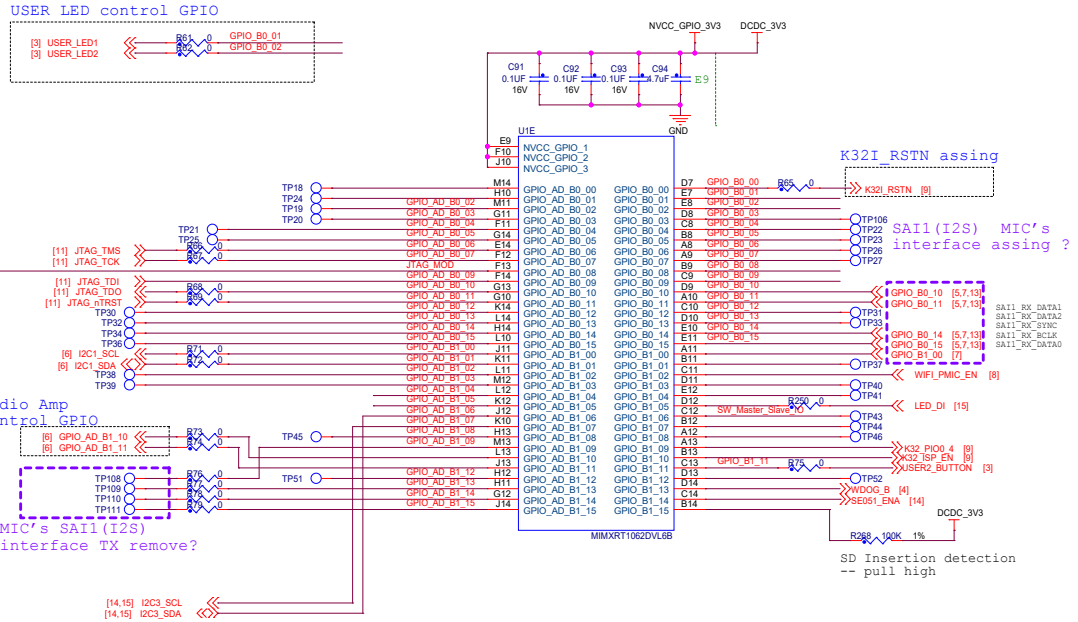
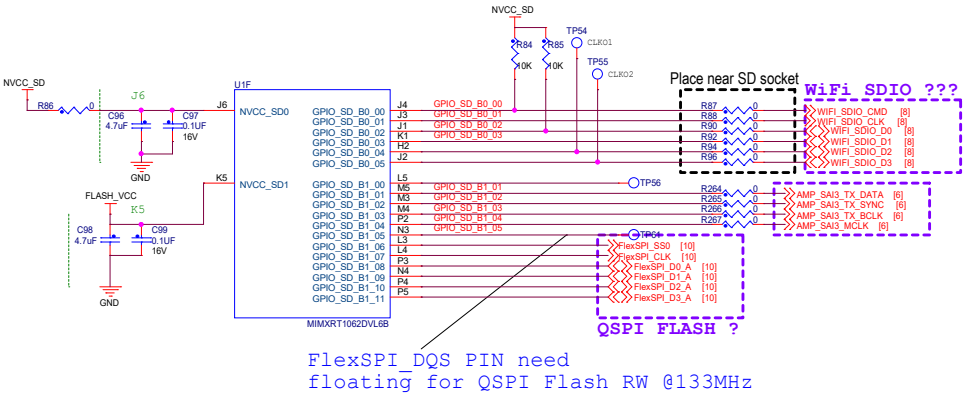
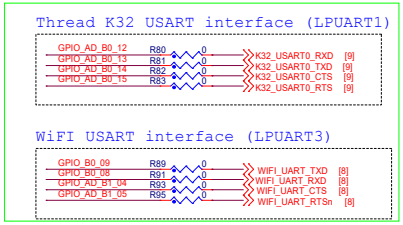
To be confirm All IO assing by Excel file

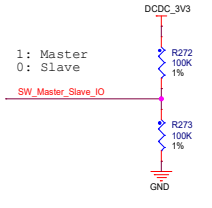


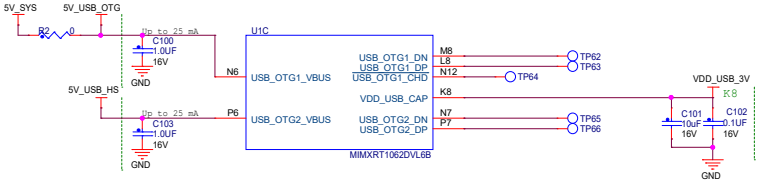


adding PU/PD Resistor for SW Master/Slave define









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05 MIMXRT1062DVL6A

DATE: Friday, July 29, 2022

DWG NO:

REV: A

DRAWN BY: Eechaw Ng / Ethan Cheng

SHEET: 5 of 15

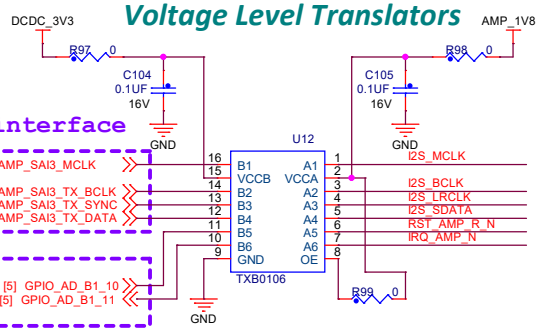
AUDIO Amp

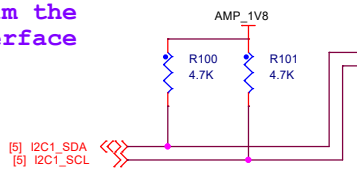
3.3V/1.8V Voltage Level Translators

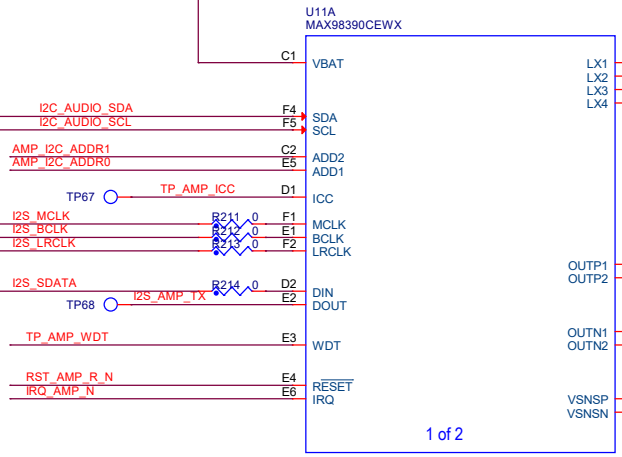
SAI3(I2S) interface

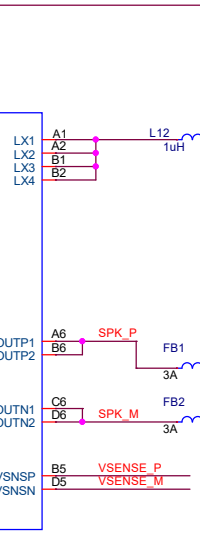
To MCU GPIO

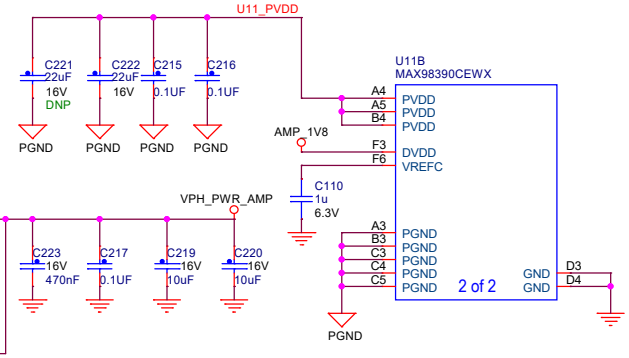
need to confrim the SAI1(I2S) interface

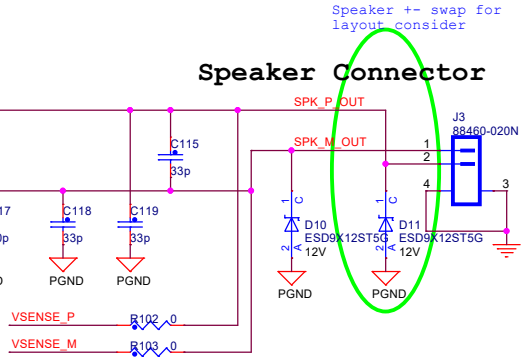




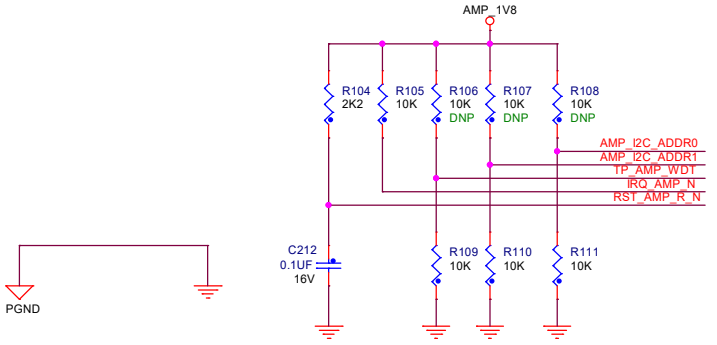






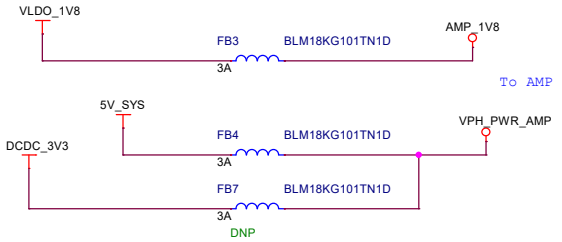


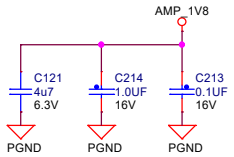
I2C Address : 0X70 (0111000x)



Audio Power

Power Domain TBC





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07 AUDIO Mic (added)

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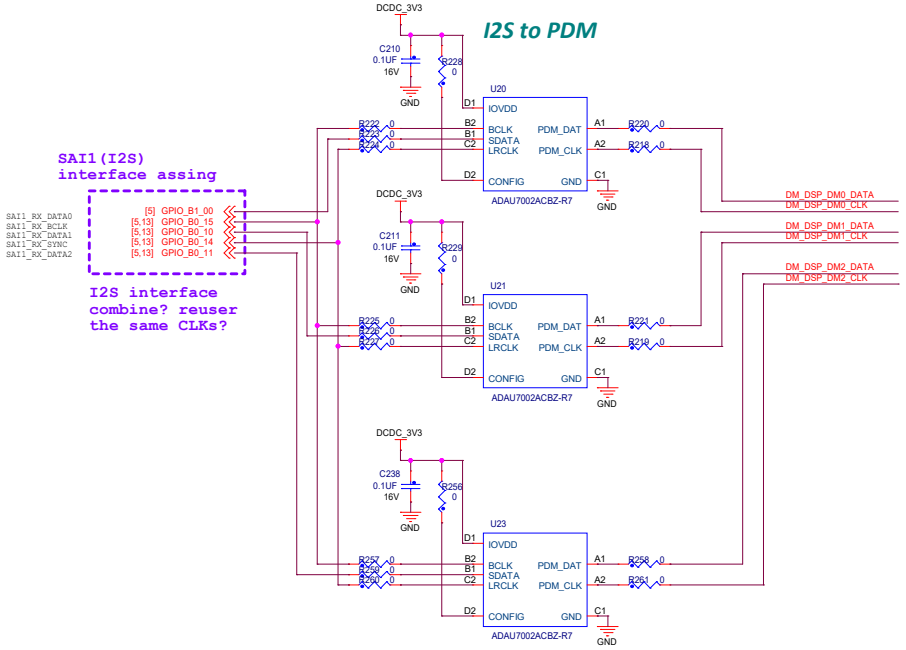
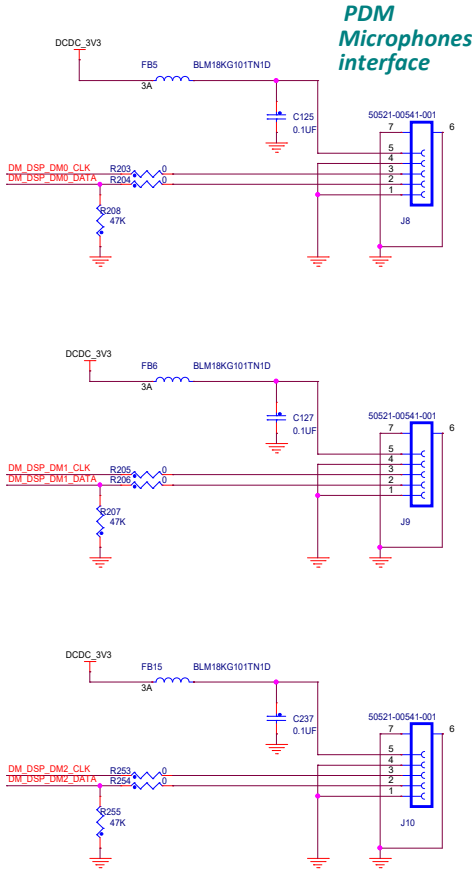
MICROPHONE Interface





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07 AUDIO Mic (added)

DATE: Sunday, July 03, 2022
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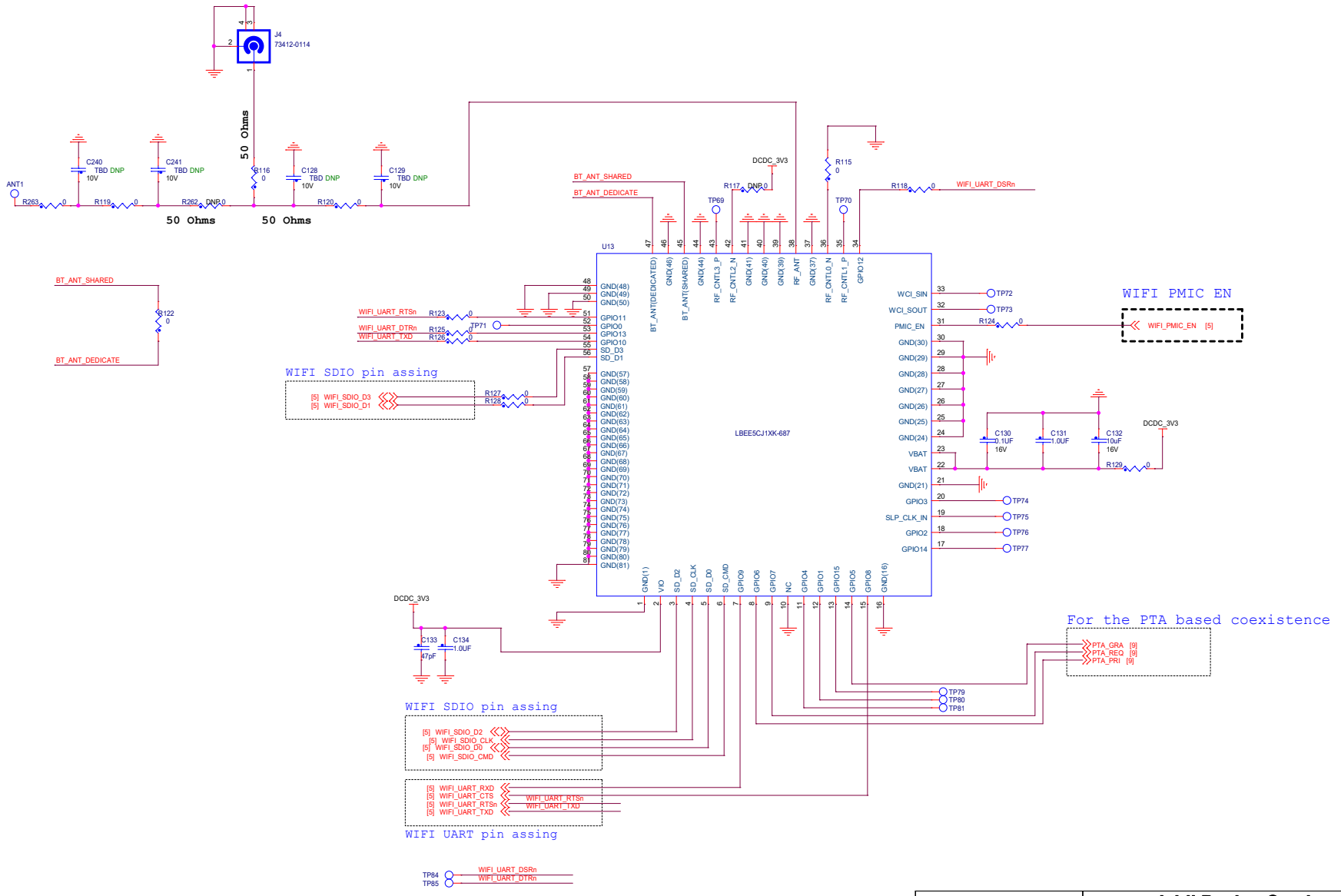
11.1 WiFi IW416



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Jabil VRC
08 WiFi IW416 (added)

DATE: Sunday, July 03, 2022
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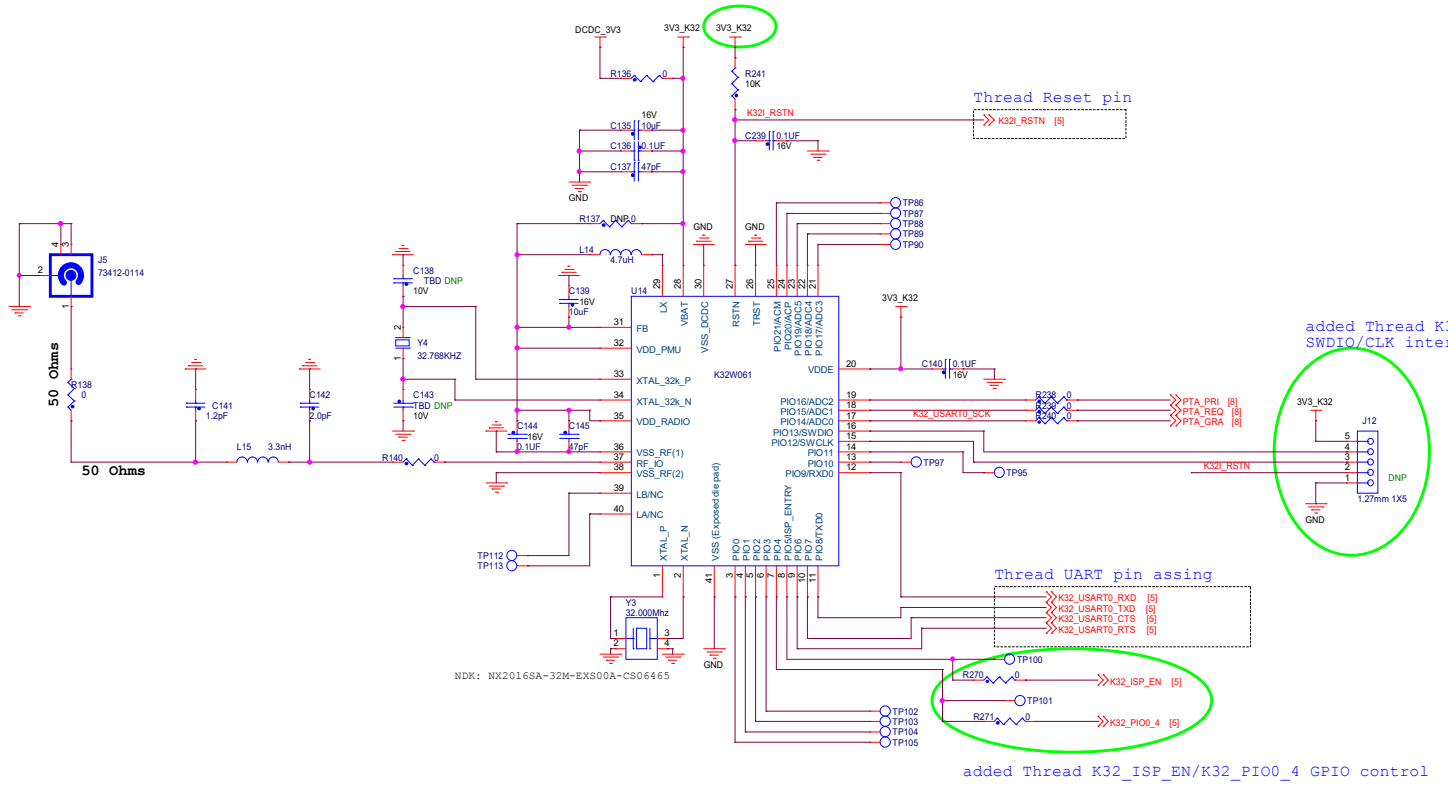
SHEET: 8 of 15

11.2 K32W061 Thread (added)



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Jabil VRC
09 K32W (added)

DATE: Sunday, July 03, 2022
DWG NO:
REV: A
DRAWN BY: Eechaw Ng / Ethan Cheng
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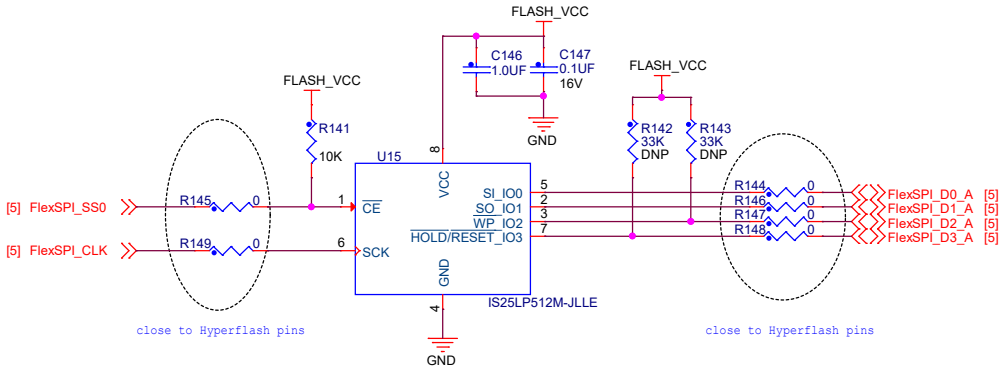
1V8 QSPI Flash



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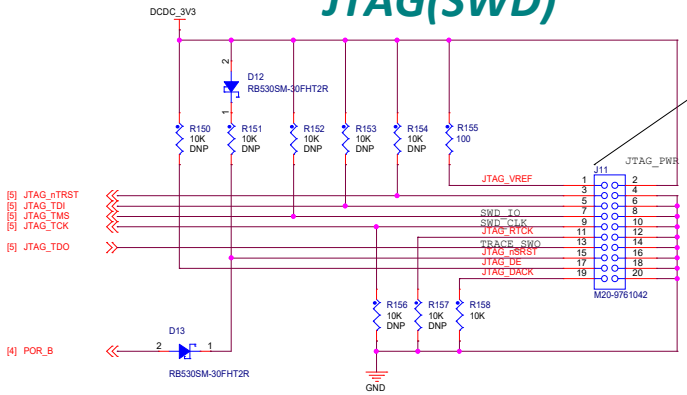
	Jabil VRC **10 QSPI FLASH**	
	DATE: Sunday, July 03, 2022 / DWG NO: / REV: A	
	DRAWN BY: Eechaw Ng / Ethan Cheng	SHEET: 10 of 15

JTAG(SWD)



1.SWD debug is enabled by default
2.Board rework and fuse programming are needed to support JTAG debug

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	Jabil VRC **11 JTAG**	
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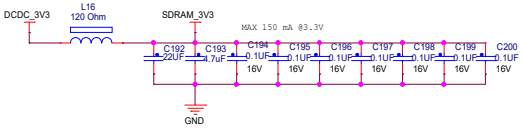
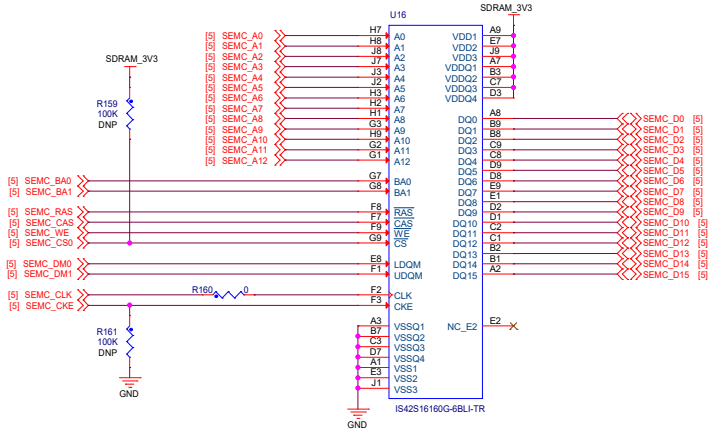
SDRAM





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	Jabil VRC **12 SDRAM**	
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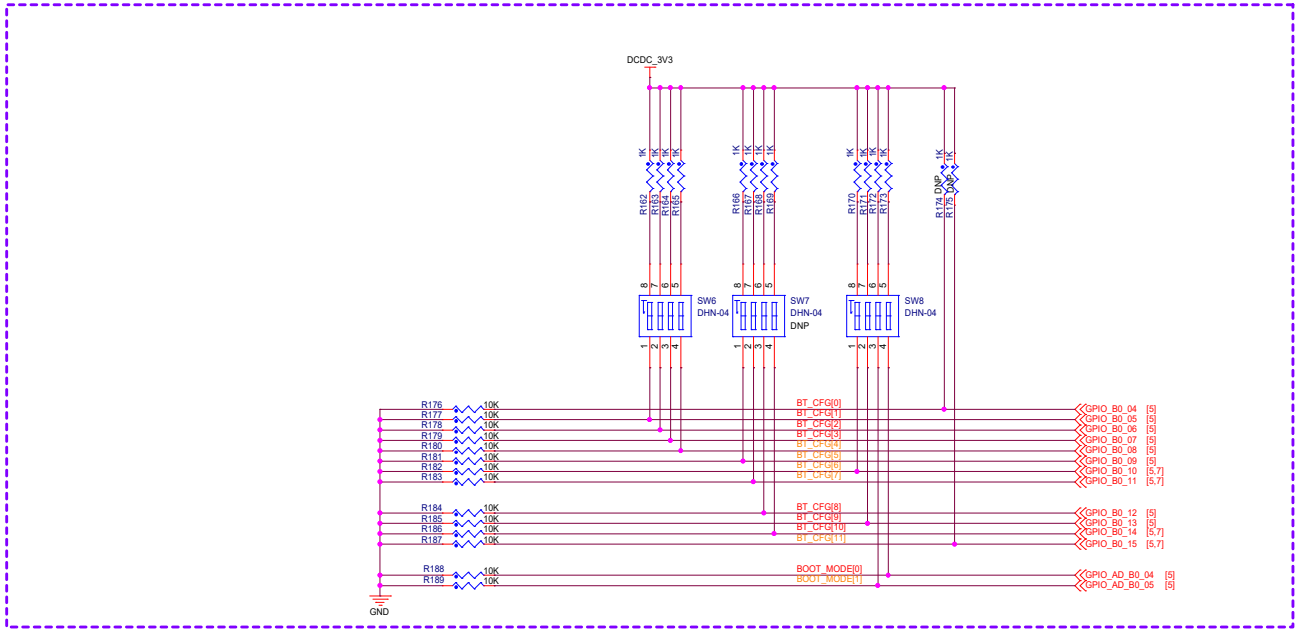
BOOT CONFIG TABLE

	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
TYPE	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**	**BOOT_CFG[7]**	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
FlexSPI1 - Serial NOR	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR*			*0*	*0*	*0*	*0*	*HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms*		*EncryptedXIP 0 - Disabled 1- Enabled*	*Reserved*
SD	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*Reserved*	*Bus Width: 0 - 1-bit 1 - 4-bit*	*SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V*	*0*	*1*	*SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104*		*SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad*	*SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct*	*Port Select: 0 - eSDHC1 1 - eSDHC2*	*Fast Boot: 0 - Regular 1 - Fast Boot*

To be Confirm can we remore those switch and release the GPIO?



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Jabil VRC
13 BOOT

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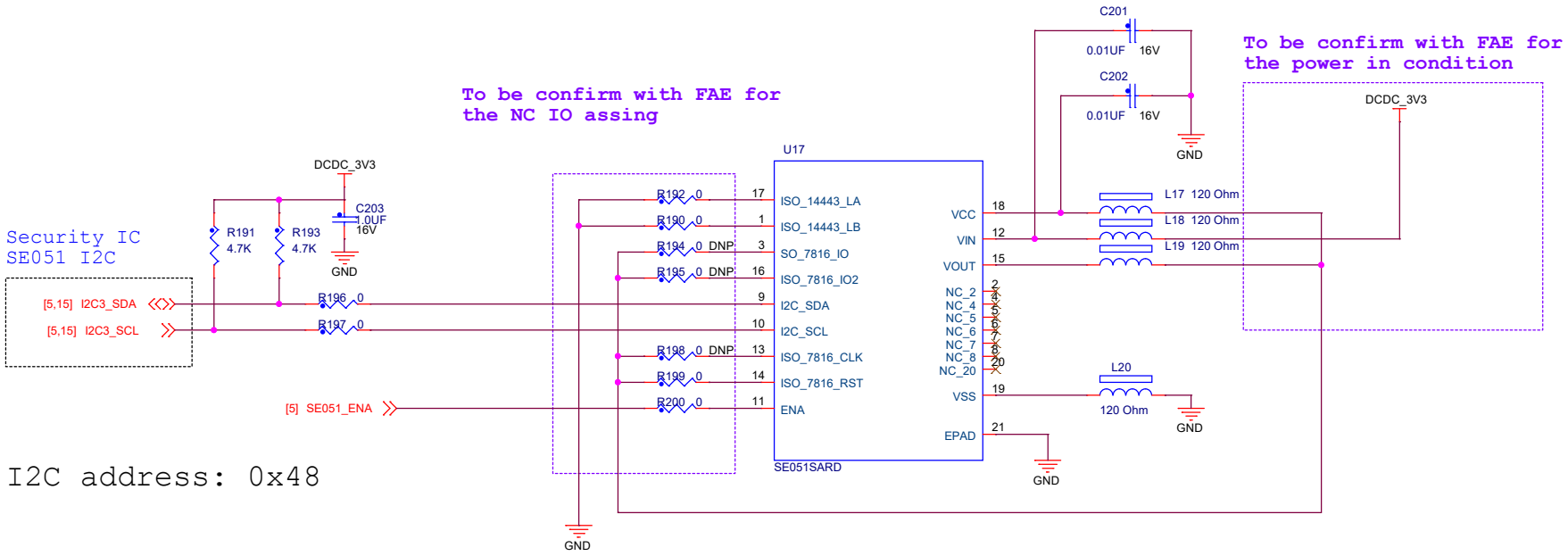
19 Security IC SE051



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	Jabil VRC **14 Security IC SE051**	
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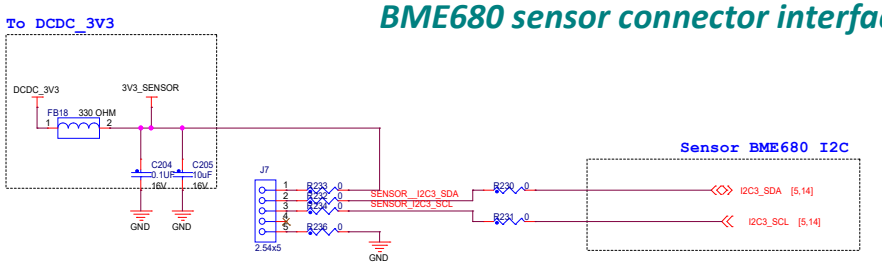
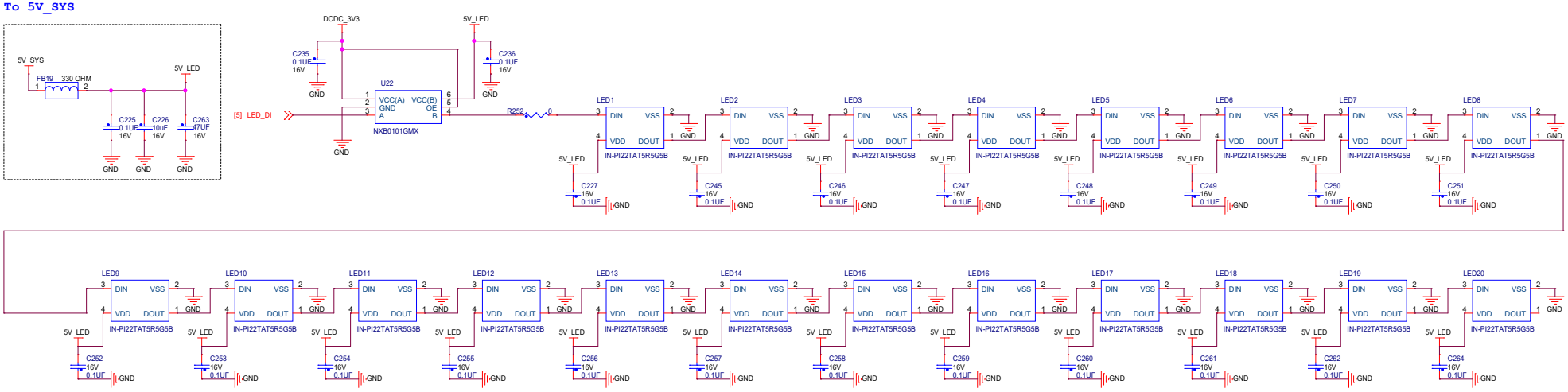
15 Sensor / RGB LED Strip

BME680 sensor connector interface



I2C address:
SDO=0 : (0x76)
SDO=1 : (0x77)

Integrated IC RGB LED (2427)



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Jabil VRC
15 Sensor

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