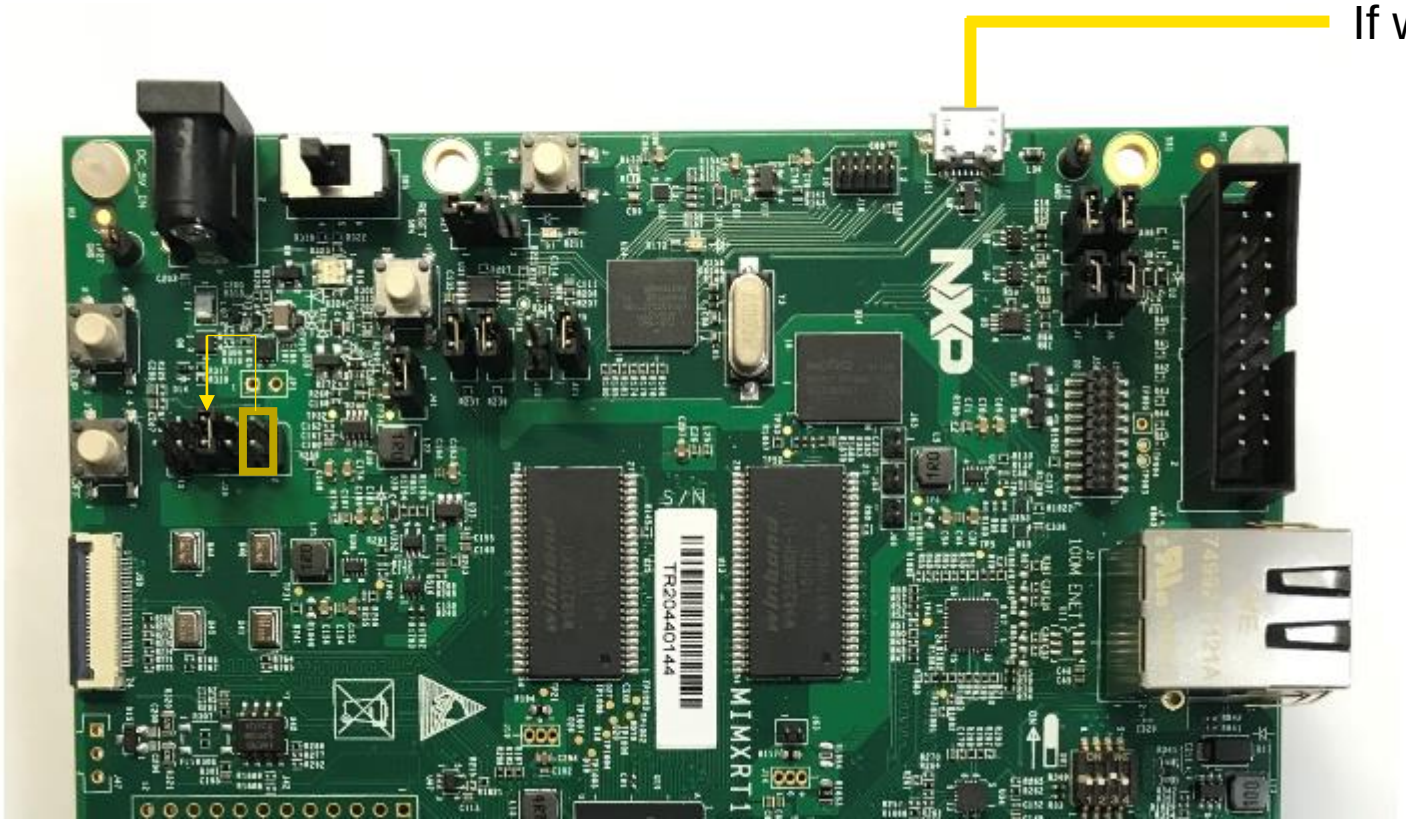
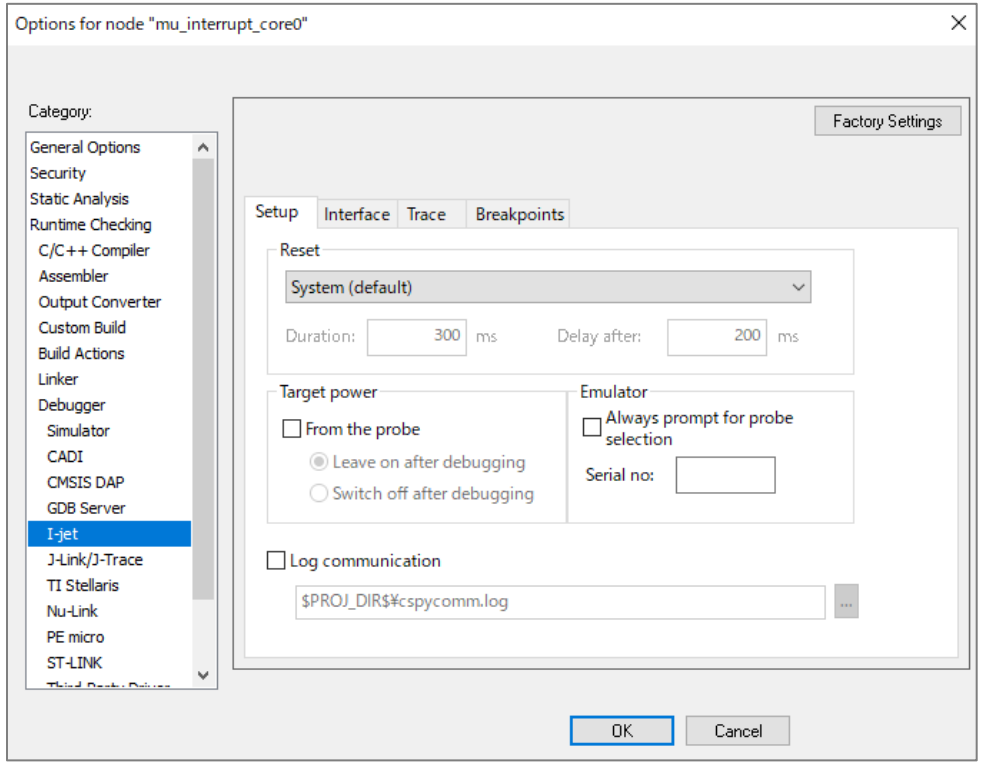
Report for i.MxRT.

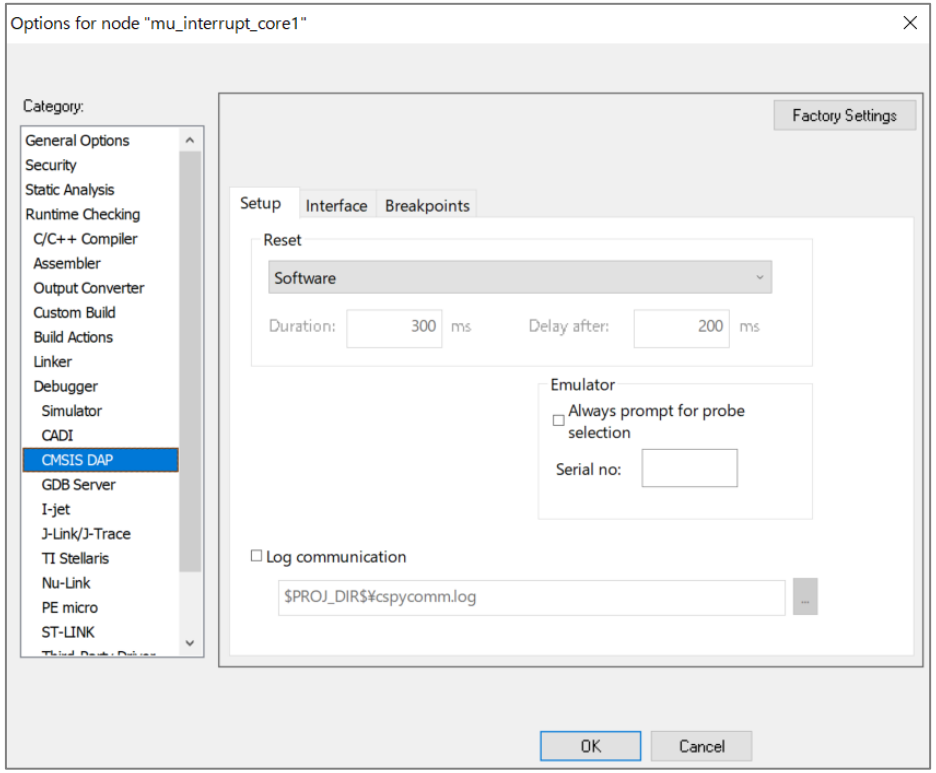
Change jumper setting from 1-2 to 5-6 on J38



Using CMSIS-DAP (default reset case)



Core0(m7)



Core1(m4)

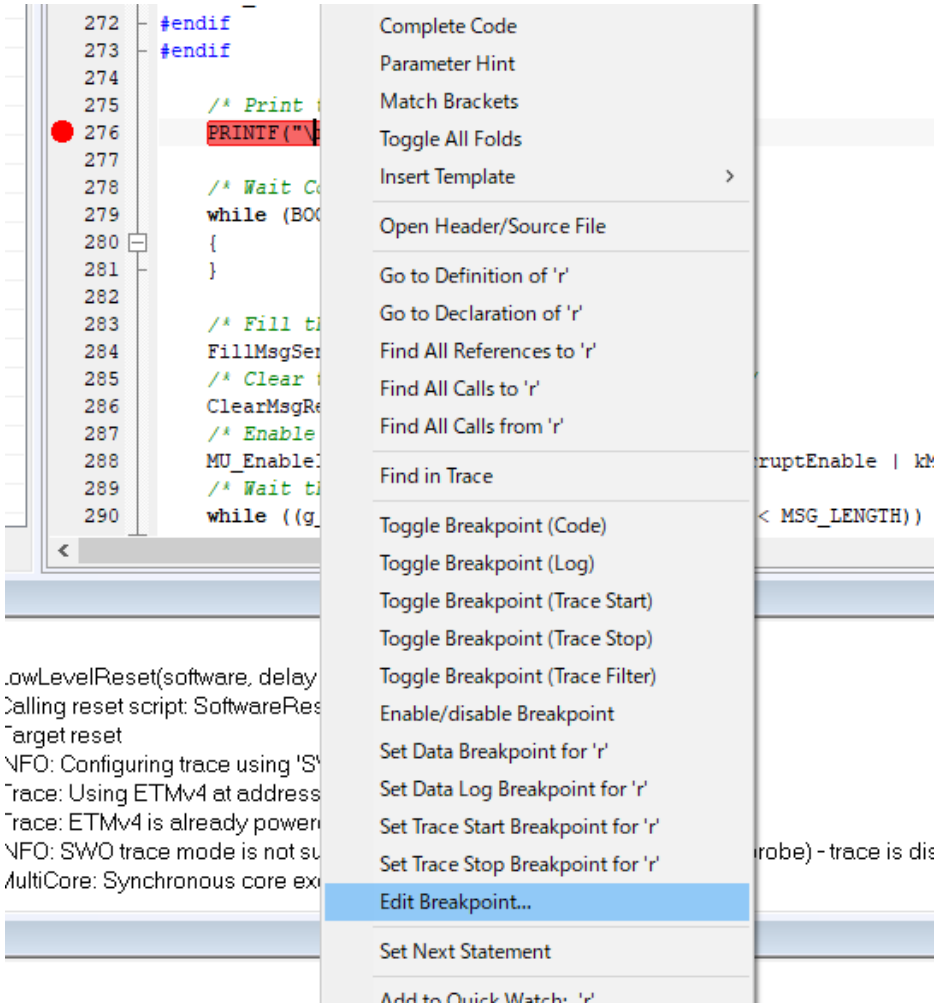
Using CMSIS-DAP

1. Configure breakpoint at previous place of “Wait Core 1 is Boot Up” in core0(M7).
2. Set “run macro for M4” in in breakpoint display.
3. Go M7
4. Stop breakpoint
   * Seeing this breakpoint, start M4 automatically
5. Go M7

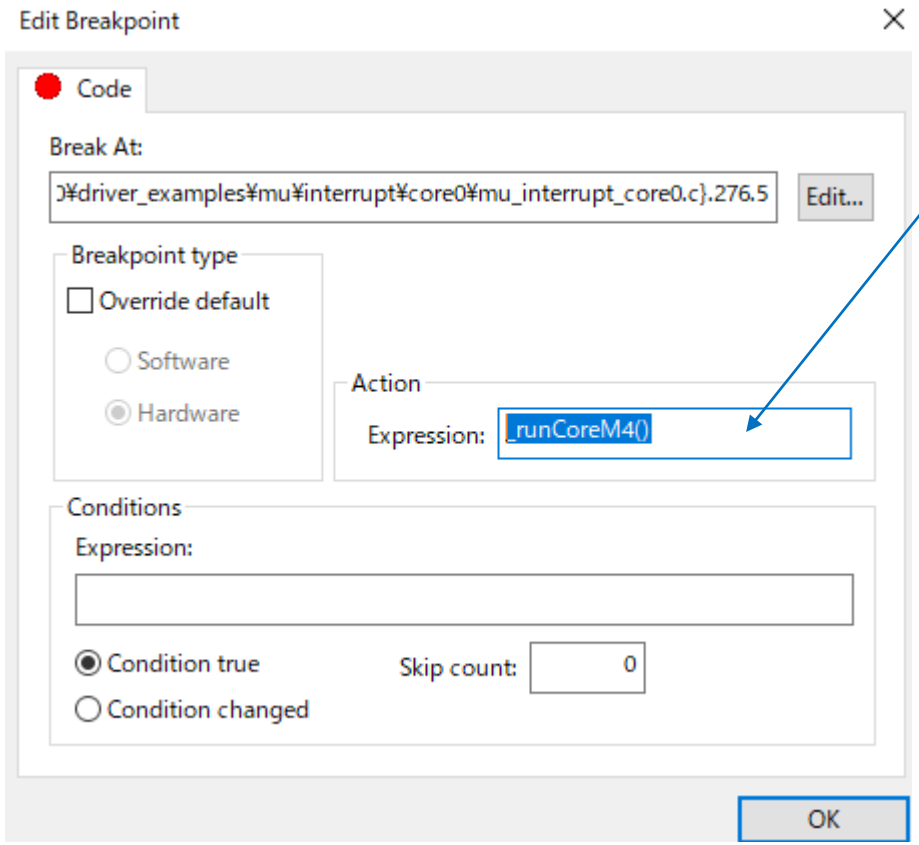
Breakpoint at PRINTF

```
267     /* Boot core 1. */
268 #if BOOT_CORE1_BY_MU
269     MU_BootCoreB(APP_MU, APP_CORE1_BOOT_MODE);
270 #else
271     APP_BootCore1();
272 #endif
273 #endif
274
275     /* Print the initial banner */
276     PRINTF("\r\nMU example interrupt!\r\n");
277
278     /* Wait Core 1 is Boot Up */
279     while (BOOT_FLAG != MU_GetFlags(APP_MU))
280     {
281     }
282
```

Set breakpoint at core0(M7 side)

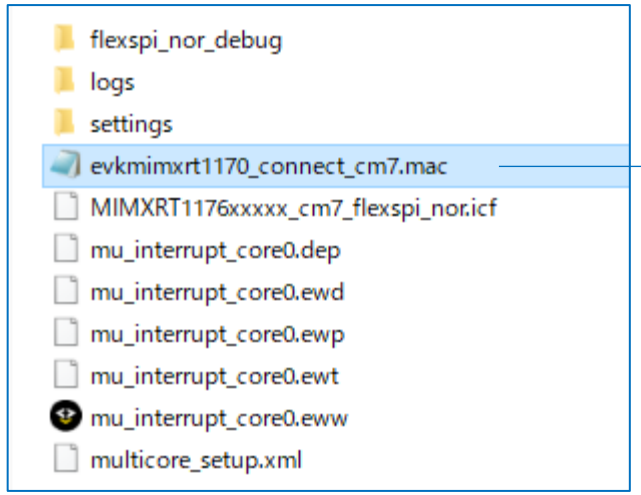


Confiture __runCoreM4 in breakpoint display on M7

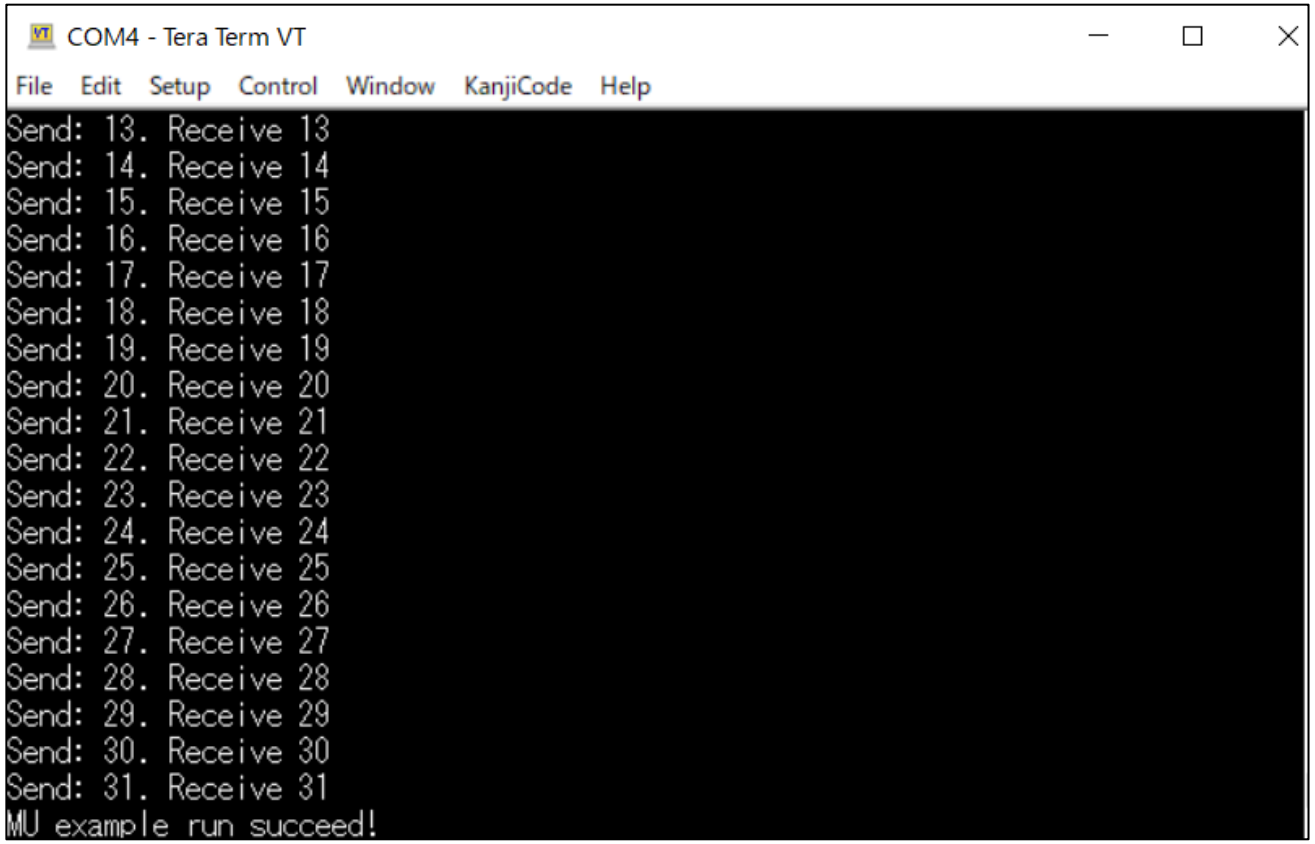



```
_runCoreM4()
{
  __writeMemory32(0xA05F0001,0xE000EDF0,"AP1_Memory");
  return 0;
}
```

Additional code

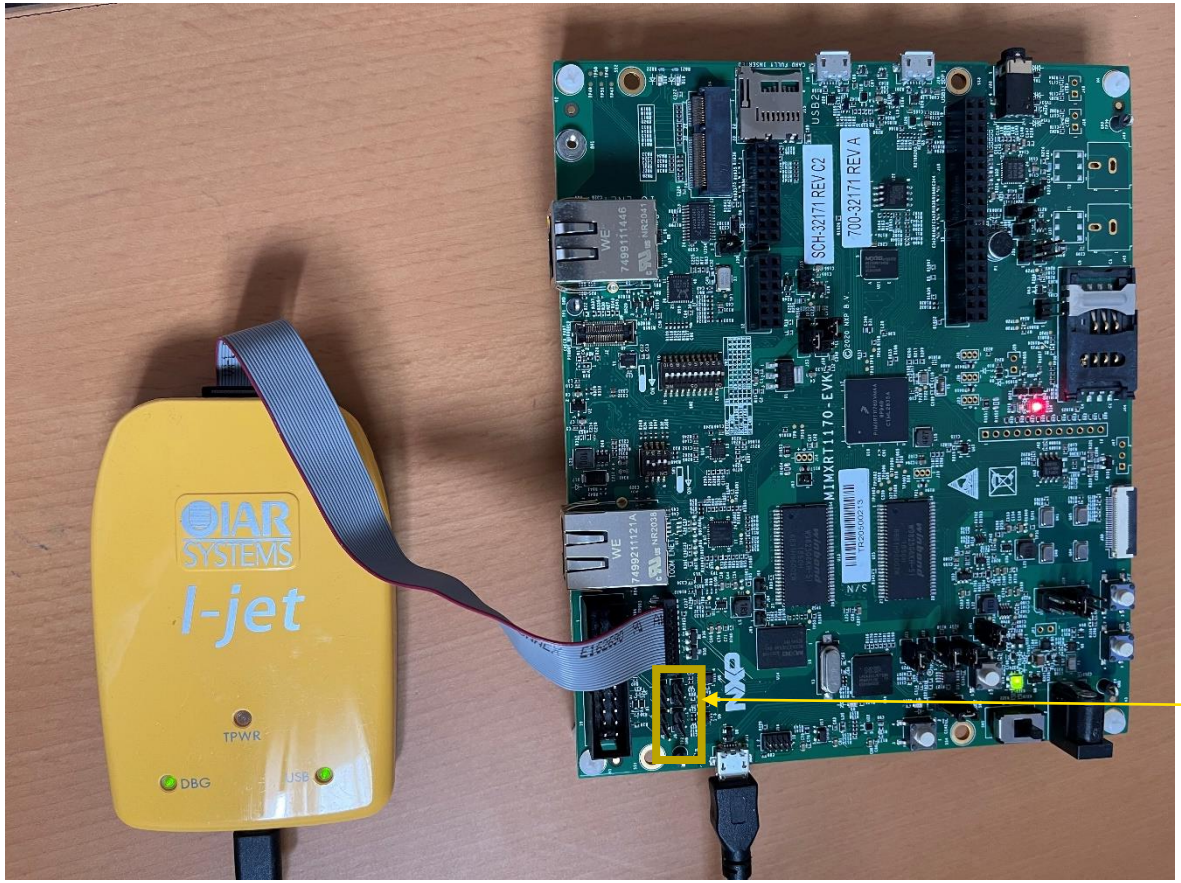



```
_runCoreM4()
{
  __writeMemory32(0xA05F0001,0xE000EDF0,"AP1_Memory");
  return 0;
}
```



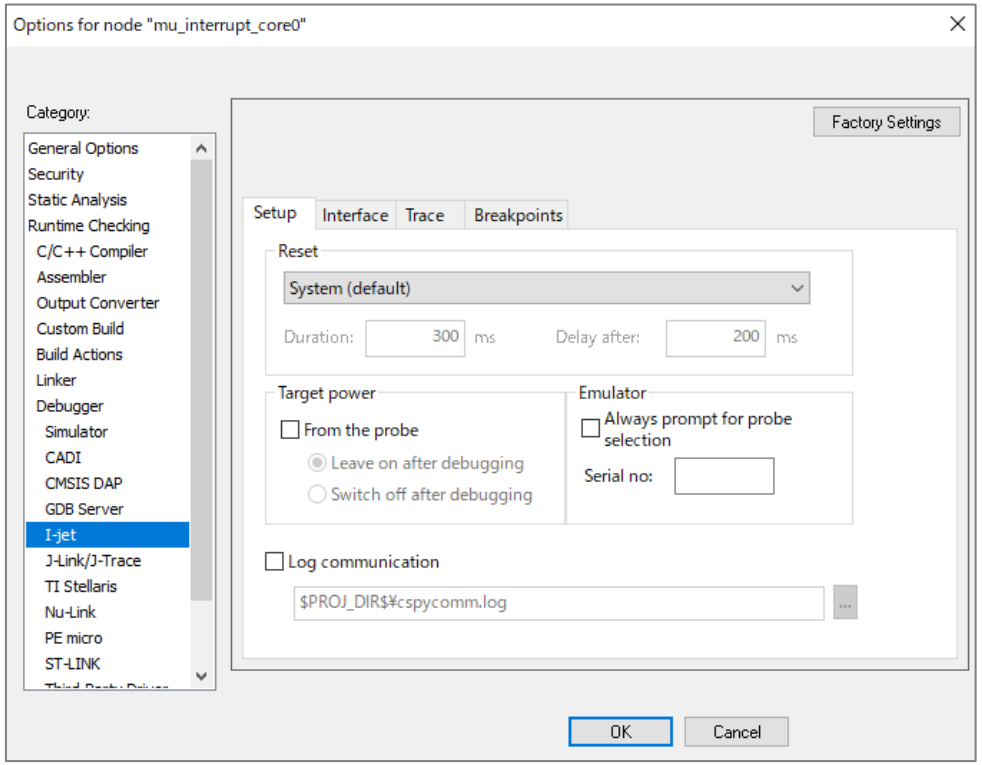
We could see expected behavior.

Before using i-jet

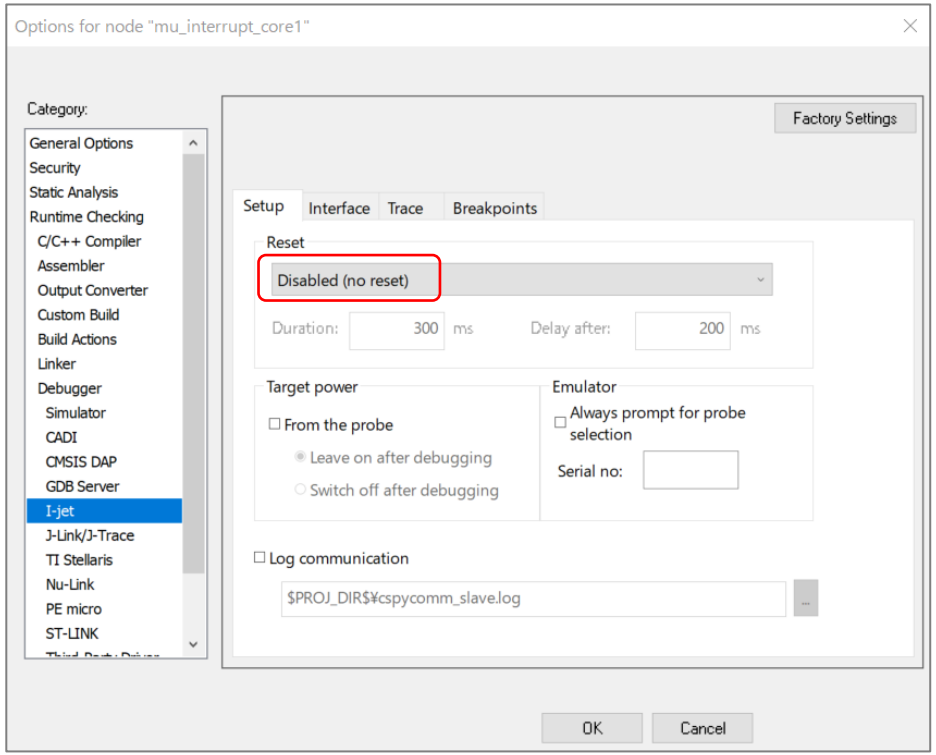


Remove jumper for J5, 6, 7,8

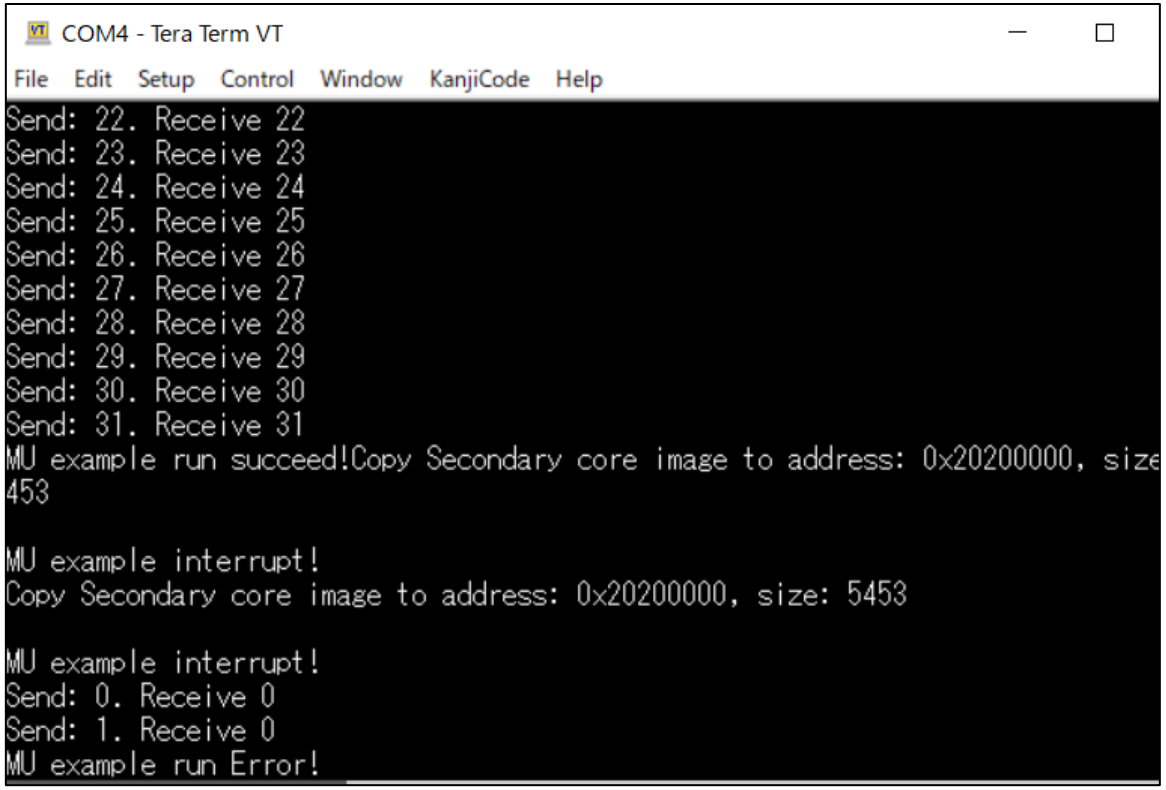
Using i-jet (default case)



Core0(m7)

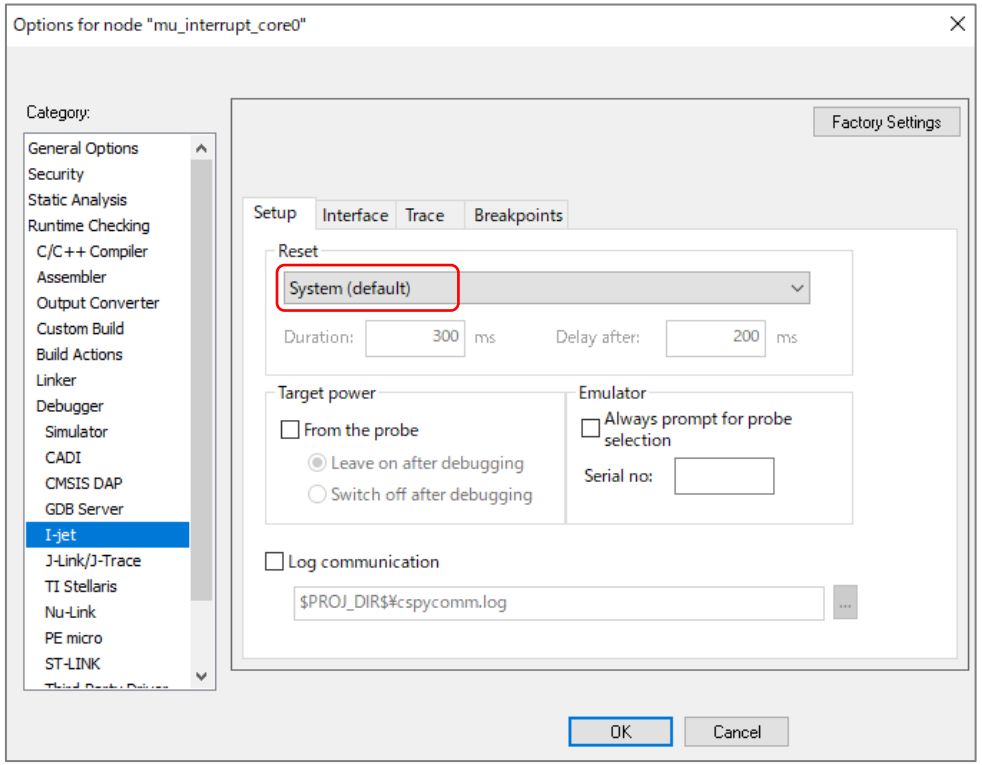


Core1(m4)

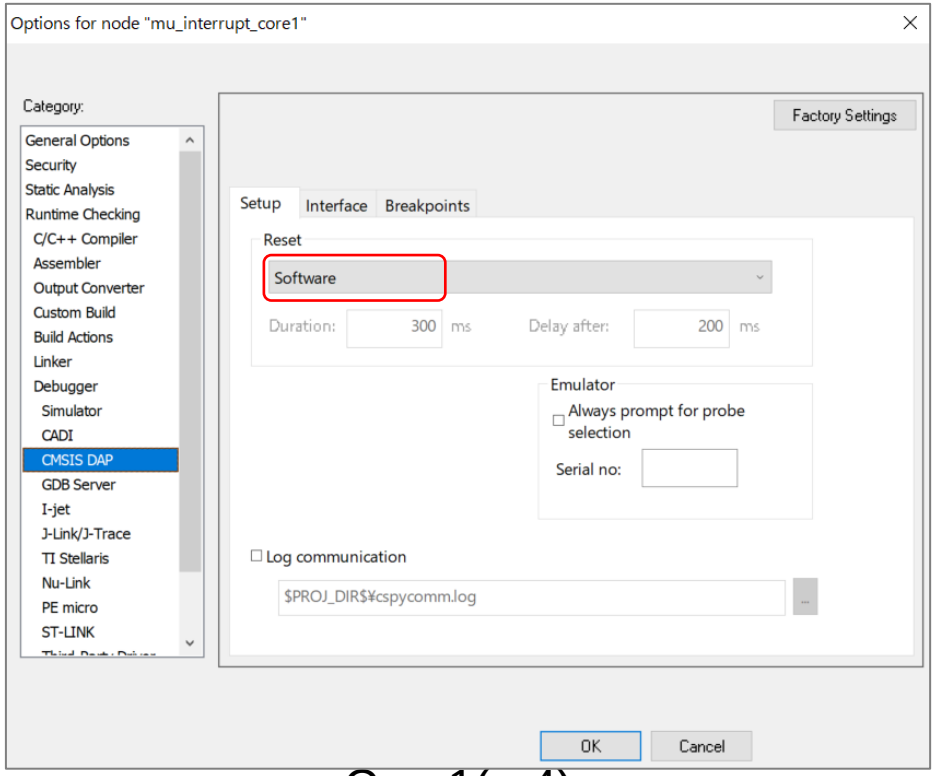


If core1(m4) is adopted “disabled” for reset type of m4, we could see some errors yet.

Using i-jet (optimized case-1)



Core0(m7)



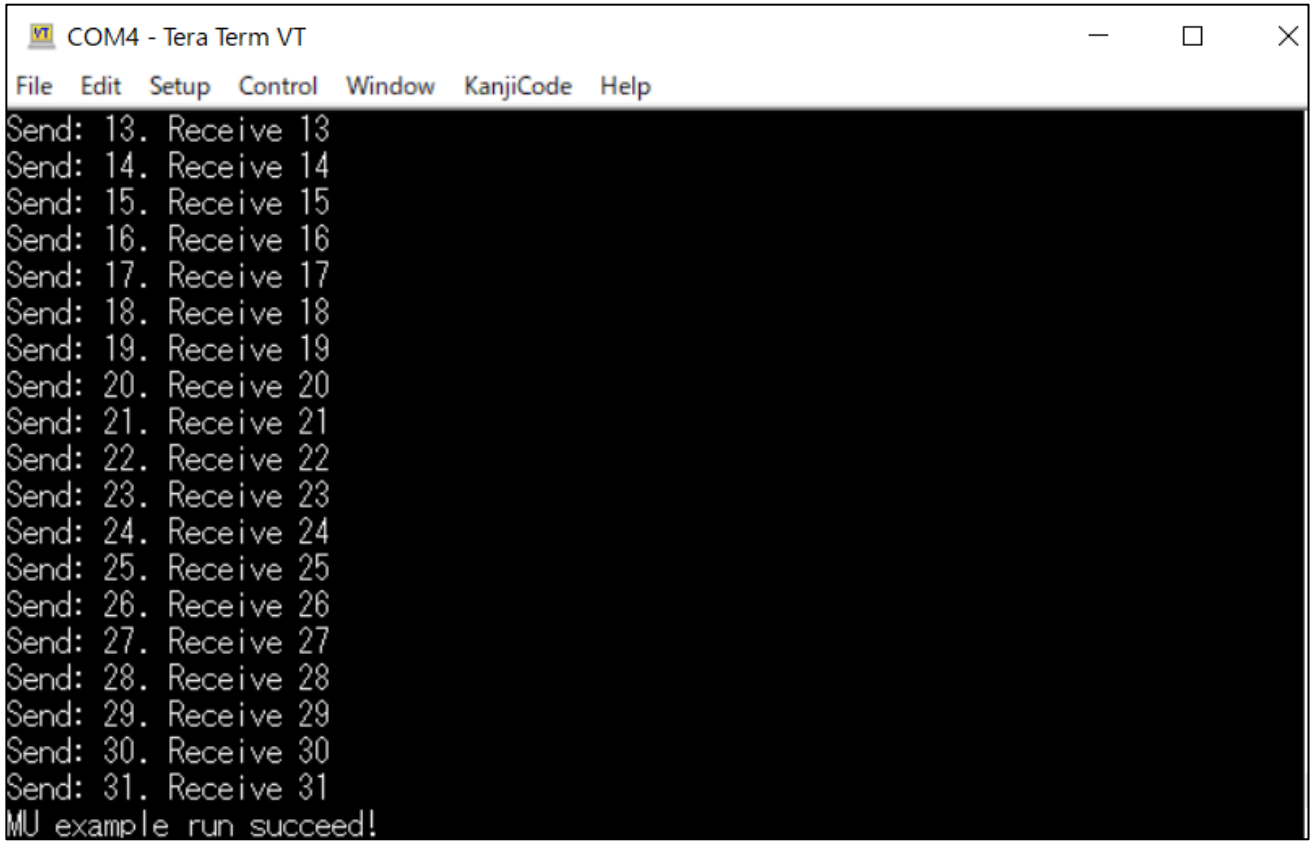
Core1(m4)

EWARM8.50.9 case

Debug display for Core1(m4)

```
Thu Apr 22, 2021 14:57:44: MultiCore: Synchronous core execution DISABLED.
Thu Apr 22, 2021 14:57:44: MultiCore: Synchronous core execution DISABLED.
Thu Apr 22, 2021 14:57:44: SWD clock detected: 12MHz
Thu Apr 22, 2021 14:57:44: Notification to core-connect hookup.
Thu Apr 22, 2021 14:57:44: Connected DAP v2 on SWD. Detected DP ID=0x6ba02477.
Thu Apr 22, 2021 14:57:44: DMAC: Enable M4 core!
Thu Apr 22, 2021 14:57:44: Connecting to TAP#0 DAP AHB-AP-CM port 0x1 (IDR=0x24770011).
Thu Apr 22, 2021 14:57:44: Recognized CPUID=0x410fc241 Cortex-M4 r0p1 arch ARMv7-M
Thu Apr 22, 2021 14:57:44: Debug resources: 6 instruction comparators, 4 data watchpoint
```

After changing reset type from “disabled” to “software”



If core1(m4) is adopted “software” for reset type, we could see expected behavior.

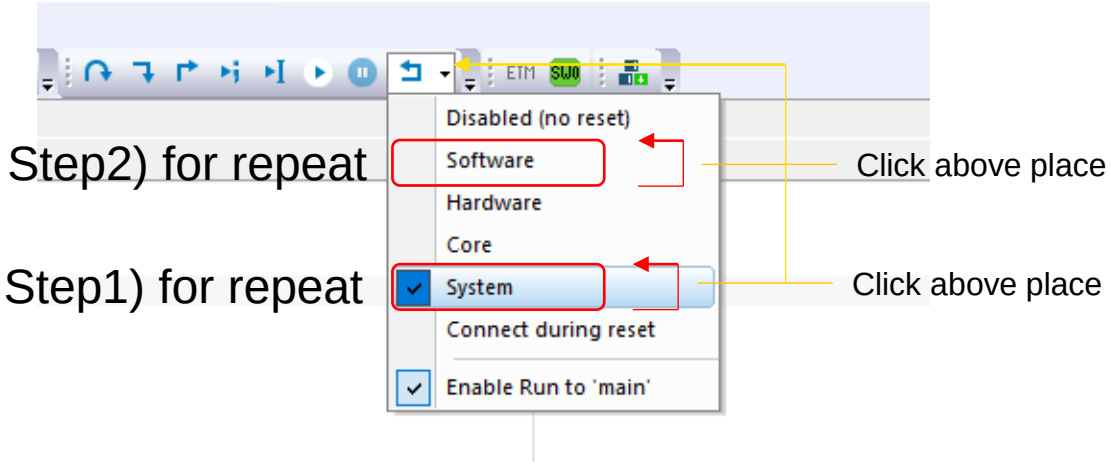
Caution to repeat this demo

EWARM8.50.9 case

1. Configure breakpoint at previous place of “Wait Core 1 is Boot Up” in core0(M7).
2. Set “run macro for M4” in in breakpoint display.
3. Go M7
4. Stop breakpoint
   * Seeing this breakpoint, start M4 automatically
5. Go M7

When repeating this demo,

1. reset with “System” on M7
2. reset with “Software” on M7
3. Go M7

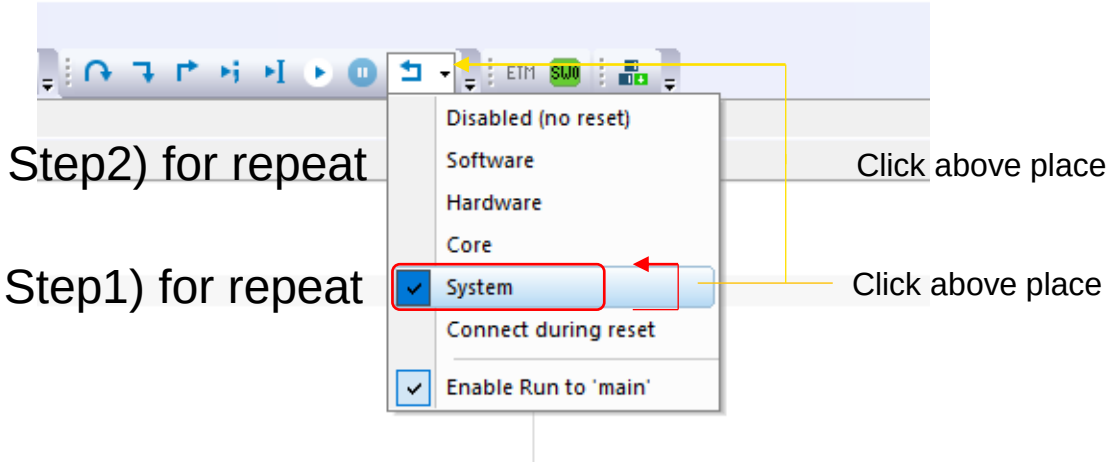


Caution to repeat this demo

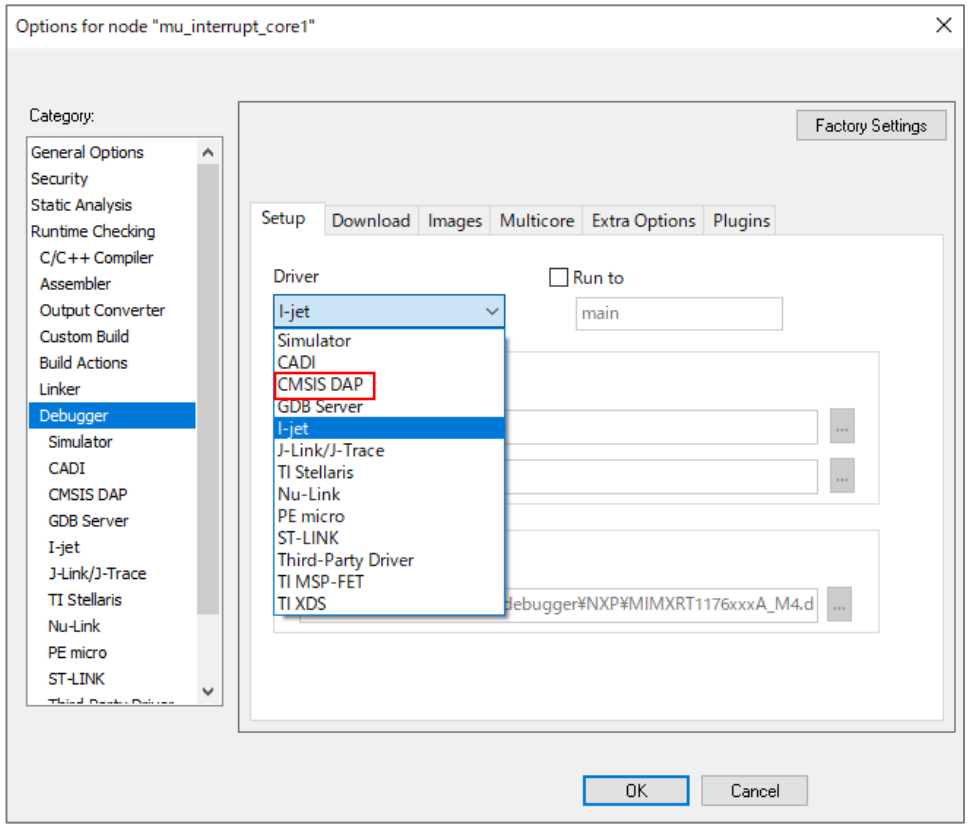
EWARM9.10.X case

1. Configure breakpoint at previous place of “Wait Core 1 is Boot Up” in core0(M7).
2. Set “run macro for M4” in in breakpoint display.
3. Go M7
4. Stop breakpoint
   * Seeing this breakpoint, start M4 automatically
5. Go M7

When repeating this demo,
1. reset with “System” on M7
2. Go M7



Appendix



After changing from CMSIS-DAP to i-jet, re-build m4 and m7 again just in case.

Thank you