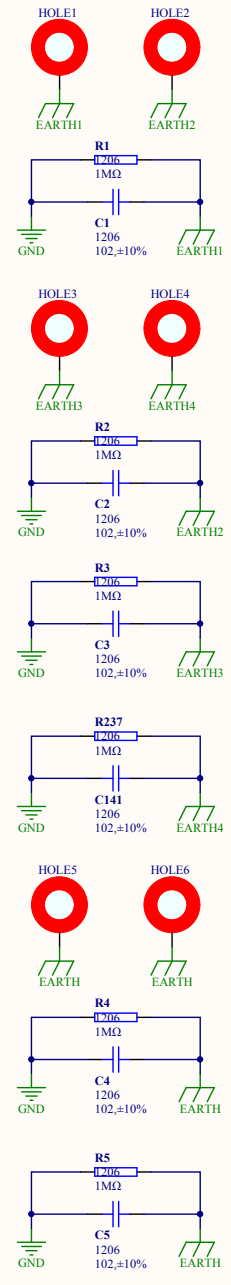
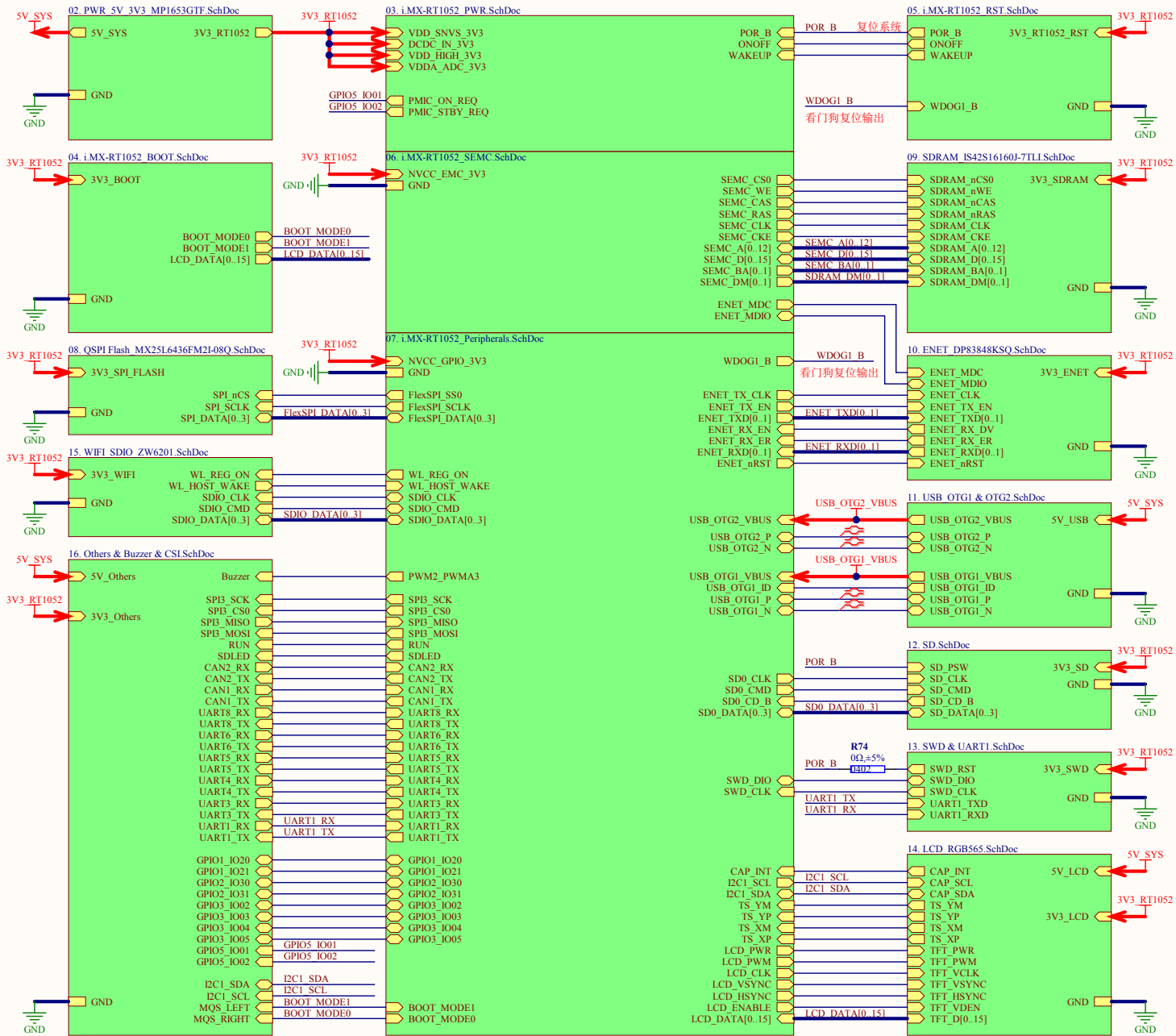
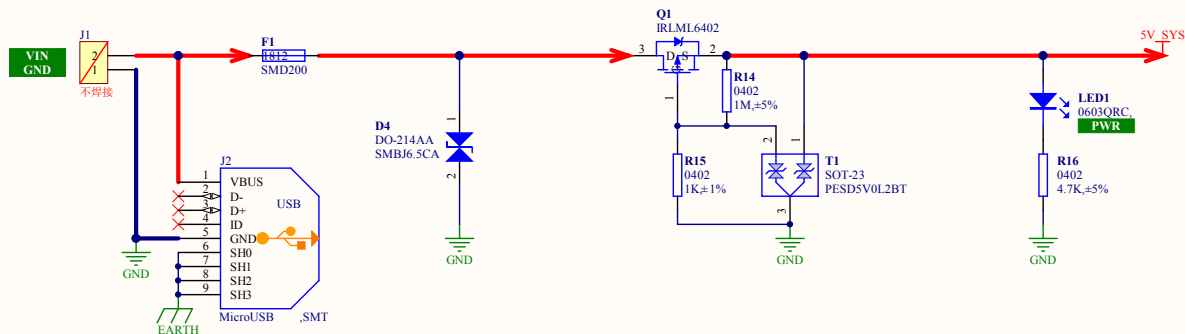
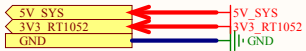


# 1. MAIN\_RT1052



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(2-1) 5V

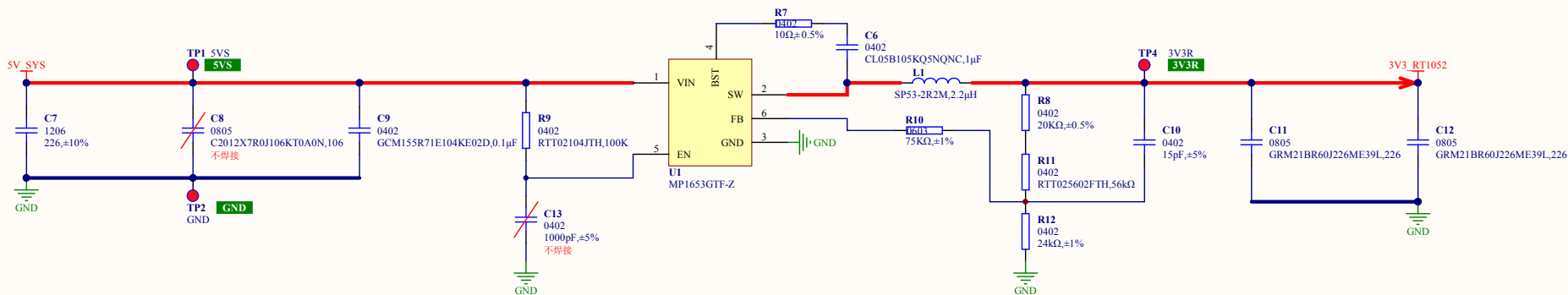


EasyARM-RT1052评估套件版本	焊接的处理器芯片型号	焊接的FLASH芯片型号	供电方案
Rev. A	PIMXRT1052CVL5A	MX25L6436FM2I-08Q (旺宏)	LD0+DCDC (5V转3/3.3V) /MP1482DN-LF-Z (12V转5V, 预留), 电路复杂
Rev. B	-	-	-
Rev. C	MIMXRT1052CVL5A	IS25LP064A-JBLE (ISSI)	LD0+DCDC (5V转3/3.3V) /MP1482DN-LF-Z (12V转5V, 预留), 电路复杂
Rev. D (最新发布版本)	MIMXRT1052CVL5B	IS25LP064A-JBLE (ISSI)	修复DCDC的Bug, 可支持单3.3V DCDC给系统供电, 电源电路简化

(2-2) 3V3

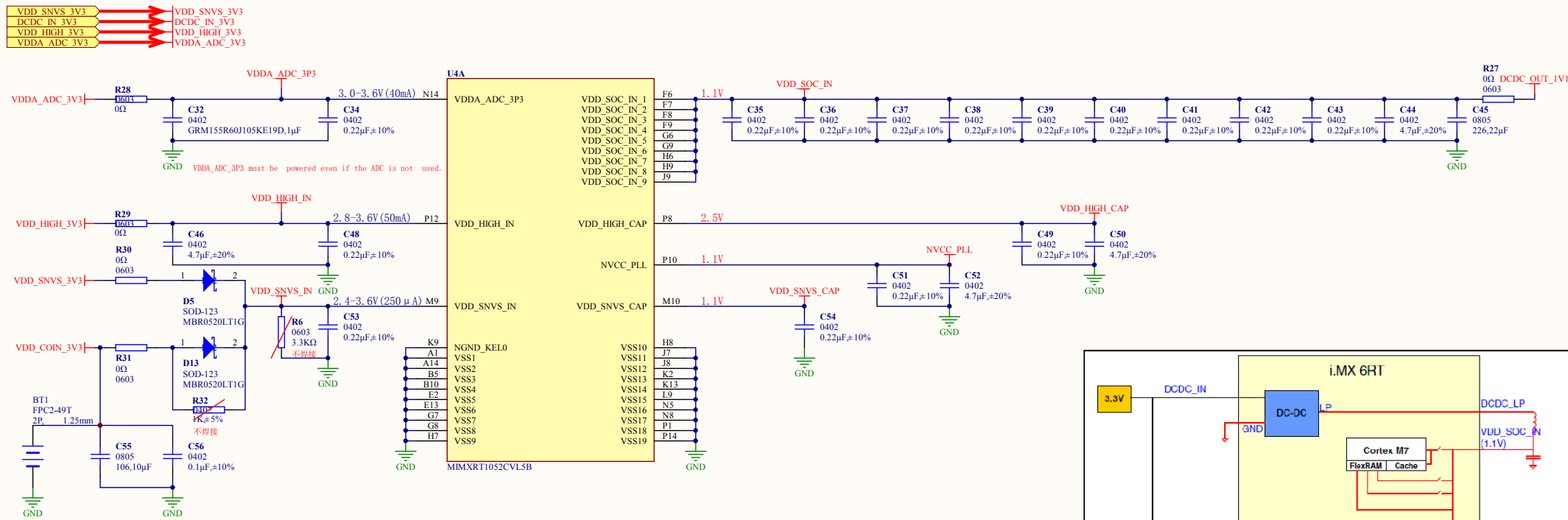
要点1: EasyARM-RT1052 Rev.D版本焊接的RT处理器版本型号为 MIMXRT1052CVL5B

B结尾版本型号的供电方式可支持单3.3V供电方案, 为简化电源电路, 这里使用MP1653给系统全部模块进行供电!

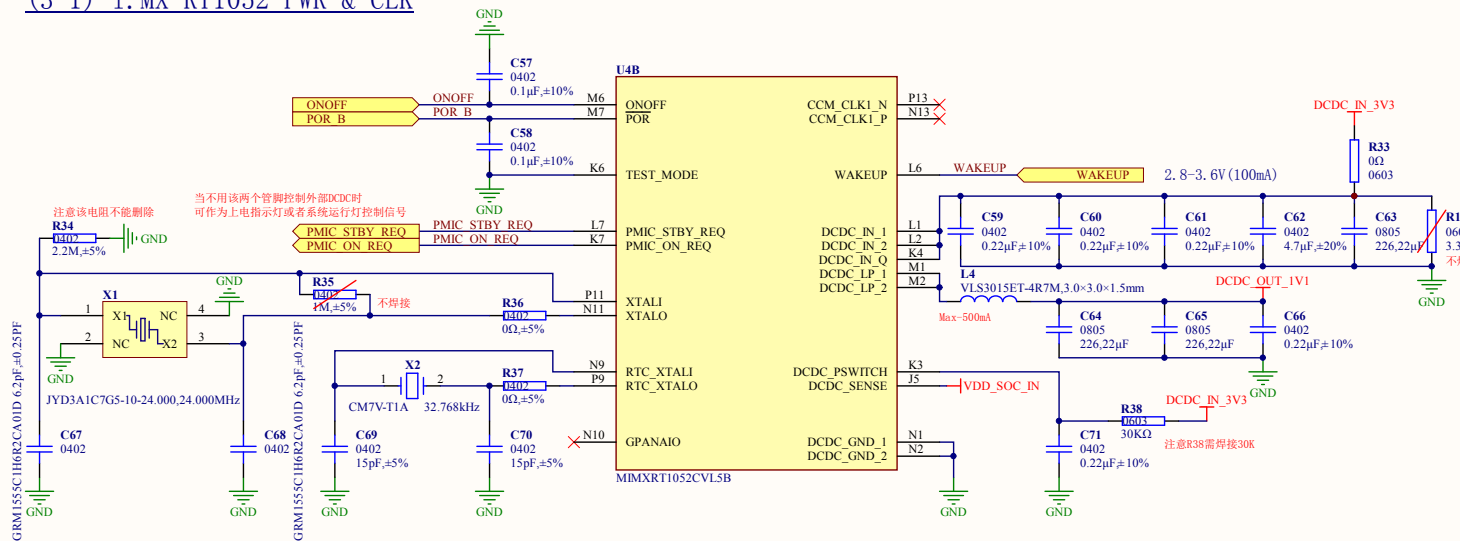
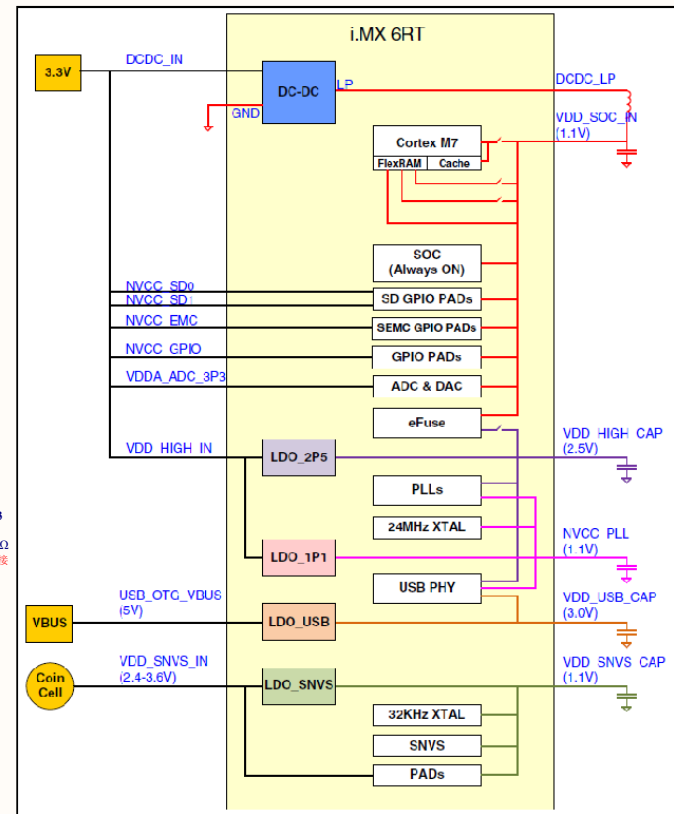


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### 3. i.MX-RT1052 PWR & CLK



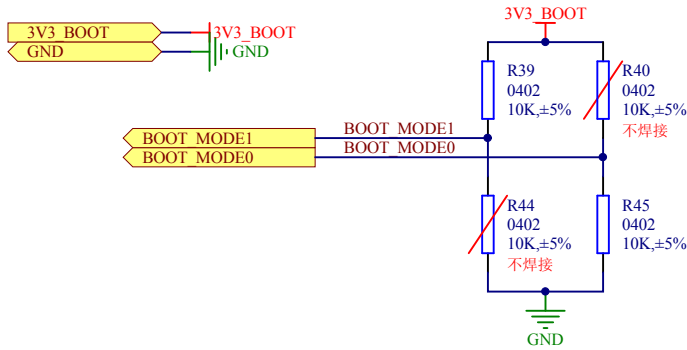
(3-1) i.MX-RT1052 PWR & CLK



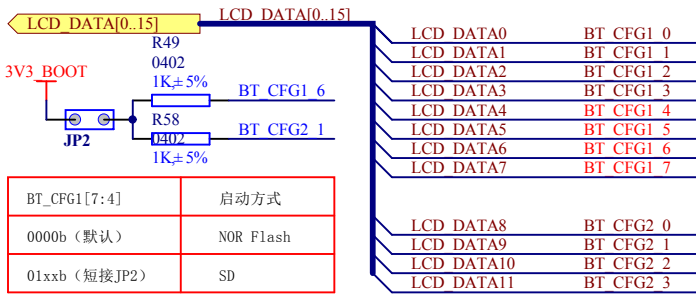
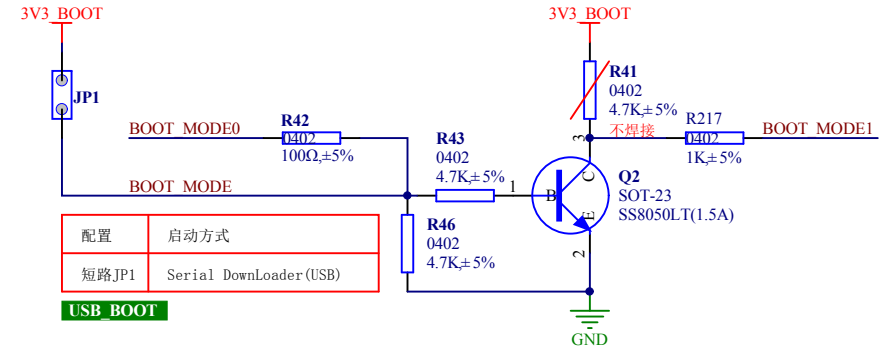
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## 4. i.MX-RT1052\_BOOT

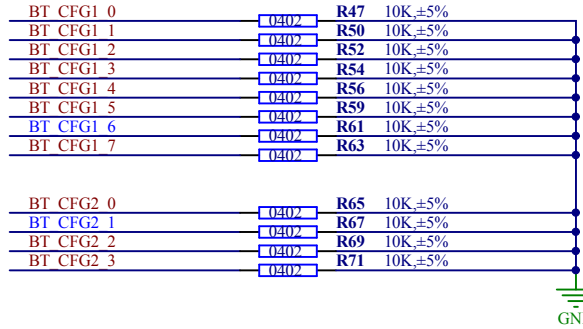
### (4-1) BT MODE SELECT



BOOT_MODE[1:0]	BOOT_TYPE
00	Boot From Fuse
01	Serial Downloader
10	Internal Boot (Default)
11	Reserved



BT_CFG1[7:4]	启动方式
0000b (默认)	NOR Flash
01xxb (短接JP2)	SD



要点1: 由于BOOT配置信号BT\_CFG1、2与LCD信号是复用的关系, 因此设计中需特别注意  
 第一: 建议仅作为LCD液晶显示输出, 当用作其它功能输出时需注意核对外接负载是否改变原本设定的采集电平  
 第二: 不建议将该配置信号作为输入使用, 如果不得不用, 建议采用隔离的方案或者采用模拟开关进行隔离处理

3. BOOT\_CFG and BOOT\_MODE signals multiplexed with LCD signals

To reduce incorrect boot-up mode selections, do one of the following:

- Use the LCD boot interface lines **only** as processes or **outputs**. Make sure that the LCD boot interface lines are not loaded down (such that the level is interpreted as low during the powerup) when the intent is to be at a high level, or the other way round.
- If the LCD boot signal must be configured as an **input**, isolate the LCD signal from the target driving source with an analog switch and apply the logic value with a second analog switch. Alternately, the peripheral devices with 3-state outputs may be used. Ensure that the output is high-impedance.

Using the LCD boot interface lines as inputs may result in a wrong boot because of the source overcoming the pull resistor value. A peripheral device may require the LCD signal to have an external or on-chip resistor to minimize signal floating. If the usage of the LC boot signal affects the peripheral device, then an analog switch, an open collector buffer, or an equivalent shall isolate the path. A pull-up or pull-down resistor at the peripheral device may be required to maintain the desired logic level. See the switch or device data sheet for the operating specifications.

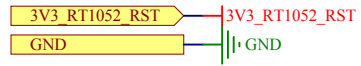
### (4-2) FLASH & SD BOOT TYPE

BOOT_CFG1[7:4]	Boot device
0000b	Serial NOR boot via FlexSPI
01xxb	SD Boot via uSDHC
10xxb	eMMC/MMC boot via uSDHC
001xb	SLC NAND boot via SEMC
0001b	Parallel NOR boot via SEMC
11xxb	Serial NAND boot via FlexSPI

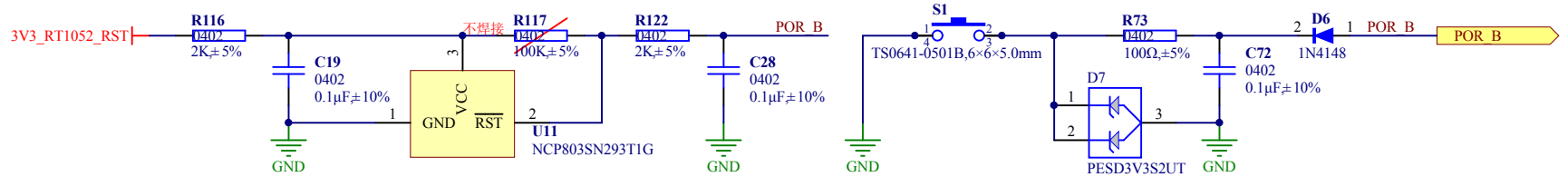
BOOT TYPE	BT_CFG2_3	BT_CFG2_2	BT_CFG2_1	BT_CFG2_0	BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG1_3	BT_CFG1_2	BT_CFG1_1	BT_CFG1_0
FlexSPI	Loop	FLASH_TYPE				0000-QSPI Flash			Hold time before read from device	0-DIS	Reserved	
Serial	0-DIS	000-3Byte	001-4Byte	010-1V8	HyperFlash				00-500us	01-1ms	EncryptedXIP	
NOR Flash	1-EN (Debug only)	011-3V3	HyperFlash	100-MXIC	Octal DDR				10-3ms	11-10ms	1-EN	
SD	Loop	Reserved	Bus Width	SD1 VOLTAGE SELECTION	0	1	SD/SDXC Speed		SD Cy EN	SD CLK SLE	Port Selet	Fast Boot
	0-DIS		0-1bit	0-3.3V			00-N/SDR12	01-H/SDR25	0-DIS	0-SD	0-SD1	0-Regular
	1-EN (Debug only)		1-4bit	1-1.8V			10-SDR50	11-SDR104	1-EN	1-direct	1-SD2	1-Fast BT

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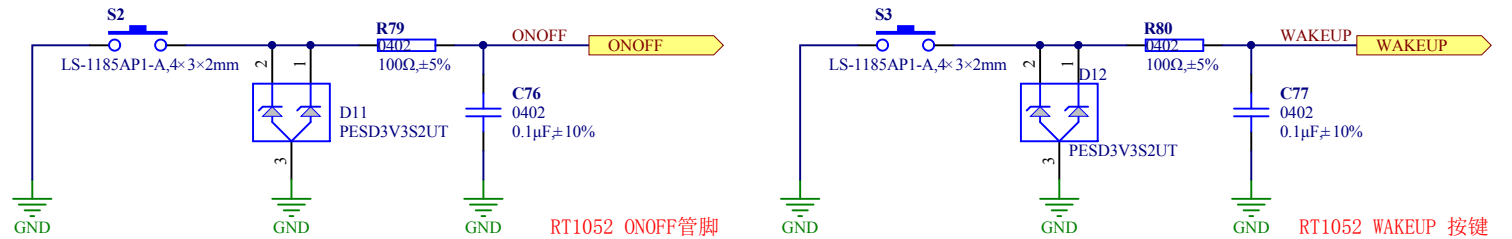
## 5. i.MX-RT1052\_RST & KEY



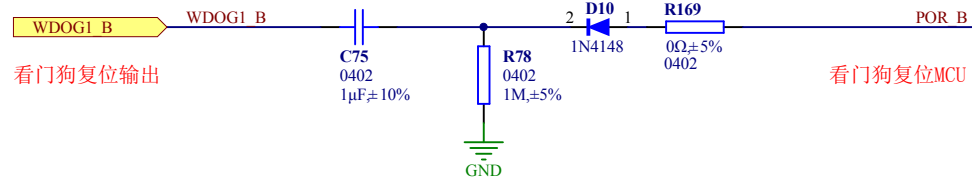
### (5-1) RT1052\_RST



### (5-2) RT1052\_FUN\_Button



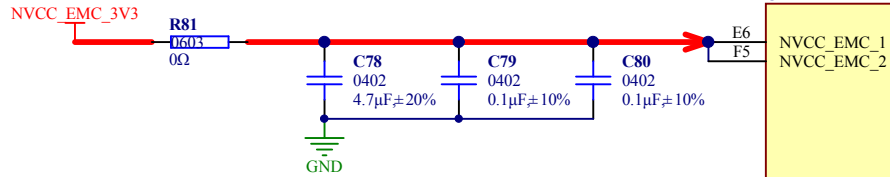
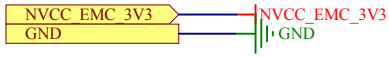
### (5-3) SYS\_WDG\_RST



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# 6. i.MX-RT1052 SMC

## (6-1) i.MX-RT1052 SMC



要点1: SMC支持8/16位SDRAM接口, 每个片选支持高达512Mb=64MB, 最大支持4个片选

- SDRAM interface
  - Support 8/16 bit modes
  - Up to **512Mb** per each Chip Select (CS) and up to 4 CS

要点2: 由于RT的列地址最小只支持9bit, 因此SDRAM容量选型需注意匹配COL地址位数, 避免选型错误! 对于ISSI及旺宏的SDRAM, 16位模式下的容量最小只支持16MB, 8MB及以下容量, RT支持不了。

i.MX RT1050 Processor Reference Manual, Rev. 1, 03/2018	
NXP Semiconductors 2807	
Memory Map and register definition	
Field	Function
COL	00b - 12 bit 01b - 11 bit 10b - 10 bit 11b - 9 bit

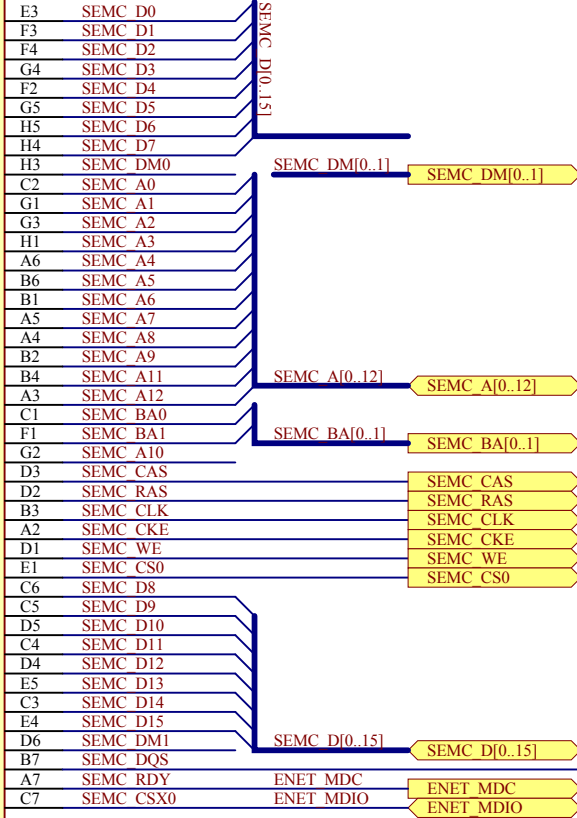
ADDRESS TABLE	
Parameter	4M x 16
Configuration	1M x 16 x 4 banks
Refresh Count	Com./Ind. 4K/64ms A1 4K/64ms A2 4K/16ms
Row Addresses	A0-A11
Column Addresses	A0-A7
Bank Address Pins	BA0, BA1
Auto Precharge Pins	A10/AP

ISSI 8MB容量的COL为8位, RT不支持, 如图所示

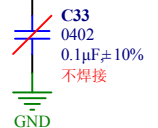
U4D

NVCC EMC 1  
NVCC EMC 2

- GPIO\_EMC 00
- GPIO\_EMC 01
- GPIO\_EMC 02
- GPIO\_EMC 03
- GPIO\_EMC 04
- GPIO\_EMC 05
- GPIO\_EMC 06
- GPIO\_EMC 07
- GPIO\_EMC 08
- GPIO\_EMC 09
- GPIO\_EMC 10
- GPIO\_EMC 11
- GPIO\_EMC 12
- GPIO\_EMC 13
- GPIO\_EMC 14
- GPIO\_EMC 15
- GPIO\_EMC 16
- GPIO\_EMC 17
- GPIO\_EMC 18
- GPIO\_EMC 19
- GPIO\_EMC 20
- GPIO\_EMC 21
- GPIO\_EMC 22
- GPIO\_EMC 23
- GPIO\_EMC 24
- GPIO\_EMC 25
- GPIO\_EMC 26
- GPIO\_EMC 27
- GPIO\_EMC 28
- GPIO\_EMC 29
- GPIO\_EMC 30
- GPIO\_EMC 31
- GPIO\_EMC 32
- GPIO\_EMC 33
- GPIO\_EMC 34
- GPIO\_EMC 35
- GPIO\_EMC 36
- GPIO\_EMC 37
- GPIO\_EMC 38
- GPIO\_EMC 39
- GPIO\_EMC 40
- GPIO\_EMC 41



要点3: SEMC\_DQS管脚建议悬空处理, 不建议复用为其它功能 否则SDRAM的时钟只能跑80M, 严重的情况甚至会影响SDRAM的使用!

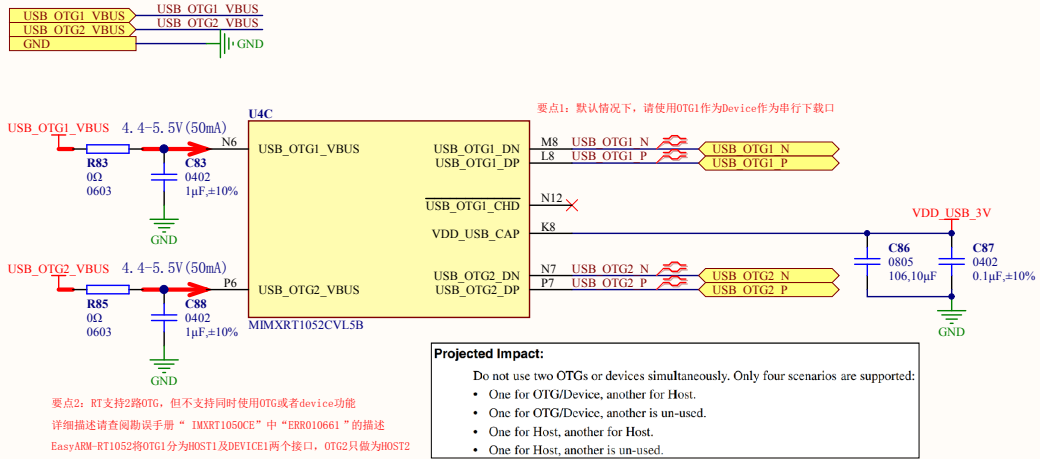


MIMXRT1052CVL5B

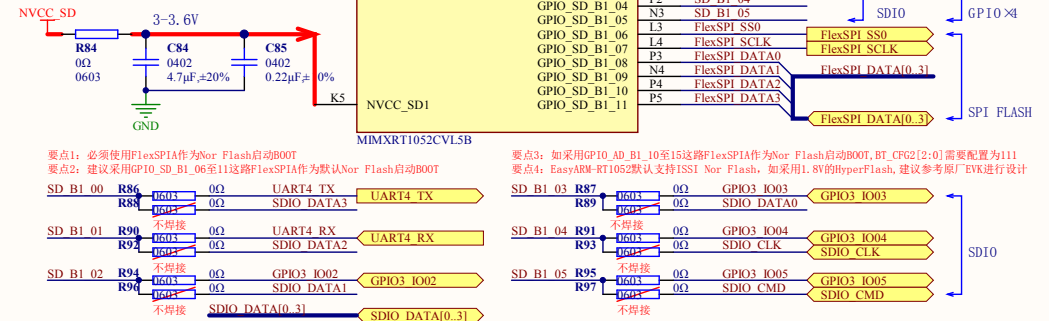
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# 7. i. MX-RT1052\_Peripherals

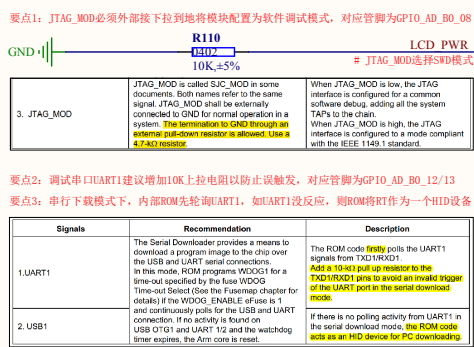
## (7-1) USB OTG1 & HOST2



## (7-2) SD & SPI FLASH



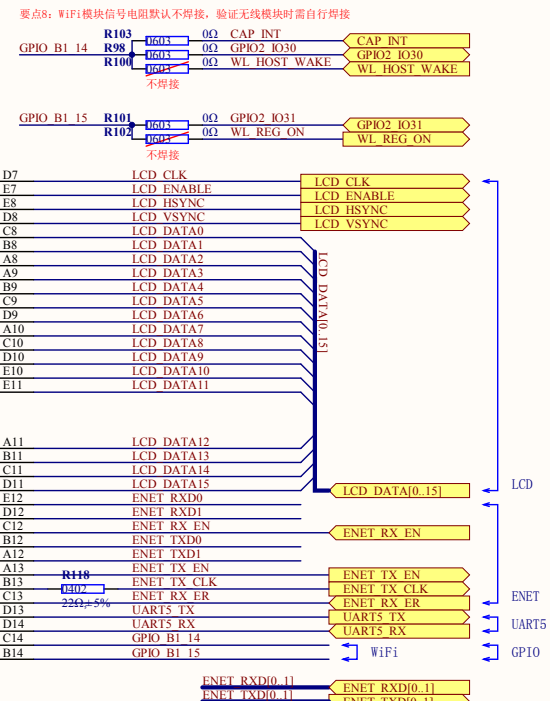
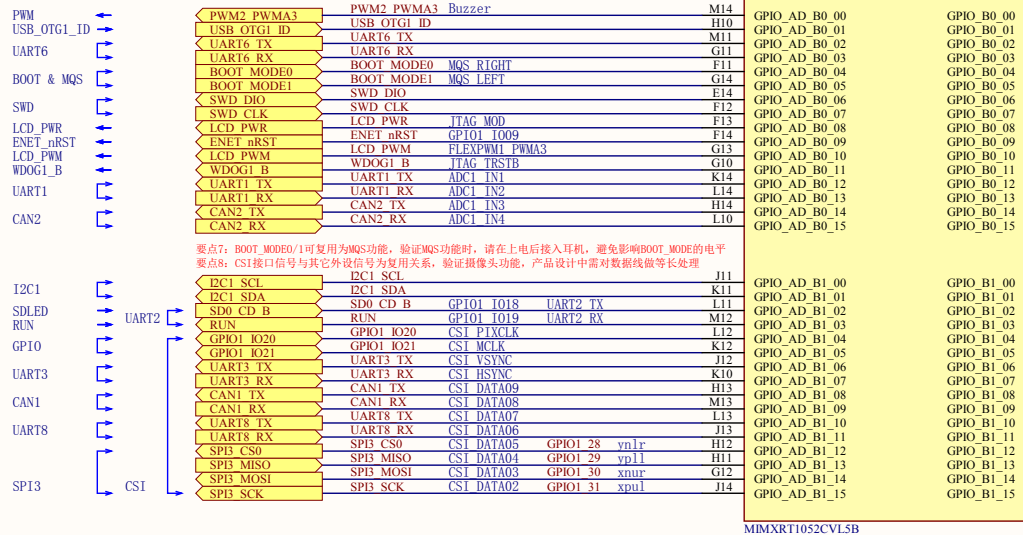
## (7-3) i.MXRT1052 Others



TSC function ports	TSC analogues instance	ADC Ain pin	GPIO ports
ylp0r	1	Ain[0]	GPIO_AD_B1_11
ylp1r	2	Ain[1]	GPIO_AD_B1_12
ylp1l	3	Ain[2]	GPIO_AD_B1_13
ynmr	4	Ain[3]	GPIO_AD_B1_14
xpu1	5	Ain[4]	GPIO_AD_B1_15

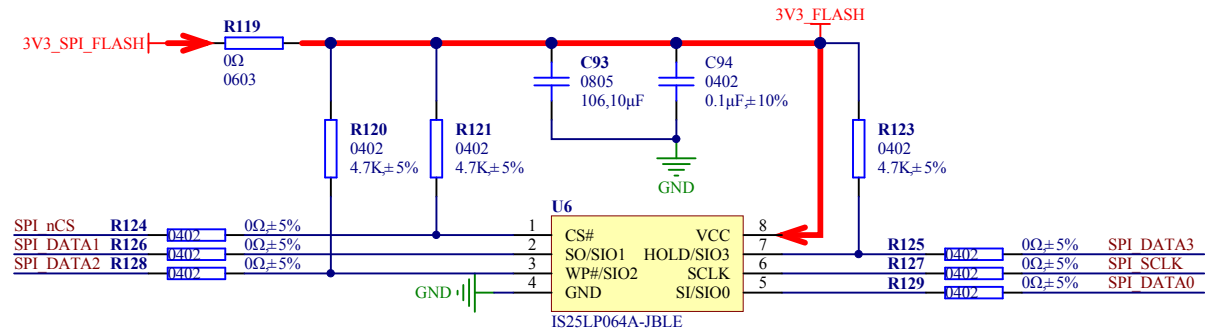
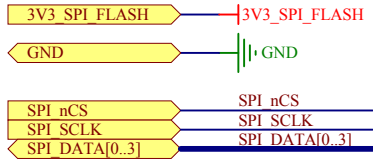
TS YM	TS YM	R184	0Ω	GPIO1 28
TS YP	TS YP	R185	0Ω	GPIO1 29
TS XP	TS XP	R186	0Ω	GPIO1 30
TS XM	TS XM	R187	0Ω	GPIO1 31
TS YN	TS YN	R188	0Ω	GPIO1 27
TS XN	TS XN	R189	0Ω	GPIO1 26



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# 8. QSPI Flash

## (8-1) QSPI Flash

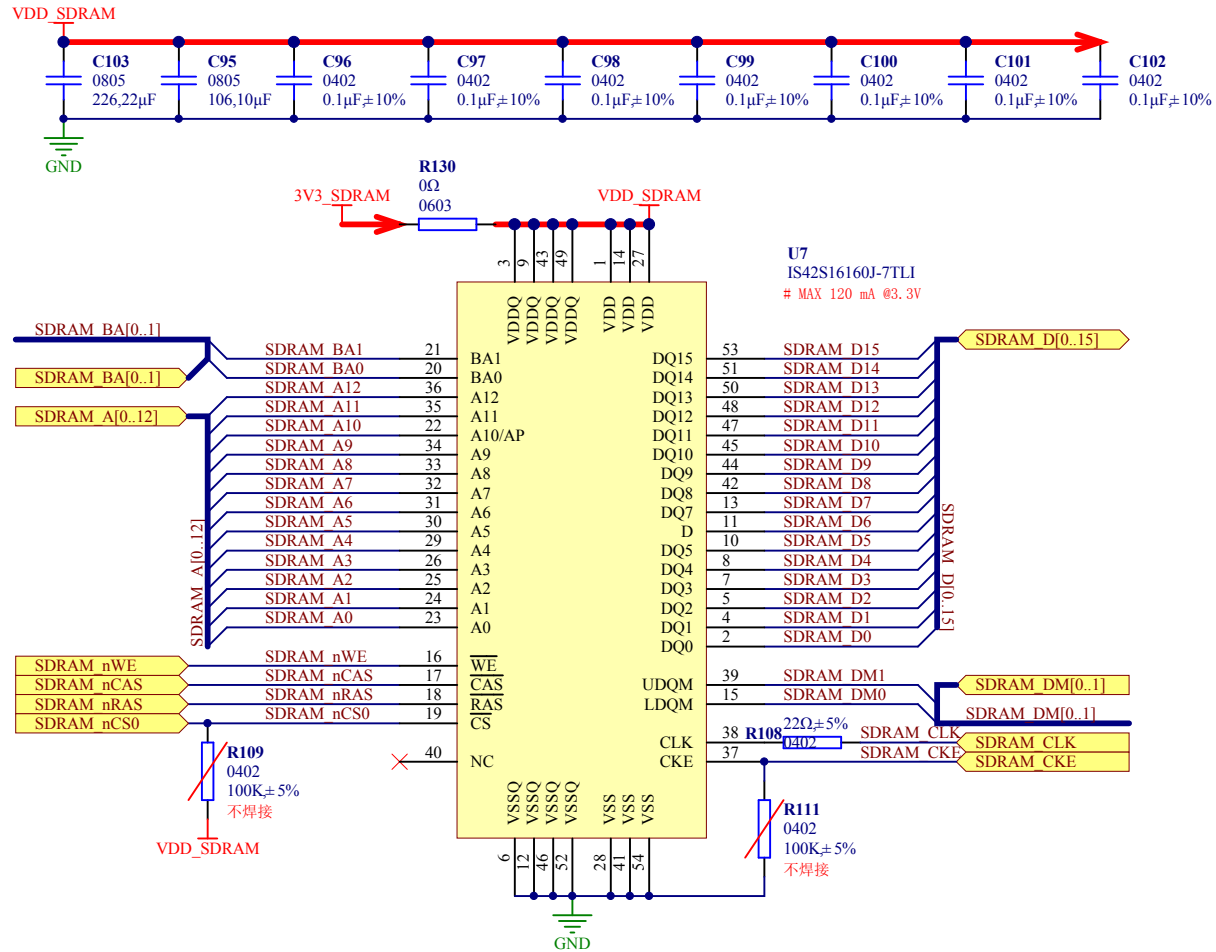
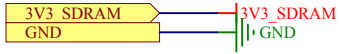


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# 9. SDRAM\_IS42S16160J-7TLI

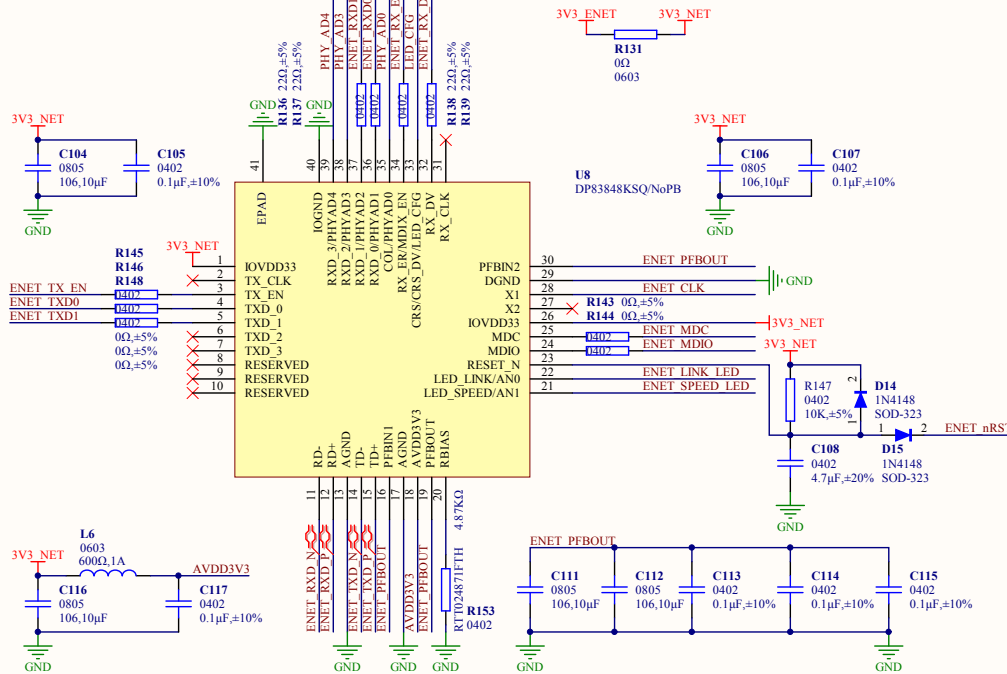
## (9-1) SDRAM-32MB



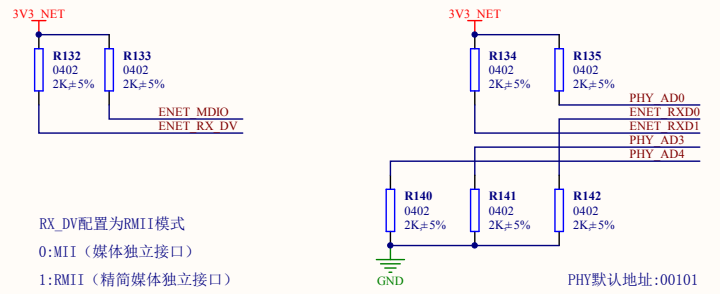
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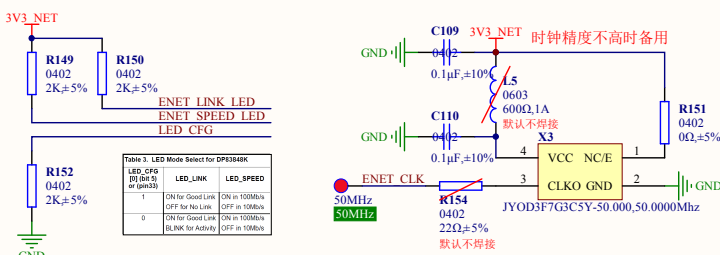
(10-1) ENET PHY



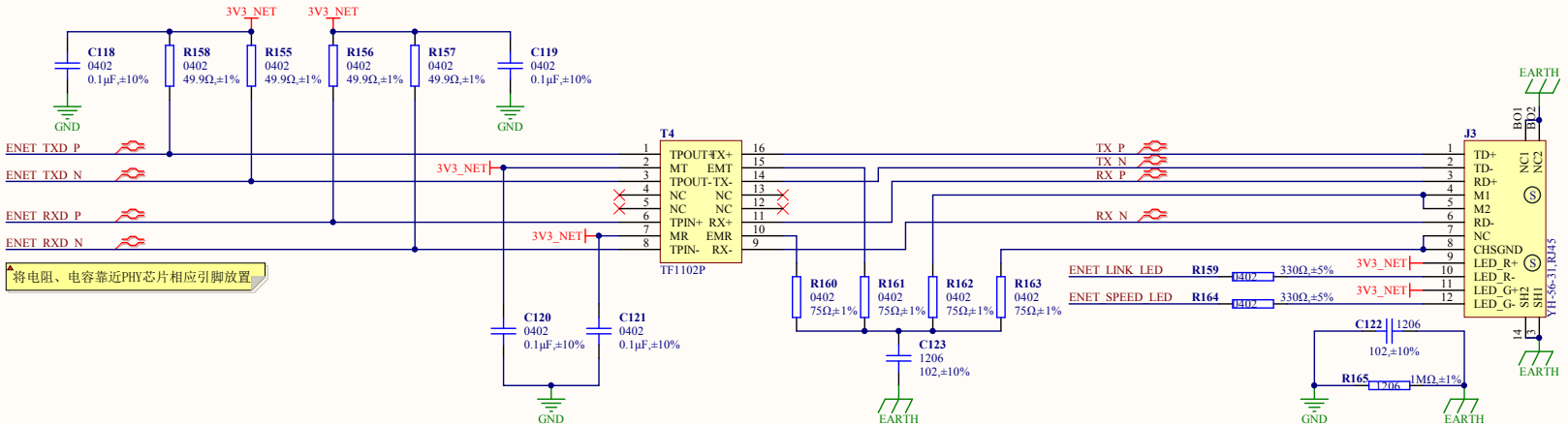
(10-2) PHY CFG & ADD



(10-3) PHY CFG & CLK



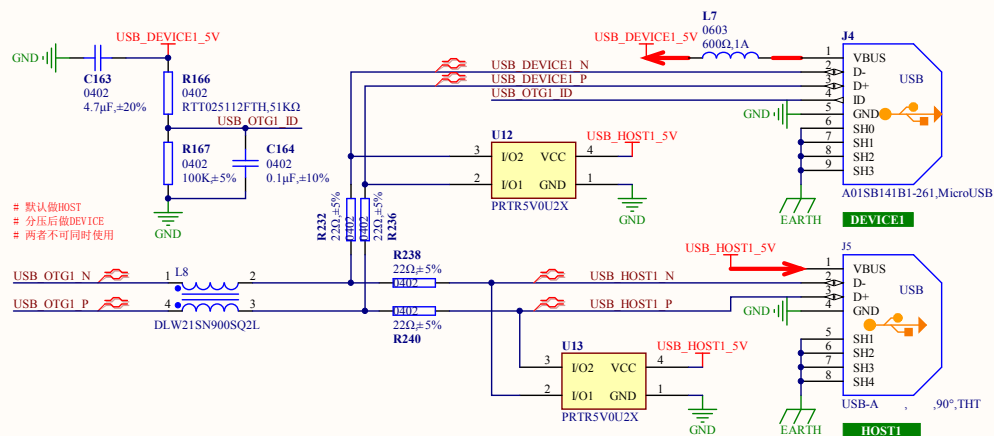
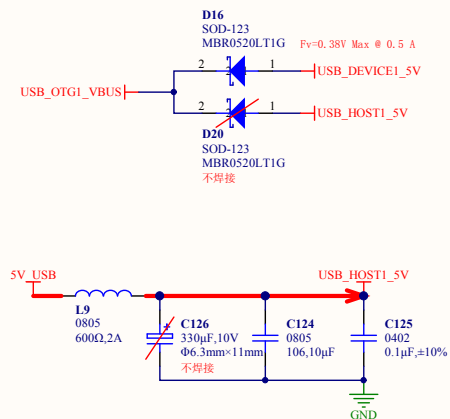
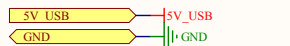
(10-4) PHY Analog



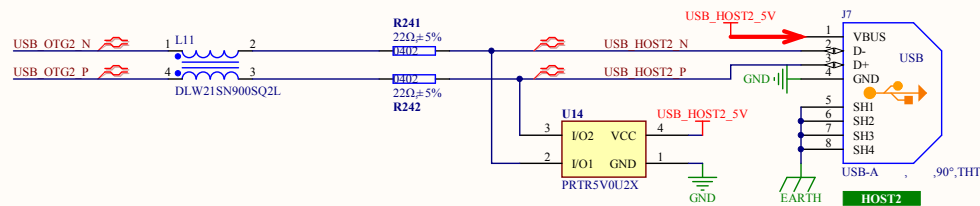
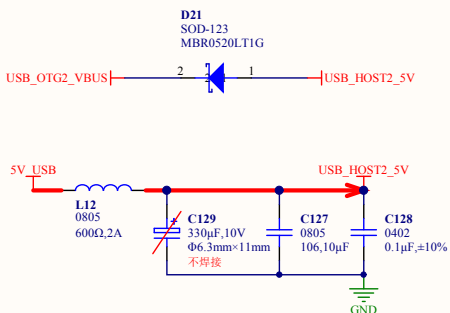
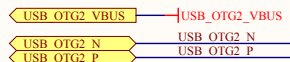
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# 11. <图纸名称>

## (11-1) USB\_OTG1

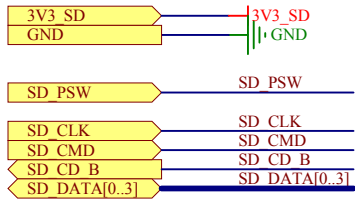


## (11-2) USB\_HOST2



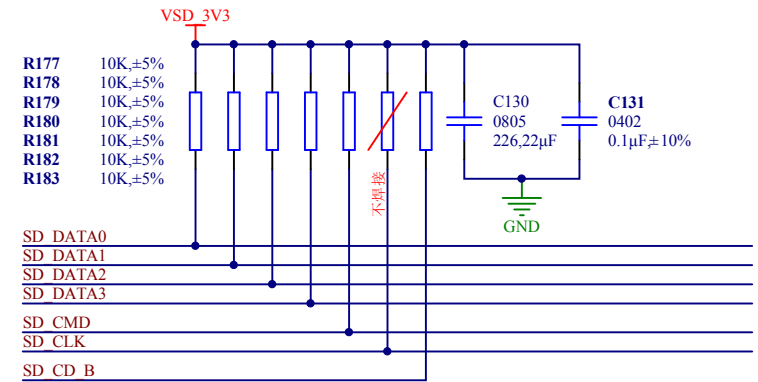
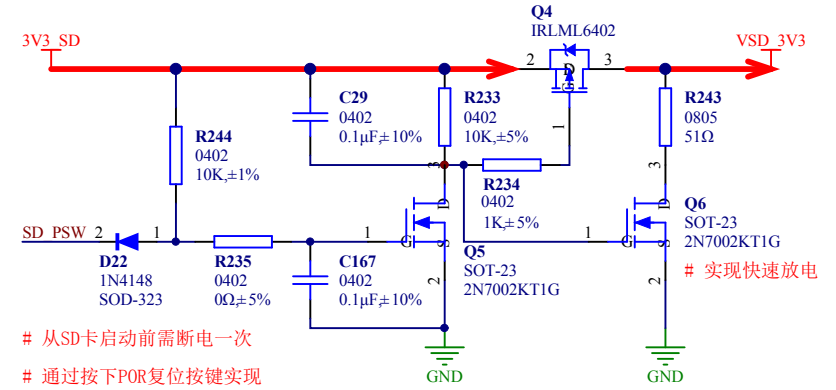
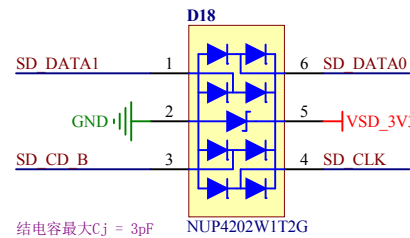
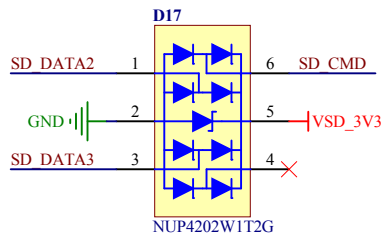
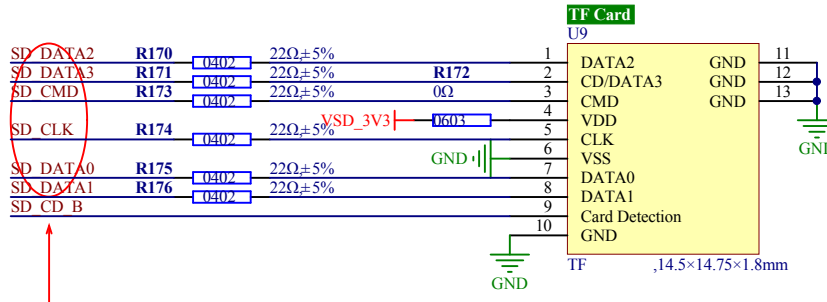
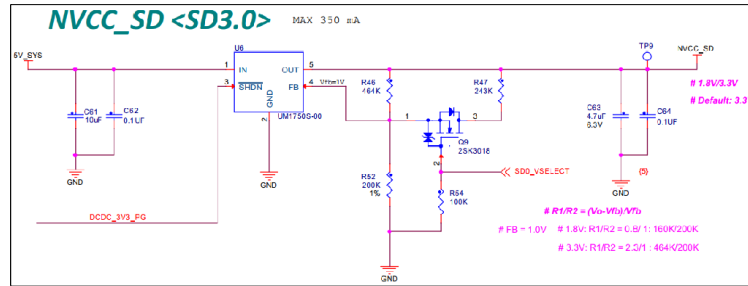
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## 12. <图纸名称>



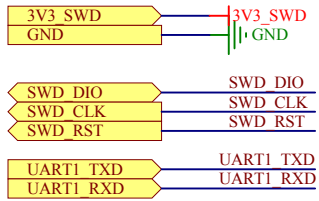
### (12-1) SD CARD(3V3)

要点1: EasyARM-RT1052为简化电源设计, SD卡默认采用3.3V供电  
如需增加兼容1.8V的SD卡, 则电源需分开设计, 可参考原厂EVK评估板, 电路如下图所示

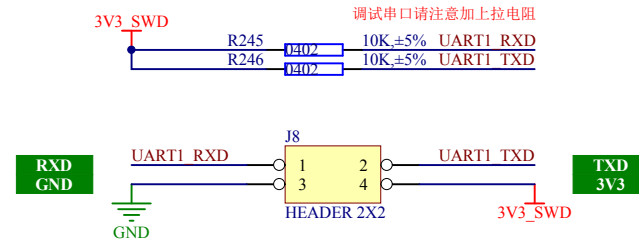
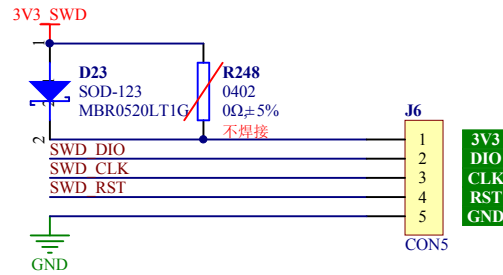


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# 13. SWD & UART1

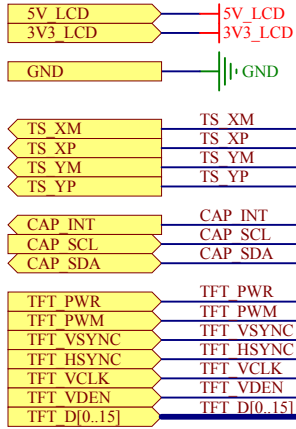


## (13-1) SWD & UART1

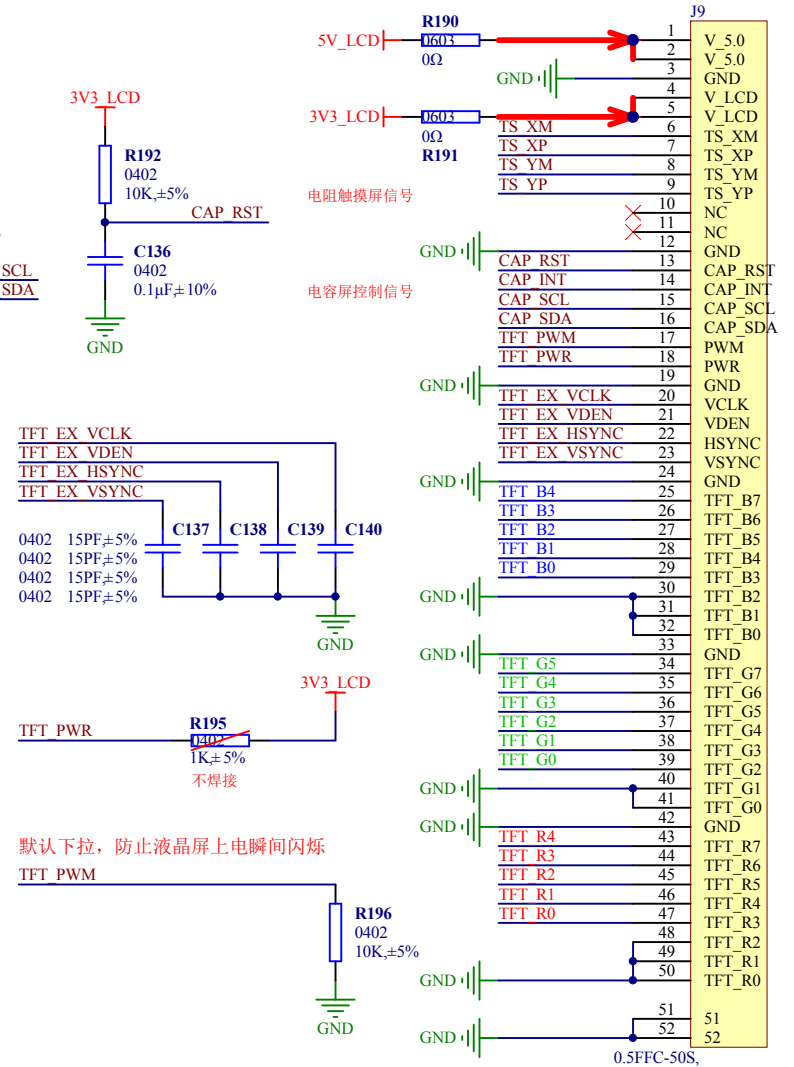
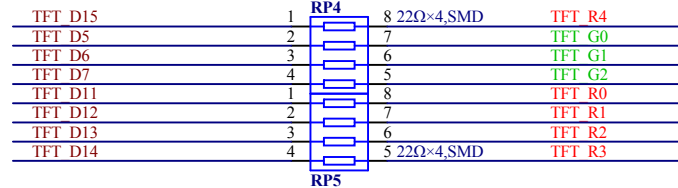
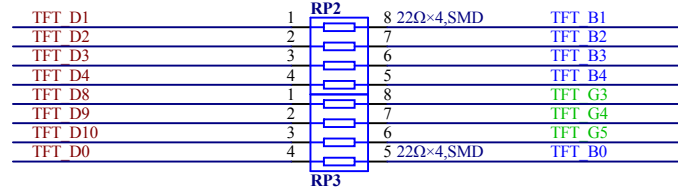
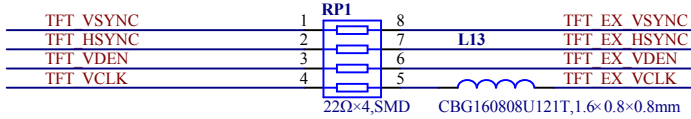
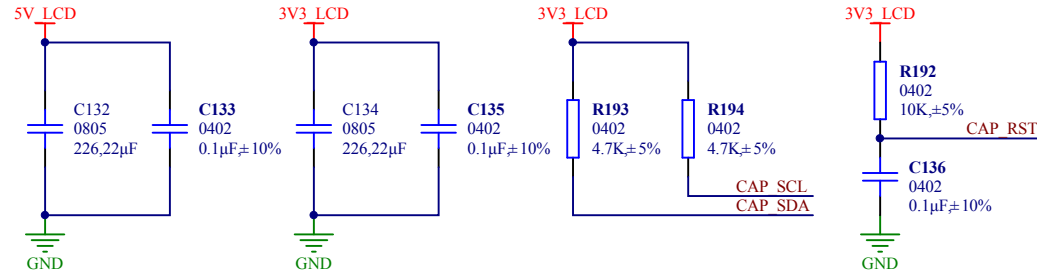


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# 14. LCD\_RGB565

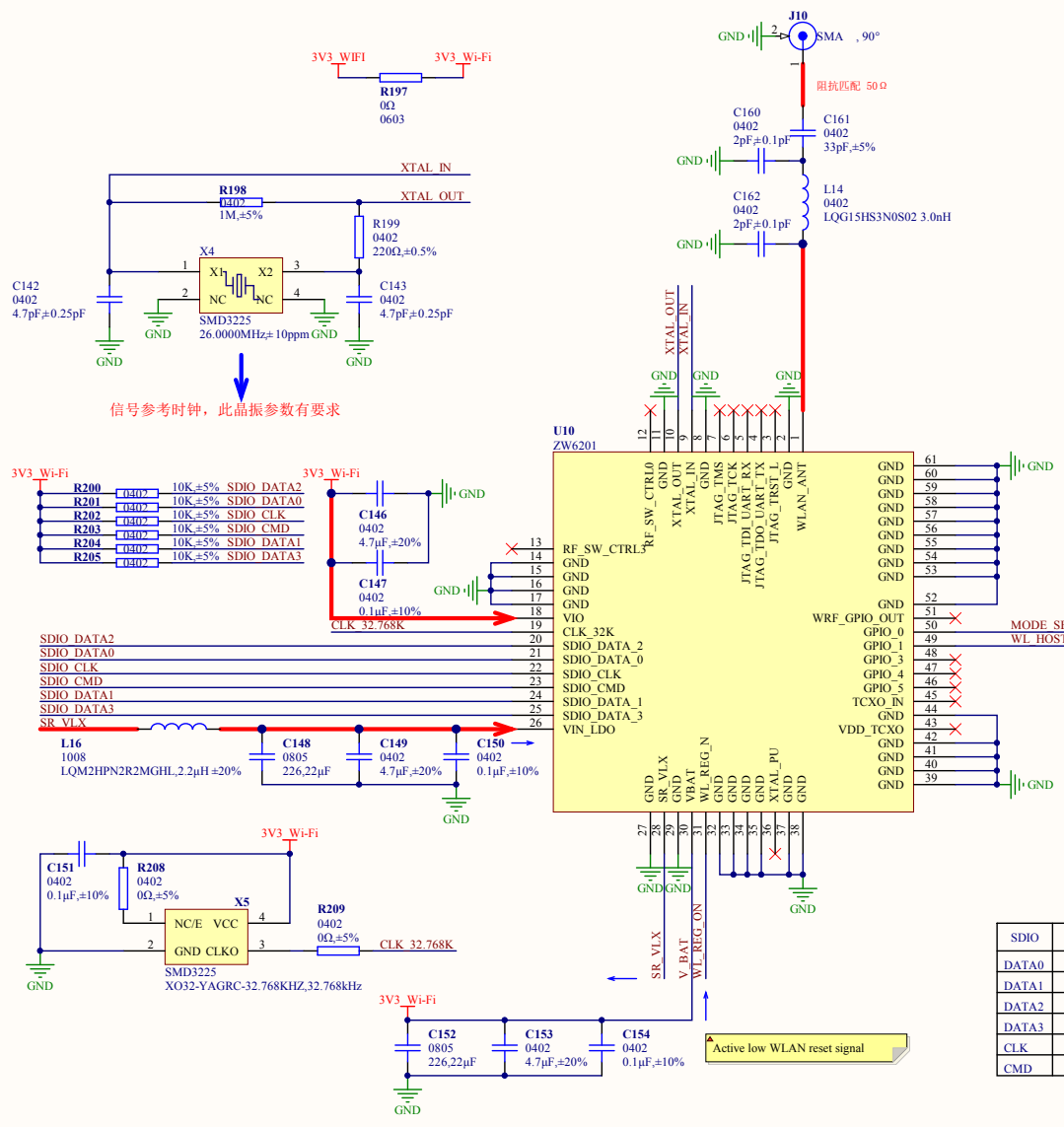
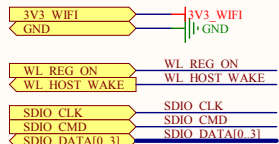


## (14-1) LCD RGB565



#	修改日期	修改内容
1		
2		
3		

(15-1) Wi-Fi



信号参考时钟，此晶振参数有要求

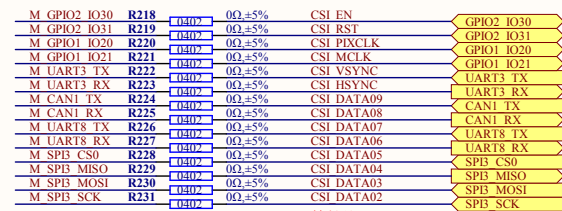
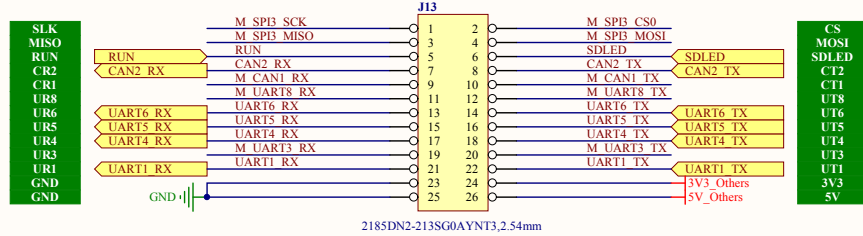
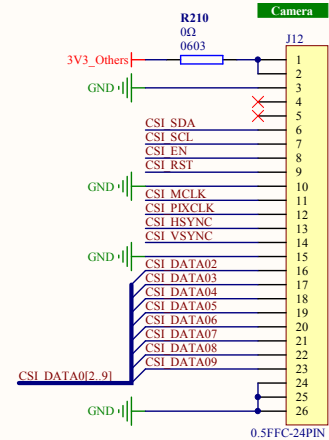
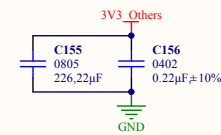
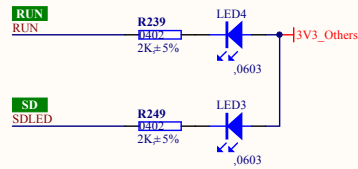
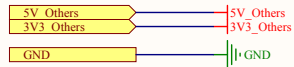
WLAN 接口模式选择  
当MODE\_SEL引脚拉低为SDIO模式，下拉电阻为0  
当MODE\_SEL引脚拉高为SPI模式，上拉电阻10K

Active low WLAN reset signal

SDIO	SPI Mode	
DATA0	DO	DATA Output
DATA1	IRQ	Interrupt
DATA2	NC	Not Used
DATA3	CS	Card Select
CLK	SCLK	Clock
CMD	DI	DATA Input

#	修改日期	修改内容
1		
2		
3		

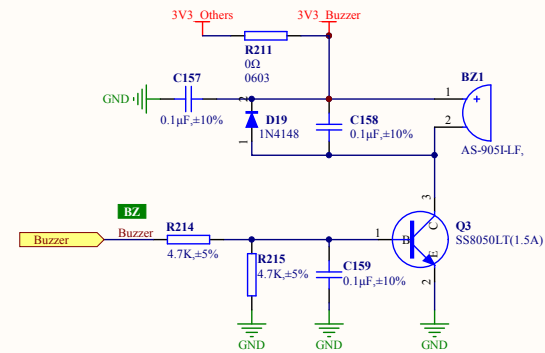
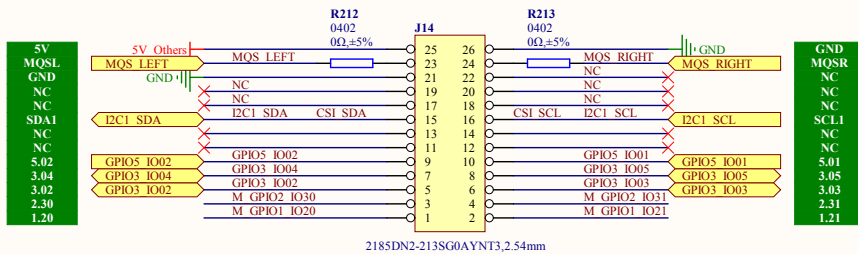
(16-1) Others-1 & CSI



等长处理

1.10.01.0133  
1.11.07.0148

(16-2) Others-2 & Buzzer



#	修改日期	修改内容
1		
2		
3		