i.MX6 SABRE Automotive Base Board

Part number MCIMXABASEV1

Table of Contents

MX6 Quad CPU2 Card

Schematic SCH-27925
Part No. MCIMX6QAICPU2

MX6 DualLite CPU2 Card

Schematic SCH-28605
Part No. MCIMX6DLAICPU2

MX6 SX CPU2 Card

Schematic SCH-28376
Part No. MCIMX6SXAICPU2

MX6 QuadPlus CPU3 Card

Schematic SCH-28615
Part No. MCIMX6QPAICPU3

Automotive Base Board

Schematic SCH-26662
Part No. MCIMXABASEV1

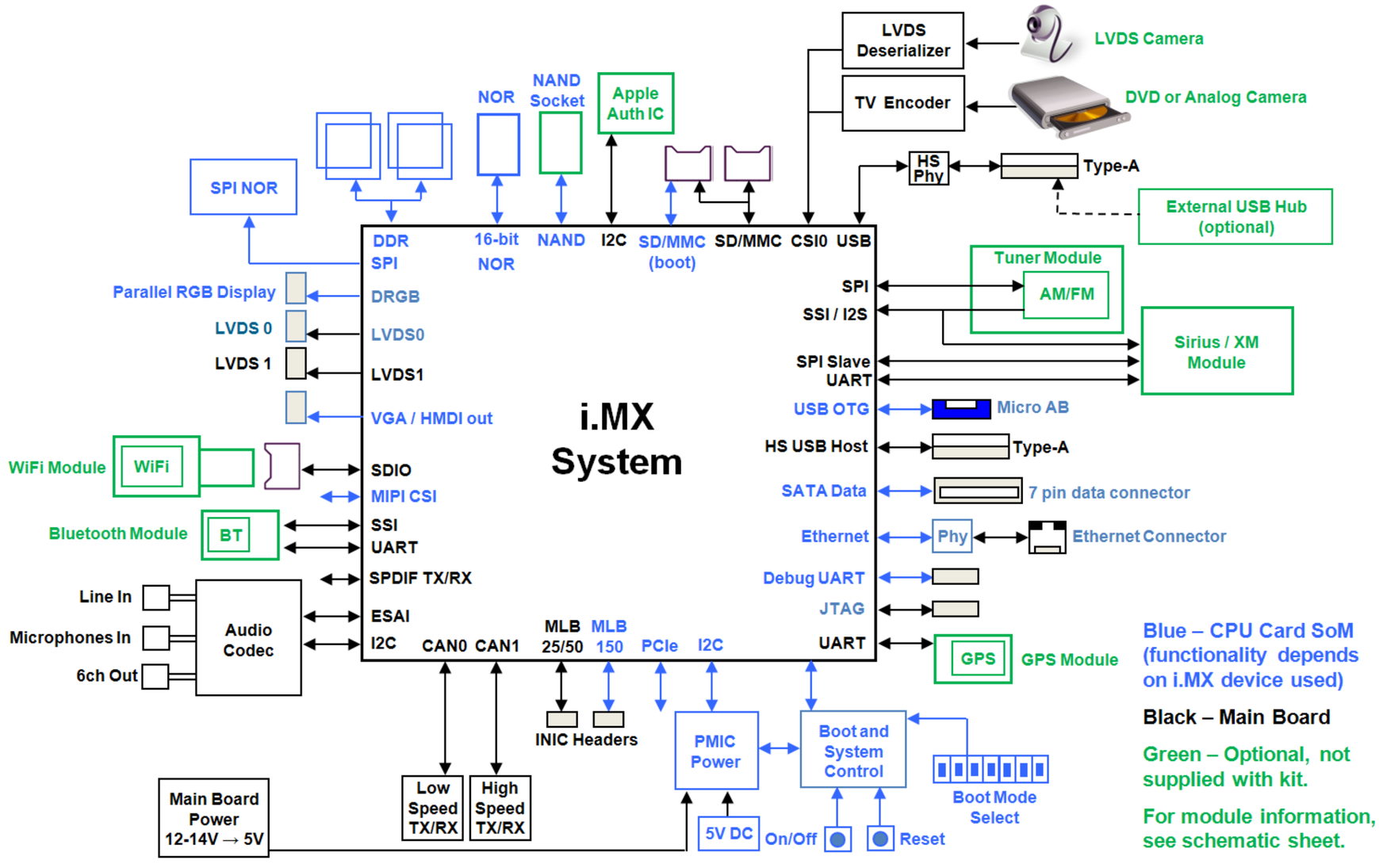
This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass production design. For an added resource, refer to Hardware Development Guide document number IMX6DQ6SDLHDG.

Consumer devices were utilized in this design when lead time for equivalent automotive-grade devices conflicted with production schedules. NXP suggests consulting component suppliers for equivalent automotive-grade device information.

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: PUBI: X

Designer: Ross M et al.	Drawing Title: MX6 Automotive Base Board		
Drawn by: Ross M et al.	Page Title: Cover		
Approved: HW Platform Team	Size C	Document Number SCH-26662 PDF: SPF-26662	Rev E4
	Date: Tuesday, March 01, 2016	Sheet 1 of 15	



ICAP Classification: CP: ___ IUO: PUBI: _X_

Drawing Title: **MX6 Automotive Base Board**

Page Title: **Block Diagram**

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LAYOUT NOTES:

- All testpoint pads should be on TOP.
- Make sure that there is GND plane on adjacent layer under the xtal circuits.
- Add vias to all ICs that have GND pad on the bottom of package (Exposed Pad)
- Some signals require differential routing and are noted on the particular schematic page.
- Route USB diff. pairs on TOP layer only 90 ohm differential, length matched unless otherwise indicated.

FAB NOTES:

- The zero ohm cut trace resistors have a "Short Layer" in layout, this layer MUST be included when generating Gerber files (films) in order to have the two pads of each resistor connected (shorted)

SCHEMATIC NOTES:

- Net names with extended names only apply with MX53 CPU Card usage.

- For example: ESAI_INT(EMI_EB1_GPI2_29) connects to MX53 I/O EMI_EB1 which is configured as GPIO2_29.

- For the MX6 interface, determine the MX6 I/O using these steps:
  1. Search for ESAI_INT on the MX6 CPU schematic Card Edge Fingers sheet.
  2. Note the complete net name; ESAI_INT(SD2_CLK_GPIO1_10) for this example.
  3. The I/O is SD2_CLK configured as GPIO1_10.

ICAP Classification: CP: ___ IUO: PUBI: X

Drawing Title: **MX6 Automotive Base Board**

Page Title: **Notes**

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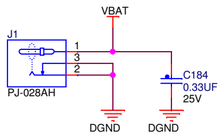
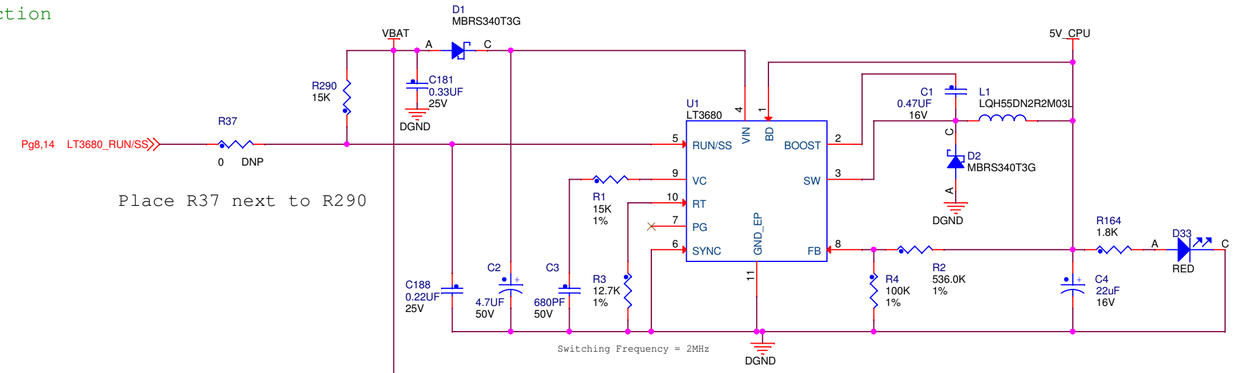
Power Supplies

Power Input 12 Vdc typical

+12V - 5.5A DC supply with integrated protection

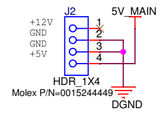


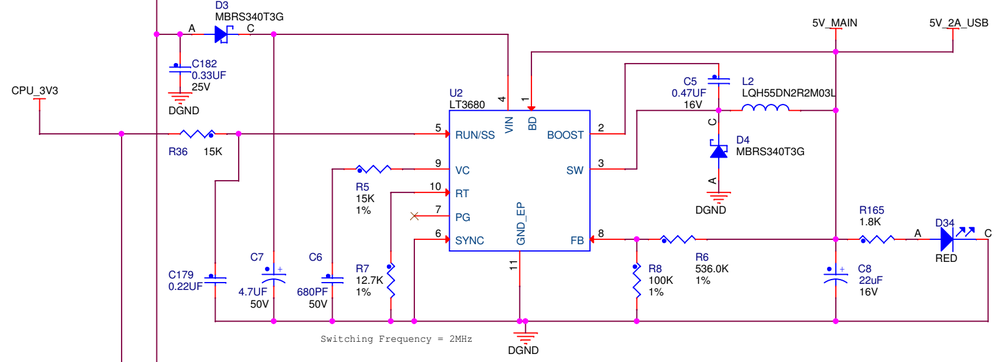


Layout Note:
Net 5V_CPU must tolerate a current of 3.5A.

Layout Note:
Add "5V CPU" to LED silkscreen

Power for SATA HDD via PATA power adapter cable



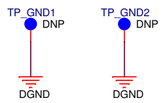


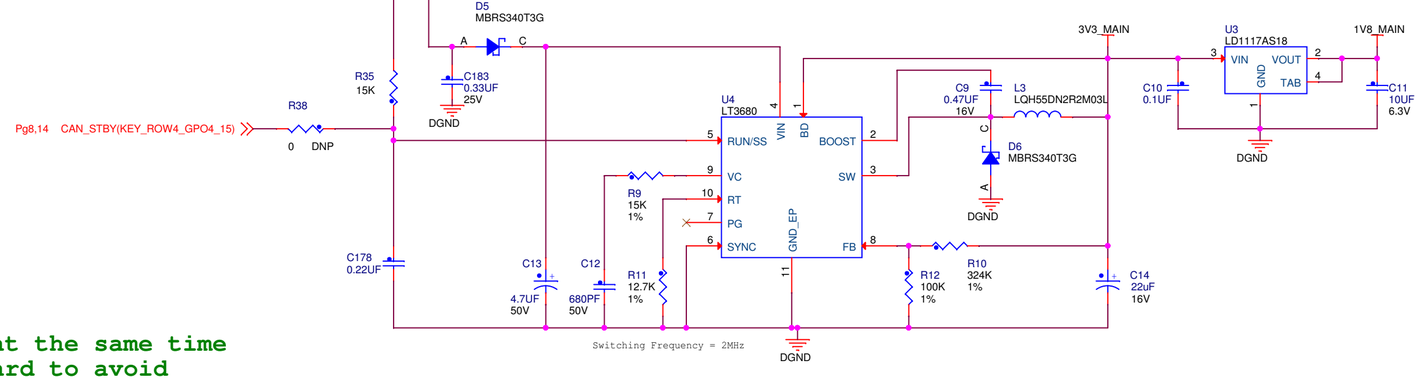
Layout Note:
Net 5V_2A_USB must tolerate a current of 2A.

Layout Note:
Net 5V_MAIN must tolerate a current of 1.5A.

Layout Note:
Add "5V MAIN" to LED silkscreen

Ground Points





Layout Note:
Net 3V3_MAIN must tolerate a current of 2A.

Layout Note:
Net 1V8_MAIN must tolerate a current of 0.5A.

Notes:

1. CAN_STBY forces 3V3_MAIN off at the same time as the 3.3 V supply on the CPU Card to avoid supply backfeed/leakage issues.

2. To enable CAN wake up, fit 0 ohms to R37 and R38, remove R290. Users could consider use of values higher than 0 ohms for soft start.

   Reverse to return to default, always-powered mode.

3. Although the 3 switchers can support up to 36 volt input, the external component selection has been set up on the assumption of a 12 to 14 volt nominal input.

ICAP Classification:	CP: ___	IUO:	PUBI: X
Drawing Title:	MX6 Automotive Base Board		
Page Title:	POWER - 12V to 5V, 3V3, 1V8		
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ESAI CODEC

5 V
VA_CS42888
RBIAS
R17
2.2K
MICIN_1
C17
0.1uF
25V
U6
BIAS
MICBIAS
MICIN
CT
CG
SHDN
VDD
A/R
TH
GAIN
MICOUT
NC_4
NC_11
GND
EP_PAD
MAX9814ETD+T
C189
0.47UF
16V
CCT
C21
0.1uF
25V
C191
2.2UF
AGND
C15
1.0UF
10V
RGPU
R13
0
DNP
R14
150K
RTHU
R15
0
RARPU
RARPD
R21
0
DNP
R23
100K
RTHD
RGPD
R26
0
C29
0.1uF
25V
AIN_3P
C31
4.7uF
10V
AIN_3N

Adjust RBIAS for electrect microphone sensitivity. 2.2kOhm is a typical value.

Adjust CCT for attack time (T=2400xCCT).

AGC response time ratio:
RARPD => 1:500
RARPU => 1:2000
NC => 1:4000

GAIN adjustment:
RGPU => Gain of 40dB
RGPD => Gain of 50dB
NC => Gain of 60dB

AGC threshold controlled by RTHU and RTHD.

5 V
VA_CS42888
RBIAS
R18
2.2K
MICIN_2
C18
0.1uF
25V
U5
MAX9814ETD+T
C190
0.47UF
16V
CCT
C24
0.1uF
25V
C192
2.2UF
AGND
C16
1.0UF
10V
RGPU
R19
0
DNP
R20
150K
RTHU
R16
0
RARPU
RARPD
R22
0
DNP
R24
100K
RTHD
RGPD
R27
0
C30
0.1uF
25V
AIN_4P
C32
4.7uF
10V
AIN_4N

Headers to solder or connect electret microphones.

J26-1
AIN3
AIN4
6XRCA
MICIN_1
MICIN_2
Molex
53261-0219
J6
DNP
J5
DNP
AGND

J26 and J27 are 6 x RCA vertical connector from Connect-Tech P/N=CTP6-612.

AIN1
AIN2
J26-2
6XRCA
R174
2.49K
R175
0
C45
10UF
16V
AIN_1P
C46
2200PF
R176
2.49K
C54
4.7UF
10V
AIN_1N
R181
2.49K
R182
0
C56
10UF
16V
AIN_2P
C62
2200PF
R183
2.49K
C68
4.7UF
10V
AIN_2N
AGND

3V3_MAIN
C39
10UF
6.3V
C40
0.1UF
DGND
TSTN1
TSTN2
TSTN3
TSTN4
TSTO
VLS
VLC
VLS
VLC
AUX_SDIN
AUX_SCLK
AUX_LRCK
TP8
TP9
TP11
SH124
MCLK
ADC_SCLK
ADC_LRCK
ADC_SDOUT1
ADC_SDOUT2
DAC_SCLK
DAC_LRCK
DAC_SDIN1
DAC_SDIN2
DAC_SDIN3
DAC_SDIN4
INT
RST
SCL/CCLK
SDA/CDOUT
AD0/CS
AD1/CDIN
Pg14 SSI_EXT1_CLK
Pg14 ESAI_SCKR
Pg14 ESAI_FSR
Pg14 ESAI_RX0
Pg14 ESAI_TX4_RX1
Pg14 ESAI_SCKT
Pg14 ESAI_FST
Pg14 ESAI_TX0
Pg14 ESAI_TX1
Pg14 ESAI_TX2_RX3
Pg14 ESAI_TX3_RX2
Pg14 ESAI_INT(EMI_EB1_GPI2_29)
Pg14 ESAI_RST_B
Pg7,10,11,12,13,14 I2C2-SCL
Pg7,10,11,12,13,14 I2C2-SDA
Pg7,10,11,12,13,14 I2C3-SCL
Pg7,10,11,12,13,14 I2C3-SDA
R179
10.0K
R180
10.0K
SH125
SH126
R184 DNP
R185 DNP
C69
10UF
6.3V
C70
0.1UF
R186
0
R187
0
CS42888
I2C ADDRESS: 1001 000*
* 0 for write and 1 for read.

U7
AIN_1P
AIN_1N
AIN_2P
AIN_2N
AIN_3P
AIN_3N
AIN_4P
AIN_4N
AIN1+
AIN1-
AIN2+
AIN2-
AIN3+
AIN3-
AIN4+
AIN4-
AOUT1+
AOUT1-
AOUT2+
AOUT2-
AOUT3+
AOUT3-
AOUT4+
AOUT4-
AOUT5+
AOUT5-
AOUT6+
AOUT6-
AOUT7+
AOUT7-
AOUT8+
AOUT8-
MUTEC
VQ
FILT+_ADC
FILT+_DAC
VA1
VA2
VD1
VD2
DGND1
DGND2
DGND3
AGND1
AGND2
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP10
TP12
C49
100UF
10V
C50
0.1UF
C51
4.7UF
25V
C52
0.1UF
C47
100UF
10V
C48
0.1UF
C57
0.01uF
C58
0.01uF
C59
0.1UF
C60
0.1UF
C193
10UF
10V
L4
120OHM
5V_MAIN
C63
0.01uF
C64
0.01uF
C65
0.1UF
C66
0.1UF
C194
10UF
10V
L5
120OHM
3V3_MAIN
AGND DGND
Connect DGND and AGND near CODEC
CS42888 only provides typical current consumption figures -
VA = 5 Volts, Itype = 80 mA
VLS,VLC,VD = 3.3 Volts, Itype = 61 mA

AOUT_1P
AOUT_2P
AOUT_3P
AOUT_4P
AOUT_5P
AOUT_6P
AOUT_7P
AOUT_8P
C19
C27
C33
C35
C37
C41
C43
C53
3.3uF
16 V
R25
R29
R31
R33
R168
R170
R172
R177
470
R28
R30
R32
R34
R169
R171
R173
R178
10.0K
C20
C28
C34
C36
C38
C42
C44
C55
2200PF
J26-3
J27-1
J27-2
J27-3
6XRCA
AOUT1
AOUT2
AOUT3
AOUT4
AOUT5
AOUT6
AOUT7
AOUT8
AGND
SH245
DGND

Left & right channels are swapped.
CODEC Odd channel numbers should be Left (white jacks) and Even channels should be Right (red jacks).

All jacks incorrect except J26-1 (AIN3 & AIN4).

SPDIF IN

Pg14 AUDIO_SPDIF_IN
R188
4.7K
3V3_MAIN
U19B
MC74HCU04
U19A
MC74HCU04
VCC
GND
R189
1.0K
C72
1UF
10V
T1
TTWB1010L
R190
110
C71
0.01uF
DGND
J29
RCA 2 CONN
Kycon KLPX-0848-2-B
J29 is a vertical RCA connector.
SPDIF IN (analogue)
U19C
U19D
U19E
U19F
MC74HCU04

ICAP Classification:	CP: ___	IUO:	PUBI: _X_
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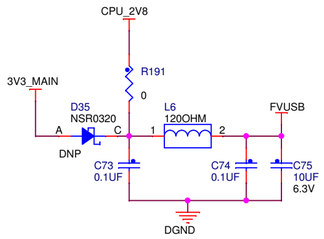
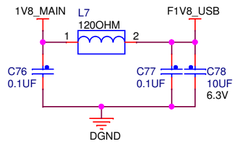
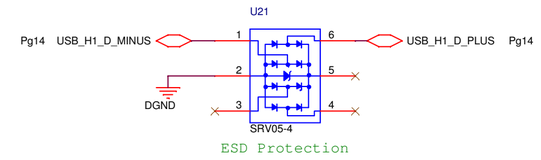
USB HOST ports







USB_H1_VBUS_IN formerly required for obsolete MX53 CPU Card.
MX6 CPU Card has on-board VBUS power source.

Host 2 port formerly used with obsolete MX53 CPU Card.

ICAP Classification: CP: ___ IUO: PUBI: X

Drawing Title: **MX6 Automotive Base Board**

Page Title: **USB**

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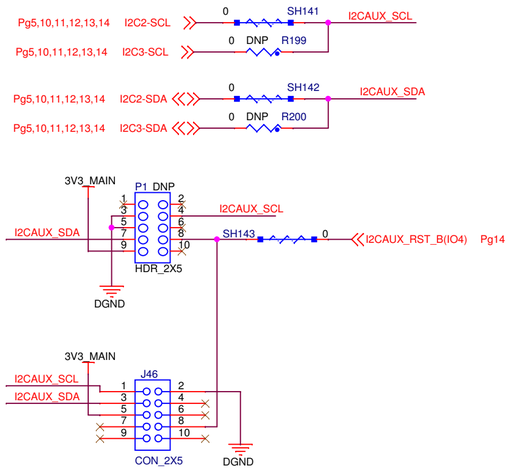
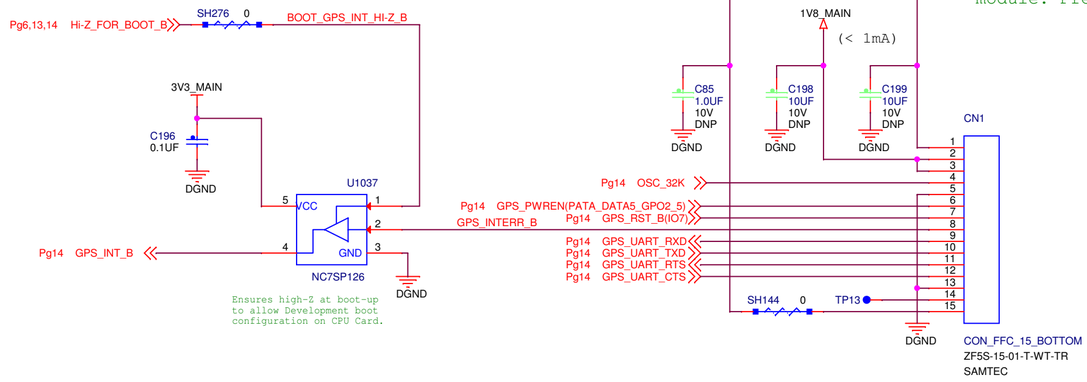
I2C Module Connector



P1 accommodates Freescale v2.0B coprocessor module.
Vtyp = 3.3 V, Imax = 7.5 mA

J46 accommodates I2C module.

GPS



CN1 is intended to provide a set of signals to interface a GPS module. The connector is not intended for a specific module. Freescale does not provide a GPS module.

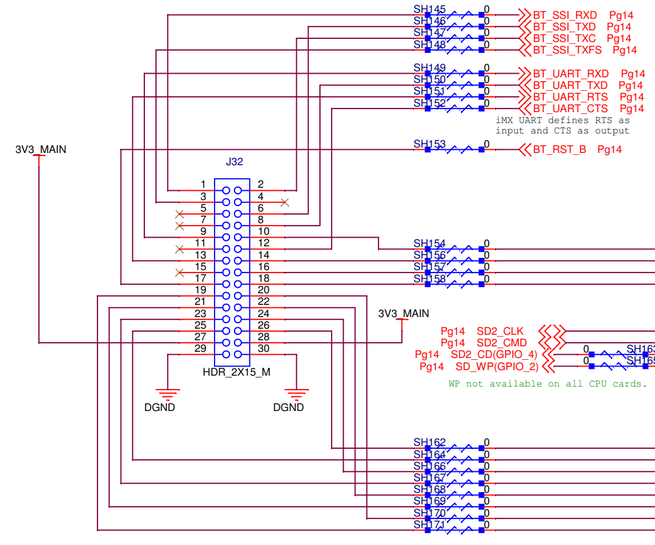
From CPU side		From GPS side
GPS_UART_TXD : Output	→	GPS_RXD : Input
GPS_UART_RXD : Input	←	GPS_TXD : Output
GPS_UART_RTS : Input	←	GPS_RTS : Output
GPS_UART_CTS : Output	→	GPS_CTS : Input

Mates with Samtec FJH flat flex cable
(0.5 mm pitch)

Bluetooth

Infineon PBA31308 Interface

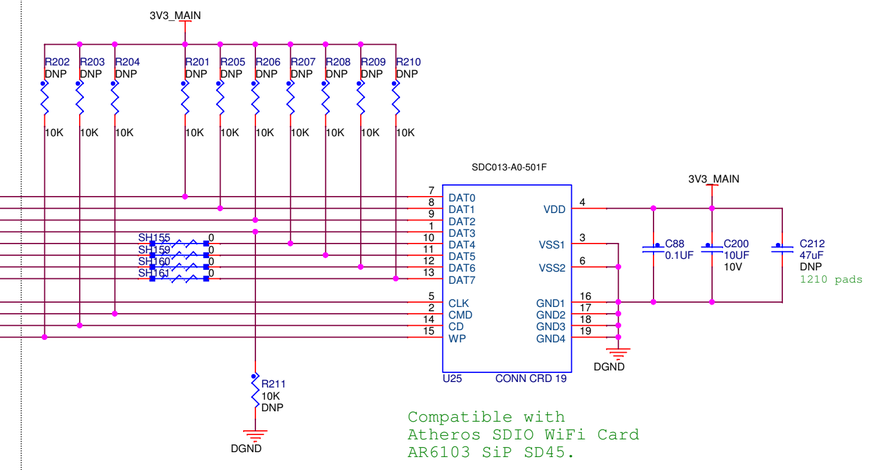
1 - PCMOUT
2 - PCMCLK
3 - PCMFR
4 - WUP-HOST
5 - WUP-BT
6 - PCMIN (wire-add)
7 -
8 - UARTRXD
9 - UARTTXD
10 -
11 -
12 - UARTCTS
13 - UARTRTS (wire-add)
14 -
15 -
16 -
17 - RESET
18 -
19 -
20 -
21 -
22 - SDA (test only)
23 -
24 - SCL (test only)
25 -
26 -
27 - 3.3 Volts
28 -
29 - GND
30 - GND



J32 compatible with Freescale board part number FD-B-TOOTH-DC

Internal number: 27421

WiFi & BT SD slot



Compatible with
Atheros SDIO WiFi Card
AR6103 SiP SD45.

Software note:
WP and CD must have MX6 on-chip
47k or 100k pull-up enabled.
47k tolerates more leakage.

ICAP Classification: CP: ___ IUO: PUBI: _X_

Drawing Title:
MX6 Automotive Base Board

Page Title:
BT, GPS, iPOD, SD Interface

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CAN

Local CAN Wake-Up

Consult NXP applications note AN00094 Figure 24.
Voltage hold capacitor is on CPU Card rev C schematic PMIC sheet.

Local CAN wake-up control

SW1
SKRPABE010
DGND

Remote switch CAN wake-up control

J33
DNP
HDR 1X2 TH
DGND

5V_MAIN

R234 0

R234
Installed - TJA1041A usage
Removed - MC33902 usage

i.MX GPIO CAN wake-up control

Pg14 MX_CAN_WAKE_PULSE_B

R212 22K R213 10K

VBAT

C D36 MURA160T3G A

Voltage and current requirements per interface -
Vbat = 5.5 to 27 Volts, Imax = 6 mA
VIO = 3.3 Volts, Imax = 1 mA

C90 56PF 50V DGND

C201 0.22UF 25V DGND

C203 2.2UF DGND

C94 2.2uF 16V DGND

3V3_MAIN

C93 0.1uF 16V DGND

TYCO ELECTRONICS P/N=5207826-4

J34
DB9

M2 M1

SH172 0 SH177 0

R216 30

R218 30

C96 56PF 50V DGND

C95 1000PF 50V DNP DGND

C97 56PF 50V DGND

U26
TJA1041AT

Vdd Vsup
WAKE VIO
INH STBY EN
CANH SPLIT CANL NERR TXD RXD
GND

SH173 0 R319 0 R217 DNR 0

R214 10K R215 10K

Standby is asserted with low voltage level.

SH174 0 CAN_STBY(KEY_ROW4_GPO4_15) Pg4,14
SH176 0 CAN_EN(PATA_DA_0_GPO7_6) Pg14
SH178 0 CAN1_NERR_B Pg14
SH179 0 CAN1_TXD Pg14
SH180 0 CAN1_RXD Pg14

Secondary CAN port with MX6 CPU Card.
Requires software to control signal steering circuit.

R250
Installed - TJA1041A usage
Removed - MC33902 usage

R250 0

C202 0.22UF 25V DGND

C204 2.2UF DGND

3V3_MAIN

C101 2.2uF 16V DGND

C100 0.1uF 16V DGND

R219 10K R221 10K

U27
TJA1041AT

SH183 0 R220 DNR 0

SH184 0 SH185 0

SH186 0 CAN2_NERR_B Pg14
SH187 0 CAN2_TXD Pg14
SH188 0 CAN2_RXD Pg14

Primary CAN port with MX6 CPU Card.

SH181 0 SH182 0

J35
HDR 2X5

1-5
2-9
3-4
4-8
5-3
6-7
7-2
8-6
9-1
10-

R222 30

R224 30

R223 DNR 0

C103 56PF 50V DGND

C102 1000PF DNP 50V DGND

C104 56PF 50V DGND

LT3680_RUN/SS Pg4,14

R225 150K

The 30-ohm termination resistors are appropriate
for point-to-point testing. In an actual system,
60-ohm termination is appropriate.

Depending on the amount of available GPIO, the CAN interfaces require 6 GPIO to allow two independent networks. However, with 4 GPIO the STBY and EN signals can be common, with the restriction being that both interfaces are always in the same state.

Because CAN2 is the primary CAN port when the MX6 CPU Card is utilized, users could consider removing R319 and installing R220.

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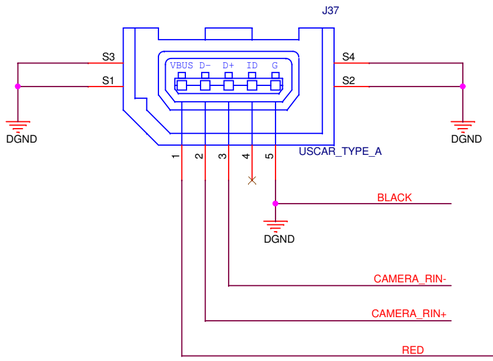
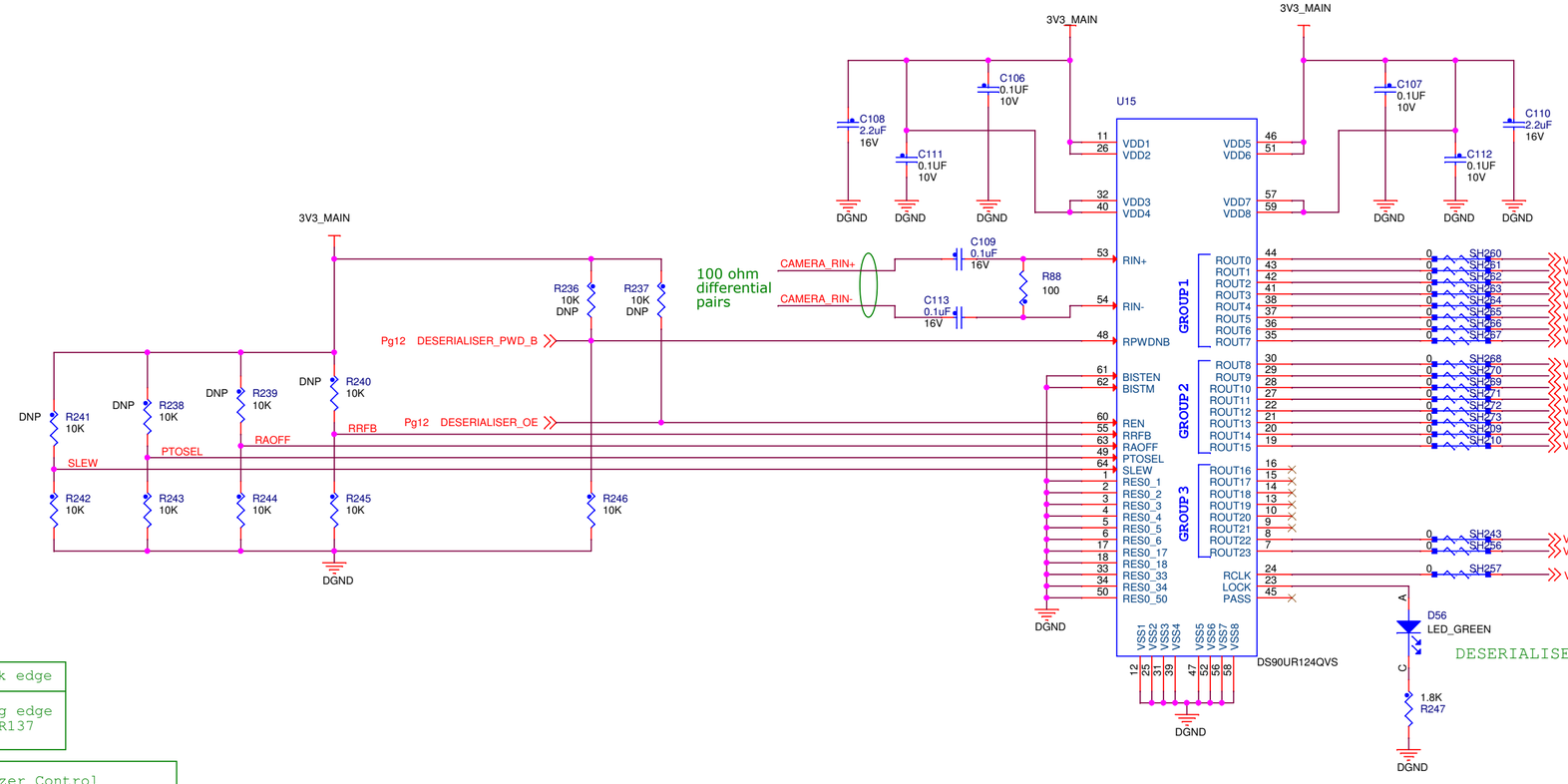
Deserialiser for Rear Camera

NOT FOR USB FUNCTION
Add a note on the silkscreen to avoid confusion with USB.



CAUTION
JP1 of National Serializer
eval board must be removed if that
board is supplied with 3V3 already.



RRFB - Receiver clock edge	
Rising edge Place R138	Falling edge Place R137

RAOFF - Randomizer Control	
DS90C241 random mode Place R135	New random mode Place R134

PTOSEL - Progressive Turn On	
Grouped mode Place R133	Spread mode Place R132

SLEW - Slew Rate Control	
Low drive 2mA Place R130	High drive 4mA Place R131

ICAP Classification: CP: ___ IUO: PUBI: X_

Drawing Title: **MX6 Automotive Base Board**

Page Title: **Camera Deserialiser**

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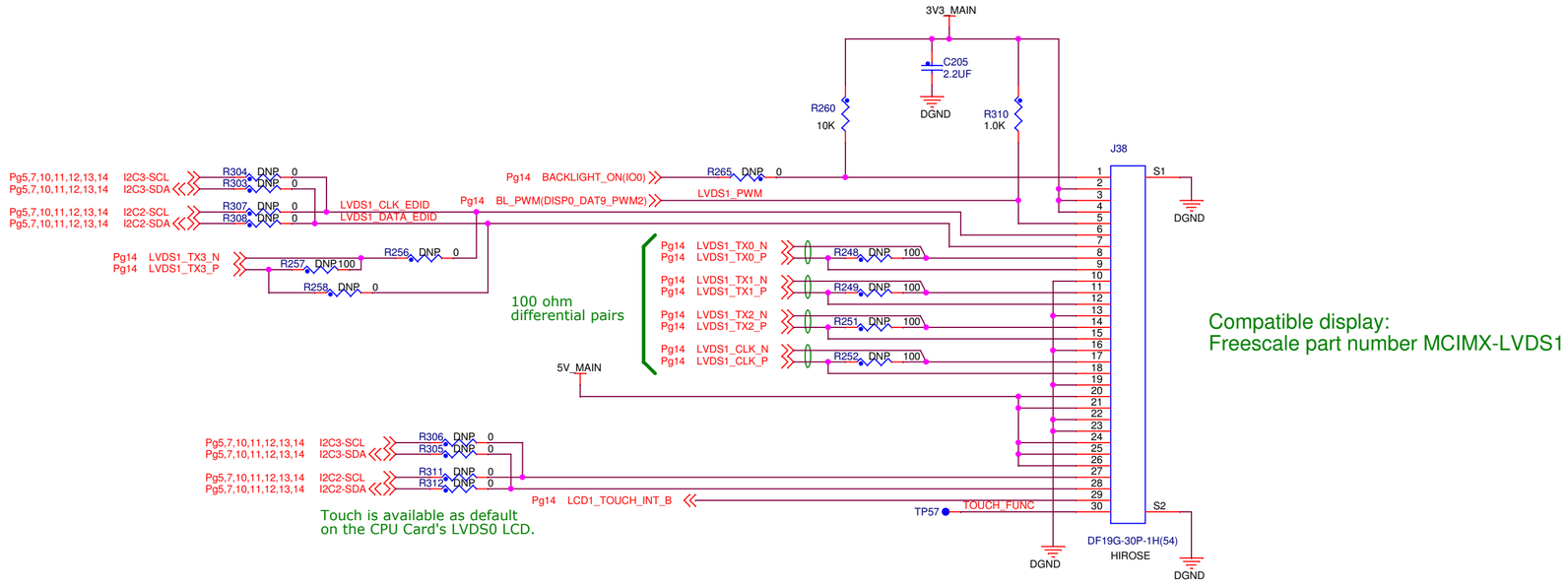
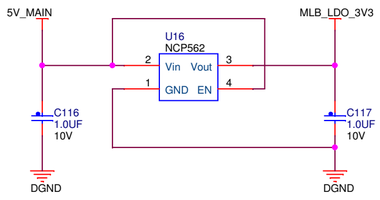
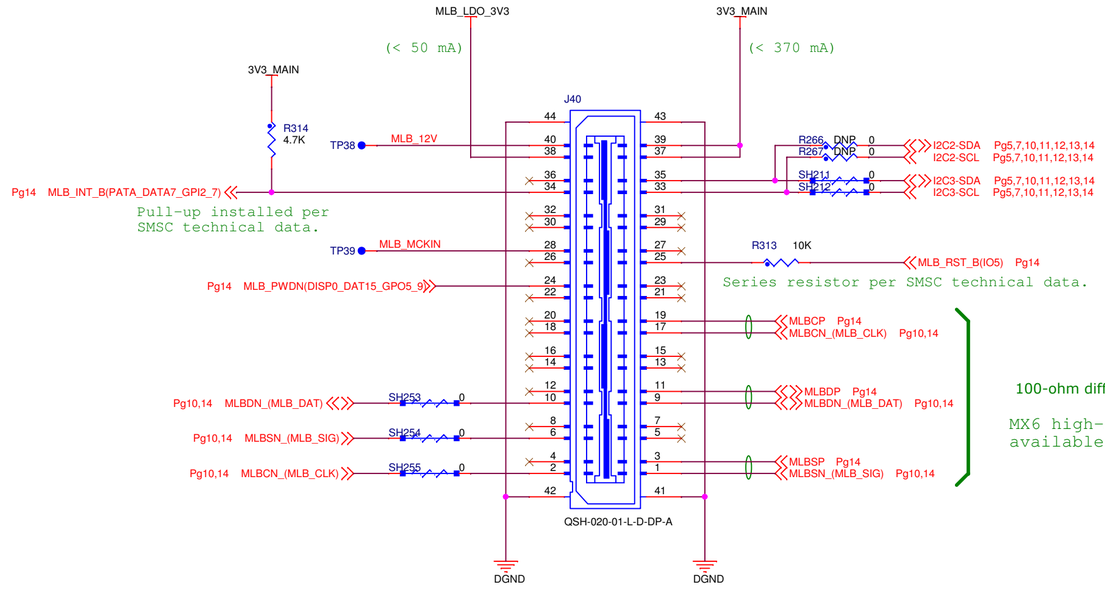
LVDS Display with Backlight Connector



Compatible display:
Freescale part number MCIMX-LVDS1

MLB Connector





I2C ADDRESS = (0x40 | R/W)

100-ohm differential pairs

MX6 high-speed signals only
available on CPU Card.

Compatible with SMSC MOST cards.

ICAP Classification: CP: ___ IUO: PUBI: X

Drawing Title: **MX6 Automotive Base Board**

Page Title: **LVDS1, MLB Interfaces**

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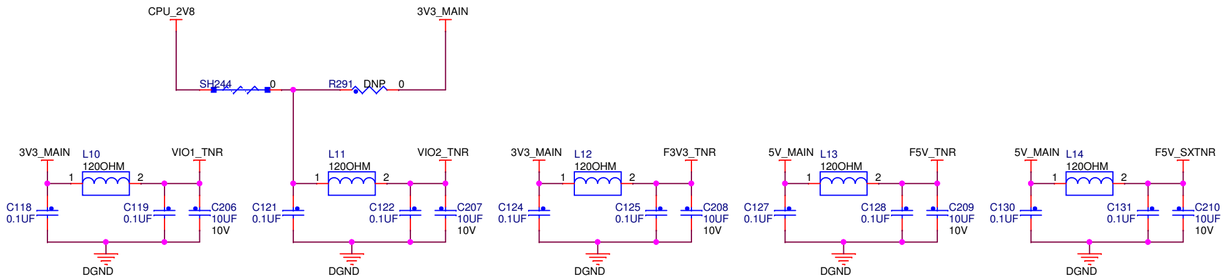
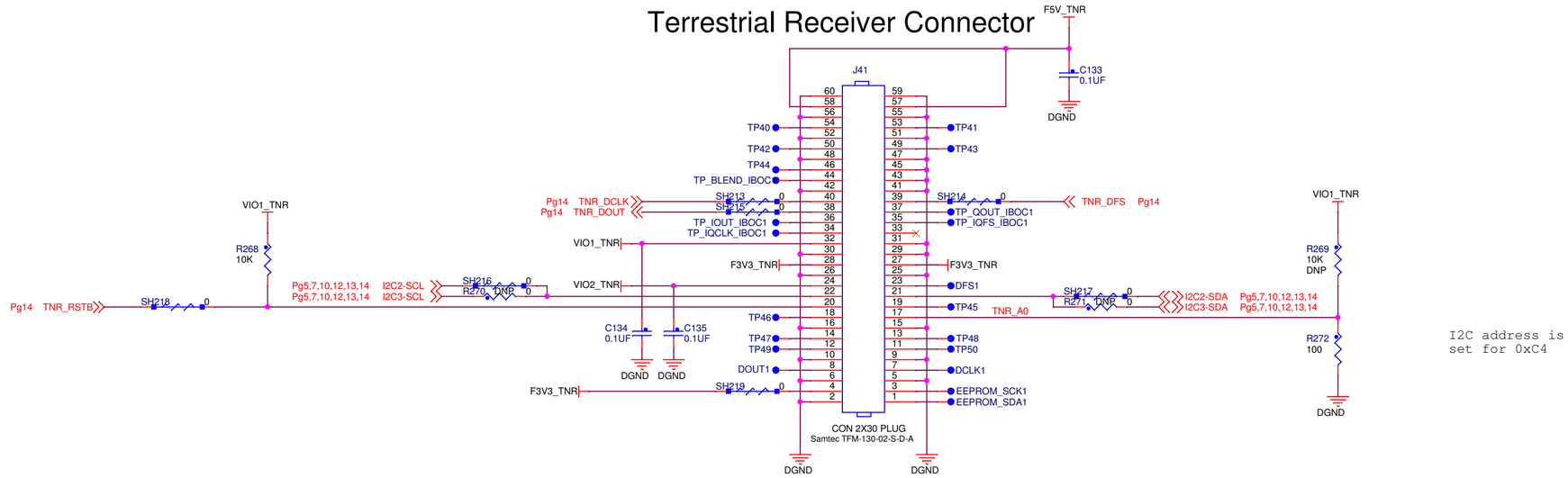
power requirements
VA - 5V @ 150ma (typ)
VD - 3.3V @ 50mA (typ)
VIO1 - 3.3V @ 5mA (typ)
VIO2 - 3.3V @ 2mA (typ)



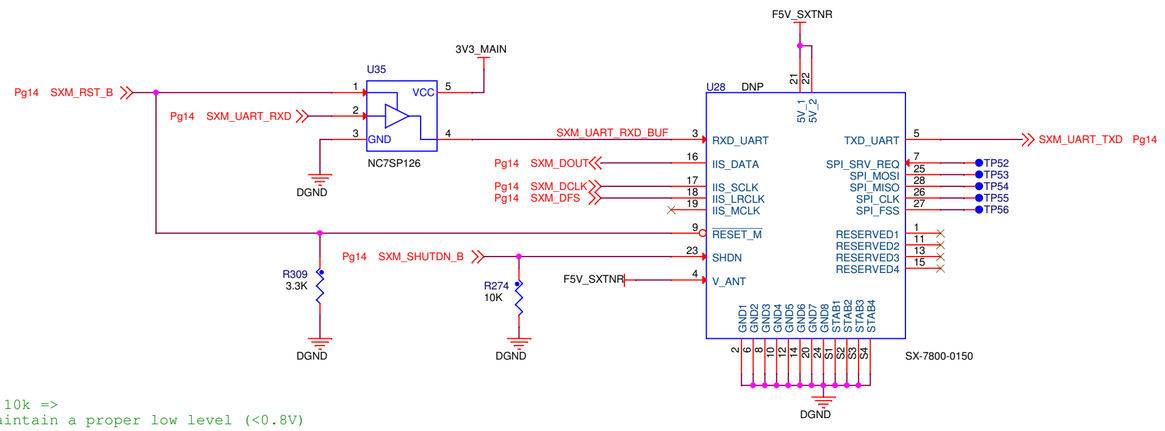
Terrestrial Receiver Connector



I2C address is set for 0xC4

Compatible with Silicon Labs Si475x/6x-EVB daughter cards.
HD is not accommodated due to the second I2S channel requirement.

Satellite Receiver



RESET_M is internally pulled-up with 10k =>
Strong pull-down R309 required to maintain a proper low level (<0.8V) until out of reset. SXM_RST_B floating at power-up.

R274 maintains a proper low level until out of shutdown.

U35 isolates SXM_UART_RXD input when in reset or in shutdown.
Indeed, the SXM has to be in reset to be allowed to enter shutdown.

ICAP Classification: CP: ___ IUO: PUBI: X

Drawing Title: **MX6 Automotive Base Board**

Page Title: **Tuner Interface**

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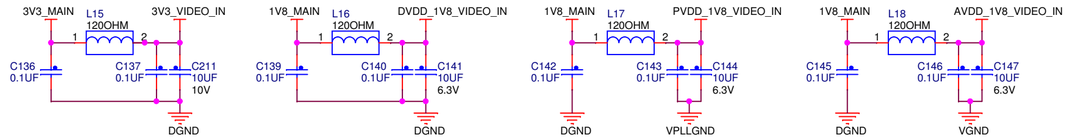
Video In ADC

Power requirements

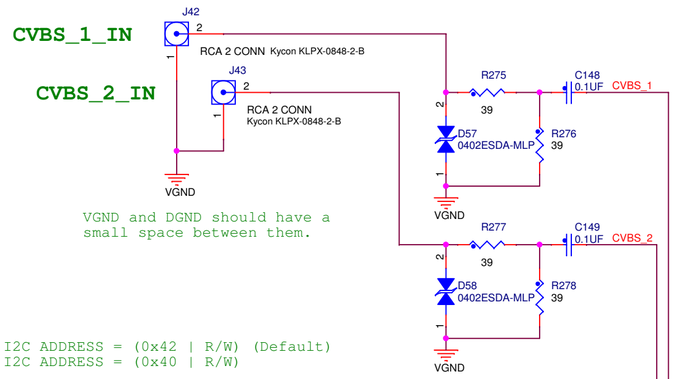
3V3 @ 5mA (max)
1V8 @ 143mA (max)



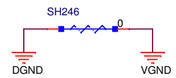
Layout Note :- VPLLGND and VGND need a separate return path to DGND near the power supply and separate from each other.

J42 and J43 are vertical RCA connectors.

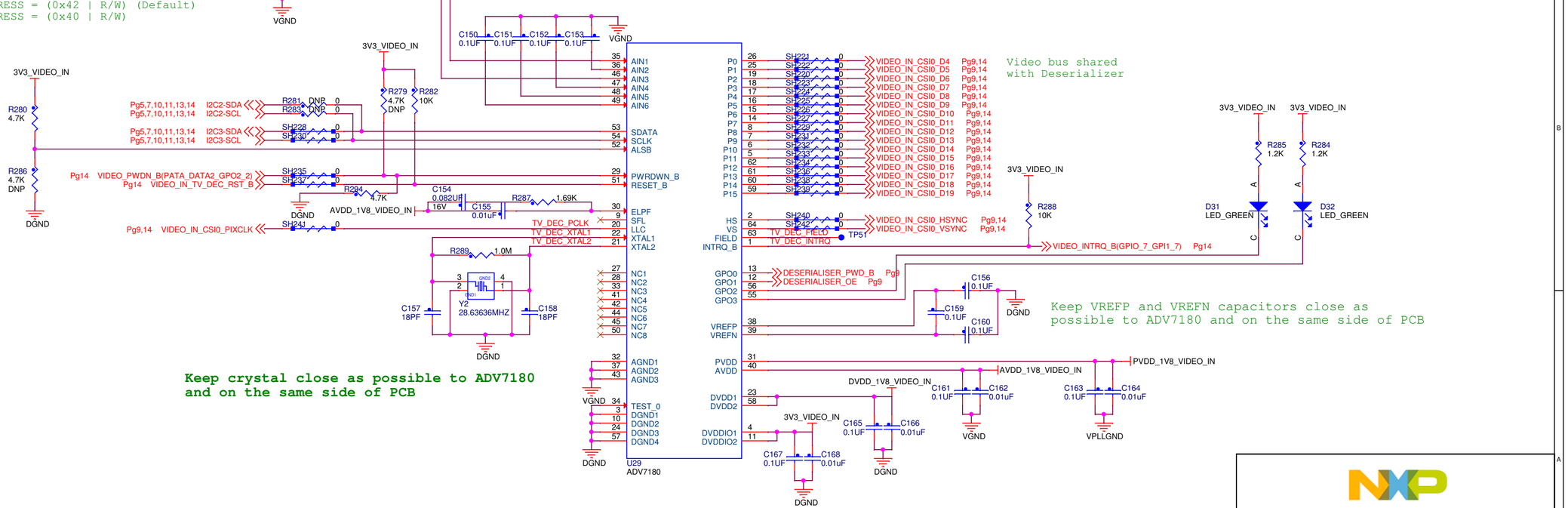
Analog Inputs
75-ohm impedance



VGND and DGND should have a small space between them.



ALSB = '1' : I2C ADDRESS = (0x42 | R/W) (Default)
ALSB = '0' : I2C ADDRESS = (0x40 | R/W)



Keep crystal close as possible to ADV7180 and on the same side of PCB

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Page Title:	Video In A/D Converter		
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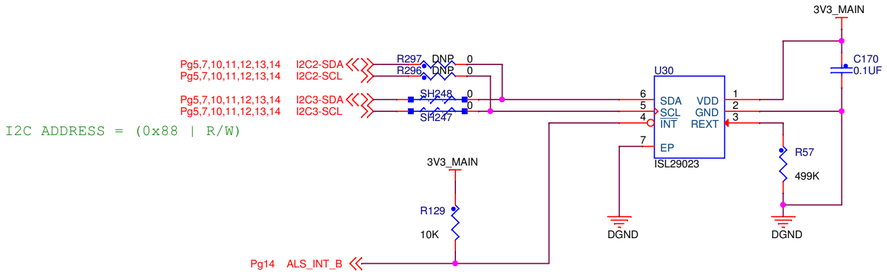
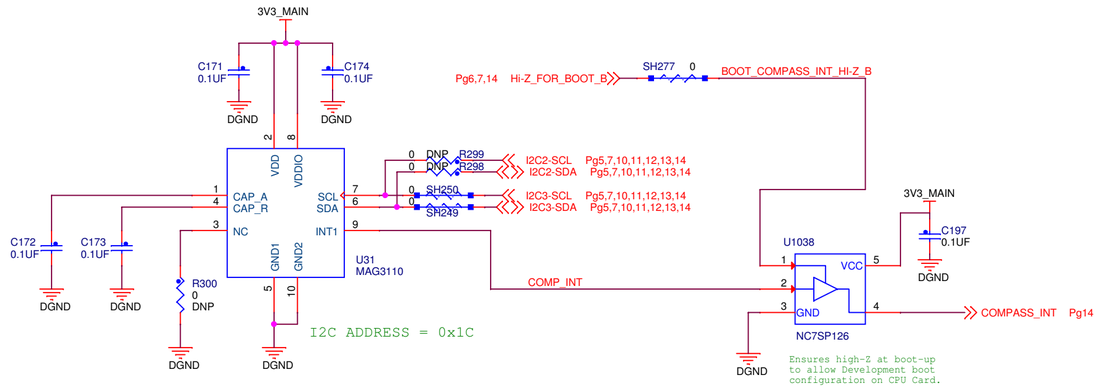
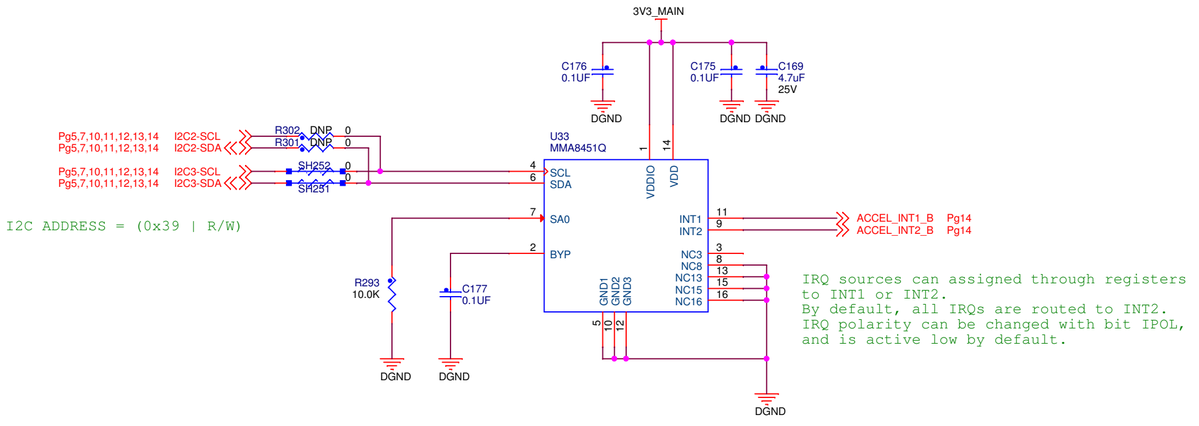
Ambient Light Sensor



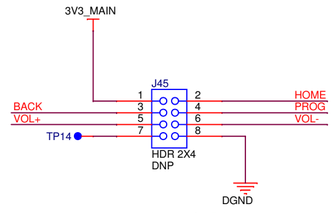
Digital eCompass



3-Axis Accelerometer



Connector for Optional External Keypad



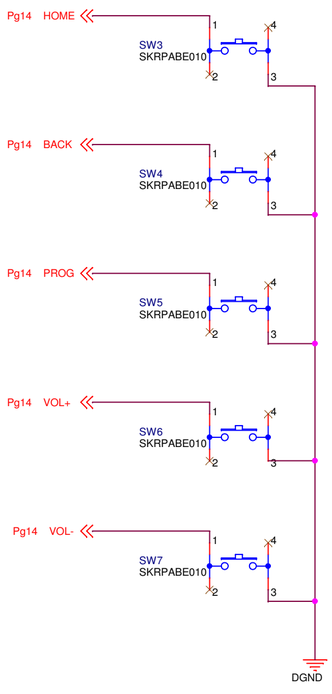
SMT header (2.54mm).

GPIOs used for keypad are muxed with a SPI if the i.MX53 CPU board is used.
i.MX53 mux table is summarized below:

	ALT0	ALT1	ALT2
HOME	DISP0_DAT16	GPIO5_10	eCSPI2_MOSI
BACK	DISP0_DAT17	GPIO5_11	eCSPI2_MISO
PROG	DISP0_DAT18	GPIO5_12	eCSPI2_SS0
VOL+	DISP0_DAT19	GPIO5_13	eCSPI2_CLK

Android Keys

All Android key functions may not be available on certain CPU Cards.



ICAP Classification: CP: ___ IUO: PUBI: X

Drawing Title: **MX6 Automotive Base Board**

Page Title: **Sensors, Keypad**

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Base Board Peripheral Reset

3V3_MAIN, R227 10K, R167 10K, D37 NSR0320, VIDEO_IN_TV_DEC_RST_B Pg12
D41 NSR0320, D38 NSR0320, CPU_MBRD_VIDEO_IN_RST_B
DGND, SW2 SKRPABE010, C105 1.0UF 10V, DGND
R226 10K
CPU_MBRD_ESAI_RST_B
Pg5 ESAI_RST_B
D39 NSR0320, D40 NSR0320
Pg4,8 LT3680_RUN/SS, R315 1.8K, LT3680_RUN/SS_R
R315 current limiter for diode clipping circuit on MX6 CPU Cards.
Pg6 USB_H2_PHY_RST_B(KEY_COL4_GPO4_14) {Pull-up resistor on the USB sheet}
D42 NSR0320, D43 NSR0320, CPU_MBRD_USB_H2_PHY_RST_B (KEY_COL4_GPO4_14)
R229 10K
Pg7 I2CAUX_RST_B(IO4)
D44 NSR0320, D45 NSR0320, CPU_MBRD_I2CAUX_RST_B(IO4)
R230 10K
Pg7 GPS_RST_B(IO7)
D46 NSR0320, D47 NSR0320, CPU_MBRD_GPS_RST_B(IO7)
R231 10K
Pg7 BT_RST_B
D48 NSR0320, D49 NSR0320, CPU_MBRD_BT_RST_B
R232 10K
Pg10 MLB_RST_B(IO5)
D50 NSR0320, D51 NSR0320, CPU_MBRD_MLB_RST_B(IO5)
R233 10K
Pg11 TNR_RSTB
D52 NSR0320, D53 NSR0320, CPU_MBRD_TNR_RST_B

EIM Bus Expansion Connector

3V3_MAIN, J36 DNP, 1V8_MAIN, S1, S2, S3, DGND
EIM_DA6 EIM_DA7 EIM_LBA EIM_OE EIM_RW EIM_D25 EIM_D26 EIM_D27 EIM_D28 EIM_D29 EIM_D30 EIM_D31 EIM_D16 EIM_D17 EIM_D18 EIM_D19 EIM_D20 EIM_D21 EIM_D22
EIM_DA0 EIM_DA1 EIM_DA2 EIM_DA3 EIM_DA4 EIM_DA5 EIM_BCLK EIM_FPGA_INT_B EIM_D23 EIM_D24 EIM_WAIT EIM_FPGA_CS_B
TP20 TP21 TP23 TP22 TP24
TYCO ELECTRONICS 5-104549-8

Expansion connector not used with MX6 CPU Cards.

CPU_2V8, VBAT
From CPU Card 3.3 V with MX6 CPU cards
Not used with MX6 CPU Cards
Internally connected

CPU_MBRD_VIDEO_IN_RST_B
Pg10 LCD1_TOUCH_INT_B, Pg5 ESAI_INT(EMI_EB1_GPI2_29) CPU_MBRD_ESAI_RST_B
Pg4,8 CAN_STBY(KEY_ROW4_GPO4_15)
Pg8 CAN_EN(PATA_DA_0_GPO7_6)
Pg12 VIDEO_INTRQ_B(GPIO_7_GPI1_7)
Pg8 CAN1_NERR_B, Pg8 CAN2_NERR_B
Pg10 MLB_INT_B(PATA_DATA7_GPI2_7)
Pg10 MLB_PWDN(DISP0_DAT15_GPO5_9)
Pg10 LVDS1_CLK_P/N, Pg10 LVDS1_TX0_P/N, Pg10 LVDS1_TX1_P/N, Pg10 LVDS1_TX2_P/N, Pg10 LVDS1_TX3_P/N
Pg8 CAN1_TXD/RXD, Pg8 CAN2_TXD/RXD
Pg10 BACKLIGHT_ON(IO0)
Pg7 BT_UART_TXD/RXD/RTS/CTS, Pg7 GPS_UART_RTS/CTS/RXD/TXD
Pg7 BT_SSI_TXC/TXD/TXFS/RXD
Pg5 ESAI_SCKT/FST/TX5_RX0/TX4_RX1/TX0/TX1/SCKR/FSR/TX2_RX3/TX3_RX2
Pg5 SSI_EXT1_CLK, Pg5 AUDIO_SPDIF_IN
Pg6 USB_H1_D_MINUS/PLUS, USB_H1_VBUS_IN, USB_H1_OC_B, USB_H1_PWR(GPIO_13_GPO4_3), USB_H2_OC_B(GPIO_12_GPI4_2)
CPU_MBRD_USB_H2_PHY_RST_B (KEY_COL4_GPO4_14)
Pg11 SXM_RST_B, Pg11 SXM_SHUTDN_B
Pg6 USB_H2_DAT0/DAT1/DAT2/DAT3/DAT4/DAT5/DAT6/DAT7, Pg6 USB_H2_NXT/DIR/STP/CLK
CPU_3V3, From CPU Card for power sequence control, TP36
J44 MX6Y0 SOCKET, CON SKT 281

5V_CPU
Do not use to avoid supply short when troubleshooting.
CPU_MBRD_I2CAUX_RST_B(IO4), CPU_MBRD_BT_RST_B, CPU_MBRD_GPS_RST_B(IO7), CPU_MBRD_MLB_RST_B(IO5), CPU_MBRD_TNR_RST_B
GPS_PWREN(PATA_DATA5_GPO2_5) Pg7
GPS_INT_B Pg7, OSC_32K Pg7
VIDEO_IN_CSI0_D4/D5/D6/D7/D8/D9/D10/D11/D12/D13/D14/D15/D16/D17/D18/D19/HSYNC/VSYNC Pg9,12
VIDEO_PWDN_B(PATA_DATA2_GPO2_2) Pg12
VIDEO_IN_CSI0_PIXCLK Pg9,12
COMPASS_INT Pg13
SD2_DATA2/DATA1/DATA3/DATA0/CMD/CLK Pg7
SD_WP(GPIO_2) Pg7, SD2_CD(GPIO_4) Pg7
ALS_INT_B Pg13
BL_PWM(DISP0_DAT9_PWM2) Pg10
ACCEL_INT1_B Pg13, ACCEL_INT2_B Pg13
TNR_DCLK Pg11, TNR_DOUT Pg11, TNR_DFS Pg11
EIM_D16/D17/D18/D19/D20/D21/D22/D23/D24/D25/D26/D27/D28/D29/D30/D31/DA0/DA1/DA2/DA3/DA4/DA5/DA6/DA7/LBA/OE/RW/BCLK/WAIT
MLBDP Pg10, MLBDN_(MLB_DAT) Pg10, MLBSP Pg10, MLBSN_(MLB_SIG) Pg10, MLBCP Pg10, MLBCN_(MLB_CLK) Pg10
Differential pairs are not used. Singled-ended used from the CPU card (MLB_DAT, MLB_SIG, MLB_CLK).
HOME Pg13, BACK Pg13, PROG Pg13, VOL+ Pg13, VOL- Pg13
SXM_DOUT Pg11, SXM_DFS Pg11, SXM_DCLK Pg11, SXM_UART_RXD Pg11, SXM_UART_TXD Pg11
TP26
I2C2-SCL Pg5,7,10,11,12,13, I2C2-SDA Pg5,7,10,11,12,13
I2C3-SDA Pg5,7,10,11,12,13, I2C3-SCL Pg5,7,10,11,12,13
EIM_WAIT, EIM_BCLK, EIM_FPGA_INT_B, EIM_FPGA_CS_B, CAN_WAKE_PULSE_B
TP29 TP30 TP31, ANALOG_MAINBOARD_ID
Hi-Z_FOR_BOOT_B, BOARD_SENSE_B
SH208 0, R235 0, DGND

SH274 0, MX_CAN_WAKE_PULSE_B, TP28
Compatibility for legacy MX53 usage
Cut 0603 short trace if used on MX53 system as another signal.
R292 used for board revision with legacy MX53 CPU Card
3V3_MAIN, R292 10K

Jumper J1000 Configuration

When used with MX6 CPU Card rev B series
1 - 2 = At all times, except during boot with SPI NOR
1 - 2 = After boot with SPI NOR
2 - 3 = During boot with SPI NOR

When used with MX6 CPU Card rev C or later
1 - 2 = At all times
2 - 3 = Not used

TP35, Hi-Z_FOR_BOOT_B Pg6,7,13
3V3_MAIN, R320 22K, J1000 HDR TH 1X3, Default = 1 - 2, R321 470, DGND
Pg8

ICAP Classification: CP: ___ IUO: PUBI: X
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REVISION HISTORY

X15 - David B Nov 12, 2012

Throughout doc - Changed all sheets from
FIUO (Freescale Internal Use Only) to PUBI (Public Information).

Revision Summary

Rev A - released Jun 2010

Rev B1 - released Jan 2011

Rev C - internal prototype only

Rev D - internal design review

Rev E - released Sep 2012

Rev E1 - Mar 2015
Updated notes throughout doc,
Changed net names with "IPOD" to "I2CAUX".

Rev E2 - Jan 2016
Sheet 6 - Changed U23, U24, Y1, J31 to DNP since only
required for use with MX53 CPU Card, which is EOL.
Sheet 7 - Replaced EOL connector CN1 with drop-in replacement.
Sheet 10 - Replaced EOL connector J38 with drop-in replacement.
Sheet 14 - Replaced EOL connector J44. The replacement is
taller profile, so now requires bumpers for CPU Card
support per updated assembly drawing.
Throughout doc - Changed title blocks to NXP.

Rev E3 - Jan 2016
Sheet 1 - Added board family graphic and disclaimer.
Sheet 5 - Added note on swapped L & R channels.

Rev E4 - Mar 2016
Design cache update

ICAP Classification: CP: ___ IUO: PUBI: X

Drawing Title:
MX6 Automotive Base Board

Page Title:
Revision History

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