i.MX233 169-Pin Package
5V Only Configuration (No Li-Ion Battery)

This schematic shows an application running off of 5V always, with no Li-Ion battery. The primary differences in this schematic compared to the Li-Ion battery case are:

1) The connection of the i.MX's PMU VDD4P2, BATT, and DCDC_BATT pins.
2) The RESET circuit.
3) The POWER button circuit (or lack thereof).

The i.MX233 should use ceramics + 100 mOhm series resistors or low-ESR tantalums for the VDD4P2 supply.

OPTIONAL RTC BACKUP

D19, R327, R238, and SC1 are optional components that may be added if the application requires the RTC to remain powered even if 5V power is lost.

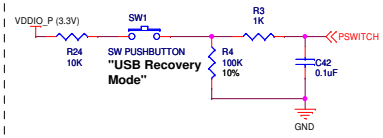
To use this circuit, populate D19, R327, and SC1, and remove R329.

Value of SuperCap required will be determined by amount of time required to power RTC without 5V present and the RTC current (typically ~13uA for the 32kHz).

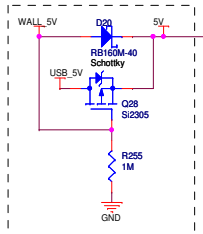
POWER & RECOVERY BUTTONS

There is no need for a POWER button in a 5V only configuration. If a 5V source is present on the VDD5V pin, the i.MX device will automatically power up. There is also no way to power down the i.MX PMU's outputs (VDDIO, VDDA, VDDM, & VDDD) if a 5V source is present on the VDD5V pin. If true power down is required, it is recommended to add a switch to the 5V source.

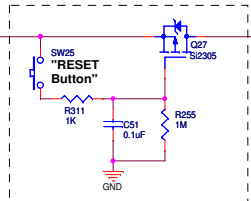
Note that button SW1 could be assigned to another function as well during normal, non-recovery operation.



NOTE: Use double vias for these VDDIO_EMI pinsand place the bypass capacitors as close as possible - one for ball L6 and one for balls L8 / L10.



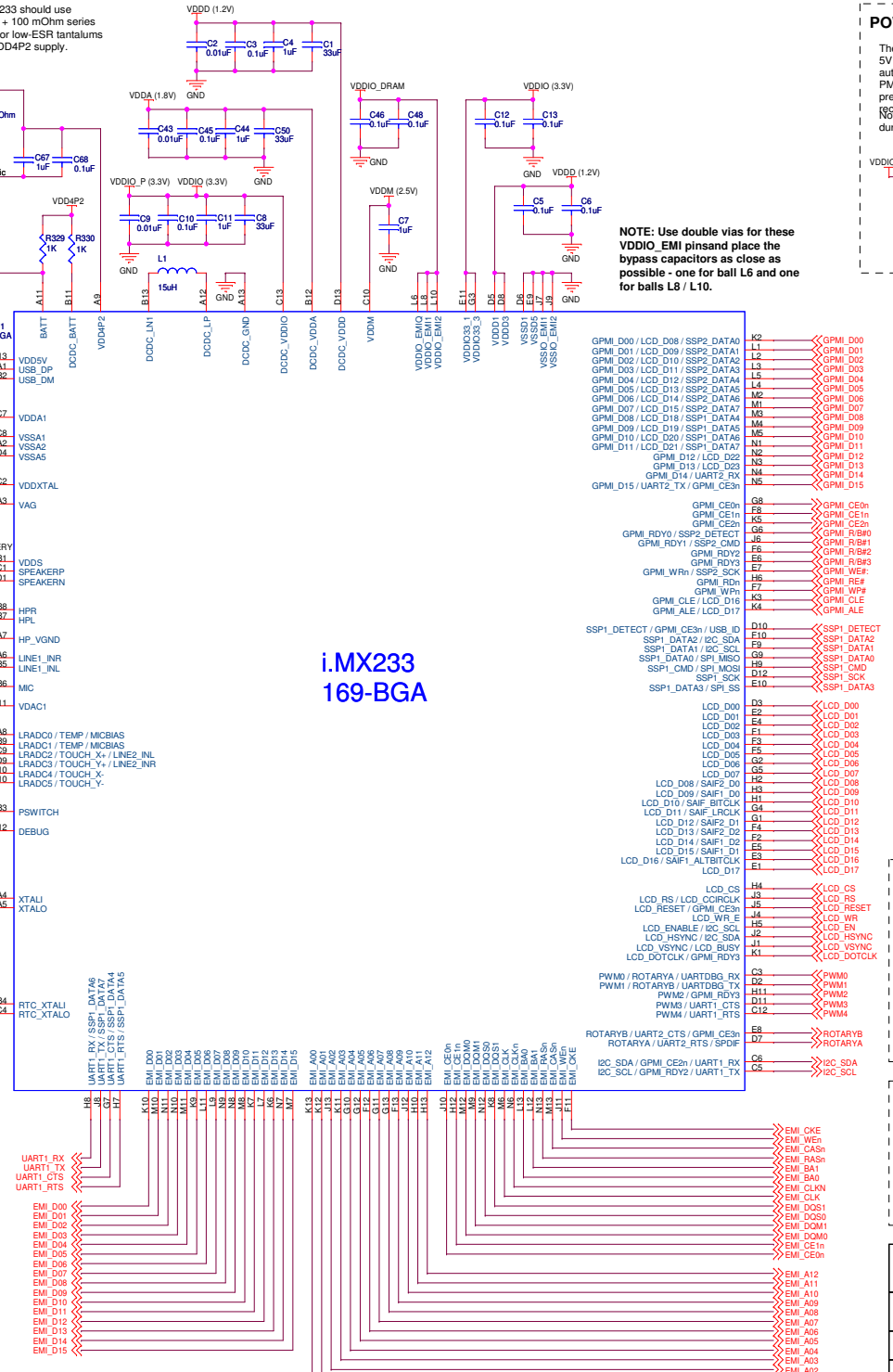
OPTIONAL USB5V / WALL 5V MUX CIRCUIT



OPTIONAL RESET CIRCUIT

Pressing the RESET button in the circuit shown above will cause a full system reset (i.e., the i.MX processor will reset and all the i.MX DCDC output rails will be pulled to ground).

If not used, short the VDD5V net to the USB5V net.



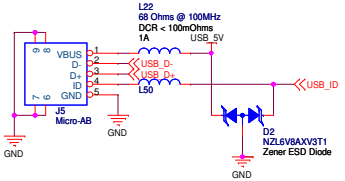
USB 2.0 Connector

Route USB D+ and D- according to the High Speed USB2.0 Design Guidelines. D+ and D- should have a 90 ohm differential trace impedance and the PCB should have a 20 mil minimum spacing between the USB data lines (D+ and D-) and other signal lines.

In order to maximize ESD immunity, the industrial design plastics should expose the USB Connector as little as possible.

The L22 ferrite is recommended for ESD immunity. Note that any ferrite in series with the USB_5V supply should have a low DCR (<100mOhms).

The D2 Zener Diode is strongly recommended to protect the VDD5V pin of the i.MX23 from damaging overvoltage conditions that can result from USB cable attachments or from ESD events.



For applications that support cable-based detection of Host or Device modes.

USB_ID — SSP1_DETECT

IMPORTANT LAYOUT DESIGN NOTES

1) The crystals should be placed as close as possible to the i.MX device.

2) For best USB jitter performance, the VDDXTAL capacitor and the crystal load capacitors should NOT connect to the ground plane near the DRAM bus routing and grounds. These ground connections should preferably be close to the VAG bypass capacitor.

3) All DCDC input & output capacitors should be located close to the i.MX device.

IMPORTANT CRYSTAL DESIGN NOTES

Consult crystal manufacturer datasheet for recommended load capacitor values (typically 10-18pF).

Cload = [(C26*C27) / (C26+C27)] + Cstray

where Cstray = stray PCB capacitance, typically 4 - 6 pF

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Drawing Title: i.MX23 REFERENCE SCHEMATICS

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