



PRODUCT SPECIFICATION

3.5” 240RGB x 320 TFT With Touch Panel

MODEL NUMBER: FLXH-9950DPTP035H-01

Rev: 03

CUSTOMER P/N:

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1. General Description

This display module consists of a transmissive 3.5 inch 240RGB x 320, TFT a-Si Active Matrix Color LCD that is electronically and mechanically integrated. The TFT display is capable of displaying 65K colors. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. The display drivers incorporated is the ST7789S, single chip IC with integrated source and gate outputs, timing controller, and power supply , maximum speed rate is 10M Hz . All LCD voltages and subsequent voltage regulation functions are provided by the integrated DC/DC converter-based power supply. All supporting components necessary for the correct operation of the driver are included on the module FPC.

The product consists with a film to glass structure 4-wires resistive touch panel.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	3.5"	Inch
LCD type	α-Si TFT	-
Display Mode	TN / Transmissive / Normally white	-
Resolution	240RGB x 320	-
View Direction	6 O'clock (best image)	-
Grayscale Reversion	12 O'clock	
Module Outline	70.0 (H) x 91.5 (V) x5.85(T)mm (Note1)	mm
Active Area	52.56(H) x 70.08(V)	mm
Pixel Size	73 x 3(H) x 219(V)	um
Pixel Arrangement	RGB Vertical stripe	-
Interface	SPI / RGB interface / MCU parallel interface	-
Front Polarizer Surface Treatment	Anti-Glare	
Display Colors	262K	-
Driver IC	ST7789S or EQU	-
Power Consumption(TFT)	66(max) (Note2)	mW
Weight	TBD	g

Note 1: Excluding hooks, posts, FPC/FPC tail etc.

Note 2: Excluding Backlight & TP Current Consumption.

3. Absolute Maximum Ratings

VSS=0V, Ta=25±2°C

Item	Symbol	Min.	Max.	Unit
LCD Supply Voltage	VDD	-0.3	4.6	V
Storage temperature	Tstg	-30	+80	°C
Operating temperature	Topa	-20	+70	°C
Storage humidity	Hstg	10	Note 1	%RH
Operating humidity	Hopa	10	Note 1	%RH

- Note 1: 90% max, if Ta is below 50 deg C; 60% max, if Ta is over 60 deg C.
- If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

4. Electrical Characteristics

4.1. DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	2.4	3.3	3.3	V
Logic Low input voltage	V _{IL}	VSS	-	0.3* VDD	V
Logic High input voltage	V _{IH}	0.7*VDD	-	VDD	V
Logic Low output voltage	V _{OL}	GND	-	0.2*VDD	V
Logic High output voltage	V _{OH}	0.8*VDD	-	VDD	V
Current Consumption(Note2)	I _{VCC}	-	15	20	mA
Sleep Mode Current Consumption	I _{VCC}	-	--	30	uA
Frame Frequency	f _{FR}	-	(70)	-	Hz

Note1 : Analog and logic power supply were tied together in internal and mark as VDD in pin out definition

Note2: Excluding the LED and Touch Panel current consumption, just LCD display part consumption.

4.2. Backlight Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Forward Voltage	V _f	Ta=25 °C, I _f =20mA	18.8	19.2	19.8	V
Forward Current	I _f	Ta=25 °C	-	20	-	mA
Reverse Voltage	V _R	-	-	-	5*6	V
Reverse current	I _R	-	-	-	10	uA
Power dissipation	P _d		-	384	396	mW
Half life			40,000 hrs			
Drive method			Constant current			
LED Configuration			6 White LEDs in series			

Note: Test condition I_f=20mA, Ta=25°C.

4.3. Touch Panel Characteristics

Features	Details	Notes
Operation Technology	Projected capacitive	--
Input Method	Bare or gloved finger or thick conductive stylus	--
Number of simultaneous touches	one and gesture	--
Min. spacing between 2 touches	18	mm
Positional Accuracy	± 2.5mm at 4 edges and 1.5mm at center	mm
Minimum Touch Area	30	mm ²
Minimum Touch Pressure	0	N
Number of touches	>10 million over lifetime	With correct input method
Connection Type	ZIF Connector	--
Anti-glare surface	No	Available on request
Optical Transmittance	87% min	Measured by LCD5100
FG Weight	TBD	g
Non-Linearity	≤ 1.5%	--
ROHS Compliance	Yes	SJ/T 11363-2006 (China)
Interface to Host	I2C	400kbps
Response Time/Speed	<10ms	Measured by Oscilloscope
I2C Address (Recommend)	0x38	
Touch controller	FT6306	Focaltech
ESD Capability	15KV	Air discharge (TP with lens)
Operating Voltage	3.30V	--

4.4. Touch panel controller FT6306 Characteristic

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V _{dd}	2.8	3.3	V	GND=0V
Operating temperature	T _{opa}	-20	70	°C	
Current Consumption	I	--	--	18	mA
Storage temperature	T _{stg}	-30	80	°C	
Operating Relative Humidity (Noncondensing)		35	70	%RH	70%RH with Ta ≤ 40C
Storage Relative Humidity		35	70	%RH	
Operating Altitude (Corresponding Pressures)		616	1075	hPa	
Storage Altitude (Corresponding Pressures)		500	1075	hPa	

5. Optical Characteristics

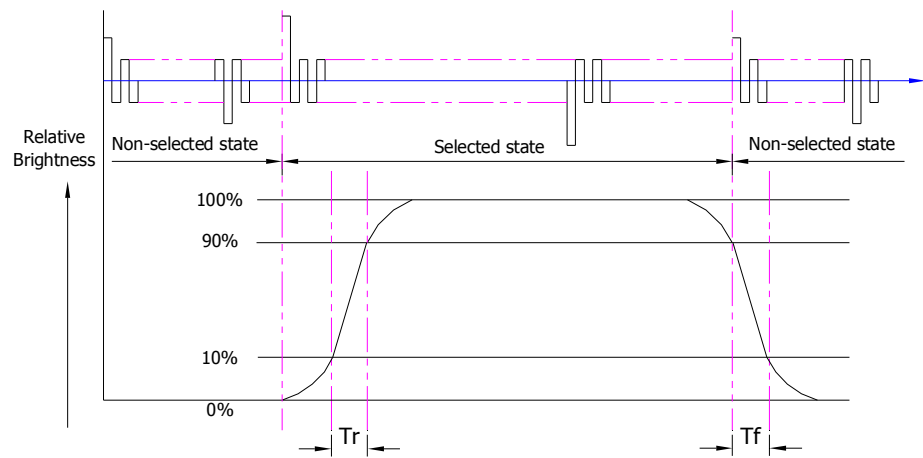
5.1. Optical Characteristics

Ta=25°C, VDD=3.3V, ILED=20mA

	Item	Symbol	Condition	Specification			Unit	
				Min.	Typ.	Max.		
Backlight On (Transmissive Mode)	Contrast ratio	CR	θ= 0° Normal viewing angle	300	400	-		
	Surface Luminance(TP Surface)	L _V		250	300	-	cd/m ²	
	Response time	T _F +T _R		-	25	50	ms	
	Color Chromaticity	Red	X _R	CR>10	0.59	0.63	0.67	-
			Y _R		0.31	0.35	0.39	
		Green	X _G		0.3	0.34	0.38	
			Y _G		0.55	0.59	0.63	
		Blue	X _B		0.11	0.15	0.19	
			Y _B		0.04	0.08	0.12	
		White	X _W		0.28	0.32	0.36	
			Y _W		0.3	0.34	0.38	
	Viewing Angle	Horizontal	θ _L	CR>10	60	65	-	-
			θ _R		60	65	-	
		Vertical	θ _U		60	65	-	
θ _D			55		60	-		
NTSC Ratio(Gamut)				45	50		%	

5.2. Definition of Response Time

5.2.1. Normally Black Type (Negative)

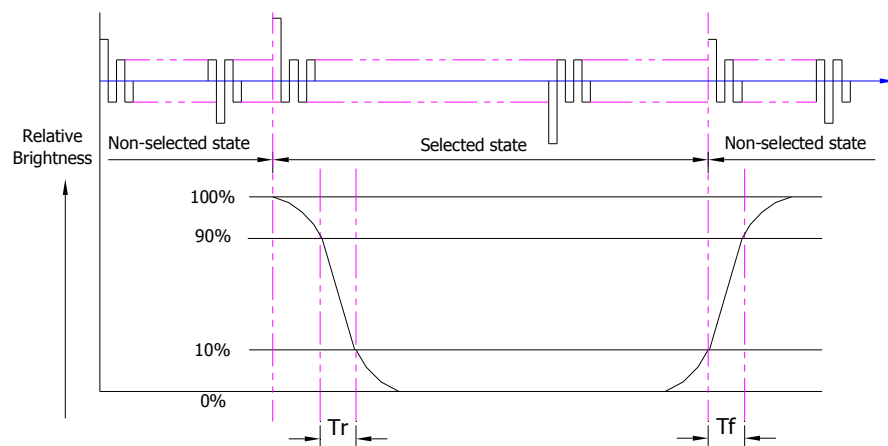


Tr is the time it takes to change from non-selected state with relative luminance 10% to selected state with relative luminance 90%;

Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Note : Measuring machine:BM-7

5.2.2. Normally White Type (Positive)



Tr is the time it takes to change from non-selected state with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

5.3. Definition of Contrast Ratio

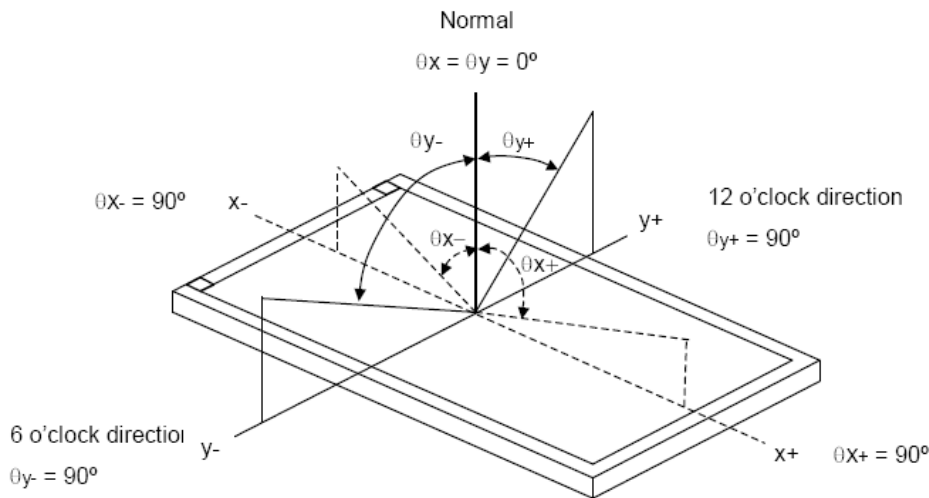
Contrast is measured perpendicular to display surface in reflective and transmissive mode.

The measurement condition is:

Measuring Equipment	BM-7 or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

5.4. Definition of Viewing Angles



Measuring machine: LCD-5100 or EQUI

5.5. Definition of Color Appearance

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)

TBD

5.6. Definition of Surface Luminance, Uniformity and Transmittance

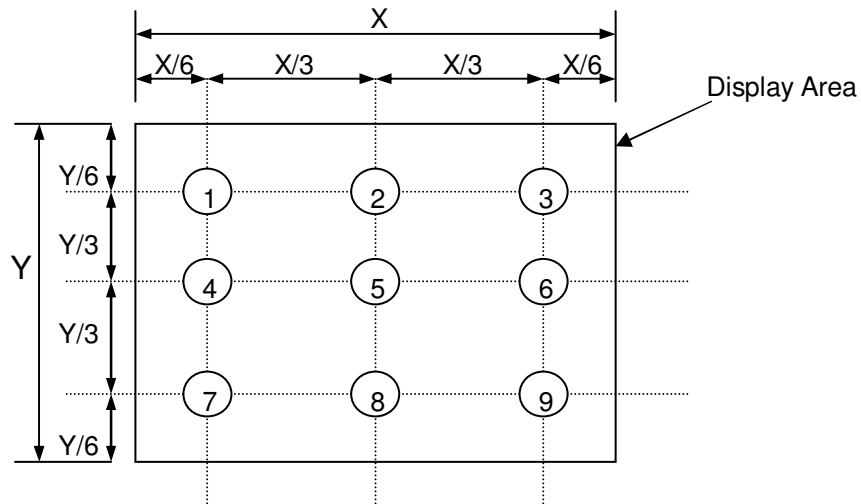
Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

5.6.1 Surface Luminance: $L_V = \text{average } (L_{P1}:L_{P9})$

5.6.2 Uniformity = $\text{Minimal } (L_{P1}:L_{P9}) / \text{Maximal } (L_{P1}:L_{P9}) * 100\%$

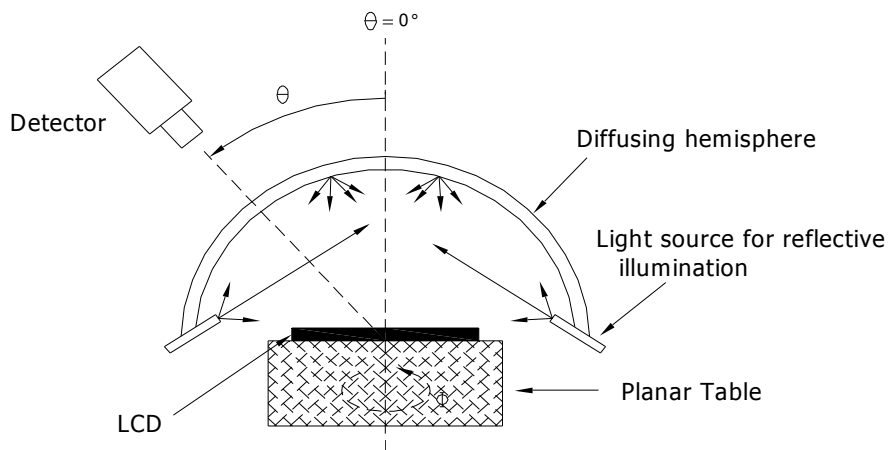
5.6.3 Transmittance = $L_V \text{ on LCD} / L_V \text{ on Backlight} * 100\%$

Note : Measuring machine: BM-7

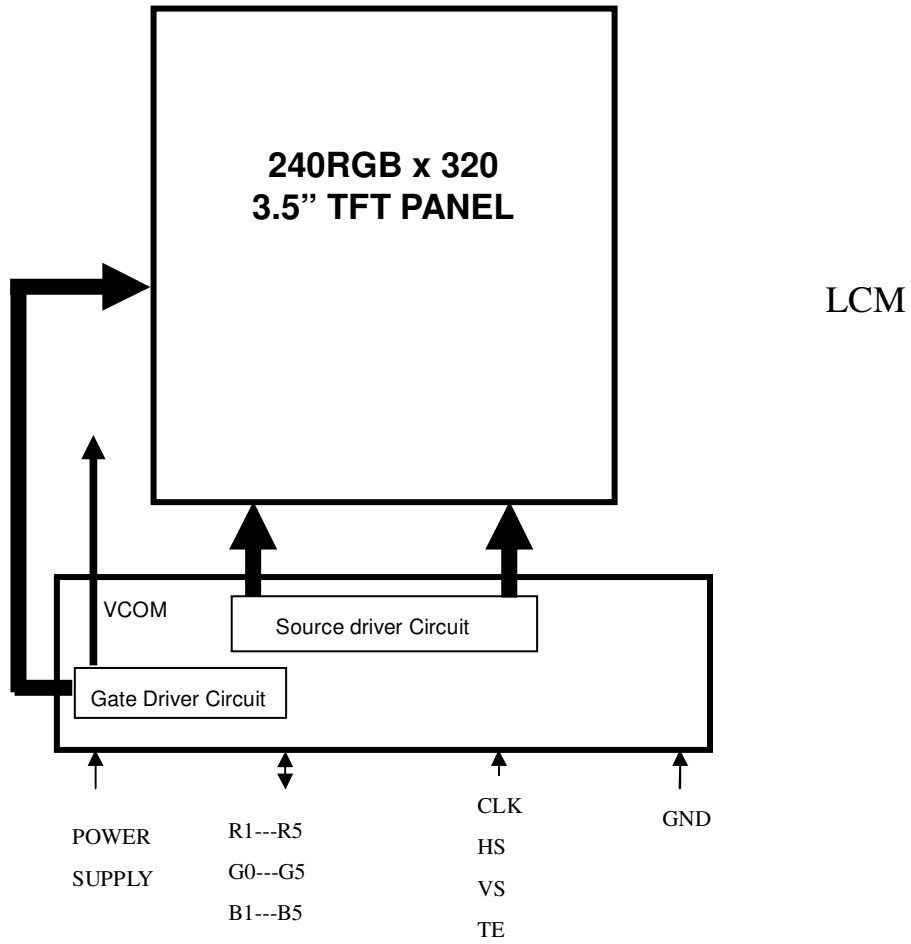


5.7. Definition of Reflectivity

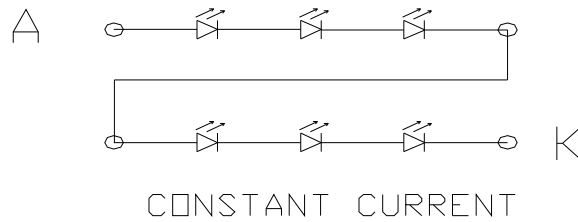
To measure the reflectivity, the detector should be aligned to the normal direction of the LCD surface corresponding azimuthally angle $\theta=0^\circ$

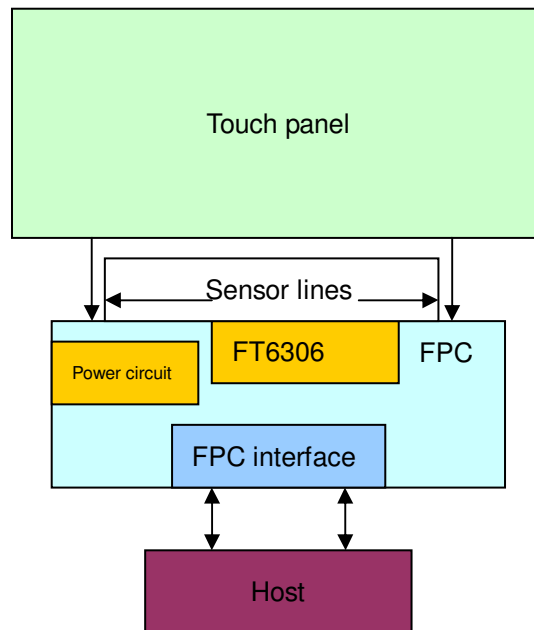


6. Block Diagram and Power Supply



BACKLIGHT SCHEMATIC





7. TFT Interface Pins Definition

No.	Symbol	I/O	Function
1	NC		NC
2	NC		NC
3	NC		NC
4	NC		NC
5	TE	O	Tearing effect signal is used to synchronize MCU to frame memory writing.
6~23	DB17~DB0	I/O	<p>-DB[17:0] are used as MCU parallel interface data bus.</p> <p>8-bit I/F: when IM3:0, DB[7:0] are used; when IM3:1, DB[17:10] are used.</p> <p>9-bit I/F: when IM3:0, DB[8:0] are used; when IM3:1, DB[17:9] are used.</p> <p>16-bit I/F: when IM3:0, DB[15:0] are used; when IM3:1, DB[17:10] and DB[8:1] are used.</p> <p>18-bit I/F: DB[17:0] are used.</p> <p>-DB[17:0] are used as RGB interface data bus.</p> <p>6-bit RGB I/F: DB[5:0] are used.</p> <p>16-bit RGB I/F: DB[17:13], DB[11:1] are used.</p> <p>18-bit RGB I/F: DB[17:0] are used.</p> <p>-If not used, please fix this pin at VDDI or DGND.</p>

24	SDA	I	-When IM3: Low, SPI interface input/output pin. -When IM3: High, SPI interface input pin. -The data is latched on the rising edge of the SCL signal.																																																																														
25	DOTCLK	I	Dot clock signal for RGB interface operation.																																																																														
26	ENABLE	I	Data enable signal for RGB interface operation.																																																																														
27	HSYNC	I	Horizontal (Line) synchronizing input signal for RGB interface operation.																																																																														
28	VSYNC	I	Vertical (Frame) synchronizing input signal for RGB interface operation.																																																																														
29	RDX	I	Read enable in 8080 MCU parallel interface.																																																																														
30	WRX	I	-Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface.																																																																														
31	DCX	I	-Display data/command selection pin in parallel interface. -This pin is used to be serial interface clock.																																																																														
32	CSX	I	Chip selection pin																																																																														
33	RST	I	This signal will reset the device and it must be applied to properly initialize the chip.																																																																														
34	IM0	I	-The MCU interface mode select.																																																																														
35	IM1	I	<table border="1"> <thead> <tr> <th>IM3</th> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>MPU Interface Mode</th> <th>Data pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>80-8bit parallel I/F</td> <td>DB[7:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>80-16bit parallel I/F</td> <td>DB[15:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>80-9bit parallel I/F</td> <td>DB[8:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>80-18bit parallel I/F</td> <td>DB[17:0],</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>3-line 9bit serial I/F</td> <td>SDA: in/out</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>4-line 8bit serial I/F</td> <td>SDA: in/out</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>80-16bit parallel I/F II</td> <td>DB[17:10], DB[8:1]</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>80-8bit parallel I/F II</td> <td>DB[17:10]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>80-18bit parallel I/F II</td> <td>DB[17:0],</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>80-9bit parallel I/F II</td> <td>DB[17:9]</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>3-line 9bit serial I/F II</td> <td>SDA: in/ SDO: out</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>4-line 8bit serial I/F II</td> <td>SDA:in/ SDO: out</td> </tr> </tbody> </table>	IM3	IM2	IM1	IM0	MPU Interface Mode	Data pin	0	0	0	0	80-8bit parallel I/F	DB[7:0]	0	0	0	1	80-16bit parallel I/F	DB[15:0]	0	0	1	0	80-9bit parallel I/F	DB[8:0]	0	0	1	1	80-18bit parallel I/F	DB[17:0],	0	1	0	1	3-line 9bit serial I/F	SDA: in/out	0	1	1	0	4-line 8bit serial I/F	SDA: in/out	1	0	0	0	80-16bit parallel I/F II	DB[17:10], DB[8:1]	1	0	0	1	80-8bit parallel I/F II	DB[17:10]	1	0	1	0	80-18bit parallel I/F II	DB[17:0],	1	0	1	1	80-9bit parallel I/F II	DB[17:9]	1	1	0	1	3-line 9bit serial I/F II	SDA: in/ SDO: out	1	1	1	0	4-line 8bit serial I/F II	SDA:in/ SDO: out
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1	1	1	0	4-line 8bit serial I/F II	SDA:in/ SDO: out																																																																												
36	IM2	I																																																																															

37	VDD	I	Power Supply
38	VSS	I	Ground
39	K	I	Cathode of Backlight LED
40	A	I	Anode of Backlight LED

7.1 Touch panel Interface Pins Definition

No.	Symbol	I/O	Function
1	GND	P	Ground connection
2	CTP_VDD	P	Power supply
3	CTP_VDD	P	Power supply
4	INT	I	Interrupt signal ;active low, require pull up resistors 10kΩ
5	SDA	I/O	I2C Serial Data Input/Output, require pull up resistors 10kΩ
6	SCL	I/O	I2C Serial Clock Input/Output, require pull up resistors 10kΩ
7	RST	I	Reset
8	GND	P	Ground connection

8. Display AC Characteristics

8.1. Power Sequence

VDD must be powered on before the VDDI.

VDDI must be powered off before the VDD.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

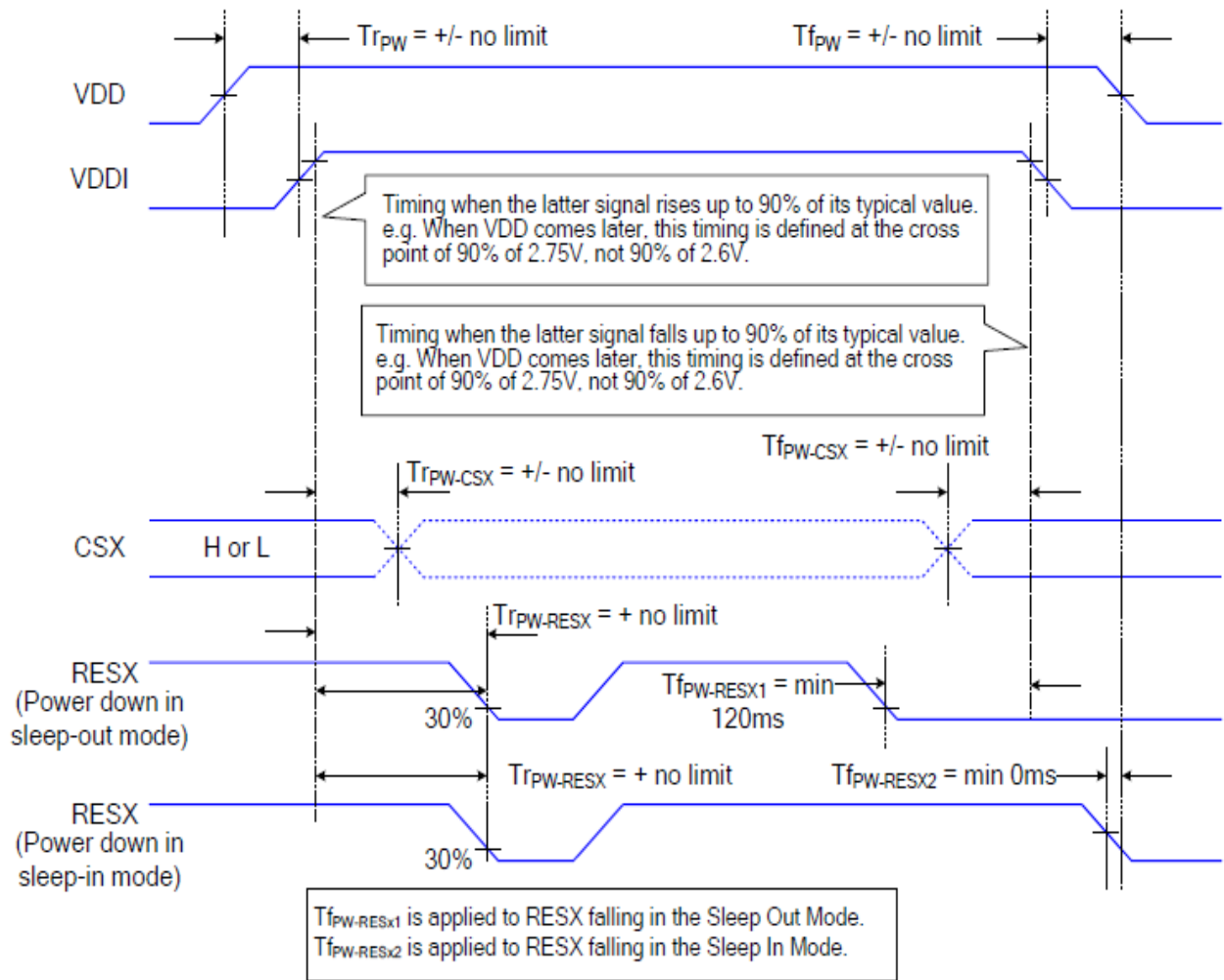
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

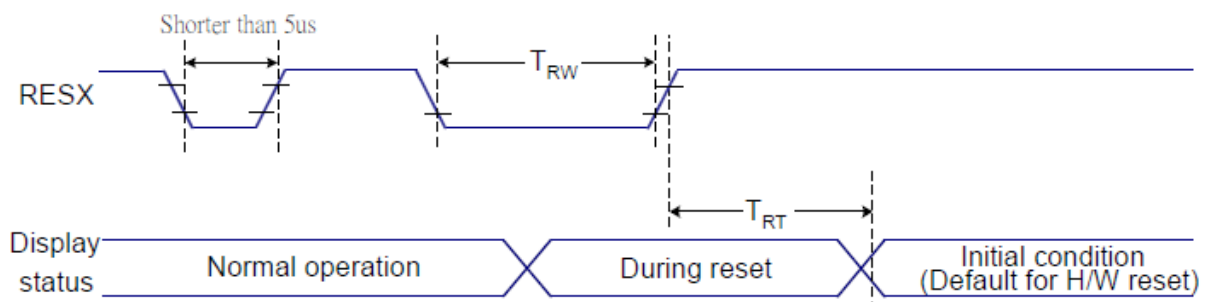
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.



8.2. Reset Timing



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 °C

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 8 Reset Timing

Notes:

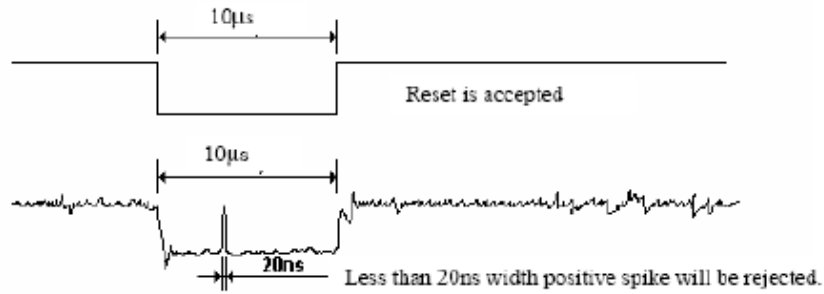
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



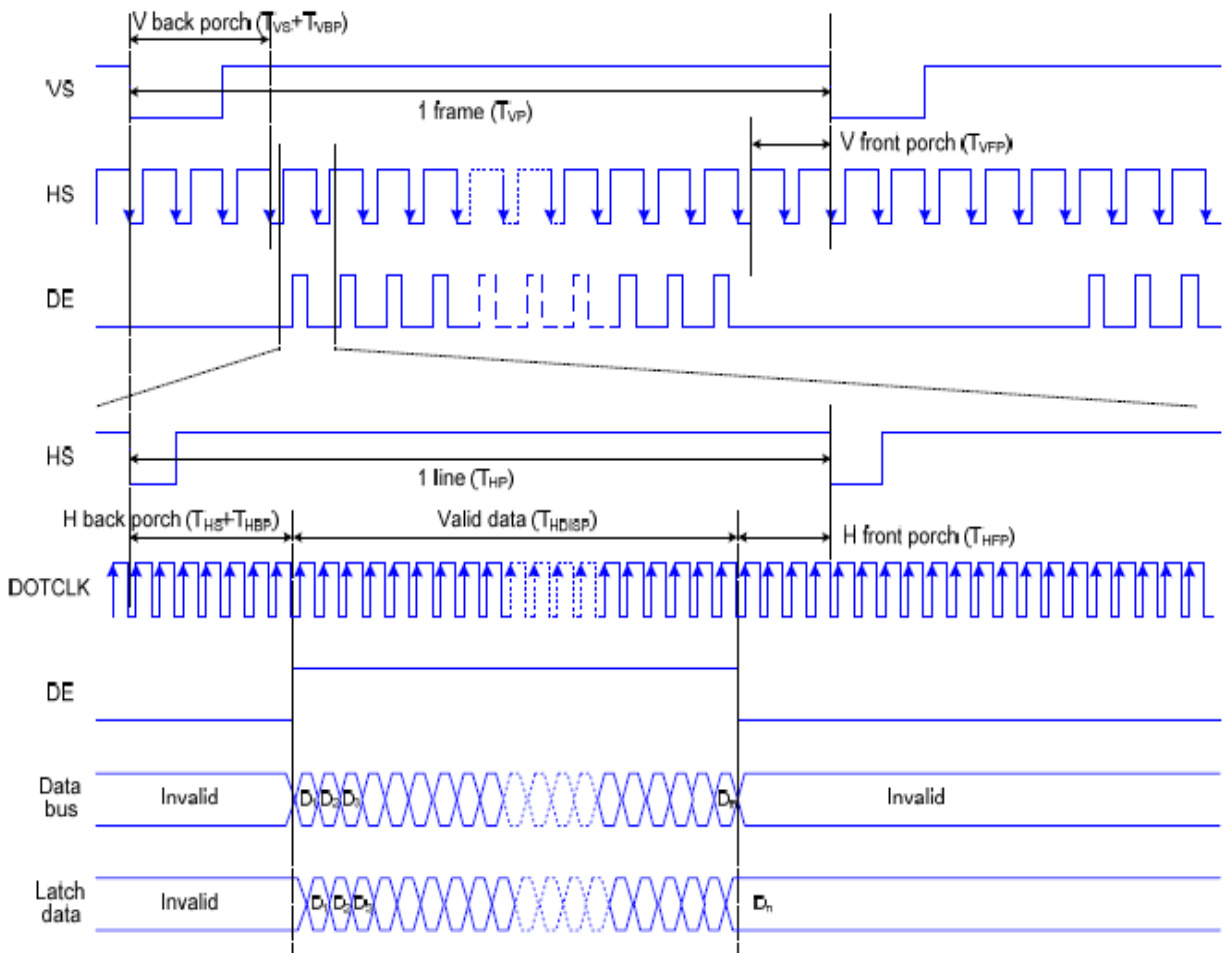
5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

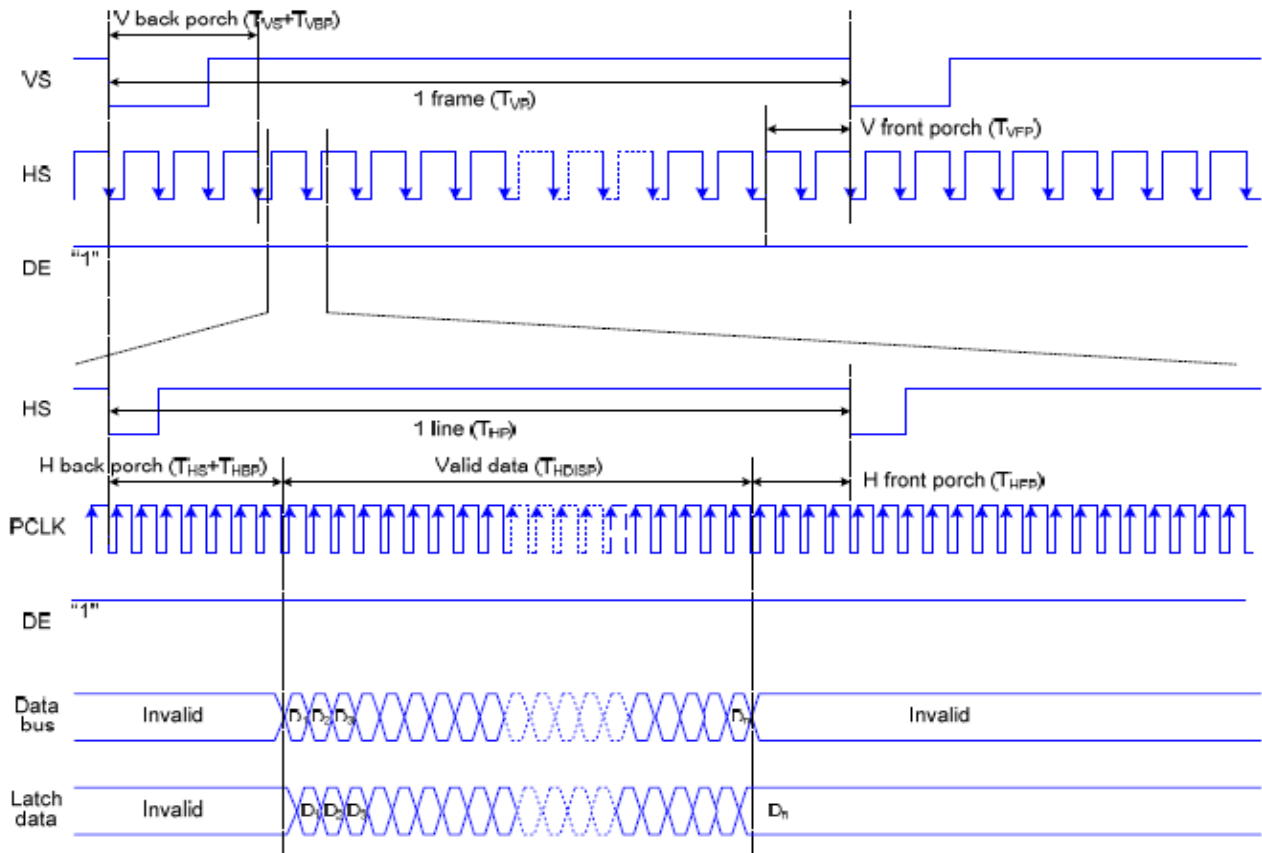
8.3. RGB Interface Timing

8.3.1. The timing chart of RGB interface DE mode is shown as below:



Note: The setting of front porch and back porch in host must match that in IC as this mode.

8.3.2. The timing chart of RGB interface HV mode is shown as below:



The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period.

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

In 6-bit RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals. In other words, one pixel data needs to take three DOTCLKs to transfer.

In 6-bit RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

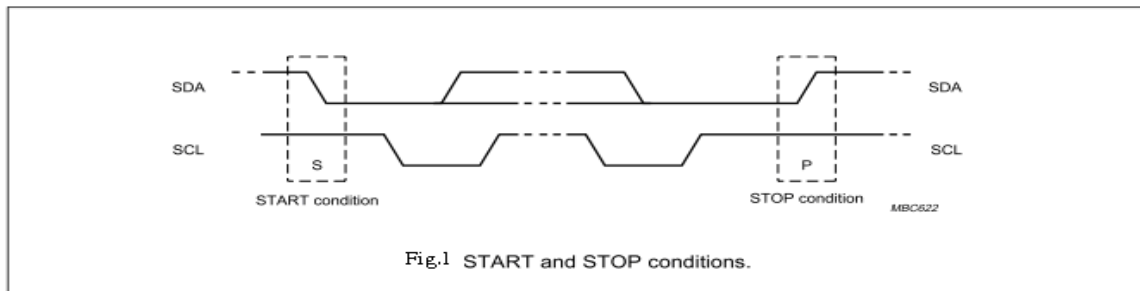
In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

8.4. Touch Panel Interface Timing

8.4.1. START and STOP conditions (See fig.1)

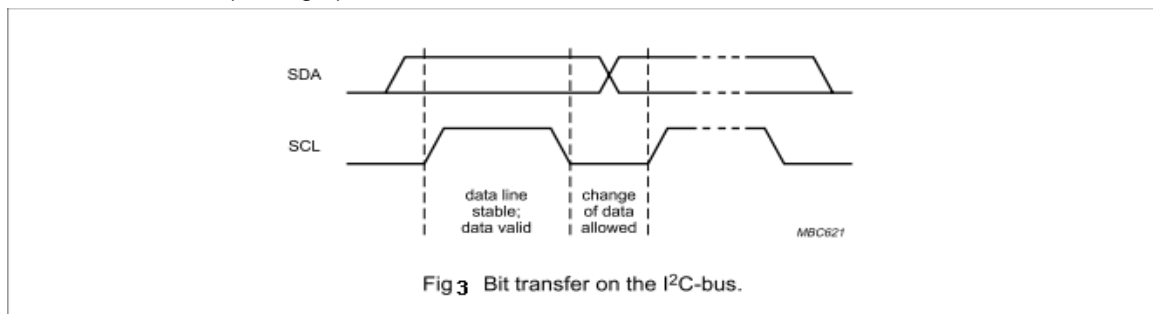
A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.



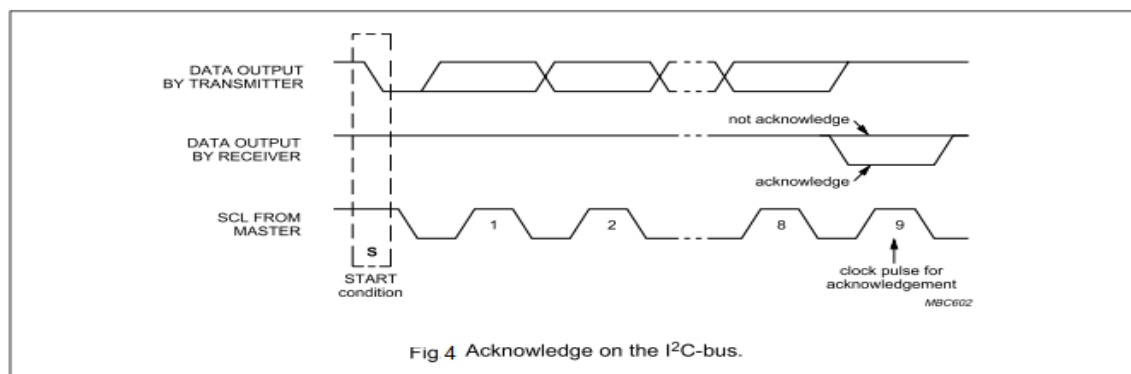
8.4.2. TRANSFERRING DATA

The data on the SDA line must be stable during the HIGH period of clock. The HIGH or LOW state of the data line can only change when clock signal on the SCL line is low (see fig.3) .



8.4.3. Acknowledge

The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. (See fig.4)



8.4.4. Touch event output

The pin CHG is the touch event output pin. It goes low when a touch event has been detected and remains low until all the event messages have been sent to Host

9. Recommended Setting and Initialization Flow

(Please reference ST7789S IC datasheet.)

10. Quality Assurance

10.1.Purpose:

This standard for Quality Assurance assures the quality of LCD module products supplied to customer by New Vision Display.

10.2.Standard for Quality Test:

New Vision Display performs the following tests to ensure the quality of product before shipment.

10.2.1. Sampling Plan:

- 10.2.1.1. ANSI / ASQC Z1.4-2008.
- 10.2.1.2. Single sampling, normal inspection.

10.2.2. Sampling Criteria:

- 10.2.2.1. Visual inspection: AQL 1.5%
- 10.2.2.2. Electrical functional: AQL 0.65%.

10.2.3. Reliability Test:

- 10.2.3.1. Detailed requirement refer to Reliability Test Specification.

10.3.Nonconforming Analysis & Disposition

10.3.1. Nonconforming analysis:

- 10.3.1.1. Customer should provide overall information of non-conforming sample for their complaints.
- 10.3.1.2. After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.
- 10.3.1.3. If New Vision Display can not finish the analysis on time, customer will be notified with the progress status.

10.3.2. Disposition of nonconforming:

- 10.3.2.1. Non-conforming product over PPM level will be replaced.
- 10.3.2.2. The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

10.4. Agreement Items

10.4.1. New Vision Display and customer shall negotiate if the following situation occurs:

10.4.1.1. There is any discrepancy in standard of quality assurance.

10.4.1.2. Additional requirement to be added in product specification.

10.4.1.3. Any other special problem.

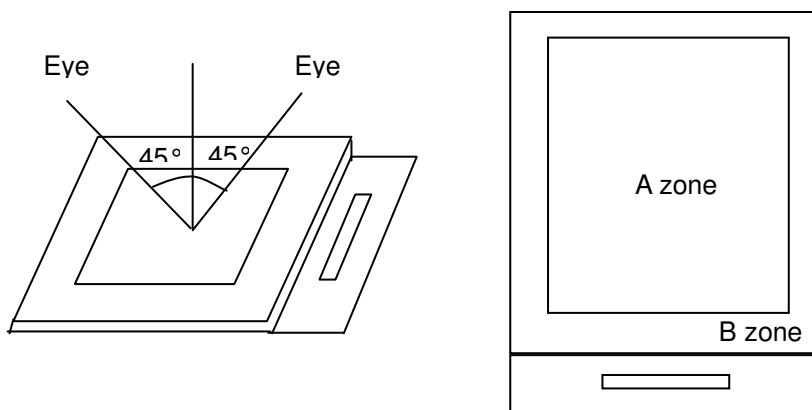
10.5. Standard of the Product Visual Inspection:

10.5.1. Appearance inspection:

10.5.1.1. The inspection must be under illumination about 750 – 1500 lux, and the distance of view must be at 35cm \pm 5cm.

10.5.1.2. The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

10.5.1.3. Definition of area: A Zone: Active Area, B Zone: Viewing Area,

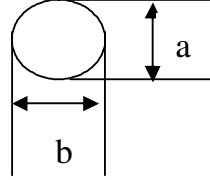
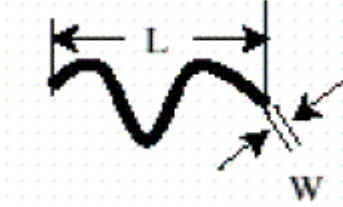
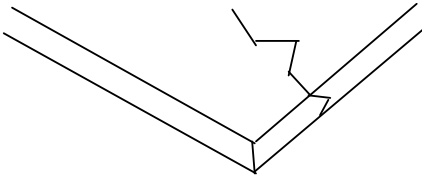


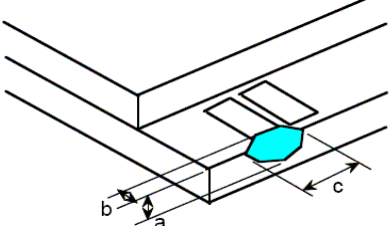
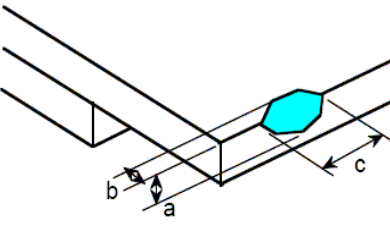
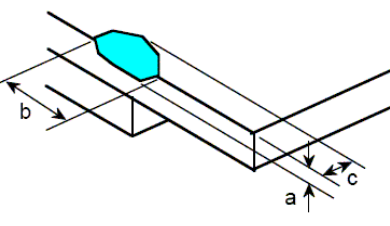
10.5.2. Basic principle:

10.5.2.1. A set of sample to indicate the limit of acceptable quality level must be discussed by both New Vision Display and customer when there is any dispute.

10.5.2.2. New item must be added on time when it is necessary.

10.6. Inspection Specification:

No.	Item	Criteria (Unit: mm)																		
01	Dot (Applied for dot defect except item 15, include Visual Defect and Functional Defect)	 <table border="1" data-bbox="810 421 1311 719"> <thead> <tr> <th>Size</th> <th>Area</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td>$\phi \leq 0.10$</td> <td></td> <td>Ignore</td> </tr> <tr> <td>$0.10 < \phi \leq 0.15$</td> <td></td> <td>2</td> </tr> <tr> <td>$0.15 < \phi \leq 0.20$</td> <td></td> <td>1</td> </tr> <tr> <td>$0.20 < \phi$</td> <td></td> <td>0</td> </tr> <tr> <td>Total</td> <td></td> <td>2 no include $\phi \leq 0.10$</td> </tr> </tbody> </table> <p>$\phi = (a + b) / 2$</p> <p>Distance between 2 defects should more than 3mm apart.</p>	Size	Area	Acc. Qty	$\phi \leq 0.10$		Ignore	$0.10 < \phi \leq 0.15$		2	$0.15 < \phi \leq 0.20$		1	$0.20 < \phi$		0	Total		2 no include $\phi \leq 0.10$
Size	Area	Acc. Qty																		
$\phi \leq 0.10$		Ignore																		
$0.10 < \phi \leq 0.15$		2																		
$0.15 < \phi \leq 0.20$		1																		
$0.20 < \phi$		0																		
Total		2 no include $\phi \leq 0.10$																		
02	Black and White line Scratch Foreign material (Line type) (Minor defect)	 <table border="1" data-bbox="628 1088 1254 1375"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td>/</td> <td>$W \leq 0.03$</td> <td>Ignore</td> </tr> <tr> <td>$L \leq 2.5$</td> <td>$0.03 < W \leq 0.05$</td> <td>3</td> </tr> <tr> <td>$L \leq 2.5$</td> <td>$0.05 < W \leq 0.10$</td> <td>2</td> </tr> <tr> <td>/</td> <td>$0.1 < W$</td> <td>0</td> </tr> <tr> <td colspan="2">Total</td> <td>3</td> </tr> </tbody> </table> <p>Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.</p>	Length	Width	Acc. Qty	/	$W \leq 0.03$	Ignore	$L \leq 2.5$	$0.03 < W \leq 0.05$	3	$L \leq 2.5$	$0.05 < W \leq 0.10$	2	/	$0.1 < W$	0	Total		3
Length	Width	Acc. Qty																		
/	$W \leq 0.03$	Ignore																		
$L \leq 2.5$	$0.03 < W \leq 0.05$	3																		
$L \leq 2.5$	$0.05 < W \leq 0.10$	2																		
/	$0.1 < W$	0																		
Total		3																		
03	Glass Crack (Minor defect)	 <p>Crack is potential to enlarge, any type is not allowed.</p>																		

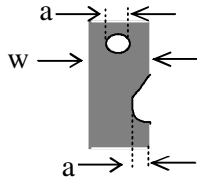
No.	Item	Criteria (Unit: mm)										
04	Glass Chipping Pad Area: (Minor defect)	 <table border="1" data-bbox="598 593 1045 750"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td>$c > 3.0, b < 1.0$</td> <td>1</td> </tr> <tr> <td>$c < 3.0, b < 1.0$</td> <td>3</td> </tr> <tr> <td colspan="2">$a < \text{Glass Thickness}$</td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	3	$a < \text{Glass Thickness}$			
Length and Width	Acc. Qty											
$c > 3.0, b < 1.0$	1											
$c < 3.0, b < 1.0$	3											
$a < \text{Glass Thickness}$												
05	Glass Chipping Rear of Pad Area: (Minor defect)	 <table border="1" data-bbox="598 1064 1045 1265"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td>$c > 3.0, b < 1.0$</td> <td>1</td> </tr> <tr> <td>$c < 3.0, b < 1.0$</td> <td>2</td> </tr> <tr> <td>$c < 3.0, b < 0.5$</td> <td>4</td> </tr> <tr> <td colspan="2">$a < \text{Glass Thickness}$</td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	2	$c < 3.0, b < 0.5$	4	$a < \text{Glass Thickness}$	
Length and Width	Acc. Qty											
$c > 3.0, b < 1.0$	1											
$c < 3.0, b < 1.0$	2											
$c < 3.0, b < 0.5$	4											
$a < \text{Glass Thickness}$												
06	Glass Chipping Except Pad Area: (Minor defect)	 <table border="1" data-bbox="598 1556 1045 1758"> <thead> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td>$c > 3.0, b < 1.0$</td> <td>1</td> </tr> <tr> <td>$c < 3.0, b < 1.0$</td> <td>2</td> </tr> <tr> <td>$c < 3.0, b < 0.5$</td> <td>4</td> </tr> <tr> <td colspan="2">$a < \text{Glass Thickness}$</td> </tr> </tbody> </table>	Length and Width	Acc. Qty	$c > 3.0, b < 1.0$	1	$c < 3.0, b < 1.0$	2	$c < 3.0, b < 0.5$	4	$a < \text{Glass Thickness}$	
Length and Width	Acc. Qty											
$c > 3.0, b < 1.0$	1											
$c < 3.0, b < 1.0$	2											
$c < 3.0, b < 0.5$	4											
$a < \text{Glass Thickness}$												

07	Glass Corner Chipping: (Minor defect)	<table border="1"> <tr> <th>Length and Width</th> <th>Acc. Qty</th> </tr> <tr> <td>$c < 3.0,$ $b < 3.0$</td> <td>Ignore</td> </tr> <tr> <td colspan="2">$a < \text{Glass Thickness}$</td> </tr> </table>	Length and Width	Acc. Qty	$c < 3.0,$ $b < 3.0$	Ignore	$a < \text{Glass Thickness}$		
		Length and Width	Acc. Qty						
$c < 3.0,$ $b < 3.0$	Ignore								
$a < \text{Glass Thickness}$									

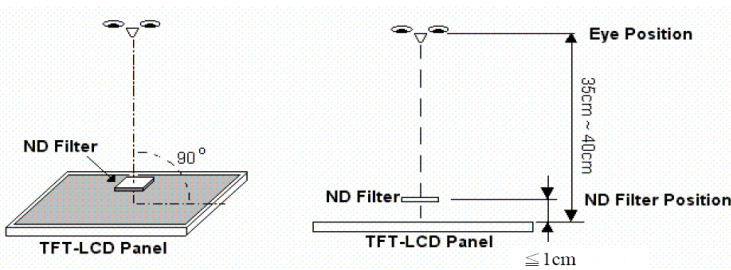
No.	Item	Criteria (Unit: mm)				
08	Glass Burr: (Minor defect)	 <table border="1"> <tr> <th>Length</th> <th>Acc. Qty</th> </tr> <tr> <td>$F < 1.0$</td> <td>Ignore</td> </tr> </table> <p>Glass burr don't affect assemble and module dimension.</p>	Length	Acc. Qty	$F < 1.0$	Ignore
Length	Acc. Qty					
$F < 1.0$	Ignore					

09	Chip on IC	<p>9.1 Corner chip</p> <table border="1"> <tr> <td>a</td> <td>b</td> <td>c</td> </tr> <tr> <td colspan="2">$\leq 0.4\text{mm}$</td> <td>$\leq 1/2t$</td> </tr> </table> <p>Inner bonding wires invisible. The chip can't attach on the surface of IC. Size a, b and c should be measured after removing the chip. t: Thickness of individual IC</p>	a	b	c	$\leq 0.4\text{mm}$		$\leq 1/2t$
		a	b	c				
$\leq 0.4\text{mm}$		$\leq 1/2t$						
<p>9.2 Rim chip</p> <table border="1"> <tr> <td>a</td> <td>b</td> <td>c</td> </tr> <tr> <td>Acceptable</td> <td colspan="2">$\leq 0.2\text{mm}$</td> </tr> </table>	a	b	c	Acceptable	$\leq 0.2\text{mm}$			
a	b	c						
Acceptable	$\leq 0.2\text{mm}$							

		<p>Inner bonding wires invisible. The chip can't attach on the surface of IC. Size a, b and c should be measured after removing the chip.</p>
--	--	---

10	<p>FPC Defect: (Minor defect)</p> 	<p>10.1 Dent, pinhole width $a < w/3$. (w: circuitry width.) 10.2 Open circuit is unacceptable. 10.3 No oxidation, contamination and distortion.</p>								
11	<p>Bubble on Polarizer (Minor defect)</p>	<table border="1"> <thead> <tr> <th>Diameter</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td>$\phi \leq 0.20$</td> <td>Ignore</td> </tr> <tr> <td>$0.20 < \phi \leq 0.30$</td> <td>4</td> </tr> <tr> <td>$0.30 < \phi$</td> <td>None</td> </tr> </tbody> </table> <p>"ϕ" is defined as item 1.</p>	Diameter	Acc. Qty	$\phi \leq 0.20$	Ignore	$0.20 < \phi \leq 0.30$	4	$0.30 < \phi$	None
Diameter	Acc. Qty									
$\phi \leq 0.20$	Ignore									
$0.20 < \phi \leq 0.30$	4									
$0.30 < \phi$	None									
12	<p>Dent on Polarizer (Minor defect)</p>	<table border="1"> <thead> <tr> <th>Diameter</th> <th>Acc. Qty</th> </tr> </thead> <tbody> <tr> <td>$\phi \leq 0.20$</td> <td>Ignore</td> </tr> <tr> <td>$0.20 < \phi \leq 0.30$</td> <td>4</td> </tr> <tr> <td>$0.30 < \phi$</td> <td>None</td> </tr> </tbody> </table> <p>"ϕ" is defined as item 1.</p>	Diameter	Acc. Qty	$\phi \leq 0.20$	Ignore	$0.20 < \phi \leq 0.30$	4	$0.30 < \phi$	None
Diameter	Acc. Qty									
$\phi \leq 0.20$	Ignore									
$0.20 < \phi \leq 0.30$	4									
$0.30 < \phi$	None									
13	<p>Bezel</p>	<p>13.1 No rust, distortion on the Bezel. 13.2 No visible fingerprints, stains or other contamination.</p>								

14	Touch Panel	<p>D: Diameter W: width L: length</p> <p>14.1 Spot: $D < 0.25$ is acceptable $0.25 \leq D \leq 0.4$</p> <p>2dots are acceptable and the distance between defects should more than 10 mm. $D > 0.4$ is unacceptable</p> <p>14.2 Dent: $D > 0.40$ is unacceptable</p> <p>14.3 Scratch: $W \leq 0.03$, $L \leq 10$ is acceptable, $0.03 < W \leq 0.10$, $L \leq 10$ is acceptable</p> <p>Distance between 2 defects should more than 10 mm. $W > 0.10$ is unacceptable.</p>
15	PCB	<p>15.1 No distortion or contamination on PCB terminals.</p> <p>15.2 All components on PCB must same as documented on the BOM/component layout.</p> <p>15.3 Follow IPC-A-600F.</p>
16	RTV	<p>16.1 The RTV glue on the surface of IC isn't permissible to be scratched. The RTV glue can't exist on the surface of polarizer.</p> <p>16.2 No visible non-metal foreign material and metal material in RTV.</p> <p>16.3 Entrapped air bubble isn't permissible to exist on the juncture of RTV glue and pins of LCD.</p> <p>16.4 Air bubble and scratch on the surface of RTV glue invisible within 0.3 m distance is acceptable and the surface of the RTV glue can't flow.</p>
17	Soldering	Follow IPC-A-610C standard

18	Dot(Electrical Defect)	<table border="1"> <tr> <td>Bright Dot</td> <td>A&B Zone</td> <td>Total</td> <td rowspan="2">Note 1</td> </tr> <tr> <td></td> <td>$N \leq 1$</td> <td>$N \leq 1$</td> </tr> <tr> <td>Dark Dot</td> <td>$N \leq 2$</td> <td>$N \leq 2$</td> <td></td> </tr> <tr> <td>Total Dot</td> <td>$N \leq 2$</td> <td>$N \leq 2$</td> <td></td> </tr> <tr> <td>Two or More Adjacent Dot</td> <td colspan="3">Not Allowed</td> </tr> </table> <p>Remark: One pixel consists of 3 sub-pixels, including R,G and B dot(Sub-pixel=Dot)</p> <p>Note 1 Bright dot is defined through 5% transmission ND filter as following:</p>  <p>Defects on the black Matrix, out of viewing area, aren't considered as a defect counted.</p>	Bright Dot	A&B Zone	Total	Note 1		$N \leq 1$	$N \leq 1$	Dark Dot	$N \leq 2$	$N \leq 2$		Total Dot	$N \leq 2$	$N \leq 2$		Two or More Adjacent Dot	Not Allowed		
		Bright Dot	A&B Zone	Total	Note 1																
	$N \leq 1$	$N \leq 1$																			
Dark Dot	$N \leq 2$	$N \leq 2$																			
Total Dot	$N \leq 2$	$N \leq 2$																			
Two or More Adjacent Dot	Not Allowed																				
19	Electrical Defect (Major defect)	<p>The below defects must be rejected.</p> <p>19.1 Missing vertical / horizontal segment, 19.2 Abnormal Display. 19.3 No function or no display. 19.4 Current exceeds product specifications. 19.5 LCD viewing angle defect. 19.6 No Backlight. 19.7 Dark Backlight. 19.8 Touch Panel no function.</p>																			

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

10.7. Classification of Defects:

- 10.7.1. Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.
- 10.7.2. Two minor defects are equal to one major in lot sampling inspection.

10.8. Identification/marketing criteria:

- 10.8.1. Any unit with illegible / wrong /double or no marking/ label shall be rejected.

10.9. Packing:

- 10.9.1. There should be no damage of the outside carton box, each packaging box should have one identical label.
- 10.9.2. Modules inside package box should have compliant mark.
- 10.9.3. All direct package materials shall offer ESD protection.

11. Reliability Specification

Item	Condition	Cycle Time	Quantity	Remark
High Temp. Operation Test	+70 °C	96hrs	8pcs	
Low Temp. Operation Test	-20 °C	96hrs	8pcs	
High Temperature and High Humidity(operation)	Ta=+50 °C, 90%RH	96 hrs	8pcs	
Thermal Shock Test	-20 °C (30min) → +70 °C (30min)	10cycles	5pcs	
Vibration Test (for packaging)	Frequency: 10Hz to 55Hz to 10Hz, Swing:1.5mm,time: X,Y,Z each 2H.	6hrs	One inner carton	
Packing Drop test (for packaging)	1 drop on a corner, 1 drop on three arris, 1 drop on six sides	1time	One inner carton	
ESD(On Final Product)	150pF, 330Ω, ±8KV & ±10KV air & contact test	10times	5pcs	

Note

1. For humidity test, DI water should be used.

Inspection Standard: Inspect after 1-2hrs storage at room temperature, the sample shall be free from the following defects:

- Air bubble in the LCD
- Seal Leakage
- Non-display
- Missing Segment
- Glass Crack
- IDD is greater than twice initial value.
- Others as per QA Inspection Criteria

2. No defect is allowed after testing.

3. ESD should be applied to LCD glass panel, not other areas (such as on IC and so on)

IDD should be within twice initial value.

In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

12. Precautions and Warranty

12.1. Safety

- 12.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.
- 12.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

12.2. Handling

- 12.2.1. Reverse and use within ratings in order to keep performance and prevent damage.
- 12.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

12.3. Storage

- 12.3.1. Do not store the LCD module beyond the specified temperature ranges.

12.4. Metal Pin (Apply to Products with Metal Pins)

12.4.1. Pins of LCD and Backlight

12.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

12.4.1.2. Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

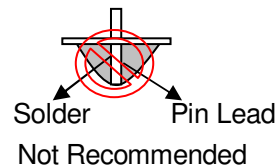
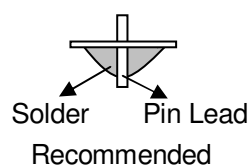
Maximum Solder Temperature: 370°C

Maximum Solder Time: 3s at the maximum temperature

Recommended Soldering Temp: 350±20°C

Typical Soldering Time: ≤3s

12.4.1.3. Solder Wetting



12.4.2. Pins of EL

12.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

12.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

12.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270~290°C

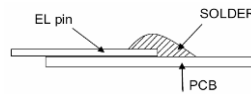
Typical Soldering Time: ≤2s

Minimum solder distance from EL lamp (body):2.0mm

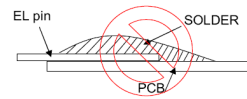
12.4.2.4. No horizontal press on the EL leads during soldering.

12.4.2.5. 180° bend EL leads three times is not allowed.

12.4.2.6. Solder Wetting

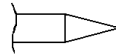


Recommended

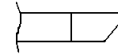


Not Recommended

12.4.2.7. The type of the solder iron:

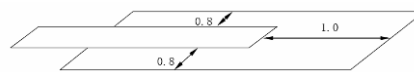


Recommended



Not Recommended

12.4.2.8. Solder Pad



12.5. Operation

12.5.1. Do not drive LCD with DC voltage

12.5.2. Response time will increase below lower temperature

12.5.3. Display may change color with different temperature

12.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear "fractured".

12.6. Static Electricity

12.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.

12.6.2. The normal static prevention measures should be observed for work clothes and benches.

12.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

12.7. Limited Warranty

12.7.1. Unless otherwise agreed between New Vision Display and customer, New Vision Display will replace or repair any of its LCD and LCM which New Vision Display found to be defective electrically and visually when inspected in accordance with New Vision Display Quality Standards, for a period of one year from date of shipment.

12.7.2. The warranty liability of New Vision Display is limited to repair and/or replacement. New Vision Display will not be responsible for any consequential loss.

12.7.3. If possible, we suggest you use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.

13. Packaging

TBD

Reference

Item	Description	Revision
ST7789S	TFT driver IC datasheet	V1.3
FT6306	TP driver IC datasheet	