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10	NOR Flash, Boot Select
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12	USB
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14	Mini PCIE
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17	Parallel Display, MIPI
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22	Card Edge Fingers
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MX6 Quad SABRE AI CPU2 Card with AVB

Revision F2

Qualcomm (Atheros)
Ethernet PHY Card - RGMII

Schematic SCH-27953
Part No. IMXAI2ETH-ATH

Broadcom
Ethernet PHY Card - RGMII

Schematic SCH-27954
Part No. IMXAI2ETH-BRC

Broadcom
Ethernet Switch Card - RGMII

Schematic SCH-27955
Part No. IMXAI2SWCH-BRC

MX6 Quad CPU2 Card

Schematic SCH-27925
Part No. MCIMX6QAICPU2

MX6 DualLite CPU2 Card

Schematic SCH-28605
Part No. MCIMX6DLAICPU2

Automotive Base Board

Schematic SCH-26662
Part No. MCIMXABASEV1

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design. For an added resource, refer to Hardware Development Guide document number IMX6DQ6SDLHDG.

Consumer devices were utilized in this design when lead time for equivalent automotive-grade devices conflicted with production schedules. Freescale suggests consulting component suppliers for equivalent automotive-grade device information.

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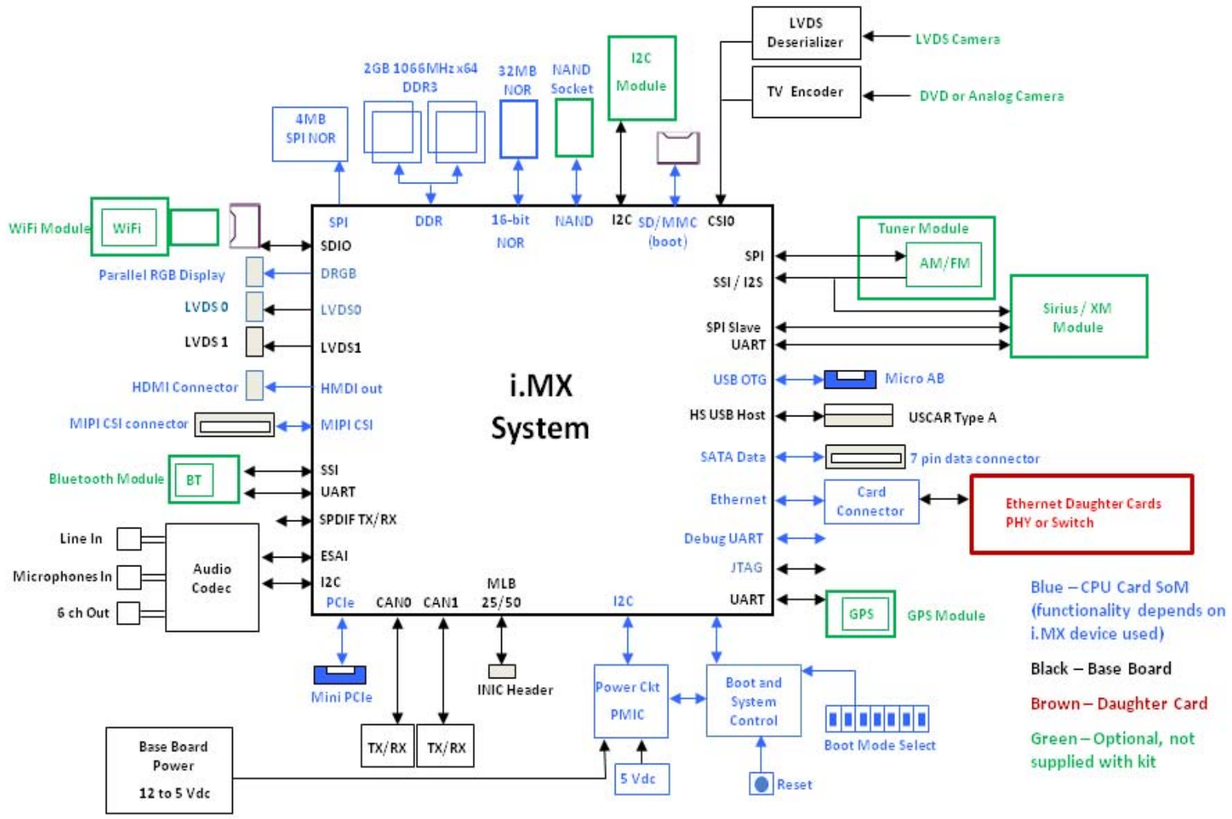
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: FIUO: PUBI: X

Designer: David B	Drawing Title: MCIMX6QAICPU2	
Drawn by: David B / Eric P	Page Title: Cover	
Approved: HW Apps Team	Size C	Document Number SCH-27925 PDF: SPF-27925 Rev F2
	Date: Monday, March 30, 2015	Sheet 1 of 24

Block Diagram



Blue – CPU Card SoM (functionality depends on i.MX device used)

Black – Base Board

Brown – Daughter Card

Green – Optional, not supplied with kit

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: _X

Drawing Title: **MCIMX6QAICPU2**

Page Title: **Block Diagram**

Size	Document Number	Rev
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Date: Wednesday, February 25, 2015 Sheet 2 of 24

I2C2 – 50 kbps Max Bus Speed
I2C2_SDA = KEY_ROW3
I2C2_SCL = EIM_EB2

Peripheral	Location	Speed (kbps)	8-Bit Write Addresses	Default Write Address
PMIC	CPU Card	400	0x10 to 0x1E	0x10
I2C Module	Base Board	50	0x20	0x20
Terrestrial Radio AM-FM	Base Board	400	0xC0, 0xC2, 0xC4, 0xC6	0xC6
ESAI Audio CODEC	Base Board	100	0x90, 0x92, 0x94, 0x96	0x90
LVDS0 Capacitive Touch	CPU Card	100	0x82	0x82
HDMI EDID	CPU Card option	100	0xA0	Option not installed
MIPI ADI Video Card	CPU Card	400	0x40, 0x42	0x42
Ethernet Card ID "ROM" *	Daughter Card	400	16 combinations	0xD0
CS2000 (Cirrus Device)	CPU Card	100	0x9C, 0x9E	0x9C

I2C3 – 400 kbps Max Bus Speed
I2C3_SDA = EIM_D18
I2C3_SCL = GPIO_3

Peripheral	Location	Speed (kbps)	8-Bit Write Addresses	Default Write Address
MOST (MLB)	Base Board	400	0x40	0x40
Port Expander A	CPU Card	400	56 combinations	0x60
Port Expander B	CPU Card	400	56 combinations	0x64
Port Expander C	CPU Card	400	56 combinations	0x68
Analog In via Video ADC	Base Board	400	0x40, 0x42	0x42
Ambient Light Sensor	Base Board	400	0x88	0x88
Compass	Base Board	400	0x1C	0x1C
Accelerometer	Base Board	400	0x3A, 0x38	0x38
RGB LCD Resistive Touch	CPU Card option	3400	0x90	Option not installed

* Ethernet Daughter Card Identification

0000 = Atheros PHY - RGMII
0001 = Broadcom PHY - RGMII
0010 = Broadcom PHY - MII (not compatible with MX6 CPU2)
0011 = Broadcom Switch - RGMII
0100 = SMSC PHY - RMII (not compatible with MX6 CPU2)

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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: MCIMX6QAICPU2

Page Title: Notes - I2C

Size	Document Number	Rev
C	SCH-27925 PDF: SPF-27925	F1

Date: Monday, February 23, 2015 Sheet 3 of 24

Boot Config	NAND Flash 64Gb	NAND Flash 16Gb	Parallel NOR Flash	SD on CPU Card	MMC on CPU Card	SATA HDD	Serial NOR Flash
S2-1	*	*	0	*	*	0	1
S2-2	0	0	0	0	1	1	1
S2-3	X	X	0	1	1	0	0
S2-4	1	1	0	0	0	0	0
S1-1	0	0	X	*	*	*	X
S1-2	0	0	X	1	*	*	X
S1-3	0	0	X	X	*	*	X
S1-4	1	1	X	0	0	*	X
S1-5	0	0	X	1	1	*	X
S1-6	X	X	1	*	*	X	X
S1-7	X	X	0	*	*	X	X
S1-8	0	0	X	*	X	X	X
S1-9	0	0	X	*	X	X	X
S1-10	0	0	0	*	*	X	X

Notes:
1 = High Level.
0 = Low Level.
X = Don't Care.
* = Switch needs to be configured for high or low depending on the application needs. Please check reference manual for boot configuration options.

Default boot configuration = SD on CPU Card

[redacted]

See switch interconnection on sheet 10.
See the two Boot Mode switches on sheet 8.

SD Speed Selection

S1-10	S1-9	Data Rate
0	0	SDR25
0	1	SDR12
1	0	SDR50
1	1	SDR104

CPU Card Identification for Software

MX6 fuses OCOTP_GP1[15:8] = 0x77
for SABRE-AI CPU2 rev F

Controlling document = Agile DOC-01878

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ICAP Classification: FCP: ___ FIUO: PUBI: X
Drawing Title: MCIMX6QAICPU2
Page Title: Notes - Boot Config & Board ID
Size C | Document Number SCH-27925 PDF: SPF-27925 | Rev F1
Date: Monday, February 23, 2015 | Sheet 4 of 24

Main Power

When CPU Card is run standalone, all power is sourced from P5V0 (Q505 pad 5).

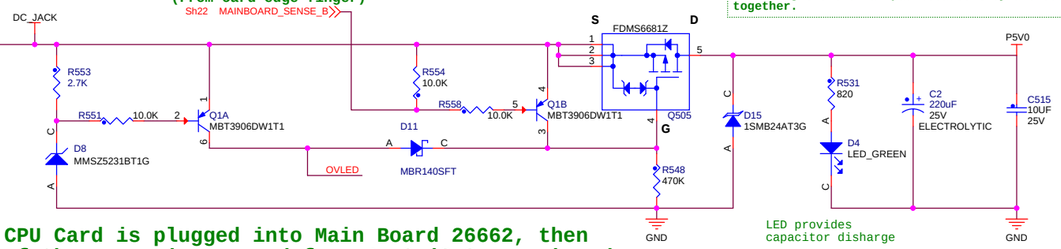
5 Vdc +/-5%
1 to 4 A typical
4.6 A estimated maximum

J8 CONN PWR 1 — DC_JACK — GND

IMPORTANT!
No fuse protection.
Use current-limited supply.

Symbol Q502 & Q505:
Base on the datasheet, FDMS6681Z is a 8-pin package with an extra thermal pad on the bottom.
Pin 5 in the symbol represents all the Drain pins including the thermal pad because they are connected together.

(From card edge finger) Sh22 MAINBOARD_SENSE_B>>



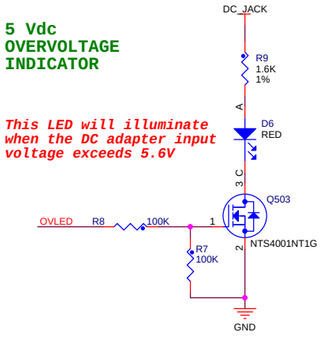
LED provides capacitor disharge

When CPU Card is plugged into Main Board 26662, then part of the power is sourced from P5V0 (2.3 A max) and part is supplied by VBAT (approx 1 A max) to avoid overloading the 5-V regulator on 26662.

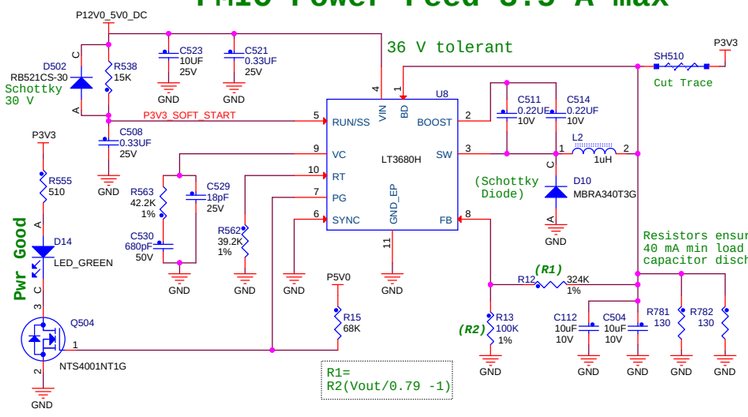
(Diode-OR to prevent backfeed from VBAT to 5V supply)

5 Vdc OVERVOLTAGE INDICATOR

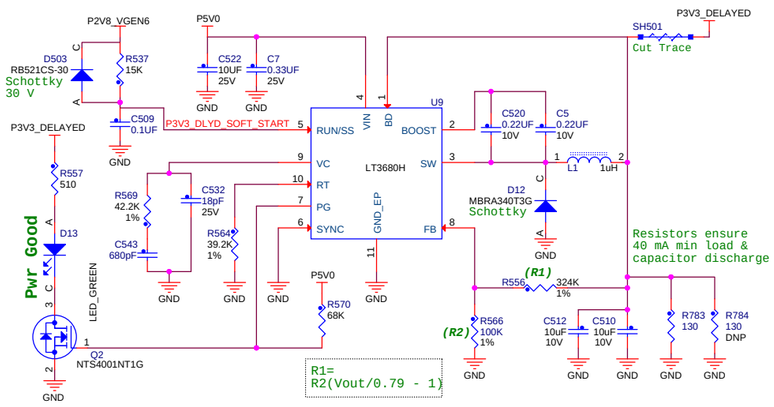
This LED will illuminate when the DC adapter input voltage exceeds 5.6V



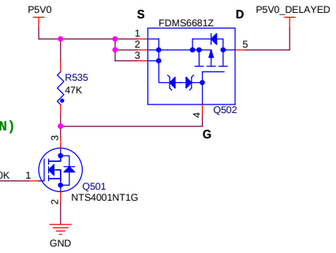
PMIC Power Feed 3.5 A max



Peripheral Power Supply 3.5 A max

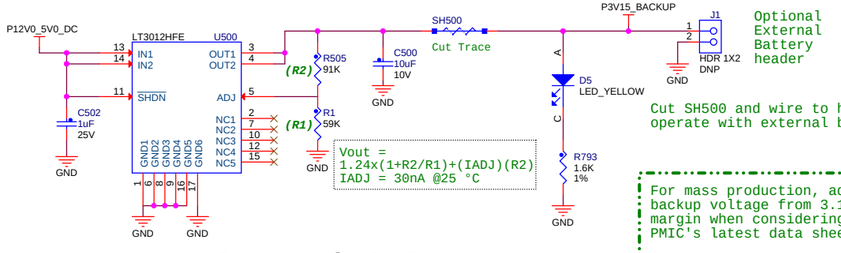


5 V delay FET



P3V3 and P3V3_DELAYED voltage is actually 3.35 V nominal for compatibilty with Main Board 26662. For customer production product, Freescale recommends R1 = 317k 1% for 3.3 V nominal.

Backup Power Supply for Real-Time Clock



3.15V @ 250mA max

For mass production, adopters should increase the backup voltage from 3.15 V to 3.20 V. This provides margin when considering both U500 tolerance and the PMIC's latest data sheet VSNVS tolerance and drop out.

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ICAP Classification: FCP: ___ FIUO: PUBI: _X

Drawing Title: **MCIMX6QAICPU2**

Page Title: **Main PWR**

Size	Document Number	Rev
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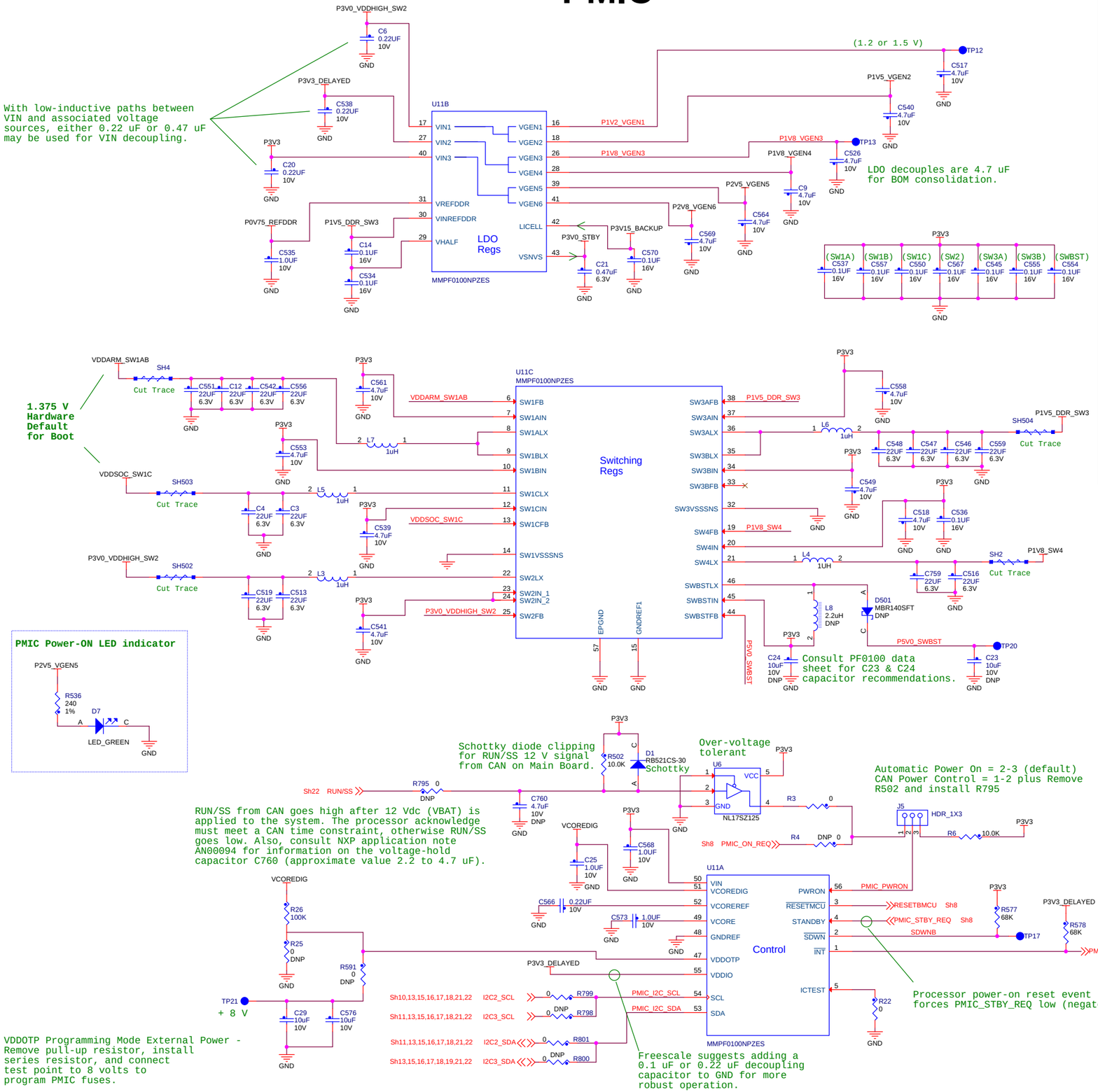
Date: Wednesday, February 25, 2015 Sheet 5 of 24

PMIC



Peripheral Power Rails

Voltage (V)	Rail Name	Block	Power Source	Generated By	Current Capability (A)
12	VBAT	MLB	Wall Supply	MB	5.5
5	P5V0_DELAYED	Para LCD	Main Power	MB or Jack	
		LVDS LCD			
		HDMI			
		MIPI			
	P5V0_OTG_VBUS	USB			0.5
	P5V0_H1_VBUS	USB	switcher	CPU	0.8
3.3	P3V3_DELAYED	NAND Flash	switcher	LT3680	3.5
		SD Card			
		NOR Flash			
		HDMI			
		LVDS LCD			
		Ethernet			
		UART			
		MIPI			
		Mini PCIE			
		MLB (MOST)			
3.0	P3V0_VDD_USB	USB	VDDUSB_CAP	iMX	-
2.8	P2V8_VGEN6	MIPI	VGEN6	PMIC	0.2
1.8	P1V8_SW4	MIPI	SW4	PMIC	1.0
	P1V8_VGEN4	SD Card	VGEN4	PMIC	0.35
1.5	P1V5_DDR_SW3	DDR	SW3A/B	PMIC	2.5
	P1V5_VGEN2	Mini PCIE	VGEN2	PMIC	0.25
1.5	ETH_VDDIO_REG	Ethernet	PHY - on-chip	AR8031	-
0.75	P0V75_REFDDR	DDR	VREFDDR	PMIC	0.01

MB = Main board 26662

PMIC Output Rails

Regulator	Voltage (V)	Power-Up Sequence	Load
VSNVS	3	0	VDD_SNVS_IN
SW1A/B	1.375	1	VDDARM_IN
SW1C	1.375	1	VDDSOC_IN
SW2	3	2	VDDHIGH_IN
VGEN2	1.5	2	mini PCIE connector
SW3A/B	1.5	3	NVCC_DRAM, NVCC_RGMII (option)
SW4	1.8	3	MIPI connector
VGEN4	1.8	3	NVCC_SD3
VGEN6	2.8	3	3V3_DELAYED enable, MIPI conn
VREFDDR	0.75	3	DRAM_VREF
VGEN5	2.5	3	Pwr LED & 5V0_DELAYED enable
SWBST	0	N/A	Not used
VGEN1	0	N/A	Not used
VGEN3	0	N/A	Not used

SW1A/B = 1.375 V for boot-up at ~800 MHz. Recommend that software increase SW1A/B to 1.425 V for 1 GHz operation.

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ICAP Classification:	FCP: ___	FIUO:	PUBI: X
Drawing Title:	MCIMX6QAICPU2		
Page Title:	PMIC		
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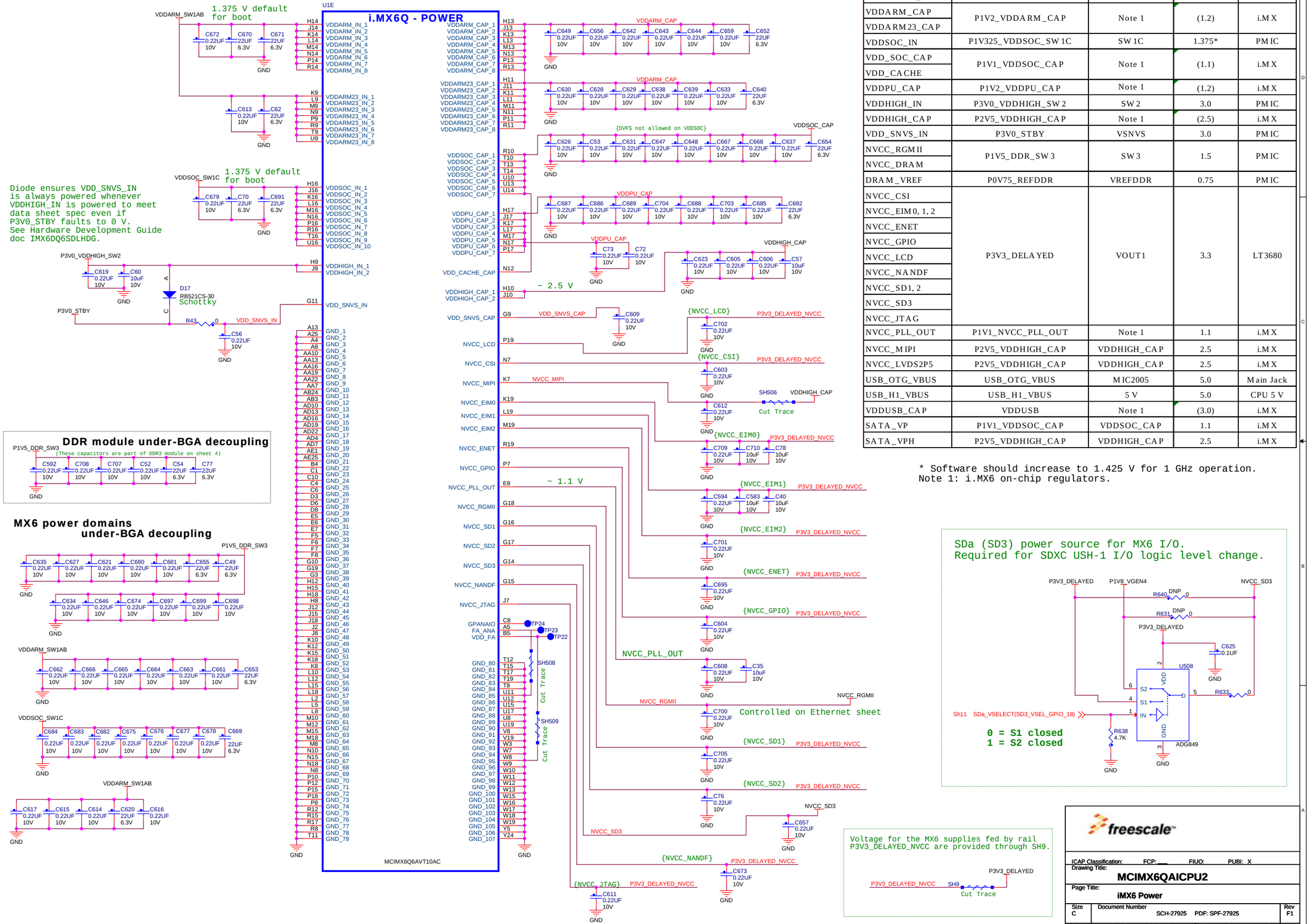
Date: Wednesday, February 25, 2015	Sheet 6 of 24		

MX6 Power



Supply Rail	Global Net	Regulator	Voltage (V)	Source
VDDARM_IN	P1V325_VDDARM_SW1AB	SW1A/B	1.375*	PMIC
VDDARM23_IN				
VDDARM_CAP	P1V2_VDDARM_CAP	Note 1	(1.2)	i.MX
VDDARM23_CAP				
VDDSOC_IN	P1V325_VDDSOC_SW1C	SW1C	1.375*	PMIC
VDD_SOC_CAP	P1V1_VDDSOC_CAP	Note 1	(1.1)	i.MX
VDD_CACHE				
VDDPU_CAP	P1V2_VDDPU_CAP	Note 1	(1.2)	i.MX
VDDHIGH_IN	P3V0_VDDHIGH_SW2	SW2	3.0	PMIC
VDDHIGH_CAP	P2V5_VDDHIGH_CAP	Note 1	(2.5)	i.MX
VDD_SNVS_IN	P3V0_STBY	VSNVS	3.0	PMIC
NVCC_RGMII	P1V5_DDR_SW3	SW3	1.5	PMIC
NVCC_DRAM				
DRAM_VREF	P0V75_REFDDR	VREFDDR	0.75	PMIC
NVCC_CSI	P3V3_DELAYED	VOUT1	3.3	LT3680
NVCC_EIM0, 1, 2				
NVCC_ENET				
NVCC_GPIO				
NVCC_LCD				
NVCC_NANDF				
NVCC_SD1, 2				
NVCC_SD3				
NVCC_JTAG				
NVCC_PLL_OUT	P1V1_NVCC_PLL_OUT	Note 1	1.1	i.MX
NVCC_MIPI	P2V5_VDDHIGH_CAP	VDDHIGH_CAP	2.5	i.MX
NVCC_LVDS2P5	P2V5_VDDHIGH_CAP	VDDHIGH_CAP	2.5	i.MX
USB_OTG_VBUS	USB_OTG_VBUS	MIC2005	5.0	Main Jack
USB_H1_VBUS	USB_H1_VBUS	5 V	5.0	CPU 5 V
VDDUSB_CAP	VDDUSB	Note 1	(3.0)	i.MX
SATA_VP	P1V1_VDDSOC_CAP	VDDSOC_CAP	1.1	i.MX
SATA_VPH	P2V5_VDDHIGH_CAP	VDDHIGH_CAP	2.5	i.MX

* Software should increase to 1.425 V for 1 GHz operation.
Note 1: i.MX6 on-chip regulators.

SDa (SD3) power source for MX6 I/O.
Required for SDXC USH-1 I/O logic level change.

Voltage for the MX6 supplies fed by rail P3V3_DELAYED_NVCC are provided through SH9.

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ICAP Classification:	FCP: ___ FIUO: PUBI: X
Drawing Title:	MCIMX6QAICPU2
Page Title:	iMX6 Power
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MX6 Control

CPU Cold Reset

Three sources (wired-OR):
Pushbutton SW1,
JTAG, and PMIC

Forces Reboot

22 kohm pull-up resistor on Base Board also

210 ms negative pulse

1.5 ms negative pulse

{2.3V Threshold}
{1.5 ms delay}
{Open Drain}

Effective pull-up resistance on MX_POR_B is approx 60 kohm due to the MX6 on-chip 100 kohm pull-up resistor.

{From PMIC}

{Wired OR}

Level Shifter
(Sink only)

(Over-voltage tolerant)

5V powers the Voltage Supervisor initially but does not allow it to reach the threshold. The 3.3V power is the final voltage in the power sequence. This will trip the threshold and begin the time-out for POR release.

JTAG Adapter Board Connector

Adapter with cable supplied with kit

{I/O Ref}

J17 slot on pin 1 side

MX6 has on-chip pull-up on TCK.

Wired OR

When Tamper is used in an end product, instead of a connection to the standby voltage sourced from the vehicle battery, a dedicated coin cell could be employed for security.

Boot Mode
Tamper
SPI NOR Write Protect

BOOT_MODE[1:0] SETTINGS
00 = Fuses
01 = Serial downloader
10 = Internal (development)
11 = Reserved

SW4/5: OFF = SPI WriteProtect Enabled

(These 3 resistors are DNP due to on-chip Pull-down on MX6)

Note 1

HEATSINK

Freescale P/N: 901-76751

Manufacturer: CTS
CTS P/N: APF19-19-13CB/A01
Description:
HW ACCESSORY,
HEATSINK FORGED
W/ADHESIVE TAPE,
0.748"L X 0.748"W X 0.5"H

R788 = bias resistor.
See Chip Errata doc IMX6DQCE.

Platform Clocks

100-ohm differential pair

Input if External Oscillator is used.

Layout: Put 100ohm resistors on top side.

100-ohm differential pairs

2.5 V Signal Level

3.3 V Signal Level

Level Shifter
Over-voltage tolerant

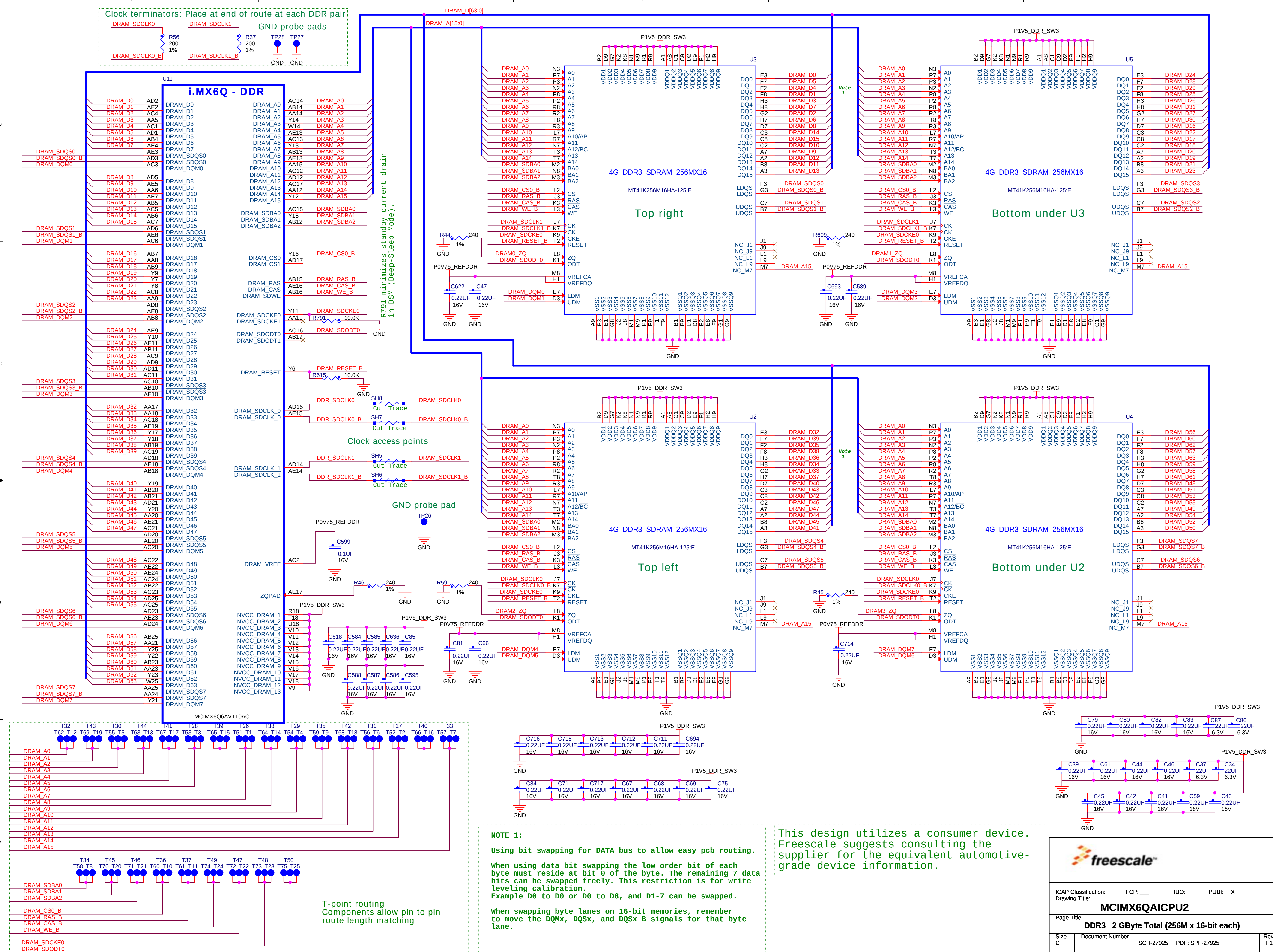
Peripheral Reset

For peripherals on CPU Card only
Two sources: Pushbutton SW2 or I/O port expander A.

RC = 68 ms
C761 provided to adjust peripheral power-up reset time out.

1. Designers should calculate the maximum current drawn from the P3V0_STBY rail for their application at hot temperature. For applications exceeding 400 uA, MX6 VDD_SNVS_IN can be directly powered by P3V0_VDDHIGH_SW2 or other 3 V source. The PF100 PMIC is limited to 400 uA. See the data sheets.

ICAP Classification:	FCP: ___	FIUO:	PUBI: X
Drawing Title:	MCIMX6QAICPU2		
Page Title:	MX6 Control, POR-RST, JTAG		
Size: C	Document Number: SCH-27925 PDF: SPF-27925		Rev: F1
Date: Monday, February 23, 2015	Sheet 8 of 24		



NOTE 1:

Using bit swapping for DATA bus to allow easy pcb routing.

When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.

This design utilizes a consumer device. Freescale suggests consulting the supplier for the equivalent automotive-grade device information.

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX6QAICPU2

Page Title: DDR3 2 GByte Total (256M x 16-bit each)

Size	Document Number		Rev
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Parallel & Serial NOR FLASH, BOOT Select

U1A

i.MX6Q - EIM

NVCC_EIM1: EIM_LBA, EIM_OE, EIM_RW, EIM_CS0, EIM_CS1, EIM_A16, EIM_A17, EIM_A18, EIM_A19, EIM_A20, EIM_A21, EIM_A22, EIM_A23, EIM_A24, EIM_A25

NVCC_EIM0: EIM_D16, EIM_D17, EIM_D18, EIM_D19, EIM_D20, EIM_D21, EIM_D22, EIM_D23, EIM_D24, EIM_D25, EIM_D26, EIM_D27, EIM_D28, EIM_D29, EIM_D30, EIM_D31, EIM_EB2, EIM_EB3, EIM_BCLK, EIM_WAIT, EIM_EB0, EIM_EB1

NVCC_EIM2: EIM_DA0, EIM_DA1, EIM_DA2, EIM_DA3, EIM_DA4, EIM_DA5, EIM_DA6, EIM_DA7, EIM_DA8, EIM_DA9, EIM_DA10, EIM_DA11, EIM_DA12, EIM_DA13, EIM_DA14, EIM_DA15

MCIMX6Q6AVT10AC

K22 EIM_LBA — EIM_LBA — R688 0 — GPS_INT_B(EIM_LBA_GPIO2_27) Sh22

J24 EIM_OE_B

K20 EIM_WE_B

H24 NOR_CE_B(EIM_CS0)

J23 — MLB_PWRDN(EIM_CS1_GPIO2_24) Sh22

SH507 Cut Trace — EIMD18_I2C3_STEER(EIM_A24) Sh19

H19 EIM_A25 — R657 0 — HDMI_CEC(EIM_A25) Sh13

C25 EIM_D16 — EIM_D16 — EIM_D16 Sh15 **ENET SPI**

F21 EIM_D17 — EIM_D17 — EIM_D17 Sh15 **ENET SPI**

D24 — EIM_D18 Sh19

G21 EIM_D19

G20 EIM_D20

H20 EIM_D21

E23 EIM_D22

D25 EIM_D23

F22 EIM_D24

G22 EIM_D25

E24 EIM_D26

E25 EIM_D27

G23 EIM_D28

J19 EIM_D29

J20 — EIM_D30 Sh19

H21 EIM_D31

Muxed flash data and I2C3_SDA

Muxed flash data and UART3_CTS

E22 EIM_EB2

F23 EIM_EB3

N22 EIM_BCLK — R674_DNP 0 — ACCEL_INT1_B(EIM_BCLK_GPIO6_31) Sh22 — ACCEL_INT2_B(EIM_BCLK_ GPIO6_31) Sh22

M25 EIM_WAIT

K21 EIM_EB0

K23 EIM_EB1

L20 EIM_DA0

J25 EIM_DA1

L21 EIM_DA2

K24 EIM_DA3

L22 EIM_DA4

L23 EIM_DA5

K25 EIM_DA6

L25 EIM_DA7

L24 EIM_DA8

M21 EIM_DA9

M22 EIM_DA10

M20 EIM_DA11

M24 EIM_DA12

M23 EIM_DA13

N23 EIM_DA14

N24 EIM_DA15

P3V3_DELAYED — R53 4.7K — I2C2_SCL Sh6,13,15,16,17,18,21,22

I2C2 Clock

(Associated data on sheet 11)

EIM_WAIT — R684 0 — USB_HOST1_OC_B(EIM_WAIT_GPIO5_0) Sh22

EIM_EB0 — R63 0 — TOUCH_INT_B(EIM_EB0_ GPIO2_GPIO[28]) Sh16

EIM_EB1 — R668 0 — COMPASS_INT(EIM_EB1_GPIO2_29) Sh22

P3V3_DELAYED — U516 — R703 0 — NC7SP126 — R107 68K — GND

Hi-Z_FOR_BOOT_B Sh8,16,22

UART3_RTS(EIM_EB3) Sh22

Ensures high-Z at boot-up to allow development boot configuration.

Option shown on sheet 11.

P3V3_DELAYED — R602 68K — Sh11 WDOG1_B — U21 NC7SP125P5X — C742 0.1UF 16V — GND

P3V3_DELAYED — C725 0.1UF 16V — C733 0.1UF 16V — GND

P3V3_DELAYED — R721 10.0K — R719 10.0K DNP — GND

NOR_WP_B/ACC

32 MB Parallel NOR Flash

NOR Flash is bottom boot-block uniform (32Kword).
NOR Flash is sized for bootloaders, kernel images, and/or nonvolatile configuration/data storage.

U510 — **FLASH TSOP56 14X20MM** — M29W256GL7AN6E

EIM_DA0 EIM_DA1 EIM_DA2 EIM_DA3 EIM_DA4 EIM_DA5 EIM_DA6 EIM_DA7 EIM_DA8 EIM_DA9 EIM_DA10 EIM_DA11 EIM_DA12 EIM_DA13 EIM_A16 EIM_A17 EIM_A18 EIM_A19 EIM_A20 EIM_A21 EIM_A22 EIM_A23 → A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23

VCCQ VCC VPP/WP

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15/A-1 → EIM_D16 EIM_D17 EIM_D18_STEERED Sh15,19 EIM_D19 EIM_D20 EIM_D21 EIM_D22 EIM_D23 EIM_D24 EIM_D25 EIM_D26 EIM_D27 EIM_D28 EIM_D29 EIM_D30_STEERED Sh19 EIM_D31

NC30 NC28 NC27 NC55 NC56

EIM_OE_B — G

EIM_WE_B — W

NOR_BYTE_B/WORD — BYTE

RP

E

R/B — NOR_RDY_BSY_B — TP36

VSS1 VSS2

P3V3_DELAYED — R739 10.0K — BYTE_B/WORD: 1 = 16-bit mode, 0 = 8-bit mode

Sh8 POR_3V3_B — Wired OR

P3V3_DELAYED — R104 150K — NOR_CE_B(EIM_CS0)

Effective pull-up resistance on NOR_CE_B(EIM_CS0) is approx 60 kohm due to the MX6 on-chip 100 kohm pull-up resistor.

Adopters should consider that U16 M25P32 may be EOL (end of life) in 2016.

4 MB SPI NOR Flash

Port = eCSPI1

Kernal and/or Boot Loader Storage

P3V3_DELAYED — C720 4.7uF 10V — C722 0.1UF 16V — GND

U16 — VCC D C S W/VPP HOLD VSS — Q — M25P32-VMW3TGB

ENET SPI — EIM_D18_STEERED — R715 0 — SPI_NOR_DIN

EIM_D16 — R711 0 — SPI_NOR_CLK

SPI_NOR_CS_B

SPI_NOR_WP_B

SPI_NOR_DOUT — R709 0 — ENET SPI EIM_D17

SPI_NOR_RST_B — R708 10.0K

P3V3_DELAYED — R702 10.0K

EIM_D19 — 74LCX125 — U512B — NOR_CS_B — R697 33 — SS1

Vih = 2.0 V

Sh11,22 BOOT_COMPLETE(SD2_DAT1_GPIO1_14) — J3 HDR_1X3 — P3V3_DELAYED — R736 4.7K — GND

Sh8 SPI_NOR_WP_B

See Control sheet for write protect switch info

Jumper Boot Selection
1 - 2 Do not boot from SPI NOR (default)
2 - 3 Boot from SPI NOR

If SPI NOR is not utilized, BOOT_COMPLETE can be used as a GPIO on either the CPU Card or Main board by installing the jumper 1 - 2 and wiring to jumper pin 3. The signal is also routed to a card edge finger.

To allow SPI NOR boot when plugged into Base Board 26662:
Base Board rev B (green): Remove R193 on Base Board
Base Board rev E (orange): No changes

Boot Configuration Select

Switch mapping with the configuration options is described on the Notes page of the schematics.

P3V3_DELAYED — NVCC_EIM2 — NVCC_EIM1 — NVCC_EIM0

R517 can be 0 ohms.

R517 120 — R525 DNP 0 — R524 DNP 0 — R522 DNP 0 — R521 DNP 0

S1 — SW_DIP-10/SM — R539 DNP 0 — R542 DNP 0 — R520 DNP 0 — R543 DNP 0 — R523 DNP 0 — R528 DNP 0 — R527 DNP 0 — R526 0 — R544 0 — R545 DNP 0 — R546 DNP 0 — R540 DNP 0 — R523 0

S2 — SW DIP-4

Bus Isolation Resistors

RN501 10K — BT_CFG1_0 R667 4.7K EIM_DA0 … BT_CFG1_7 R55 4.7K EIM_DA7

RN500 10K — BT_CFG2_0 R66 4.7K EIM_DA8 … BT_CFG2_7 R61 4.7K EIM_DA15

RN502 10K — BT_CFG3_0 R74 4.7K EIM_A16 … BT_CFG3_7 R694 4.7K EIM_A23

RN503 10K — BT_CFG4_0 R60 4.7K EIM_A24 … BT_CFG4_7 R699 4.7K EIM_EB3

DNP

GND

To avoid resistor divider with R53 I2C pull-up, R666 is DNP.

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ICAP Classification:	FCP: ___	FIUO:	PUBI: X
Drawing Title:	MCIMX6QAICPU2		
Page Title:	NOR FLASH, BOOT_SEL		
Size: C	Document Number: SCH-27925 PDF: SPF-27925		Rev: F1
Date: Tuesday, February 24, 2015		Sheet 10 of 24	

NAND FLASH, MLB, SD-MMC, CAN

U1B

i.MX6Q

MCIMX6Q6AVT10AC

NVCC_SD1

Sh22 SDb_CMD	B21	SD1_CMD
Sh22 SDb_CLK	D20	SD1_CLK
Sh22 SDb_DAT0	A21	SD1_DAT0
Sh22 SDb_DAT1	C20	SD1_DAT1
Sh22 SDb_DAT2	E19	SD1_DAT2
Sh22 SDb_DAT3	F18	SD1_DAT3

NVCC_SD2

Sh22 HOME_(SD2_CMD_ GPIO1_11)	F19	SD2_CMD
Sh22 ESAI_INT(SD2_CLK_GPIO1_10)	C21	SD2_CLK
Sh18 I2CPORTEXP_RST_B(SD2_DAT0_GPIO1_15)	A22	SD2_DAT0
Sh10,22 BOOT_COMPLETE(SD2_DAT1_GPIO1_14)	E20	SD2_DAT1
SDa_WP(SD2_DAT2_GPIO1_13)	A23	SD2_DAT2
Sh22 BACK_(SD2_DAT3_ GPIO1_12)	B22	SD2_DAT3

NVCC_SD3

SDa_CMD(SD3_CMD)	B13	SD3_CMD
SDa_CLK(SD3_CLK)	D14	SD3_CLK
SDa_DAT0(SD3_DAT0)	E14	SD3_DAT0
SDa_DAT1(SD3_DAT1)	F14	SD3_DAT1
SDa_DAT2(SD3_DAT2)	A15	SD3_DAT2
SDa_DAT3(SD3_DAT3)	B15	SD3_DAT3
SDa_DAT4(SD3_DAT4)	D13	SD3_DAT4
SDa_DAT5(SD3_DAT5)	C13	SD3_DAT5
SDa_DAT6(SD3_DAT6)	E13	SD3_DAT6
SDa_DAT7(SD3_DAT7)	F13	SD3_DAT7
Sh20 SDa_RST_B(SD3_RST)	D15	SD3_RST

Reset is active low.

VDDHIGH_CAP

B11	MLB_CP	
A11	MLB_CN	
B9	MLB_SP	
A9	MLB_SN	
A10	MLB_DP	
B10	MLB_DN	

NVCC_ENET

V20	ENET_MDC	ESAI_TX5_RX0(ENET_MDC) Sh22
V23	ENET_MDIO	ESAI_SCKR(ENET_MDIO) Sh22
U21	ENET_CRS_DV	ESAI_SCKT(ENET_CRS_DIV) Sh22
V22	ENET_REF_CLK	RGMII_CLK(ENET_REF_CLK)
W23	ENET_RX_ER	USB_OTG_ID(ENET_RX_ER) Sh12,21 **AVB Signal, sh 21**
V21	ENET_TX_EN	ESAI_TX3_RX2(ENET_TX_EN) Sh22
W21	ENET_RXD0	VIDEO_ADC_INT_B(ENET_RXD0_GPIO1_27) Sh22
W22	ENET_RXD1	ESAI_FST(ENET_RXD1) Sh22
U20	ENET_TXD0	ESAI_TX4_RX1(ENET_TXD0) Sh22
W20	ENET_TXD1	AVB_MLBCLK(ENET_TXD1) Sh21 **AVB Signal, sh 21**

DNP
R108 Ra 0 — ENET_REF_CLK Sh15 — From ENET Daughter Card
R109 Rb 0 — RGMII_REF_CLK(GPIO_16) — From MX6

Use of GPIO_16 as a clock source eliminates the need for 125 MHz external oscillator on the ENET Daughter Cards See note 1.

P3V3_DELAYED
R91 1.6K 1%
ENET_MDIO(KEY_COL1) Sh15

NVCC_GPIO

W5	KEY_COL0	UART4_TXD(KEY_COL0) Sh20
V6	KEY_ROW0	UART4_RXD(KEY_ROW0) Sh20
U7	KEY_COL1	
U6	KEY_ROW1	MLB_INT_B(KEY_ROW1) Sh15,22 **ENET SPI**
W6	KEY_COL2	ENET_CAN1_IO(KEY_COL2) Sh19
W4	KEY_ROW2	CAN1_RXCAN(KEY_ROW2) Sh22
U5	KEY_COL3	MAINBOARD_SPDIF_IN(KEY_COL3) Sh22
T7	KEY_ROW3	
T6	KEY_COL4	CAN2_TXCAN(KEY_COL4) Sh22
V5	KEY_ROW4	CAN2_RXCAN(KEY_ROW4) Sh22

P3V3_DELAYED — **I2C2 Data**
R19 4.7K
(Associated clk on sheet 10)
I2C2_SDA Sh6,13,15,16,17,18,21,22

P3V3_DELAYED — **I2C3 Clock**
R23 4.7K
(Associated data on sheet 19)
I2C3_SCL Sh6,13,15,16,17,18,21,22

T5	GPIO_0	GPS_32_kHz(CLKO_GPIO_0) Sh22
T4	GPIO_1	SDb_CD(GPIO_1) Sh22
T1	GPIO_2	GPIO_2 Sh21
R7	GPIO_3	
R6	GPIO_4	CAN1_NERR_B(GPIO_4_GPIO1_4) Sh22
R4	GPIO_5	ESAI_TX2_RX3(GPIO_5) Sh22
T3	GPIO_6	GPIO_6 Sh21
R3	GPIO_7	UART2_TXD(GPIO_7) Sh19
R5	GPIO_8	UART2_RXD(GPIO_8) Sh19
T2	GPIO_9	GPIO_9
R2	GPIO_16	RGMII_REF_CLK(GPIO_16)
R1	GPIO_17	
P6	GPIO_18	ESAI_TX0(GPIO_17) Sh22
P5	GPIO_19	SDa_VSELECT(SD3_VSEL_GPIO_18) Sh7
		GPIO_19 Sh21 **AVB Signal, sh 21**

NVCC_NANDF

F15	NANDF_CS0	NANDF_CE0_B	R680 0 SDa_CD_B(GPIO6_15)
C16	NANDF_CS1	NANDF_CE1_B	
A17	NANDF_CS2	NANDF_CS2_B	
D16	NANDF_CS3	NANDF_CE3_B	R49 0 ESAI_TX1(NANDF_CS3) Sh22
A16	NANDF_ALE	NANDF_ALE	
C15	NANDF_CLE	NANDF_CLE	
E15	NANDF_WP_B	NANDF_WP_B	
B16	NANDF_RB0	NANDF_RB0	
A18	NANDF_D0	NANDF_D0	R649 0 SDb_DAT4 Sh22
C17	NANDF_D1	NANDF_D1	R648 0 SDb_DAT5 Sh22
F16	NANDF_D2	NANDF_D2	R647 0 SDb_DAT6 Sh22
D17	NANDF_D3	NANDF_D3	R648 0 SDb_DAT7 Sh22
A19	NANDF_D4	NANDF_D4	
B18	NANDF_D5	NANDF_D5	
E17	NANDF_D6	NANDF_D6	
C18	NANDF_D7	NANDF_D7	

E16	SD4_CLK	NAND_BT_WIFI_IO(SD4_CLK) Sh19
B17	SD4_CMD	R201 0 — NAND_BT_WIFI_OUT(SD4_CMD) Sh19
D18		
B19	SD4_DAT0	USB_OTG_OC_B(SD4_DAT0_GPIO2_8) Sh12
F17	SD4_DAT1	LVDS0_PARADISP_PWM3(SD4_DAT1) Sh16,17
A20	SD4_DAT2	LVDS1_PWM4(SD4_DAT2) Sh22
E18	SD4_DAT3	CAN2_NERR_B(SD4_DAT3_GPIO2_11) Sh22
C19	SD4_DAT4	PROG_(SD4_DAT4_ GPIO2_12) Sh22
B20	SD4_DAT5	UART2_RTS(SD4_DAT5) Sh22
D19	SD4_DAT6	UART2_CTS(SD4_DAT6) Sh22
	SD4_DAT7	VOL+_(SD4_DAT7_ GPIO2_15) Sh22

Steering logic on Sheet 19

NAND Flash Socket
(TSOP48)

U19 — 980020-48-P2

P3V3_DELAYED
C737 10uF 10V
C736 0.1UF 16V
C738 0.1UF 16V
GND

NANDF_D0	29	I/O0	
NANDF_D1	30	I/O1	
NANDF_D2	31	I/O2	
NANDF_D3	32	I/O3	
NANDF_D4	41	I/O4	
NANDF_D5	42	I/O5	
NANDF_D6	43	I/O6	
NANDF_D7	44	I/O7	
NANDF_CLE	16	CLE	
NANDF_ALE	17	ALE	
NANDF_CE0_B	9	CE1n	
	8	REn	
	18	WEn	
NANDF_WP_B	19	WPn	
NANDF_RB0	7	R/B1n	
NANDF_NC48	48	NC48/GND	
	47	NC47	
	46	NC46	
	45	NC45	
	40	NC40	
	39	NC39/VCC	

12	VCC_12		
37	VCC_37		
1	NC1		
2	NC2		
3	NC3		
4	R/B4n	NANDF_RB3	R758 0
5	R/B3n	NANDF_RB2	R754 0
6	R/B2n	NANDF_RB1	R750 0
10	CE2n	NANDF_CE1_B	
11	NC11		R738 DNP 0 NANDF_CE0_B
14	CE3n	NANDF_CE3N	
15	CE4n	NANDF_CE4N	R755 DNP 0 NANDF_CS2_B
20	NC20		R729 DNP 0 NANDF_CE1_B
21	NC21		
22	NC22		R727 DNP 0 NANDF_CE3_B
23	NC23		
24	NC24		
25	NC25/GND	NANDF_NC25	R724 0 GND
26	NC26		
27	NC27		
28	NC28		
33	NC33		P3V3_DELAYED
34	NC34/VCC	NANDF_NC34	R728 0
35	NC35/DQS		
38	NC38		
13	VSS_13		
36	VSS_36		GND

Sh19 NANDF_RE_B(SD4_CMD)
Sh19 NANDF_WE_B(SD4_CLK)

P3V3_DELAYED
R762 10.0K
R760 0
GND

P3V3_DELAYED
R740 0
NANDF_NC39
R752 10.0K DNP
GND

Compatible 64 Gb NAND Flash: MT29F64G08AFAAAWP. Freescale suggests consulting supplier for automotive grade device information and/or lower density memory.

NAND FLASH is not included with shipped boards.

Sh17 DISP0_DAT8 WDOG1_B — R753 0 Ra
R604 DNP 0 Rb — WDOG1_B Sh10 — WDOG pull-up on sheet 10.
R32 0 Rc — ESAI_FSR(GPIO_9) Sh22
GPIO_9

ESAI_FSR into processor or WDOG1 out of processor

WDOG1 Options to reset parallel NOR flash
Cluster - remove Ra, install Rb, remove Rc - uses parallel NOR flash, no audio
Infotainment - install Ra, remove Rb, install Rc - with audio, no parallel LCD (default)

Freescale recommends utilizing a fixed-supply for CD and WP pull-up voltage. Pull-ups should be on the same supply rail as the associated i.MX inputs, in this case NVCC_NANDF and NVCC_SD2.

SD USH-1 & MMC

P3V3_DELAYED
NVCC_SD3
R642 10.0K DNP
R695 10.0K
R701 10.0K

SDa_DAT0(SD3_DAT0)	7	DAT0	
SDa_DAT1(SD3_DAT1)	8	DAT1	
SDa_DAT2(SD3_DAT2)	9	DAT2	
SDa_DAT3(SD3_DAT3)	1	DAT3	
SDa_DAT4(SD3_DAT4)	R636 0 SDa_4	10	DAT4
SDa_DAT5(SD3_DAT5)	R643 0 SDa_5	11	DAT5
SDa_DAT6(SD3_DAT6)	R650 0 SDa_6	12	DAT6
SDa_DAT7(SD3_DAT7)	R674 0 SDa_7	13	DAT7
SDa_CLK(SD3_CLK)		5	CLK
SDa_CMD(SD3_CMD)		2	CMD
SDa_CD_B(GPIO6_15)		14	CD
SDa_WP(SD2_DAT2_GPIO1_13)		15	WP

J14 — CONN CRD 19 SDC013-A0-501F

VDD	4	P3V3_SDa_SWITCHED
VSS1	3	
VSS2	6	
GND1	16	
GND2	17	
GND3	18	
GND4	19	

TP29
C696 10uF 10V
GND

SD, SDXC - Remove CMD pull-up resistor (default)
MMC, eMMC - Install CMD pull-up resistor

Socket handles 500 mA
SDXC = 800 mA max

SD Slot Pin Order

9
1
10
2
11
3
4
5
12
6
13
7
8
14
15

Note 1 --
Freescale strongly suggests that users validate their designs over temperature while running their system software. Noisy system conditions may dictate use of an external reference oscillator.

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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: **MCIMX6QAICPU2**

Page Title: **NAND FLASH, SD-MMC, MLB**

Size	Document Number	Rev
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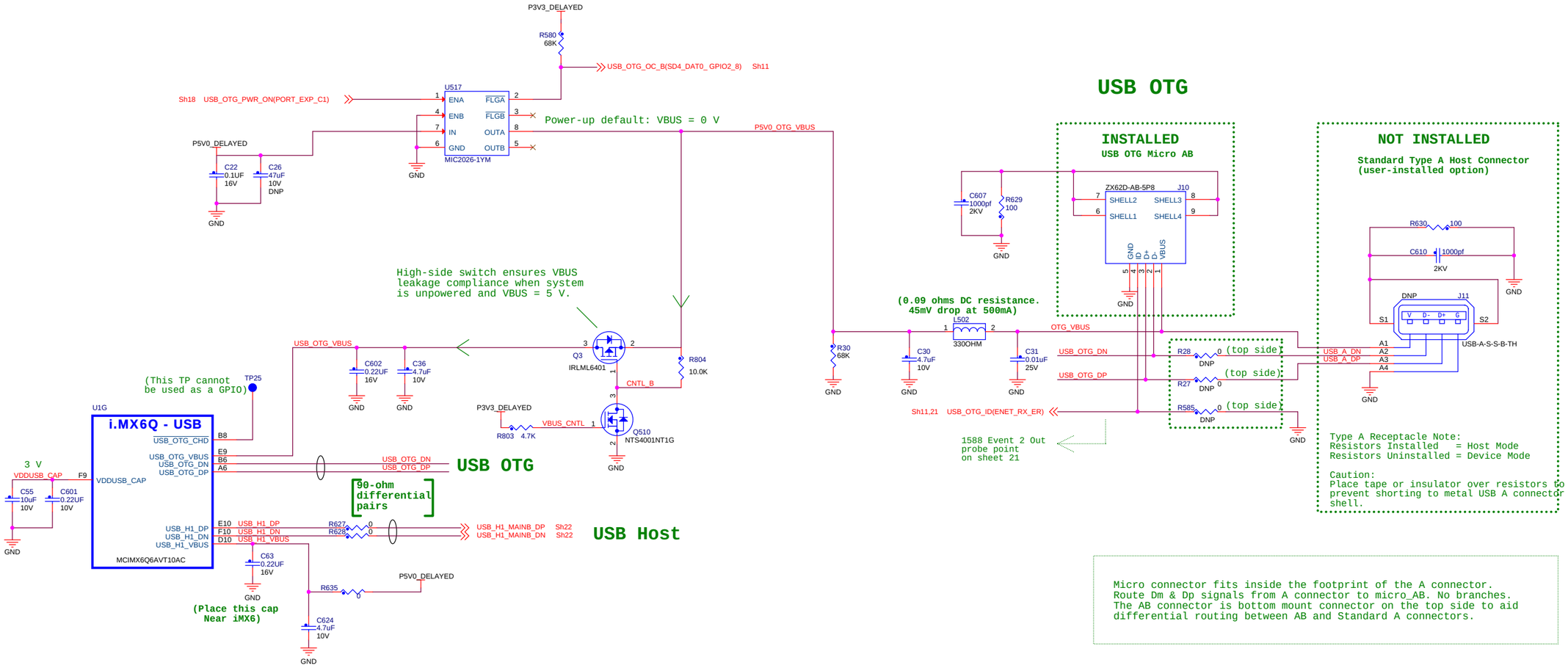
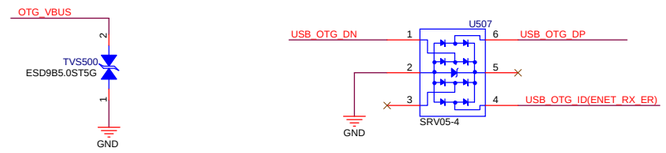
Date: Monday, February 23, 2015 Sheet 11 of 24

USB OTG/ HOST



ESD Protection



USB_OTG_ID could cause backfeed through U507 when P3V3_DELAYED is not powered up.
Therefore, pin 5 is not connected to a positive supply.

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ICAP Classification: FCP: ___ FIUO: PUBI: _X

Drawing Title: **MCIMX6QAICPU2**

Page Title: **USB**

Size	Document Number	Rev
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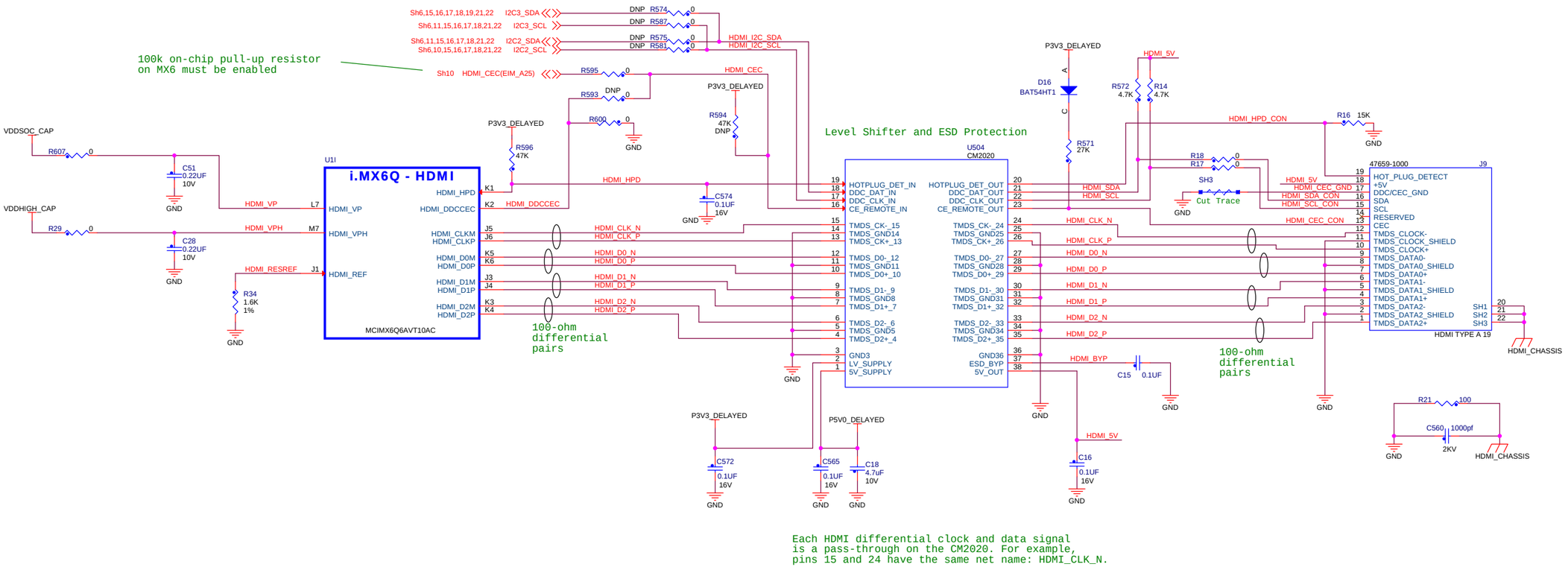
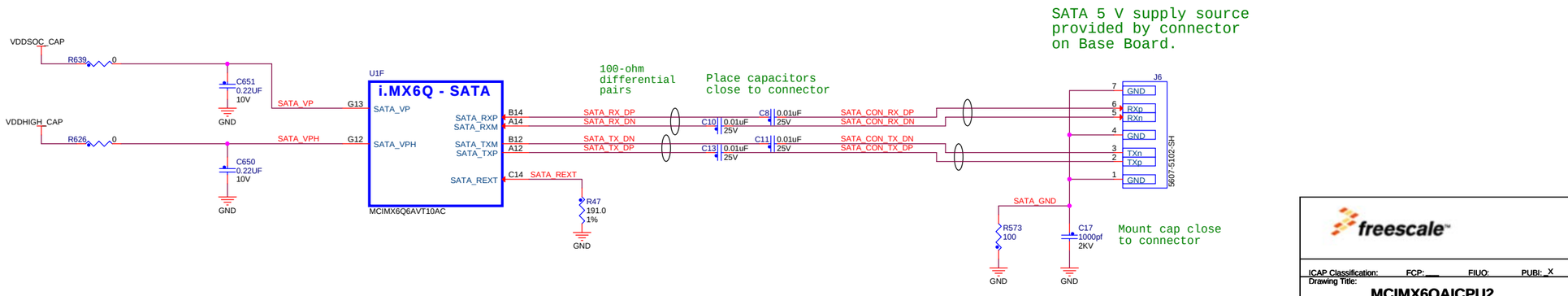
HDMI

HDMI for demonstration and prototyping; not used in vehicle.
Connecting I2C to DDC conflicts with audio.



SATA



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ICAP Classification:	FCP: ___	FIUO:	PUBI: _X
Drawing Title: MCIMX6QAICPU2			
Page Title: HDMI, SATA			
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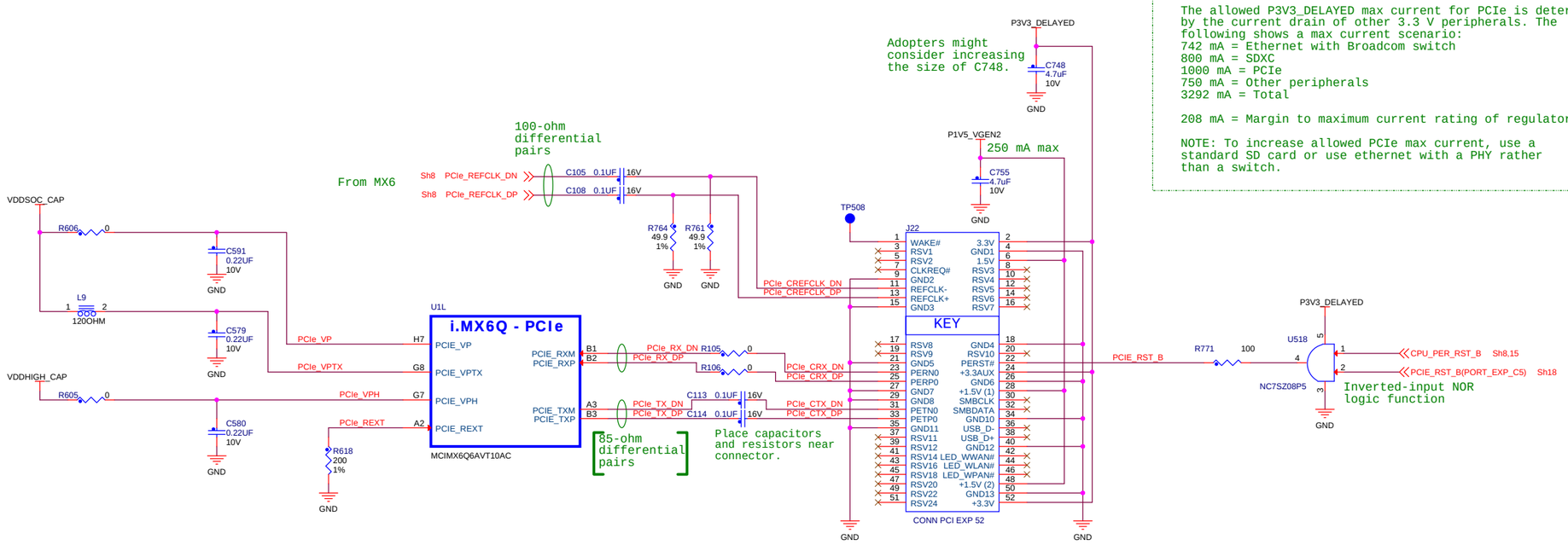
PCIE Connector

Facilitates both Mini and Half-Mini Form Factor

PCIe provided to support USB3.0.
Circuit board Tx and Rx passed PCIe 2.5G compliance test.
Reference Clock as sourced by i.MX is non-compliant.



The allowed P3V3_DELAYED max current for PCIe is determined by the current drain of other 3.3 V peripherals. The following shows a max current scenario:
742 mA = Ethernet with Broadcom switch
800 mA = SDXC
1000 mA = PCIe
750 mA = Other peripherals
3292 mA = Total

208 mA = Margin to maximum current rating of regulator

NOTE: To increase allowed PCIe max current, use a standard SD card or use ethernet with a PHY rather than a switch.

Layout considerations

TX pairs are usually routed on top layer

Length/skew compensation (trace serpentines) are not required for this Bus

Please remove ref plane under edgefinger pads

Use wide pair-to-pair spacing
(At least 5H TX vs TX and RX vs RX
use at least 7H for RX vs RX

If a mini PCIe extender is needed, adopters might consider M-Factors Storage JB-E0F0-8KNH or equivalent.

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ICAP Classification: FCP:___ FIUO: PUBI: _X

Drawing Title: MCIMX6QAICPU2

Page Title: Mini PCI Express

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Ethernet

U1K

i.MX6Q - RGMII

RGMII_TXC	D21	RGMII_TXC
RGMII_TD0	C22	RGMII_TXD0
RGMII_TD1	F20	RGMII_TXD1
RGMII_TD2	E21	RGMII_TXD2
RGMII_TD3	A24	RGMII_TXD3
RGMII_TX_CTL	C23	RGMII_TX_CTL
RGMII_RXC	B25	RGMII_RXC
RGMII_RD0	C24	RGMII_RXD0
RGMII_RD1	B23	RGMII_RXD1
RGMII_RD2	B24	RGMII_RXD2
RGMII_RD3	D23	RGMII_RXD3
RGMII_RX_CTL	D22	RGMII_RX_CTL

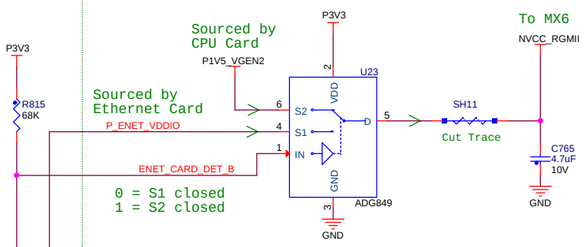
MCIMX6Q6AVT10AC

NVCC_RGMII Power Control

Ensures that NVCC_RGMII does not float if ethernet daughter card is not installed.

P3V3 powers up before other supplies

Bulk capacitor included due to remote I/O supply on Daughter Card.
Adopters with i.MX and PHY on same board do not need bulk capacitor.



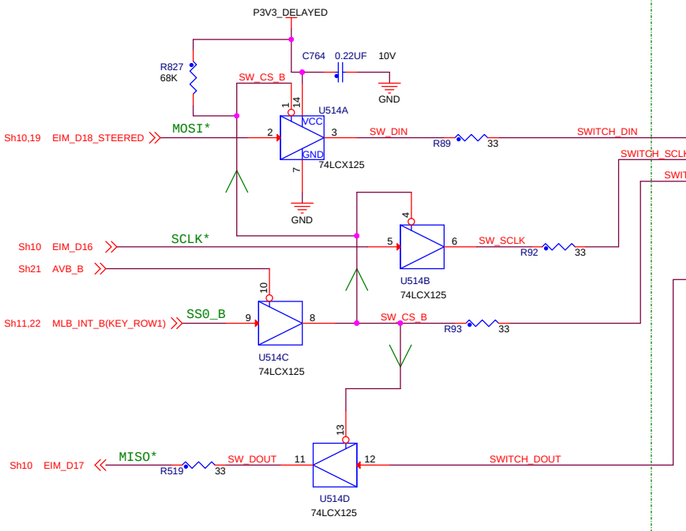
P_ETH_VDDIO_PWR Chart per Daughter Card

Atheros PHY RGMII: 1.5 or 1.8 V (default = 1.5 V)
Broadcom PHY RGMII: 2.5 V
Broadcom Switch: 2.5 V
Broadcom PHY MII: 3.3 V <-- Not used with MX6 CPU2

SPI for Switch Card Only

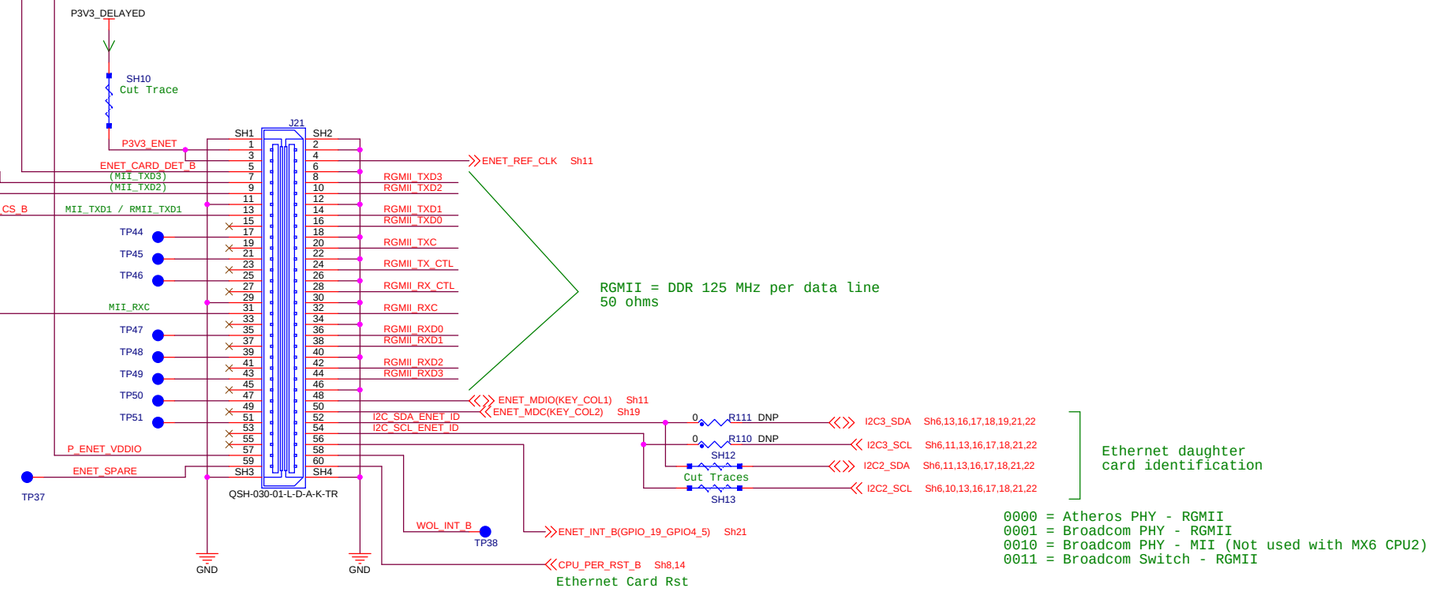
Resistor termination on switch card.
SS0-B also has clipping diode on switch card.

Avoid MLB_INT_B(KEY_ROW1) contention: do not plug card into Base Board MLB connector during ENET Switch use.



* On same bus as SPI NOR flash. Ensure SPI NOR flash select on sheet 10 not asserted when SPI accessing ENET card. Alternately, place jumper J3 on sheet 10 in position 1-2.

Connector pin assignment per Agile DOC-01898.



RGMII = DDR 125 MHz per data line
50 ohms

Ethernet daughter card identification

0000 = Atheros PHY - RGMII
0001 = Broadcom PHY - RGMII
0010 = Broadcom PHY - MII (Not used with MX6 CPU2)
0011 = Broadcom Switch - RGMII

Mating conn = Samtec QTH series

Compatible Ethernet Daughter Cards

27953 = Atheros PHY - RGMII
27954 = Broadcom PHY - RGMII
27955 = Broadcom Switch - RGMII

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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: MCIMX6QAICPU2

Page Title: Ethernet

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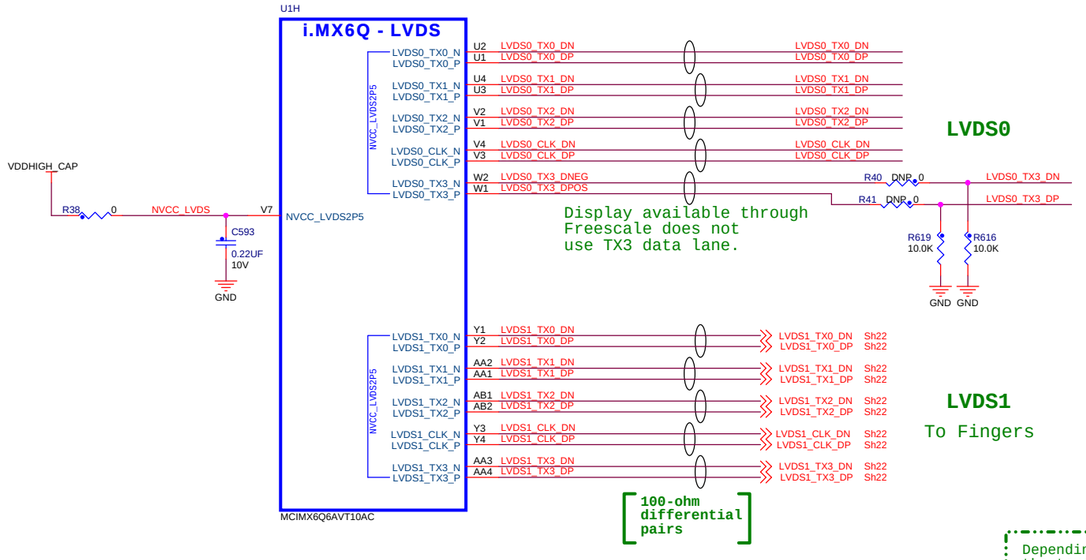
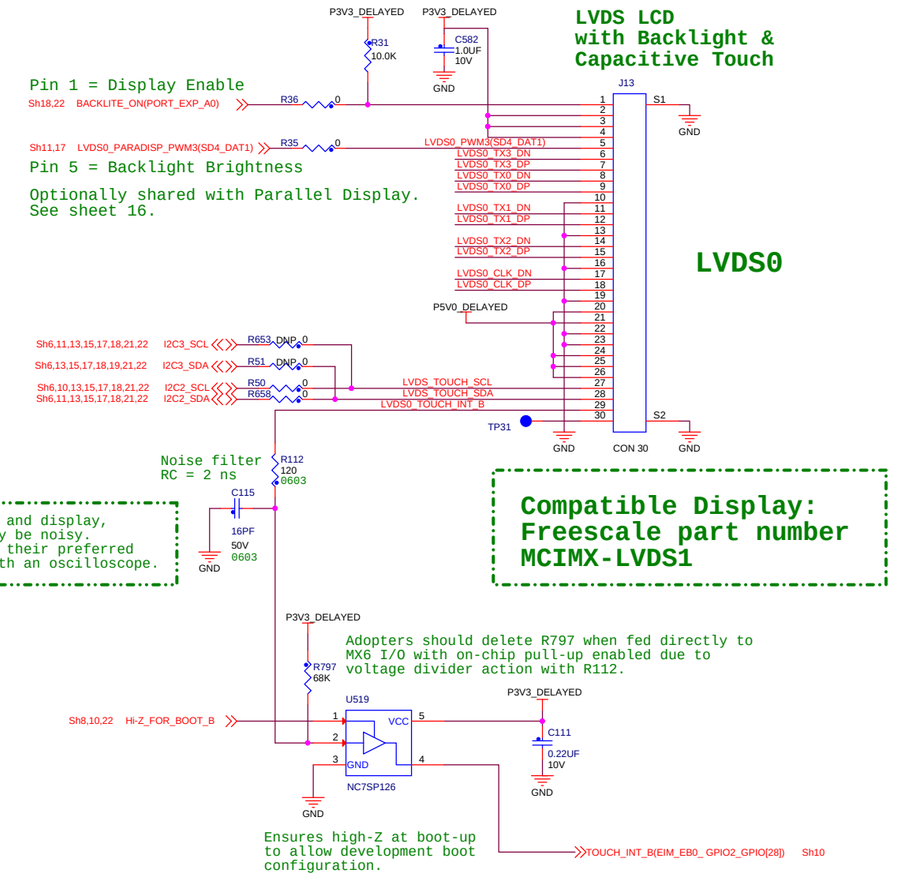
LVDS Displays



NVCC_LVDS2P5 also powers on-chip DDR I/O predrivers, and must be powered whether LVDS is used or not.



The MCIMX-LVDS1 display with touch can be placed in Sleep through the I2C port. However, INT_B must be driven with a falling edge to wake up the display, which is not allowed due to U1514.

The MCIMX-LVDS1 is not an automotive-grade display. For an automotive system, most likely the display with be placed in sleep and awakened through the I2C port. Adopters should consider their preferred display's requirements.

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ICAP Classification:	FCP: ___	FIUO:	PUBI: X
Drawing Title: MCIMX6QAICPU2			
Page Title: LVDS Displays			
Size C	Document Number SCH-27925 PDF: SPF-27925		Rev F1
Date: Tuesday, February 24, 2015	Sheet 16 of 24		

Display Connectors

MCLK sourced from MX6 to MIPI connector

Test point and resistors faciliate wiring audio over to MIPI conenctor test points.

Position A = default

CSI0_DATA_EN re-purposed as CS2000 Lock Detect for media clock recovery. See sheet 21. (WP not used for Base Board WiFi SD slot.)

i.MX6Q - DISP; CSI

MCIMX6Q6AVT10AC

100-ohm differential pairs

100-ohm differential pairs

Remove resistors if Parallel Display quality impacted by Base Board loading.

To Main Board

AVB Signal

Optionally shared with LVDS0 Display. See sheet 15.

Parallel LCD backlight control (default) with optional path to touch IRQ.
Audio not used in parallel display application.
Remove R730 if audio quality is degraded by backlight path.

For Boundary Devices LCD this is IRQ output for Touch which is not the default.

Could be used as Contrast with other LCDs.

XF2M-4015-1A OMRON CON_1X40

Parallel Display Connector

MIPI Connector

Driven from MX6

100-ohm differential pairs

100-ohm differential pairs

QSH-030-01-L-D-A-K-TR

Compatible SAMTEC cable HQCD-030-01.72-TTR-TTR-1-N

**Compatible 7" 800 x 480 LCD and software driver available from Boundary Devices.
If touch is desired, order the LCD with I2C pull-ups removed.**

Email: info@boundarydevices.com

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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: MCIMX6QAICPU2

Page Title: Parallel Display, MIPI port

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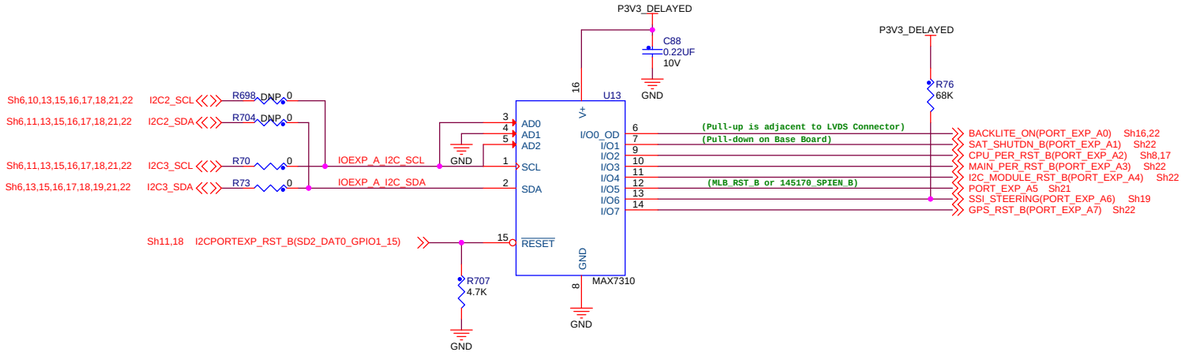
C	SCH-27925 PDF: SPF-27925	F1

Date: Tuesday, February 24, 2015 Sheet 17 of 24

I2C I/O Expanders

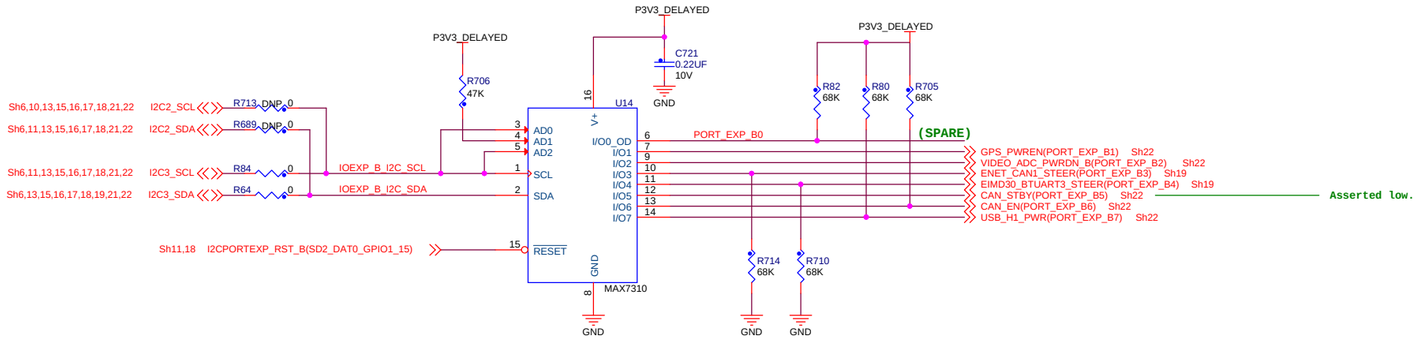
Port Expander A

7-bit Slave Addr(6:0): "0110000"



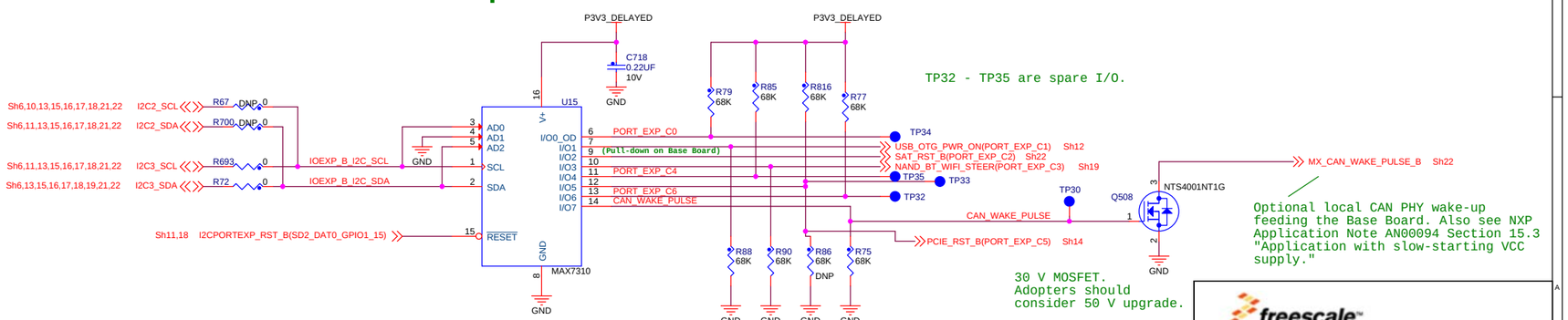
Port Expander B

7-bit Slave Addr(6:0): "0110010"



Port Expander C

7-bit Slave Addr(6:0): "0110100"



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ICAP Classification:	FCP: ___	FIUO:	PUBI: X

Drawing Title: **MCIMX6QAICPU2**

Page Title: **I2C - I/O Expanders**

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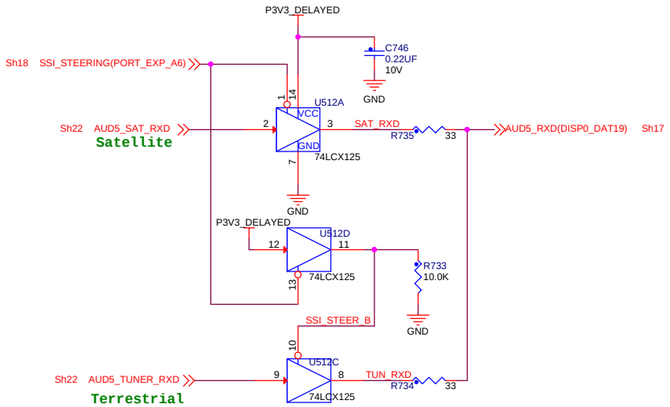
Date: Monday, February 23, 2015	Sheet 18 of 24	

Steering Logic

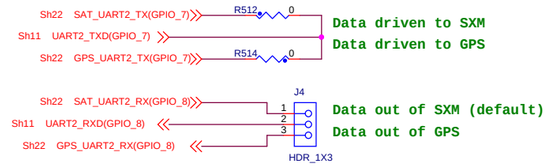
SATELLITE AND TERRESTRIAL TUNER AUDIO DATA STEERING



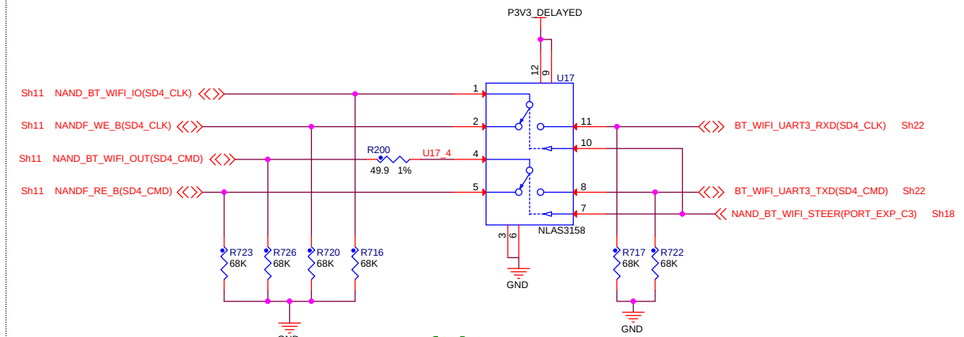
Default = Terrestrial Tuner

Steering logic required due to accommodating a superset of peripherals. For a more robust implementation, Freescale recommends adopters eliminate steering logic especially on the fast signals, since a subset of peripherals will be used in an actual application.

UART2 SHARED BETWEEN GPS AND SATELLITE



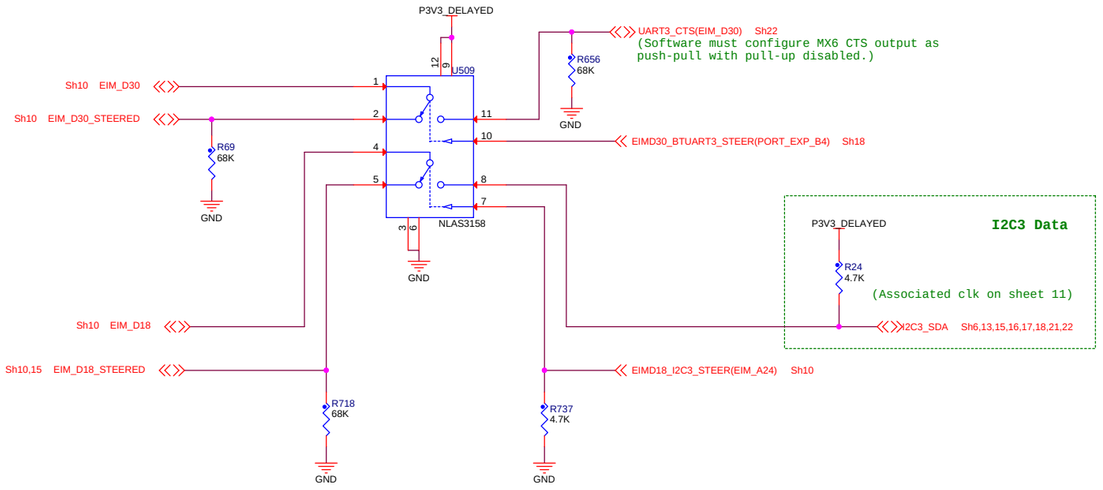
NAND FLASH AND BT_WIFI DATA STEERING



Default = NAND FLASH

R200 controls reflection on RE_B signal back to processor.

EIM, UART3, and I2C STEERING

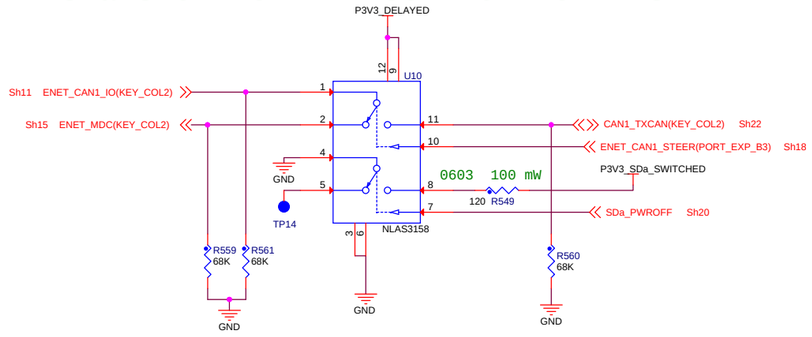


I2C3 Data

(Associated clk on sheet 11)

Default = EIM

ETHERNET AND CAN DATA STEERING SDa SLOT POWER DISCHARGE FOR RESET



Default = Ethernet

R549 is for discharge current-limiting for SDXC support. Adopters might consider 0805 for operation at temperature extremes, if their available 0603 is not rated to 100 mW.

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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: **MCIMX6QAICPU2**

Page Title: **Steering logic**

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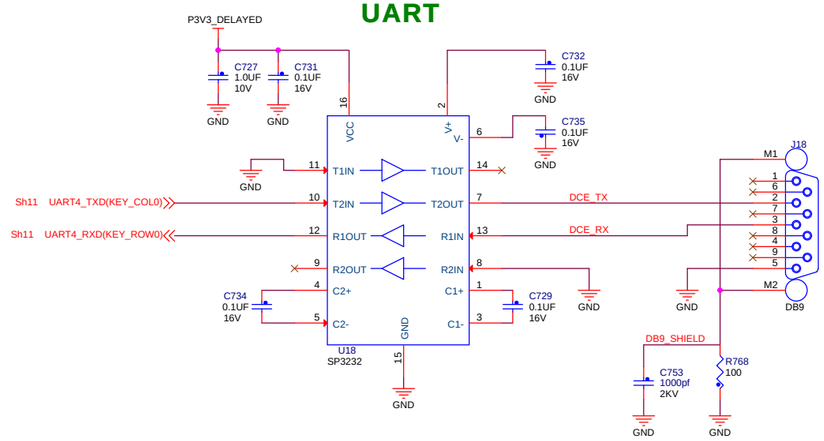
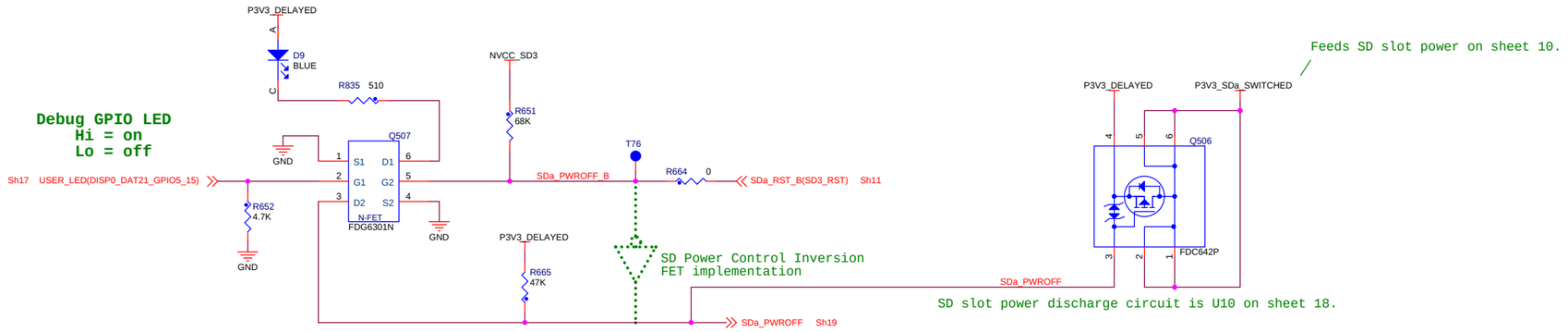
Date: Monday, February 23, 2015 Sheet 19 of 24

Debug

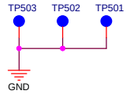
UART



Debug LED and SDXC Power Control Inverter

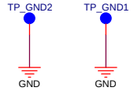


GND Loops as Mechanical Spacers



Place on bottom of board
Label as GND

Ground Test Points



Place on top of board
Label as GND

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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: **MCIMX6QAICPU2**

Page Title: **Debug UART, LED, Test Points**

Size	Document Number	Rev
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Date: Monday, February 23, 2015 Sheet 20 of 24

AVB

Block diagram on sheet 23

SPDT switches accommodate AVB or legacy (MLB) mode for development purposes. Freescale recommends adopters eliminate these switches and unused signals, since use of both AVB and legacy modes is unlikely in an actual application.

Software Notes

1. Config GPIO_19 with 100k pull-up to avoid floating.
2. Hi drive needed on SPI due to 4.7k pull-downs.

A = Pos edge trigger (default)
B = Neg edge trigger

Sh11,12 USB_OTG_ID(ENET_RX_ER) — 1588 Event 2 Out — TP41

USB OTG cable must be disconnected to monitor TP41.

Control Low = AVB Switch on / Control High = Legacy Switch off

Control Low = Listener Switch on / Control High = Head Unit Switch off

P3V3_DELAYED — U502 NLAS3158 — R818 68K

Sh11 GPIO_19 — AVB_1588_OUT0 — Sh11 GPIO_2 — 145170_SPIDATIN

ENET_INT_B(GPIO_19_GPIO4_5) Sh15

MLBDAT(GPIO_2) Sh22 — R501 68K — AVB_B

One shot required due to CS2000 min input pulse width

SH14 Cut Trace — C768 0.22UF 10V — R833 4.7K

U522 SN74LVC1G123 — 1SHOT_CLR_B — 1SHOT_B_IN — 1SHOT_A_BAR — R831 0 — R832 68K — R500 68K — C767 18pF 25V — RC

200 ns — 8 ns — 1SHOT_OUT — R203 0 — A = default

P3V3_DELAYED — U503 NLAS3158

Sh18 PORT_EXP_A5 — 145170_SPIEN_B — Sh11 GPIO_6 — 145170_SPICLK

MLB_RST_B(PORT_EXP_A5) Sh22 — Termination on Base Board

MLBSIG(GPIO_6) Sh22 — R510 68K

1588_OUT0 — Sh17 DISP0_DAT17_AVB_SDMA1 — U511_2_4

P3V3_DELAYED — U511 NLAS3158 — R513 68K — DISP0_DAT17 Sh17 — AVB_B — LISTENER_B

Listener = 1588 Out 0
Head = 145170

AVB_SDMA_IN1_1588_IN0

P3V3_DELAYED — U506 NLAS3158

Sh11 AVB_MLBCLK(ENET_TXD1) — AVB_SDMA_IN1_1588_IN0 — Sh8,22 AUDIO_REF_24MHZ — SYNCED_AUDIO_24MHZ

MLBCLK(ENET_TXD1) Sh22 — R511 68K

Listener = Recovered Clk
Head = Local Osc

LISTENER_B — AVB_B — LOCAL_AUDIO_24MHZ

P3V3_DELAYED — R87 68K — AVB_B Sh15

To ENET SPI Control

SW3 97C02ST

Local Oscillator, CS2000 Clock Synthesizer, & MLE145170 Configured as Programmable Divider

P3V3_DELAYED — C766 0.22UF 10V

P3V3_DELAYED — SYNTH_VDD — L501 120OHM — C32 0.1UF 16V — C27 1.0UF 10V

LISTENER_B — U521 NC7SZ125L6X — SYNTH_24MHZ_BUF — R826 0

Sh6,11,13,15,16,17,18,22 I2C2_SDA — R33 0
Sh6,10,13,15,16,17,18,22 I2C2_SCL — R5 0
Sh6,13,15,16,17,18,19,22 I2C3_SDA — R42 0 DNP
Sh6,11,13,15,16,17,18,22 I2C3_SCL — R39 0 DNP

SYNTH_SCL — SYNTH_SDA

U505 CS2000CP — SDA/CDIN — SCL/CCLK — AD0/CS — CLK_IN — XTI/REF_CLK — XTO — CLK_OUT — AUX_OUT — VD — GND

R741 0 — SYNTH_AD0 — TP40 — 1588 Event 0 Out

SYNTH_24MHZ — P3V3_DELAYED — R506 68K — LD_B — D20 BLUE — Q500 NTS4001NT1G — Lock Detect

AVB_LOCK_DETECT Sh17

24.576 MHz Audio Ref — TP42 — R202 820

TP43 SDMA Event 1 In / 1588 Event 0 In

P3V3_DELAYED — C38 0.22UF 10V — R94 68K

U7 MLE145170 — D_IN — CLK — ENB — D_OUT — F_IN — OSC_IN — OSC_OUT — VDD — VSS — F_V — PHI_V — PHI_R — PD_OUT — LD — F_R — REF_OUT

145170_SPIDATIN — 145170_SPICLK — 145170_SPIEN_B

Software must configure GPIO function to emulate SPI interface (Bit Bang).

U7 CLK must be stable on power up; see data sheet. R96 value ensures logic low.

R97 4.7K — R96 4.7K

MLE145170 divides Audio Ref Clk to achieve frequencies of 8, 4, 1.5, 1.333, 1, 0.75 kHz etc.

AUDIO_REF_24MHZ — 5170_OSCI — R95 10.0K

This design utilizes a commercial-grade -40 to 85 C device. Freescale suggests consulting the supplier for equivalent automotive-grade device information.

P3V3_DELAYED — R83 0 — L10 120OHM — AUDOSC_VCC — C33 0.1UF 16V — Y1 24.576MHZ — LOC_OSC — R81 0 — LOCAL_AUDIO_24MHZ

Low-jitter timing ref

Position 1: Board Config - On = AVB, Off = Legacy
Position 2: Audio Master Clock - On = Listener (Sync'd), Off = Head Unit (Local)

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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: MCIMX6QAICPU2

Page Title: AVB

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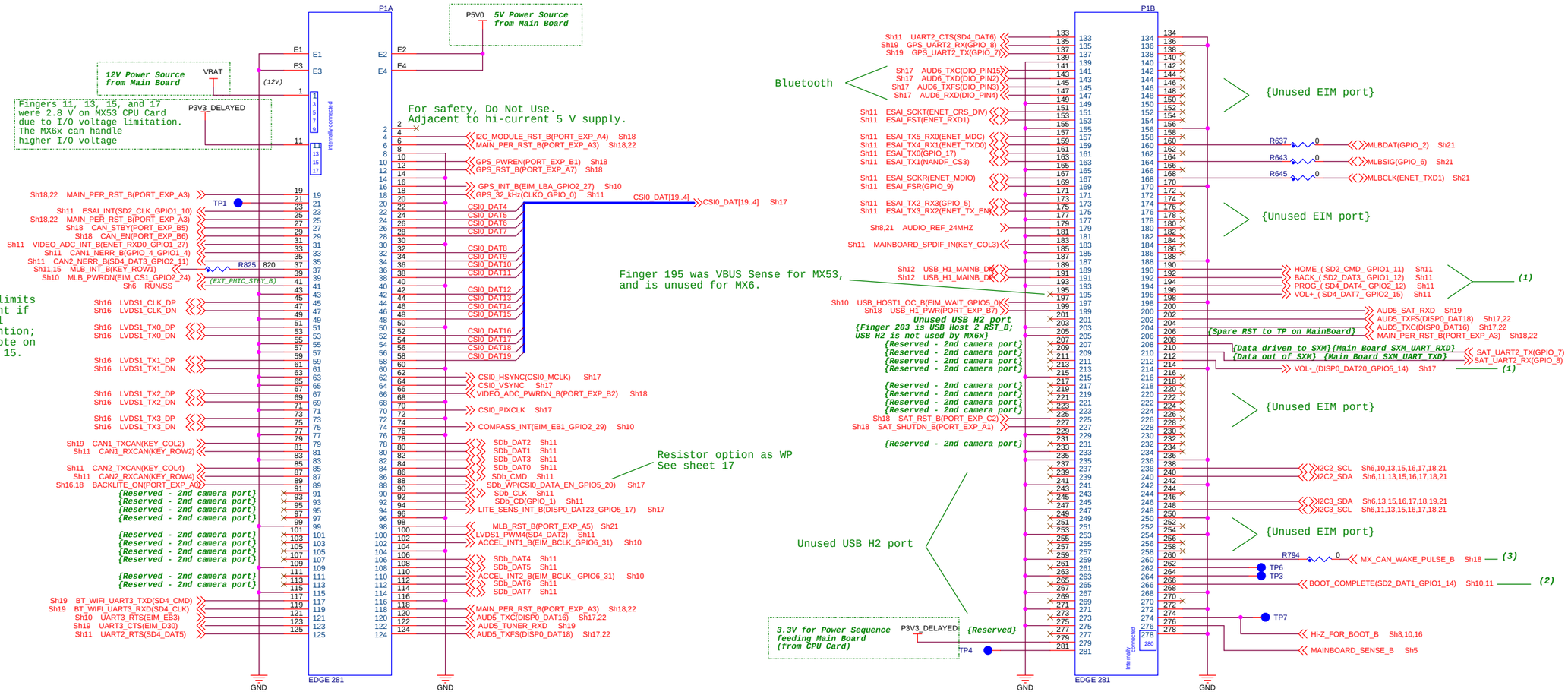
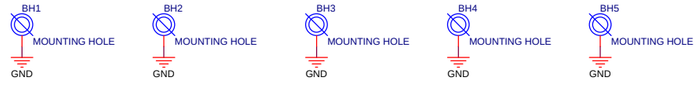
Date: Wednesday, February 25, 2015 Sheet 21 of 24

CARD EDGE FINGERS
BOARD-TO-BOARD CONNECTION

Mating connector on Base Board



Plated and Grounded Mounting Holes (130mil hole - 256mil pad)
Label = GND



NOTES:

1 If not Android, can be used as GPIO on Main Board. Main Board schematic cross-reference table does not apply to MX6.

2 Could be used as spare GPIO if SPI NOR is not needed.

3 Could be used as spare open-drain GPIO if not needed for local CAN PHY wake up.

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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: **MCIMX6QAICPU2**

Page Title: **Card Edge Fingers**

Size	Document Number	Rev
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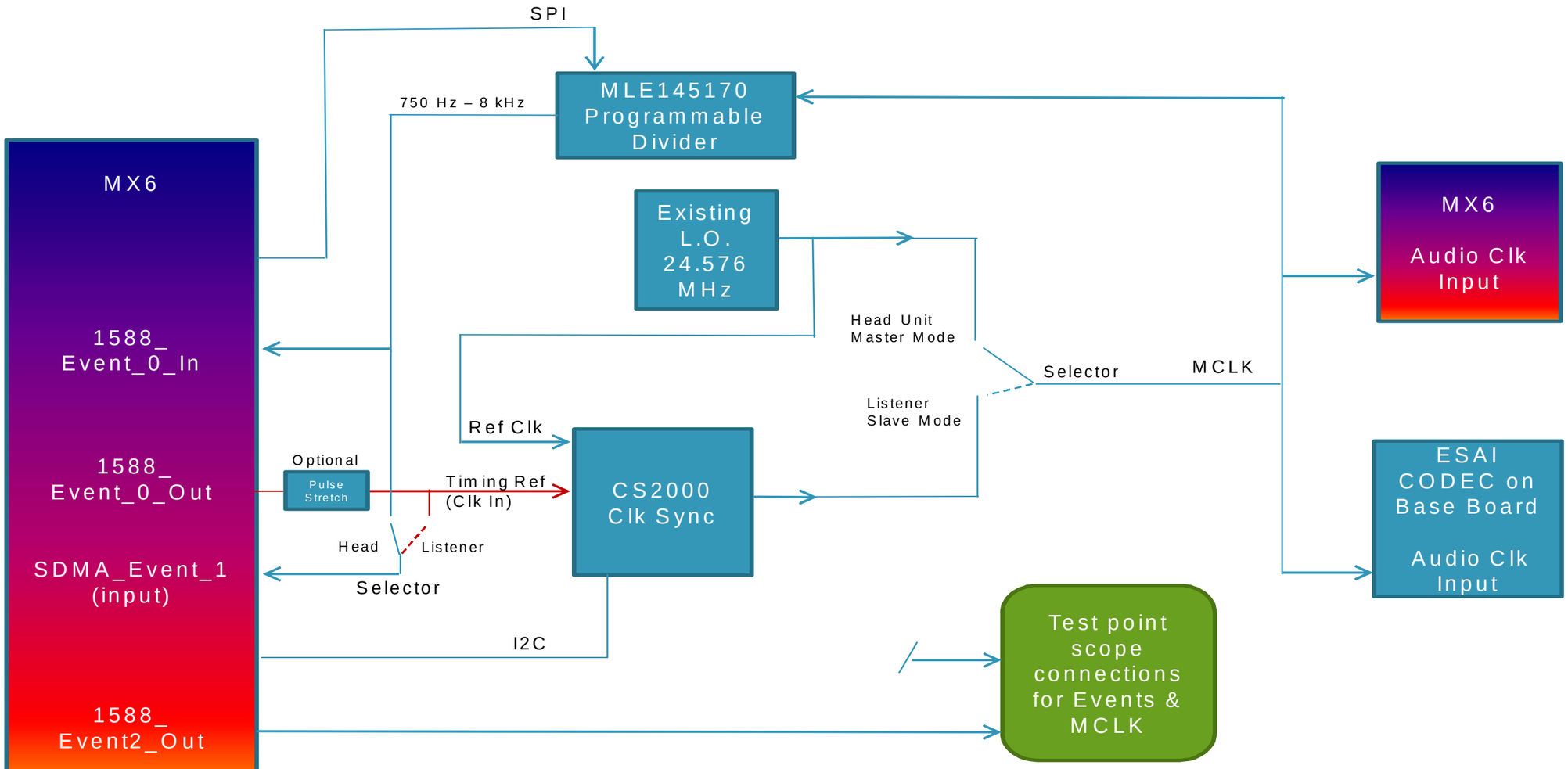
Date: Monday, February 23, 2015 Sheet 22 of 24

AVB Clock Distribution Block Diagram



AVB/Legacy selector switches not shown for simplicity.

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ICAP Classification:	FCP: ___ FIUO:	PUBI: X
Drawing Title:	MCIMX6QAICPU2	
Page Title:	AVB Clock Distribution Block Diagram	
Size C	Document Number SCH-27925 PDF: SPF-27925	Rev F1
Date: Monday, February 23, 2015	Sheet 23 of 24	

A	Initial release. Not manufactured.	6/11/13
B	Sheet 11 - Added zero ohm R201. [ENGR00270289] Sheet 19 - Added 49.9 ohm R200 series resistor to U17.4. [ENGR00270289] Throughout doc - Updated notes.	7/17/13

From Professional Services

BX1	Sheet 11 - Removed MLB connector; MLB provided on Base Board. Sheet 21 - Added CS2000 (Cirrus Clock Synthesizer) and ML145170 (Phase Frequency Detector) to support AVB feature. Sheet 8 - 24MHz Audio Clock Oscillator move to Sheet 21. Sheet 11 - Changed ENETref clk to IMX6 source: R108 = DNP, R109 = install. Sheet 22 - PU removed on MLB_INT_B(KEY_ROW1(GPIO4_9); PU on Base Board.	1/22/14

David's edits

BX2	Fixed BOM Assy Opt column entries.	1/22/14
BX3	Updated notes. Sheet 21 - Fixed power line filter to CS2000.	1/23/14
BX4	Ran DRC and fixed minor errors. No net changes.	1/24/14
BX4a	Sheet 21 - Added notes and dashed boxes around circuits.	1/24/14
BX5	Sheet 14 - Deleted back-up oscillator intersheet reference. Sheet 21 - Deleted backup PCIe oscillator; was DNP on rev B. Added PD to MLBDAT(GPIO_2). Moved PD to DISP0_D16. Changed TP from TH to SM.	1/27/14
BX6	Sheet 6 - Changed R553 to 0402 to consolidate BOM. Sheet 8 - Reduced values for clock Differential Bypass to 820 ohm and 2.7k to sharpen rise/fall times. Sheet 15 - Added SPI signals on J21. Added buffer chip. Sheet 22 - Changed R637, R643, R645 to installed to use MLB on Base Board.	1/28/14
BX7	Sheet 5 - LED too bright; changed R793 to 1.6k. Sheet 12 - Added VDDUSB_CAP note per IC designer. Sheet 14 - Added note to subheading and current limitation note. Changed connector footprint from Mini PCIe to Half Mini PCIe to match previous rev. Sheet 15 - Added AND gate to SS path to prevent backfeed.	2/5/14
BX8	Sheet 15 - Removed AND gate added in rev BX7. Backfeed solution is clipping diode on daughter card. Added bulk capacitor to NVCC_RGMII with a note. Sheet 20 - Change R651 power from P3V3_DELAYED to NVCC_SD3 to avoid backfeed with 1.8 V SDXC. Sheet 21 - Added lock detect LED for CS2000. Changed test points from SM pads to SM loops to accommodate scope probes. Sheet 23 - Added AVB signal table.	2/17/14
BX9	Sheet 21 - Footprints too big on SM loops. Changed to TH loops.	2/17/14
BX10	Sheet 21 - Footprints too big on TH loops selected. Changed to smaller footprint per Layout Designer suggestion; accommodates 26-guage wire.	2/18/14
BX11	Added series R (820-Ohm) to MLB_INT signal to prevent potential drivers at both end of the trace driving hard into each other.	2/20/14
BX12	Added BUF to SYNTH clk output to drive more than 20pF load. Added series R (0-Ohm) to SYNCED_AUDIO_24MHZ output signal for pontential series termination tuning. Added AVB CLK distribution tree block diagram on pg. 23 . Added more design notes for better explanation.	2/27/14
BX13	Changed C766 to 0.22uF 0201 package.	02/28/14
BX14	Added R827 (87kOhm) Pull-up to SW_CS_B net to disable the Tri-state Buffer on the SPI bus in scenario when BRCM ENET Switch board is not connected. Added testpoints to some unused pins of J21.	03//17/14
BY1	Changed bottom 5 mounting holes to plated and grounded to enhance EMC for working with ENET daughterboards.	04/04/14

C	Released to revision C. Not manufactured.	04/08/14
D	Component FDMS6681Z schematic symbol was updated to correct off-grid pin 5, which consequently caused pin 5 to disconnect from the associated nets, and unintentionally affected layout. Fixed Q502.5 and Q505.5 schematic and layout problem and release rev. D	04/25/14
E	This rev letter skipped to sync schem with layout. PCB layout was rev E and associated with schem rev D. Rev E schem not in Agile and not manufactured.	09/30/14
EX1	Sheet 3 - Renamed addr 0x20; now I2C Module. Sheet 4 - Updateded card identification fuse setting at bottom of sheet. Sheet 5 - Updated C1 part number due to EOL. Sheet 6 - Added note on decouple cap at bottom of sheet. Sheet 8 - Changed JTAG connector to slotted. Updated JTAG note - added "cable". Sheet 11 - Updated WDOG, SD Slot notes. Added note 1 near title block. Changed CD & WP pull-up resistor supply to unswitched 3.3 V (P3V3_DELAYED) per SW Team request to eliminate false card detects. Sheet 14 - Updated note on Ref Clock at top of sheet. Added Extender note at bottom of sheet. Sheet 15 - Added SPI NOR note at bottom left. Sheet 17 - Added option resistor and LD (Lock Detect) as default on CSI0_DATA_EN. Moved DISP0_DAT16 option back to sheet 17 - now R829, R830. Sheet 18 - Changed net name on PORT_EXP_A4. Added note on PORT_EXP_A5. Sheet 20 - Increase LED D9 resistor to 510 ohms to reduce brightness. Was R547, now R835. Cost reduction: Changed mechanical spacers from capacitors C747, C757, C758 to test loops TP501, TP502, TP503. Sheet 21 - Added several notes. Removed R509 pull-down on MLB_RST_B(PORT_EXP_A5); added termination note. Changed R96 and R97 from 68k to 4.7k to ensure logic low at power up due to i.MX on-chip 100k pull-up; see MLE145170 data sheet. Added off-sheet lock detect (LD) path. Increased LED D20 resistor to 820 ohms; was R2, now R836. Modified path for TP43 signal because no MX6 on-chip path for DMA Event 0. Added one shot to stretch 1588 event pulse width; guarantees trigger of CS2000. Sheet 22 - Added note on R825. Changed net name on finger 4. Sheet 23 - Updated block diagram. Sheet 24 - Updated AVB signal Assignment.	10/6/14
EX2	Sheet 6 - Added note on VIN decouple capacitors. Sheet 10 - Changed parallel NOR flash from U523 back to U510. Sheet 14 - Updated PCIE connector; footprint now covers half and full mini.	10/7/14
EX3	Sheet 21 - U522 input A and B net names were misnamed; swapped them. Added switch illustration.	10/8/14
EX4	Sheet 21 - Changed ref designators because these are top side: R836 -> R202, R837 -> R203, SH511 -> SH14.	10/8/14
EX5	Sheet 21 - Changed U522 one-shot input default to pos edge trigger per feedback from EU SW Team (Rui S)	10/13/14
EX6	Sheet 8 - Added U523. Sheet 17 & 21 - Changed net name LD to AVB_LOCK_DETECT.	10/13/14
F	Released for prototype build.	10/17/14
F1	Released for production. No electrical changes. Sheet 1 - Removed "Freescale Internal Use Only"; updated title block. Sheet 2 - Fixed block diagram. Sheet 5 - Added note on Backup Power Supply. Sheet 6 - Added power-on reset note at bottom. Added voltage note near TP12 due to possible PMIC change. Sheet 10 - Added U16 EOL note.	02/25/15
F2	No electrical changes. Sheet 12 - Removed note on VDDUSB_CAP (suggested ESD clamp).	10/17/14

AVB SIGNAL ASSIGNMENT v3

Ref	AVB Associated Name	MX6Q Ball & ALT Mode	Comment
TP43	ENET_1588_EVENT0_IN	ENET_TXD1 (ALT4)	Legacy system function = MLB CLK
TP40	ENET_1588_EVENT0_OUT	GPIO_19 (ALT1)	Legacy system function = ENET INT_B
TP41	ENET_1588_EVENT2_OUT	ENET_RX_ER (ALT4)	Legacy system function = USB_OTG_ID
TP40	SDMA Event 1	DISP0_DAT17(ALT4)	Legacy system function = RGB Disp (cluster)
TP42	MCLK, 24.576 MHz	CLK2_P/N config'd as input	Audio master clock
--	Programmable Divider SPI SS_B	(Port_Exp_A5 for bit bang)	Legacy system function = MLB_RST_B from I2C port exp.
--	Programmable Divider SPI SCLK	GPIO_6 (ALT5) for bit bang	Legacy system function = MLBSIG
--	Programmable Divider SPI MOSI	GPIO_2 (ALT 5) for bit bang	Legacy system function = MLBDAT

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%.
   All voltages are DC.
   All polarized capacitors are aluminum electrolytic.

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals
   Green text Denotes - Extra Notes to be considered.

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: **MCIMX6QAICPU2**

Page Title: **Notes and Revision History**

Size	Document Number	Rev
C	SCH-27925 PDF: SPF-27925	F2

Date: Monday, March 30, 2015 Sheet 24 of 24