i.MX6 SMART DEVICE SYSTEM

MCIMX6DL-SDP

Table of Content

GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum

2. Critical compenents that require tolerances tighter than listed in Note 1are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.

3. Interrupted lines coded with the same letter or letter combinations are electrically connected.

4. Device type number is for reference only. The number varies with the manufacturer.

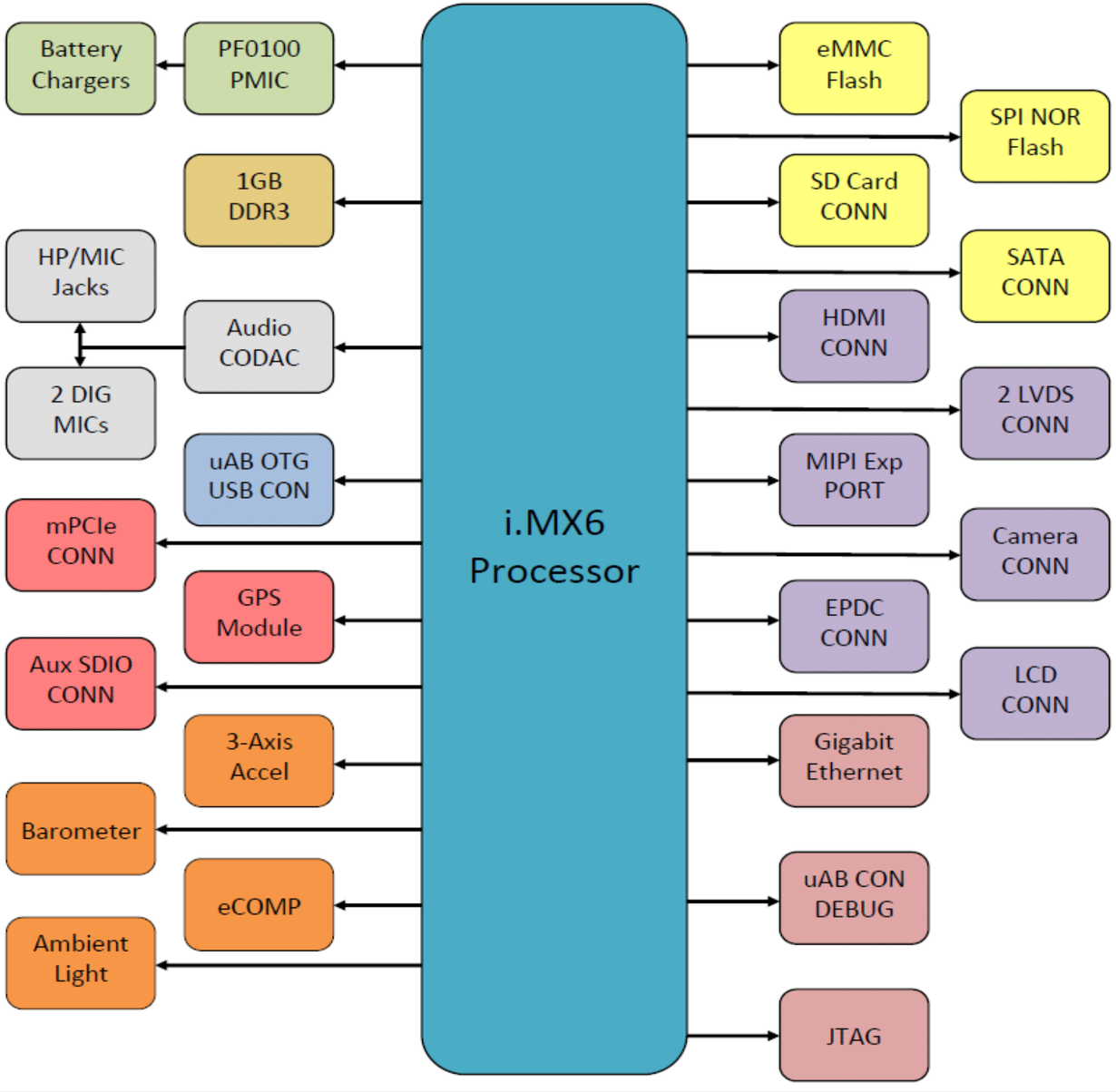
5. Special signal usage:
   _B or 'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC
Current Output: ~ 5A (depending on application)
Polarity:
Inner Diameter: 2.1mm
Outer Diameter: 5.5mm

Smart Device System Block Diagram



Revision History

Rev. Code	Date	Description
X1	11/02/2011	Rev X1 Draft
A	12/15/2011	Release to Prototype Phase
AX1	02/09/12	Draft Rev B Respin: - Changed Audio CODEC to WM8962 per Marketing Request. - Removed two digital microphones. Changed mics to Wolfson WM2730 per Marketing. - Connected NVCC_JTAG rail to GEN_3V3. - Added PFET Switch to SWBST supply to isolate it from System power. - Changed HDMI Media guard to CM2020 IC to correct I2C HDMI issue. - Changed voltage sides on U9 level shifter. - Changed SW4 to 3.15V output. Moved audio 1.8V to GEN_1V8. - Changed camera 1V5 supply to VGEN2, other 1V5 loads moved to VGEN1. - Added isolation PFETs to Audio voltage supplies. - Switched USB_OTG_ID to pin ENET_RX_ER, USBOTG_OC to pin EIM2 and USBH1_OC to pin EIM_D30 to match pinmux functionality. - Added parallel termination resistors to PCIe differential clock traces. - Added next generation DEVSLP option for SATA connection. - Moved DISP0_PWR_EN to NANDF_WP_B to correct pull up voltage issue. - Deleted auxiliary 3.15V voltage regulator. - Designated several capacitors on processor core power rails as DNP. Validation proved unnecessary. - Moved I2C3 SDA from GPIO_16. This pin must be unconnected for Ethernet 1588 (time stamp) functionality to work. - Added shield ground pins to LVDS connectors. - Changed extrnal speaker capacitors to higher voltage rating. - Changed external regulator to supply 3.0V power to VSNVS. - Changed PF0100 microprocessor program circuit to DNP. - Added 5V supply to LCD expansion headers. - Connected HPOUTFB directly to Audio GND. - Connected VDDOTP to ground to boot PMIC from program settings. - Added isolation to prevent back powering board from USB when no battery present. - Back annotated Schematic to Layout. REFDES may have changed from Rev A. - Populated optional "PWRON" button circuit for use with Android. - Removed write protect on NOR Flash. - Removed LC filter circuit from external speakers. - Added an additional 2 100uF capacitors to MPCIE_3V3 next to connector. - Updated Power Rail, IOMUX, and Configuration Tables.
B	02/17/12	Release to Production
B1	04/11/12	Release to Production - Depopulated Q512 because of schematic error. - Cut trace to U12 pin 5 to prevent false USB plug in detects. - Added schematic page to detail applicable board TDAs that affect Rev B boards. - Populating CAN components U517 and U518 per Marketing Request. - Added resistor RX1 across pads for C55 to improve 24MHz clock stability. - Pull up resistors R629 and R639 have been changed to DNP. - R30 is DNP to support TO1.0 issue on i.MX6 DualLite Silicon.
B2	05/04/12	- Changed Marketing part number to MCIMX6DL-SDP - Changed R7, R112 and R585 to DNP - Changed C540 to "POPULATED" - Added notes that the SATA interface does not exist on the i.MX6 Duallite version of the i.MX6 Processor Familiy.
B3	05/25/12	- Changed DDR3 Memory to new 1.35V capable memory MT41K128M16JT. - Changed C540 to 1.0 uF per Wolfson recommendation. - Changed R183 and R189 to 2.37K pull ups to bring I2C rise time into specification.
B4	07/18/12	- Removed buffers U500 and U528 from digital microphone data outputs. A note is added to show required hand wire modification. - The Battery Charge Done LED is disconnected and R522 is depopulated. New parts RX2, CX1 and UX1 are added. Traces show required hand modifications. - Optional Power On Circuit has been disabled and U511 and R570 are now DNP. A new Diode DX1 has been added to allow EIM_D29 to sense a button press. - RESET button SW2 now connects to the PWRON pin of the PMIC. - Added 10K pull down resistor RX3 to SDCKE0 trace. - SIM Card Connector CON1 is now populated by default. - Battery Connector Header CON3 is now populated by default. - Changed resistors R174 and R176 and to depopulated by default. LVDS0 EDID will not be connected to I2C2 channel unless needed.
B5	09/25/12	- Changed U1 to i.MX 6 TO1.2 processor. - Changed C68 and C612 to DNP. - Populated C682 and C716 with 22uF capacitors.
C1	10/01/12	- All hand wire changes made in Revision B4 are now formally made in the netlist and the layout files. - Q512 is changed to populated. - Optional Start Up circuit has been modified. - PMIC Programming Micro-Processor is removed. - CX1 capacitor is changed to C504 - DX1 diode is changed to D4 - RX1 resistor changed to R216 - RX2 resistor changed to R19 - RX3 resistor changed to R635 - UX1 buffer changed to U507 - Add DNP Input to U13 buffer for USB_OTG_PWR_EN. Buffer now powered from GEN_3V3. - FA_ANA and VDD_FA signals now connected to ground. - Added resistor options to EIM_DA7 trace to EPD connector. - Connected EIM_DA9 to EPDC connector J508 to supply SDCE5 if needed. - Optional LDO U9 is now depopulated. - Added Connector J13 to support BT from SDIO Card through DNP resistors. - Added GPIO control of Battery Charge Enable pins through DNP resistor. - Changed C594 to 0.22uF - Changed C31 to 47uF. - Added C555 as second 22uF capacitor in parallel with C546. - Changed C561, C562, C586 and C596 to 0.47uF. - Added additional 47uF bulk capacitor C769 to SD2 socket VDD supply. - Added option to route HDMI DDC comms seperate from I2C2 comms channel. - C597 populated to provide de-bounce to RESET circuit. - Depopulated C68, C612. Populated C682, C716 closer to pins. - Depopulated C39, C606, C607, C608, C609, C610, C673 and C681. - Added DNP R302 to provide alternate 5V supply path to USB_H1_VBUS. - Added DNP R632 to provide alternate gating of PMIC_5V source (tied to VDDSOC). - Added DNP L25 and L26 to provide alternate 2.8V supply path to camera modules. - Added test pads to LVDS third data lanes to support testing with will 24-bit panels. - Changed capacitors C6 and C7 to Zero Ohm resistors. - Changed Battery Charge ICs U502 and U503 to MAX8903C version.
C2	11/09/12	- Moved Ferrite Beads L10 and L17 to pads for L25 and L26. Camera Analog Voltage supply moved to VGEN3. - Added notes for 24MHz crystal and USB layout design. - Changed R17, R21, R25, R27, R68, R85, R582, and R660 to 1% resistors due to lead time availability issues.
C3	02/20/13	- Changed BT500 Battery Holder to new manufacturer due to parts availability. - Changed R17, R21, R25, R27, R68, R85, R582, and R660 to 0.5% resistors due to parts availability. - Changed R97 and R106 pull up resistors to 4.7 Ohm. - Changed R19 pull up resistor to 10K Ohm.
C4	04/02/13	- DNP BH1, BH2 Standoffs. - Changed U8 part number to Programmed part MMPF0100F0ZES - Changed R17, R21, R25, R27, R68, R85, R582, and R660 to 1% resistors due to lead time availability issues.
C5	02/16/15	- Updated Manufacturing numbers for U8, U512, U519

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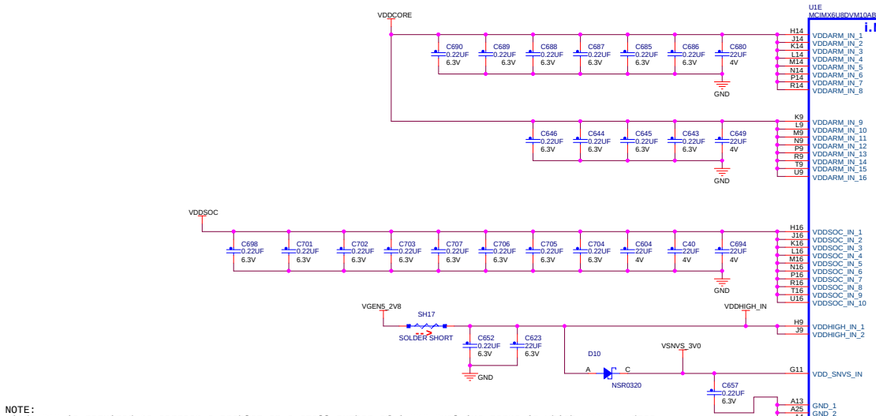
Multimedia Application Division, Wireless & Mobile System Group

ICAP Classification: FCP: FIUO: PURI: X

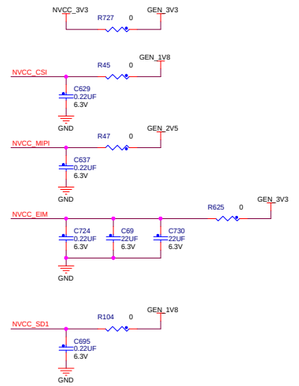
Designer: Mark Middleton	Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM		
Drawn by: Mark Middleton	Page Title: TITLE PAGE		
Approved: <Approver>	Size: D	Document Number: SOURCE:SCH-27417 PDF:SPF-27417	Rev: C5
	Date: Monday, February 16, 2015	Sheet 1 of 25	



NOTE:
Diode D10 is required to correct a problem on a small number of i.MX6 DualLite parts in which VDDSNVS does not come up when VDDHIGH_IN is applied. A similar problem was corrected on i.MX6Q TO1.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

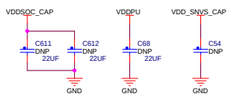
NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.



NOTE:
Freescale has validated two difference sets of decoupling capacitors and board layouts for use with the i.MX 6 processor. The customer is free to choose the desired decoupling scheme. This scheme uses fewer components. The alternate scheme can be found on the ARD board. Refer to SCH-27142 and LAY-27142.

Extra Bulk Capacitors



NOTE:
In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitive loading on the internal processor LDOs. The coponents/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.

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Date: Monday, February 16, 2015	Sheet 2 of 25	

U1A
MCIMX6U8DVM10AB

i.MX6U - EIM

NVCC_EIM1

EIM_LBA K22
EIM_OE J24
EIM_RW K20
EIM_CS0 H24
EIM_CS1 J23
EIM_A16 H25
EIM_A17 G24
EIM_A18 J22
EIM_A19 G25
EIM_A20 H22
EIM_A21 H23
EIM_A22 F24
EIM_A23 J21
EIM_A24 F25
EIM_A25 H19
EIM_D16 C25
EIM_D17 F21
EIM_D18 D24
EIM_D19 G21
EIM_D20 G20
EIM_D21 H20
EIM_D22 E23
EIM_D23 D25
EIM_D24 F22
EIM_D25 G22
EIM_D26 E24
EIM_D27 E25
EIM_D28 G23
EIM_D29 J19
EIM_D30 J20
EIM_D31 H21
EIM_EB2 E22
EIM_EB3 F23
EIM_BCLK N22
EIM_WAIT M25
EIM_EB0 K21
EIM_EB1 K23
EIM_DA0 L20
EIM_DA1 J25
EIM_DA2 L21
EIM_DA3 K24
EIM_DA4 L22
EIM_DA5 L23
EIM_DA6 K25
EIM_DA7 L25
EIM_DA8 L24
EIM_DA9 M21
EIM_DA10 M22
EIM_DA11 M20
EIM_DA12 M24
EIM_DA13 M23
EIM_DA14 N23
EIM_DA15 N24

NVCC_EIM2

EIM_WAIT R132 0 DI0_D0_CS 9
EIM_BCLK R122 0 DI0_D1_CS 9
EIM_D21 R125 0 USB_OTG_OC 11
EIM_D24 R137 0 USB_OTG_PWR_EN 11
EIM_D25 R127 0 UART3_TXD 17
EIM_D26 R126 0 UART3_RXD 17
EIM_EB3 R136 0 SENSOR_PWR_EN 14
EIM_D28 R128 0 TS_INT 9
EIM_D30 R134 0 USB_H1_OC 11
EIM_EB0 R124 0 GPS_RESET_B 17
EIM_D18 R129 0 GPS_PPS 17
EIM_D20 R131 0 GPS_PWREN 17
EIM_D28 R135 0 DISP0_RD 9
EIM_D31 R133 0 DISP0_RST_B 9
EIM_DA9 R171 0 ALS_INT 14

Depopulate R121, R123, R133, R138, R139, R167, R168, and R627 when using E-BOOK Card in 16-bit Data Mode.

EIM_CS1 R627 0 DOK_B 18
EIM_DA15 R167 0 BARD_INT 14
EIM_D16 R168 0 COMP_INT 14
EIM_D23 R139 0 CHG_STATUS1_B 18
EIM_D19 R123 0 PCIE_PWR_EN 16
EIM_DA13 R133 0 CHG_STATUS2_B 18
EIM_DA14 R121 0 CHG_FLT2_B 18
EIM_A25 R138 0 CHG_FLT1_B 18

SECURE HDMI COMMUNICATIONS

EIM_DA15 R217 0 DNP COMP_INT 14
EIM_D16 R218 0 DNP HDMI_DDC_DAT_IN 7,22
EIM_EB2 R219 0 DNP HDMI_DDC_CLK_IN 7,22

NOTE:
To configure SD board to run in Secure HDMI mode:
1) Depopulate R153 and R154 (schematic page 22)
   This removes HDMI comms channel from I2C2.
2) Populate R218 and R219.
   This connects HDMI comms to DDC capable pins.
3) Depopulate R168.
   This deconflicts HDMI comms from the compass interrupt.
4) Populate R217 to connect COMP_INT to a processor.
   This connects COMP_INT to a different GPIO pin.
5) R167 may be left populated or depopulated as desired.

U1C

i.MX6U - CONTROL

MX6_ONOFF 19 D12 ONOFF
POR_B 13,19,20,21 C11 POR
BOOT_MODE0 21 C12
BOOT_MODE1 21 F12
TEST_MODE 21 E12
TAMPER 21 E11
PMIC_STBY_REQ 19 F11
PMIC_ON_REQ 19 D11
BOOT_MODE0
BOOT_MODE1
TEST_MODE
TAMPER
PMIC_STBY_REQ
PMIC_ON_REQ
VDD_SNVS_IN

NVCC_JTAG
JTAG_TCK H5 JTAG_TCK 13
JTAG_TMS G5 JTAG_TMS 13
JTAG_TDI G6 JTAG_TDI 13
JTAG_TDO H3 JTAG_TDO 13
JTAG_TRST H4 JTAG_nTRST 13
JTAG_MOD JTAG_MOD 13

CLK1_N C7 CLK1_N 16
CLK1_P D7 CLK1_P 16
CLK2_N C5
CLK2_P D5

CPU_XTALI A7
CPU_XTALO B7
XTALI
XTALO
R75 10M DNP
Y1 24MHz
R216 2.2M
C55 18PF
C51 18PF
RTC_XTALI D9
RTC_XTALO C9
RTC_XTALI
RTC_XTALO
R510 10M DNP
QZ500 32.768KHZ
C624 18PF
C639 18PF
GND

MCIMX6U8DVM10AB

Note:
1) R216 is required to correct a known 24MHz slow starting issue present on some iMX 6 part. Please refer to the i.MX 6 Processor Errata, issue # ERR003745 for more details.

2) Per bulletin EB830, the i.MX6 processor may drive the 24 MHz crystal up to 250 uW. Freescale recommends following the guidelines contained in the bulletin.

The HW Developer Guide contains additional information.

U1H

i.MX6U - LVDS

GEN_2V5 R600 0 LVDS_2V5 V7 NVCC_LVDS2P5
C632 0.22UF 6.3V GND

LVDS0_TX0_N U2 LVDS0_TX0_N 7
LVDS0_TX0_P U1 LVDS0_TX0_P 7
LVDS0_TX1_N U4 LVDS0_TX1_N 7
LVDS0_TX1_P U3 LVDS0_TX1_P 7
LVDS0_TX2_N V2 LVDS0_TX2_N 7
LVDS0_TX2_P V1 LVDS0_TX2_P 7
LVDS0_CLK_N V4 LVDS0_CLK_N 7
LVDS0_CLK_P V3 LVDS0_CLK_P 7
LVDS0_TX3_N W2 TP32 16767721 TP32
LVDS0_TX3_P W1 TP31 16767721 TP31

NVCC_LVDS2P5

LVDS1_TX0_N Y1 LVDS1_TX0_N 7
LVDS1_TX0_P Y2 LVDS1_TX0_P 7
LVDS1_TX1_N AA2 LVDS1_TX1_N 7
LVDS1_TX1_P AA1 LVDS1_TX1_P 7
LVDS1_TX2_N AB1 LVDS1_TX2_N 7
LVDS1_TX2_P AB2 LVDS1_TX2_P 7
LVDS1_CLK_N Y3 LVDS1_CLK_N 7
LVDS1_CLK_P Y4 LVDS1_CLK_P 7
LVDS1_TX3_N AA3 TP509 TP509
LVDS1_TX3_P AA4 TP510 TP510

MCIMX6U8DVM10AB

NVCC_LVDS2P5 also powers on-chip DDR I/O predrivers, and must be powered whether LVDS is used or not.

U1D

i.MX6U - DISP; CSI

NVCC_CSI

CSI0_HSYNCH 8,9 P4 CSI0_MCLK
CSI0_PIXCLK 8,9 P1 CSI0_PIXCLK
CSI0_VSYNCH 8,9 N2 CSI0_VSYNC
PCIE_WAKE_B 16 P3 CSI0_DATA_EN
AUD3_TXC 10 P2 CSI0_DATA4
AUD3_TXD 10 N1 CSI0_DATA5
AUD3_TXFS 10 N3 CSI0_DATA6
AUD3_RXD 10 N5 CSI0_DATA7
I2C1_SDA 22 N4 CSI0_DATA8
I2C1_SCL 22 M1 CSI0_DATA9
UART1_TX 13 M3 CSI0_DATA10
UART1_RX 13 M2 CSI0_DATA11
CSI0_DAT12 8,9 L1 CSI0_DATA12
CSI0_DAT13 8,9 M4 CSI0_DATA13
CSI0_DAT14 8,9 M5 CSI0_DATA14
CSI0_DAT15 8,9 L5 CSI0_DATA15
CSI0_DAT16 8,9 L3 CSI0_DATA16
CSI0_DAT17 8,9 M6 CSI0_DATA17
CSI0_DAT18 8,9 L2 CSI0_DATA18
CSI0_DAT19 8,9 CSI0_DATA19

NVCC_LCD

DI0_DISP_CLK N19 DSP0_CLK R113 33 DISP0_CLK 9
DI0_PIN2 N25 DI0_PIN2 R41 33 DISP0_HSYNCH 9
DI0_PIN3 N20 DI0_PIN3 R44 33 DISP0_VSYNCH 9
DI0_PIN4 P25 DI0_PIN4 R42 33 DISP0_CNTRST 9
DI0_PIN15 N21 DI0_PIN15 R43 33 DISP0_DRDY 9

DISP0_DAT0 P24 DISP0_DAT0 R91 33 DISP0_DAT0 9
DISP0_DAT1 P22 DISP0_DAT1 R90 33 DISP0_DAT1 9
DISP0_DAT2 P23 DISP0_DAT2 R89 33 DISP0_DAT2 9
DISP0_DAT3 P21 DISP0_DAT3 R85 33 DISP0_DAT3 9
DISP0_DAT4 P20 DISP0_DAT4 R84 33 DISP0_DAT4 9
DISP0_DAT5 R25 DISP0_DAT5 R83 33 DISP0_DAT5 9
DISP0_DAT6 R23 DISP0_DAT6 R81 33 DISP0_DAT6 9
DISP0_DAT7 R24 DISP0_DAT7 R80 33 DISP0_DAT7 9
DISP0_DAT8 R22 DISP0_DAT8 R79 33 DISP0_DAT8 9
DISP0_DAT9 T25 DISP0_DAT9 R76 33 DISP0_DAT9 9
DISP0_DAT10 R21 DISP0_DAT10 R74 33 DISP0_DAT10 9
DISP0_DAT11 T23 DISP0_DAT11 R73 33 DISP0_DAT11 9
DISP0_DAT12 R20 DISP0_DAT12 R72 33 DISP0_DAT12 9
DISP0_DAT13 U25 DISP0_DAT13 R67 33 DISP0_DAT13 9
DISP0_DAT14 T22 DISP0_DAT14 R65 33 DISP0_DAT14 9
DISP0_DAT15 T21 DISP0_DAT15 R64 33 DISP0_DAT15 9
DISP0_DAT16 U24 DISP0_DAT16 R60 33 DISP0_DAT16 9
DISP0_DAT17 V25 DISP0_DAT17 R59 33 DISP0_DAT17 9
DISP0_DAT18 U23 DISP0_DAT18 R57 33 DISP0_DAT18 9
DISP0_DAT19 T20 DISP0_DAT19 R56 33 DISP0_DAT19 9
DISP0_DAT20 V24 DISP0_DAT20 R54 33 DISP0_DAT20 9
DISP0_DAT21 V23 DISP0_DAT21 R53 33 DISP0_DAT21 9
DISP0_DAT22 W24 DISP0_DAT22 R52 33 DISP0_DAT22 9
DISP0_DAT23 DISP0_DAT23 R51 33 DISP0_DAT23 9

HSYNC
VSYNC
CNTRST
DRDY

NVCC_MIPI

CSI_CLK0M 8 F4 CSI_CLK0M
CSI_CLK0P 8 F3 CSI_CLK0P
CSI_D0M 8 E1 CSI_D0M
CSI_D0P 8 E2 CSI_D0P
CSI_D1M 8 D1 CSI_D1M
CSI_D1P 8 D2 CSI_D1P
CSI_REXT D4 CSI_REXT
R605 6.04K 1%
GND

DSI_CLK0M H3 DSI_CLK0M 8
DSI_CLK0P H4 DSI_CLK0P 8
DSI_D0M G2 DSI_D0M 8
DSI_D0P G1 DSI_D0P 8
DSI_D1M H2 DSI_D1M 8
DSI_D1P H1 DSI_D1P 8
DSI_REXT G4 DSI_REXT
R38 6.04K 1%
GND

MCIMX6U8DVM10AB

U1E

i.MX6U - NC PINS

SATA_REXT C14 NC_C14
R619 191.0 1%
GEN_2V5 R87 0 SATA_VPH
C668 0.22UF 6.3V
GND
NC_E1 E1
NC_E2 E2
NC_F1 F1
NC_F2 F2
NC_G12 G12
NC_G13 G13
NC_N12 N12
VDDSOC_VP R96 0 SATA_VP
C678 0.22UF 6.3V
VDDSOC_CAP
{NVCC_CACHE POWER}
C667 0.22UF 6.3V
GND

NC_A9 A9
NC_A10 A10
NC_A11 A11
NC_A12 A12
NC_A14 A14
SATA_TXP 6
SATA_RXN 6
NC_B9 B9
NC_B10 B10
NC_B11 B11
NC_B12 B12
NC_B14 B14
SATA_TXN 6
SATA_RXP 6

MCIMX6U8DVM10AB

Note: The SATA interface on the i.MX6 DualLite Processor is disabled. These pins have been diabled. This block has been left in only to provide continuity with other Smart Devices that use the same PCB,

U1F

i.MX6U - HDMI

VDDSOC_VP R48 0 C638 0.22UF 6.3V GND
GEN_2V5 R46 0 C625 0.22UF 6.3V GND
HDMI_VP L7 HDMI_VP
HDMI_VPH M7 HDMI_VPH
HDMI_RESREF J1 HDMI_REF
R37 1.6K 1%
GND

HDMI_HPD K1 HDMI_HPD 7
HDMI_DDCCEC K2 HDMI_DDCCEC 7
R653 0 HDMI_CEC_IN
R656 0
GND
HDMI_CLKM J5 HDMI_CLKM 7
HDMI_CLKP J6 HDMI_CLKP 7
HDMI_D0M K5 HDMI_D0M 7
HDMI_D0P K6 HDMI_D0P 7
HDMI_D1M J3 HDMI_D1M 7
HDMI_D1P J4 HDMI_D1P 7
HDMI_D2M K3 HDMI_D2M 7
HDMI_D2P K4 HDMI_D2P 7

MCIMX6U8DVM10AB

U1G

i.MX6U - USB

USB_OTG_CHD B8
USB_OTG_VBUS E9
USB_OTG_DN B6 USB_OTG_DN 11
USB_OTG_DP A6 USB_OTG_DP 11
VDDUSB F9
VDDUSB_CAP
C627 10UF 6.3V
C633 0.22UF 6.3V
GND
USB_OTG_VBUS
C642 0.22UF 10V
GND
USB_H1_DP E10 USB_HOST_DP 16
USB_H1_DN F10 USB_HOST_DN 16
USB_H1_VBUS D10
LDO_USB_IN
R301 0
USB_H1_VBUS
PMIC_5V
R302 0 DNP
C651 0.22UF 10V
GND

MCIMX6U8DVM10AB

U1B

i.MX6U

NVCC_ENET

ENET_MDC V20 RGMII_MDC 12
ENET_MDIO V23 RGMII_MDIO 12
ENET_CRS_DV V22 ENET_REFCLK RGMII_nRST 12
ENET_REF_CLK W23 USB_OTG_ID 11
ENET_RX_ER V21 ETH_WOL_INT 12
ENET_TX_EN
ENET_RXD0 W21 UOK_B 11,18
ENET_RXD1 W22 RGMII_INT 12
ENET_TXD0 U20 DISP0_PWR_EN 9
ENET_TXD1 W20 USB_H1_PWR_EN 11

ETH_3V3
R623 68K
C726 1.0UF
ENET_REF_CLK 12
Place C726 close to i.MX6.
R624 68K
GND

NVCC_SD1

SD1_CMD B21
SD1_CLK D20
SD1_DAT0 A21
SD1_DAT1 C20
SD1_DAT2 E19
SD1_DAT3 F18
DISP0_PWM

NVCC_SD2

SD2_CMD F19
SD2_CLK C21
SD2_DAT0 A22
SD2_DAT1 E20
SD2_DAT2 A23
SD2_DAT3 B22

NVCC_SD3

SD3_CMD B13
SD3_CLK D14
SD3_DAT0 E14
SD3_DAT1 F14
SD3_DAT2 A15
SD3_DAT3 B15
SD3_DAT4 D13
SD3_DAT5 C13
SD3_DAT6 E13
SD3_DAT7 F13
SD3_RST D15
R553 0

ACCL_INT_IN 14
CSI_RST_B 8
CSI0_PWN 8,9
CSI0_RST_B 8,9
CSI_PWN 8
SD2_CMD
SD2_CLK
SD2_DATA0 15
SD2_DATA1 15
SD2_DATA2 15
SD2_DATA3 15
SD3_CMD 6
SD3_CLK 6
SD3_DATA0 6
SD3_DATA1 6
SD3_DATA2 6
SD3_DATA3 6
SD3_DATA4 6
SD3_DATA5 6
SD3_DATA6 6
SD3_DATA7 6
HEADPHONE_DET 10
SD3_RST

NVCC_GPIO

KEY_COL0 V6 KEY_COL0 9
KEY_ROW0 U7 KEY_ROW0 9
KEY_COL1 U6 KEY_COL1 9
KEY_ROW1 W5 KEY_ROW1 9
KEY_COL2 W4 KEY_ROW2 KEY_COL2 9
KEY_ROW2 V5 KEY_ROW2 9
KEY_COL3 T7 KEY_COL3 9
KEY_ROW3 T6 KEY_ROW3 9
KEY_COL4 V7 KEY_COL4 9
KEY_ROW4 T5 KEY_ROW4 9
R652 0 HDMI_CEC_IN 7

CSI1_CLK W5 CSI1_CLK 22
CSI1_MOSI V6 CSI1_MOSI 22
CSI1_MISO U7 CSI1_MISO 22
CSI1_CS0 U6 CSI1_CS0 22
CODEC_PWR_EN 10
I2C2_SCL T7 I2C2_SCL 22
I2C2_SDA T6 I2C2_SDA 22
KEY_COL4 9
KEY_ROW4 9

CSI1_MCLK
GPIO_0 T5 GPIO_0_CLKO 8,9
GPIO_1 T4 KEY_ROW5 9
GPIO_2 T1 KEY_ROW6 9
GPIO_3 R7 I2C3_SCL 22
GPIO_4 R6 KEY_COL7 9
GPIO_5 R4 KEY_ROW7 9
GPIO_6 R5 I2C3_SDA 22
GPIO_7 P6 SPDIF_CLK 9
GPIO_8 T2 DISP0_SER_RS 9
GPIO_9 R2 KEY_COL6 9
GPIO_16 R1 X
GPIO_17 P5 SPDIF_OUT 9
GPIO_18 P4 PMIC_INT_B 19
GPIO_19 KEY_COL5 9

NVCC_GPIO

KEY_ROW4 R676 0 SATA_DEVSLP 6
KEY_COL4 R36 0 PCIE_DIS_B 16
KEY_COL7 R564 0 KEY_VOL_UP 21
KEY_ROW7 R66 0 KEY_VOL_DN 21
SPDIF_CLK R114 0 CAN1_TX 15
DISP0_SER_RS R69 0 CAN1_RX 15
SPDIF_OUT R556 0 PCIE_RST_B 16
KEY_COL5 R661 0 CAN1_STBY 15
KEY_ROW5 R300 0 WDOG_B 21
KEY_ROW6 R588 0 USR_DEF_RED_LED 21
KEY_COL6 R597 0 MICROPHONE_DET 10

Refer to build options table for assembly options on muxed signal resistors.

NVCC_ENET

RGMII_TXC D21 RGMII_TXCLK 12
RGMII_TD0 C22 RGMII_TXD0 12
RGMII_TD1 F20 RGMII_TXD1 12
RGMII_TD2 E21 RGMII_TXD2 12
RGMII_TD3 A24 RGMII_TXD3 12
RGMII_TX_CTL C23 RGMII_TXEN 12
RGMII_RXC B25 RGMII_RXCLK 12
RGMII_RD0 C24 RGMII_RXD0 12
RGMII_RD1 B23 RGMII_RXD1 12
RGMII_RD2 B24 RGMII_RXD2 12
RGMII_RD3 D23 RGMII_RXD3 12
RGMII_RX_CTL D22 RGMII_RXDV 12

NVCC_NAND

NANDF_CS0 F15 DISP_RST_B 8
NANDF_CS1 C16 DISP_PWR_EN 8
NANDF_CS2 A17 CABC_EN0 7
NANDF_CS3 D16 CABC_EN1 7
NANDF_ALE A16 CAP_TCH_INT0 7
NANDF_CLE C15 CAP_TCH_INT1 7
NANDF_WP E15 DISP0_WR 9
NANDF_RB0 B16 AUX_5V_EN 20
NANDF_D0 A18 SD3_CD_B 6
NANDF_D1 C17 SD3_WP 6
NANDF_D2 D17 SD2_CD_B 15
NANDF_D3 A19 SD2_WP 15
NANDF_D4 C18 SD2_DATA4 15
NANDF_D5 B18 SD2_DATA5 15
NANDF_D6 E17 SD2_DATA6 15
NANDF_D7 C18 SD2_DATA7 15
SD4_CLK E16 SD4_CLK 5
SD4_CMD B17 SD4_CMD 5
SD4_DAT0 D18 SD4_DAT0 5
SD4_DAT1 B19 SD4_DAT1 5
SD4_DAT2 F17 SD4_DAT2 5
SD4_DAT3 A20 SD4_DAT3 5
SD4_DAT4 E18 SD4_DAT4 5
SD4_DAT5 C19 SD4_DAT5 5
SD4_DAT6 A20 SD4_DAT6 5
SD4_DAT7 D19 SD4_DAT7 5

GEN_3V3 GEN_1V8
C622 0.22UF 6.3V GND
U514 VCCA VCCB GND NC NLSV1T34
C641 0.22UF 6.3V GND
7,8 DISP0_CONTRAST
DISP0_PWM

U1K

i.MX6U - RGMII

MCIMX6U8DVM10AB

Layout: High speed data lines : 50 ohms

U1I

i.MX6U - PCIe

PCIE_VP H7 PCIE_VP
PCIE_VPTX G8 PCIE_VPTX
PCIE_VPH G7 PCIE_VPH
PCIe_REXT A2 PCIE_REXT
PCIE_RXM B1 PCIE_RXM 16
PCIE_RXP B2 PCIE_RXP 16
PCIE_TXM A3 PCIE_TXM 16
PCIE_TXP B3 PCIE_TXP 16
R604 200 1%
GND

MCIMX6U8DVM10AB

Extra Bulk Capacitors

SATA_VP C681 DNP GND
SATA_VPH C673 DNP GND
HDMI_VP C609 DNP GND
HDMI_VPH C610 DNP GND
PCIE_VP C608 DNP GND
PCIE_VPTX C606 DNP GND
LVDS_2V5 C39 DNP GND
PCIE_VPH C607 DNP GND

NOTE:
In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitve loading on the internal processor LDOs. The coponents/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X
Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM
Page Title: CPU SIGNAL
Size D | Document Number SOURCE:SCH-27417 PDF:SPF-27417 | Rev C5
Date: Monday, February 16, 2015 | Sheet 3 of 25

Clock terminators: Place at end of route at each DDR pair

GND probe pads

DRAM_SDCLK0 — R118 200 1% — DRAM_SDCLK0_B

DRAM_SDCLK1 — R43 200 1% — DRAM_SDCLK1_B

TP17 GND, TP16 GND

U1J
MCIMX6U8DVM10AB

i.MX6U - DDR

DRAM_D0	AD2	DRAM_D0	DRAM_A0	AC14	DRAM_A0
DRAM_D1	AE2	DRAM_D1	DRAM_A1	AB14	DRAM_A1
DRAM_D2	AC4	DRAM_D2	DRAM_A2	AA14	DRAM_A2
DRAM_D3	AA5	DRAM_D3	DRAM_A3	Y14	DRAM_A3
DRAM_D4	AC1	DRAM_D4	DRAM_A4	W14	DRAM_A4
DRAM_D5	AD1	DRAM_D5	DRAM_A5	AE13	DRAM_A5
DRAM_D6	AB4	DRAM_D6	DRAM_A6	AC13	DRAM_A6
DRAM_D7	AE4	DRAM_D7	DRAM_A7	Y13	DRAM_A7
DRAM_SDQS0	AE3	DRAM_SDQS0	DRAM_A8	AB13	DRAM_A8
DRAM_SDQS0_B	AD3	DRAM_SDQS0_B	DRAM_A9	AE12	DRAM_A9
DRAM_DQM0	AC3	DRAM_DQM0	DRAM_A10	AA15	DRAM_A10
			DRAM_A11	AC12	DRAM_A11
DRAM_D8	AD5	DRAM_D8	DRAM_A12	AD12	DRAM_A12
DRAM_D9	AE5	DRAM_D9	DRAM_A13	AC17	DRAM_A13
DRAM_D10	AA6	DRAM_D10	DRAM_A14	AA12	DRAM_A14
DRAM_D11	AE7	DRAM_D11	DRAM_A15	Y12	DRAM_A15
DRAM_D12	AB5	DRAM_D12			
DRAM_D13	AC5	DRAM_D13	DRAM_SDBA0	AC15	DRAM_SDBA0
DRAM_D14	AB6	DRAM_D14	DRAM_SDBA1	Y15	DRAM_SDBA1
DRAM_D15	AC7	DRAM_D15	DRAM_SDBA2	AB12	DRAM_SDBA2
DRAM_SDQS1	AD6	DRAM_SDQS1			
DRAM_SDQS1_B	AE6	DRAM_SDQS1_B			
DRAM_DQM1	AC6	DRAM_DQM1			
DRAM_D16	AB7	DRAM_D16	DRAM_CS0	AD17	DRAM_CS0_B
DRAM_D17	AA8	DRAM_D17	DRAM_CS1		
DRAM_D18	AB9	DRAM_D18			
DRAM_D19	Y9	DRAM_D19			
DRAM_D20	Y7	DRAM_D20	DRAM_RAS	AB15	DRAM_RAS_B
DRAM_D21	Y8	DRAM_D21	DRAM_CAS	AE16	DRAM_CAS_B
DRAM_D22	AC8	DRAM_D22	DRAM_SDWE	AB16	DRAM_WE_B
DRAM_D23	AA9	DRAM_D23			
DRAM_SDQS2	AD8	DRAM_SDQS2			
DRAM_SDQS2_B	AE8	DRAM_SDQS2	DRAM_SDCKE0	Y11	DRAM_SDCKE0
DRAM_DQM2	AB8	DRAM_DQM2	DRAM_SDCKE1	AA11	
DRAM_D24	AE9	DRAM_D24	DRAM_SDODT0	AC16	DRAM_SDODT0
DRAM_D25	Y10	DRAM_D25	DRAM_SDODT1	AB17	
DRAM_D26	AE11	DRAM_D26			
DRAM_D27	AB11	DRAM_D27			
DRAM_D28	AC9	DRAM_D28			
DRAM_D29	AD9	DRAM_D29			
DRAM_D30	AD11	DRAM_D30	DRAM_RESET	Y6	DRAM_RESET_B
DRAM_D31	AC11	DRAM_D31			
DRAM_SDQS3	AC10	DRAM_SDQS3			
DRAM_SDQS3_B	AB10	DRAM_SDQS3			
DRAM_DQM3	AE10	DRAM_DQM3			
DRAM_D32	AA17	DRAM_D32	DRAM_SDCLK_0	AD15	DRAM_SDCLK0
DRAM_D33	AA18	DRAM_D33	DRAM_SDCLK_0	AE15	DRAM_SDCLK0_B
DRAM_D34	AC18	DRAM_D34			
DRAM_D35	AE19	DRAM_D35			
DRAM_D36	Y17	DRAM_D36			
DRAM_D37	Y18	DRAM_D37			
DRAM_D38	AB19	DRAM_D38			
DRAM_D39	AC19	DRAM_D39			
DRAM_SDQS4	AD18	DRAM_SDQS4			
DRAM_SDQS4_B	AE18	DRAM_SDQS4	DRAM_SDCLK_1	AD14	DRAM_SDCLK1
DRAM_DQM4	AB18	DRAM_DQM4	DRAM_SDCLK_1	AE14	DRAM_SDCLK1_B
DRAM_D40	Y19	DRAM_D40			
DRAM_D41	AB20	DRAM_D41			
DRAM_D42	AB21	DRAM_D42			
DRAM_D43	AD21	DRAM_D43			
DRAM_D44	Y20	DRAM_D44			
DRAM_D45	AA20	DRAM_D45			
DRAM_D46	AE21	DRAM_D46			
DRAM_D47	AC21	DRAM_D47			
	AD20	DRAM_SDQS5			
DRAM_SDQS5_B	AE20	DRAM_SDQS5			
DRAM_DQM5	AC20	DRAM_DQM5			
DRAM_D48	AC22	DRAM_D48			
DRAM_D49	AE22	DRAM_D49			
DRAM_D50	AE24	DRAM_D50			
DRAM_D51	AC24	DRAM_D51			
DRAM_D52	AB22	DRAM_D52			
DRAM_D53	AC23	DRAM_D53			
DRAM_D54	AD25	DRAM_D54			
DRAM_D55	AC25	DRAM_D55			
	AD23	DRAM_SDQS6			
DRAM_SDQS6	AE23	DRAM_SDQS6			
DRAM_SDQS6_B	AD24	DRAM_SDQS6			
DRAM_DQM6		DRAM_DQM6			
DRAM_D56	AB25	DRAM_D56			
DRAM_D57	AA21	DRAM_D57			
DRAM_D58	Y25	DRAM_D58			
DRAM_D59	Y22	DRAM_D59			
DRAM_D60	AB23	DRAM_D60			
DRAM_D61	AA23	DRAM_D61			
DRAM_D62	Y23	DRAM_D62			
DRAM_D63	W25	DRAM_D63			
DRAM_SDQS7	AA25	DRAM_SDQS7			
DRAM_SDQS7_B	AA24	DRAM_SDQS7			
DRAM_DQM7	Y21	DRAM_DQM7			

DRAM_VREF	AC2	NVCC_DRAM_1	T18
		NVCC_DRAM_2	U18
		NVCC_DRAM_3	V10
		NVCC_DRAM_4	V11
		NVCC_DRAM_5	V12
		NVCC_DRAM_6	V13
		NVCC_DRAM_7	V14
		NVCC_DRAM_8	V15
		NVCC_DRAM_9	V16
		NVCC_DRAM_10	V17
		NVCC_DRAM_11	V18
		NVCC_DRAM_12	V9
		NVCC_DRAM_13	
ZQPAD	AE17	ZQPAD	R18

DRAM_D[63:0]

DRAM_A[15:0]

DDR_1V5

U3 — 2G_DDR3_SDRAM_128MX16 — Top right

U5 — 2G_DDR3_SDRAM_128MX16 — Bottom under U3

U2 — 2G_DDR3_SDRAM_128MX16 — Top left

U4 — 2G_DDR3_SDRAM_128MX16 — Bottom under U2

MT41K128M16JT

Note 1

R89 240 GND

R599 240 GND

R99 240 GND

R119 240 GND

DDR_VREF

C653 0.22UF 16V GND

C47 0.22UF 16V GND

C717 0.22UF 16V GND

C618 0.22UF 16V GND

C72 0.22UF 16V GND

C56 0.22UF 16V GND

C734 0.22UF 16V GND

R635 10.0K 1%

R602 10.0K

SH21 DRAM_SDCLK0 — DRAM_SDCLK0

SH20 DRAM_SDCLK0_B — DRAM_SDCLK0_B

0

Clock access points

SH18 DRAM_SDCLK1 — DRAM_SDCLK1

SH19 DRAM_SDCLK1_B — DRAM_SDCLK1_B

0 GND probe pad

TP15 GND

C621 0.1UF 16V GND

R107 240 1%

DDR_1V5

1 GByte DDR3

T-point routing
Components allow pin to pin route length matching

T32 T62 T12 T43 T69 T19 T30 T55 T5 T44 T63 T13 T41 T67 T17 T28 T53 T3 T39 T65 T15 T26 T51 T1 T38 T64 T14 T29 T54 T4 T35 T59 T9 T42 T68 T18 T31 T56 T6 T27 T52 T2 T40 T66 T16 T33 T57 T7

DRAM_A0 DRAM_A1 DRAM_A2 DRAM_A3 DRAM_A4 DRAM_A5 DRAM_A6 DRAM_A7 DRAM_A8 DRAM_A9 DRAM_A10 DRAM_A11 DRAM_A12 DRAM_A13 DRAM_A14 DRAM_A15

T34 T58 T8 T45 T70 T20 T46 T71 T21 T36 T60 T10 T37 T61 T11 T49 T74 T24 T47 T72 T22 T48 T73 T23 T50 T75 T25

DRAM_SDBA0 DRAM_SDBA1 DRAM_SDBA2 DRAM_CS0_B DRAM_RAS_B DRAM_CAS_B DRAM_WE_B DRAM_SDCKE0 DRAM_SDODT0

C647 C613 C614 C666 C76 C48 0.22UF 16V 6.3V

C619 C728 C617 C616 C615 C620 0.22UF 6.3V 16V

C736 C735 C733 C732 C731 C718 0.22UF 16V

C75 C64 C737 C57 C58 C59 C67 0.22UF 16V

C70 C71 C73 C74 C79 C78 C49 0.22UF 16V 6.3V

C37 C53 C44 C46 C36 C35 22UF 6.3V 16V

C727 C45 C42 C41 C52 C43 C77 0.22UF 6.3V 16V

NOTE 1:

Using bit swapping for DATA bus to allow easy pcb routing.

When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.

NOTE 2:

Pull down resistor RX3 is added to trace SDCKE0 in Rev B4 by soldering to an existing open via. Change will be made permanent in layout with the Rev C board.

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ICAP Classification: FCP:___ FIUO:___ PUBI: X

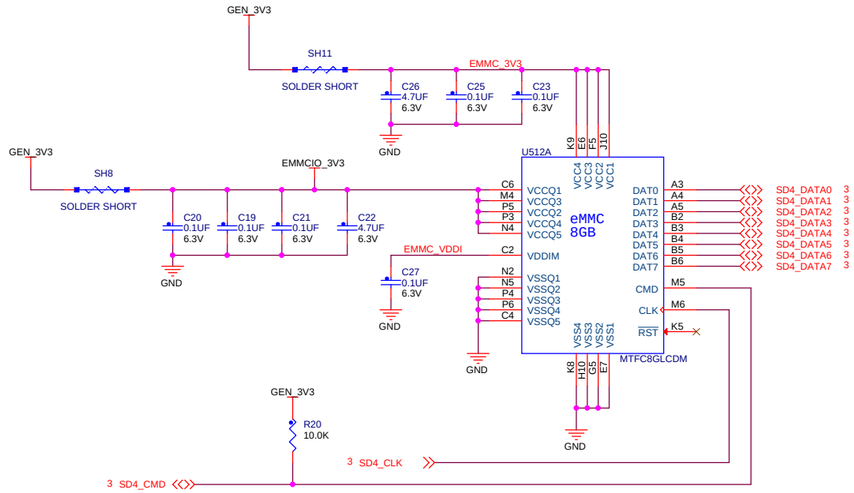
Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM

Page Title: DDR3 MEMORY

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 4 of 25

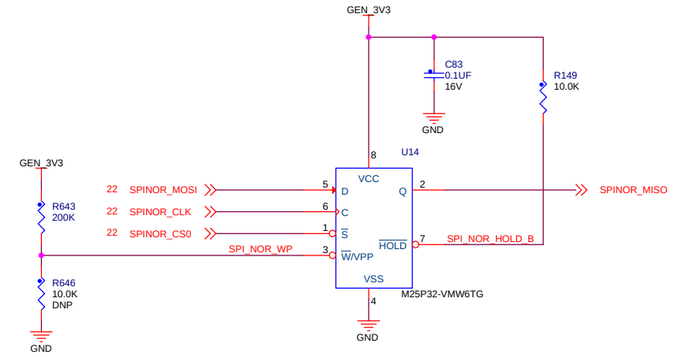
8GB eMMC MEMORY

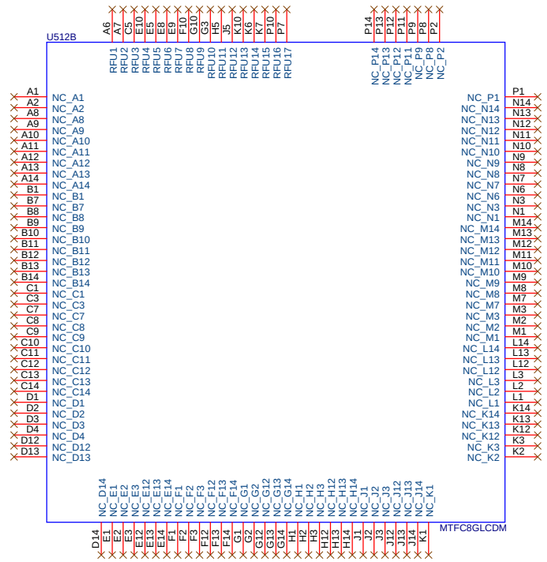


Layout:
50ohm, SD singals(SD_DATAx, SD_CMD, SD_CLK) control.

NOTE:
RST_B pin is not enabled by default. It must be turned on by software. Therefore, part with RST_B pin can be used in existing designs that do not connect this pin.

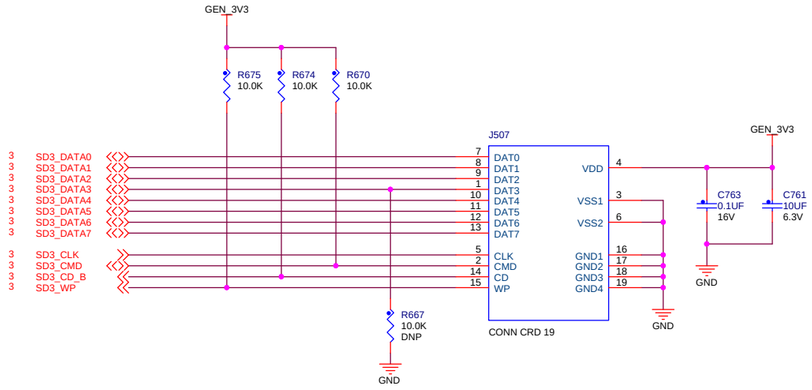
4MB SPI NOR FLASH





ICAP Classification:	FCP: ___	FIUO: ___	PUBI: X
Drawing Title:	MCIMX6DL-SMART DEVICE PLATFORM		
Page Title:	eMMC, SPI NOR FLASH		
Size: C	Document Number: SOURCE:SCH-27417 PDF:SPF-27417		Rev: C5
Date: Monday, February 16, 2015		Sheet 5 of 25	

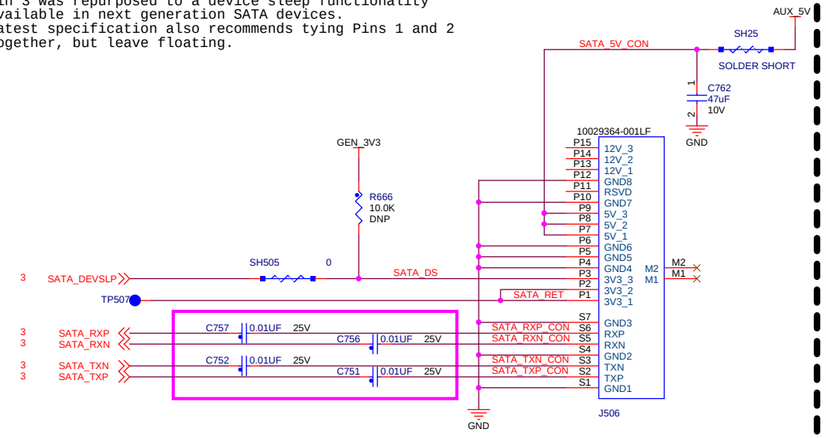
SD CARD SOCKET



Layout:
50ohm, SD signals(SD_DATAx, SD_CMD, SD_CLK) length equal

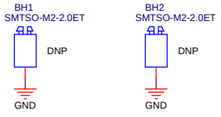
SATA CONNECTOR

NOTE:
The new SATA specification retires the 3V3 pins as they were not being used by regular sized SATA devices. Pin 3 was repurposed to a device sleep functionality available in next generation SATA devices. Latest specification also recommends tying Pins 1 and 2 together, but leave floating.



Layout:
1. 100ohm diff pairs, length equal
2. Mount these capacitors very close to the connector J506.

hard drive standoff



Note: The SATA interface on the i.MX6 DualLite Processor is disabled. These parts have been populated only to provide continuity with other Smart Devices that use the same PCB, and simplify manufacturing both MCIMX6Q-SDP and MCIMX6DL-SDP boards on the same manufacturing line.

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

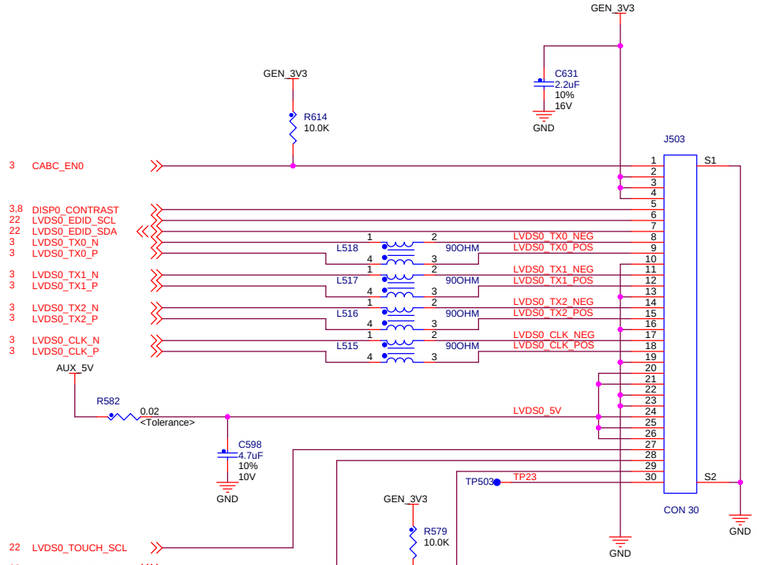
Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM

Page Title: SD CARD, SATA

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

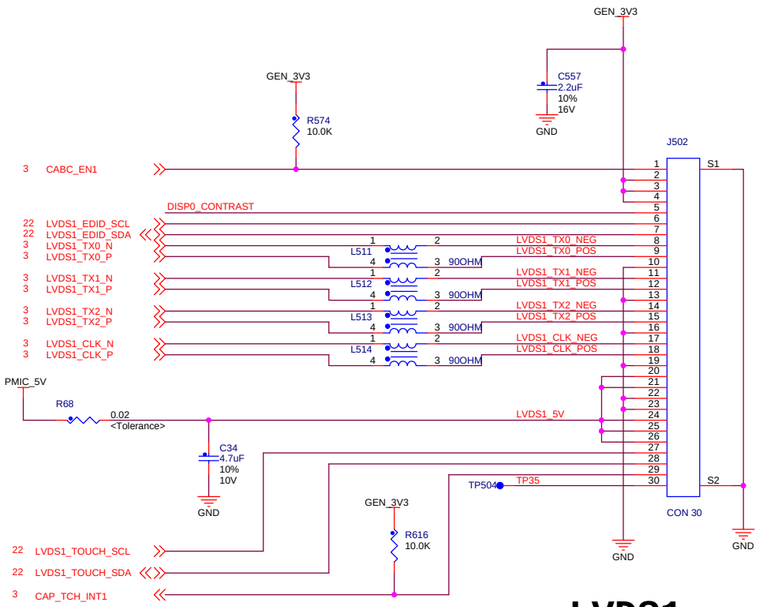
Date: Monday, February 16, 2015 Sheet 6 of 25

LVDS



Place L515, L516, L517 and L518
CMCs close to J403 connector.

LVDS0

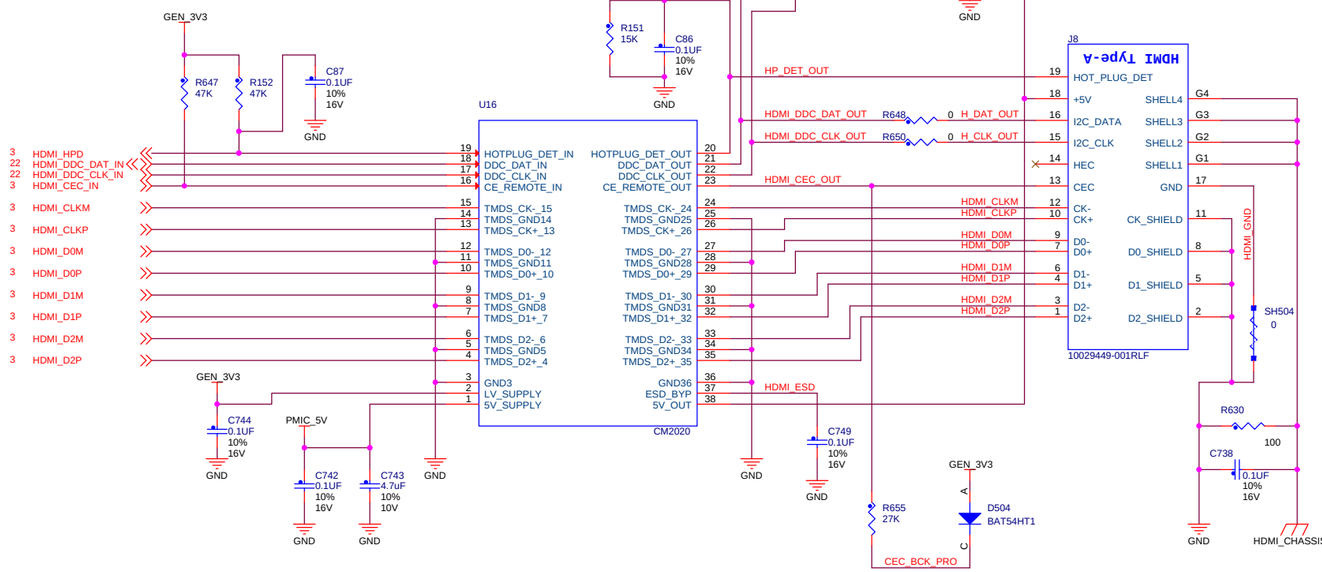


LVDS1

Layout: LVDS 100 ohm differential pairs

Place L511, L512, L513 and L514
CMCs close to J402 connector.

HDMI



Layout: HDMI 100 ohm differential pairs

NOTE:
When using HDMI, I2C2 bus is limited to 100 kHz
to read EDID values due to HDMI standards.
I2C2 bus speed should be limited to 100 kHz whenever
Hot Plug Detect is high.

LVDS Connector notes:
Pin 1: This pin is the Display Enable pin. It is used to
Enable/Disable the HannStar display.
Pin 5: This pin is the Display Brightness control. It
provides a PWM signal to the display to increase/
decrease display brightness depending on PWM
duty cycle. This signal is shared by all displays, so all
displays will change brightness together.

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

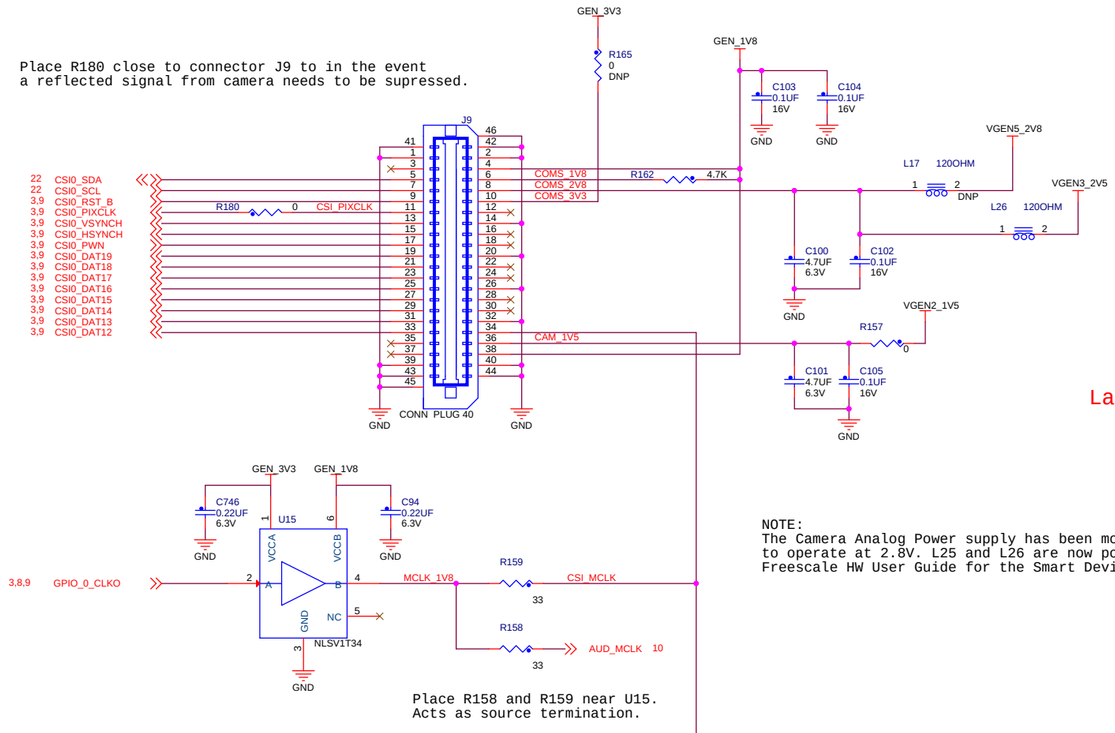
Drawing Title: **MCIMX6DL-SMART DEVICE PLATFORM**

Page Title: **LVDS, HDMI**

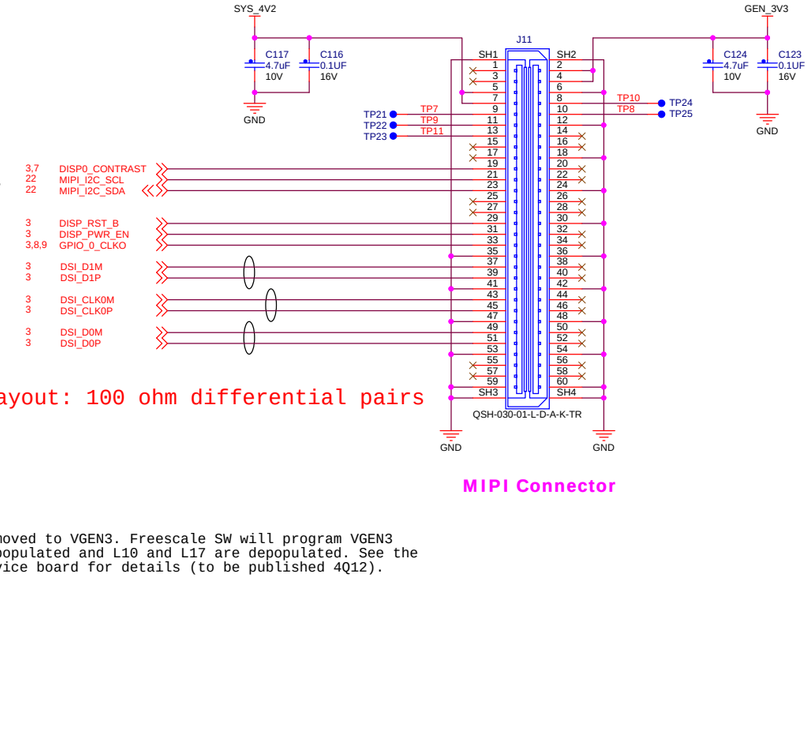
Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 7 of 25

CSI CMOS Sensor
OV5642 5M Pixel

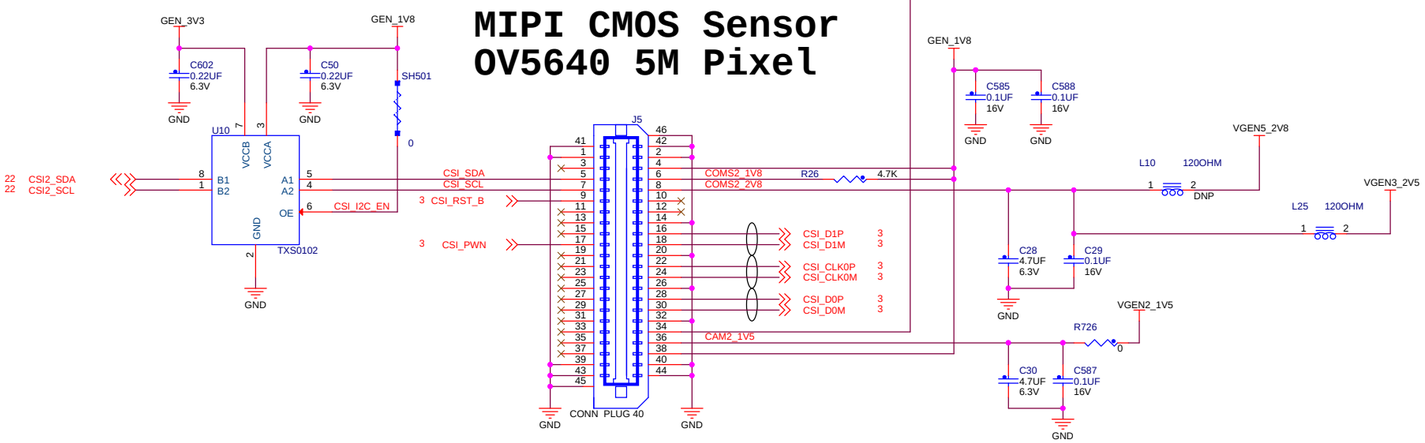


MIPI DISPLAY
EXP PORT



NOTE:
The Camera Analog Power supply has been moved to VGEN3. Freescale SW will program VGEN3 to operate at 2.8V. L25 and L26 are now populated and L10 and L17 are depopulated. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

MIPI CMOS Sensor
OV5640 5M Pixel



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ICAP Classification: FCP:___ FIUO:___ PUBI: X

Drawing Title:
MCIMX6DL-SMART DEVICE PLATFORM

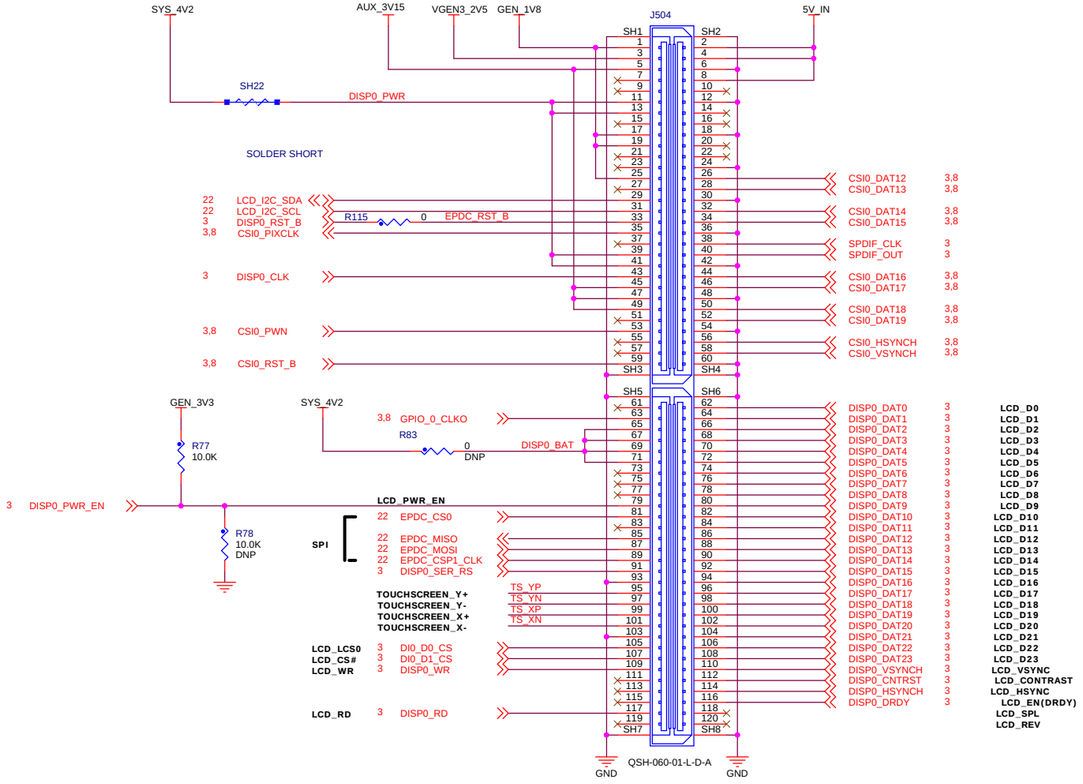
Page Title:
CAMERA, EXP PORT

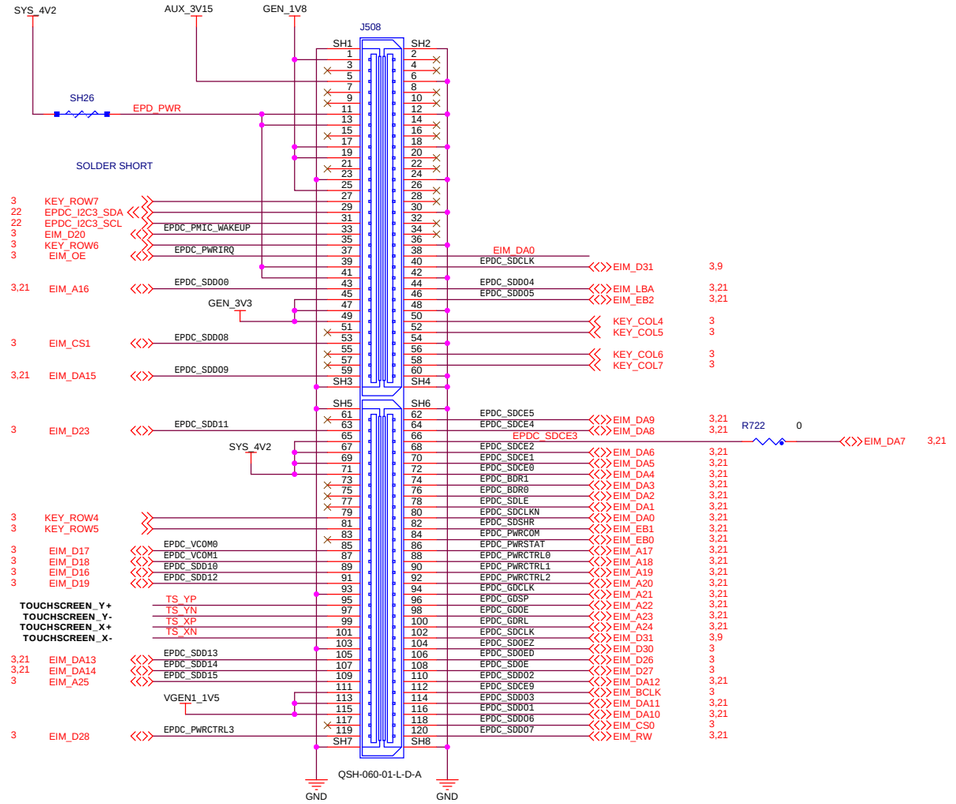
Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 8 of 25

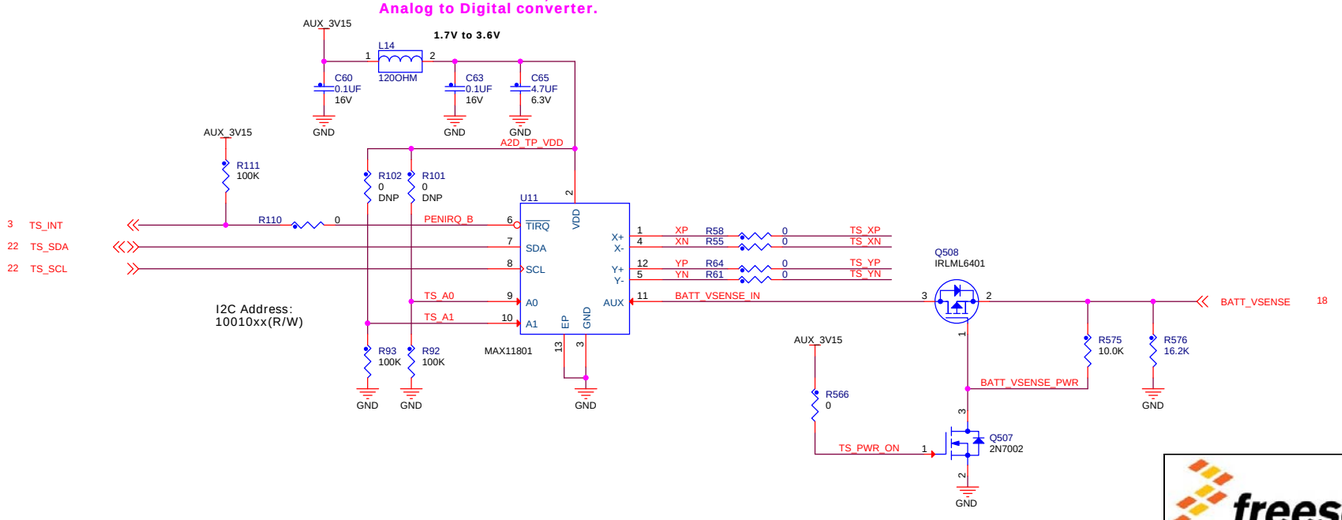
DISP0 Expansion Connector

For MX60 EPD





Touch Panel decoder, Analog to Digital converter.



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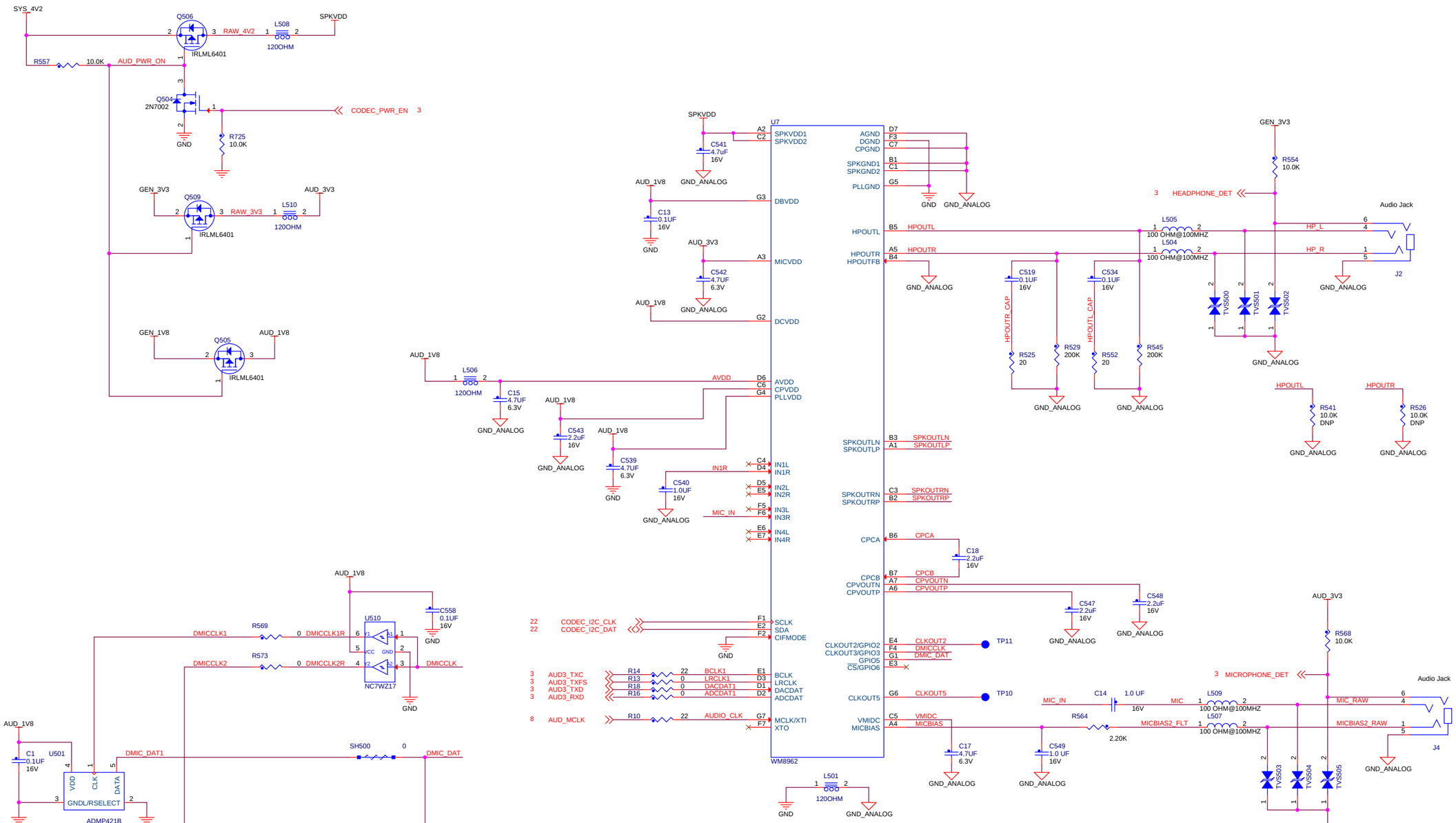
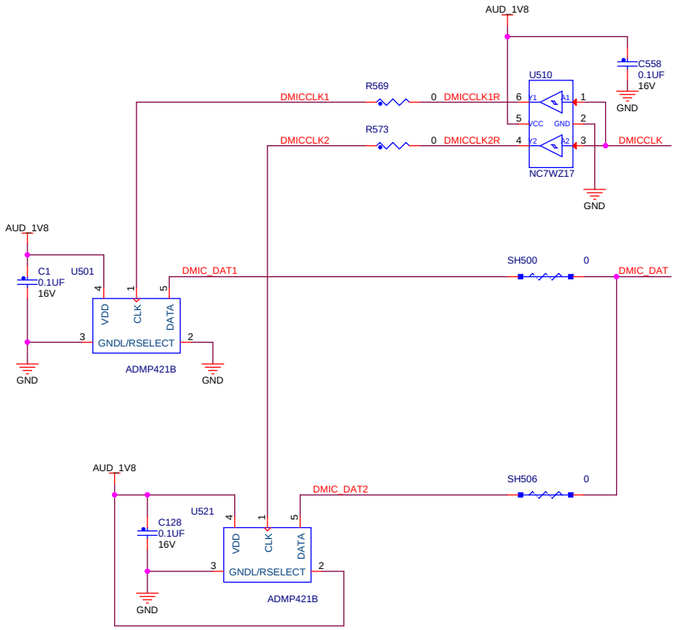
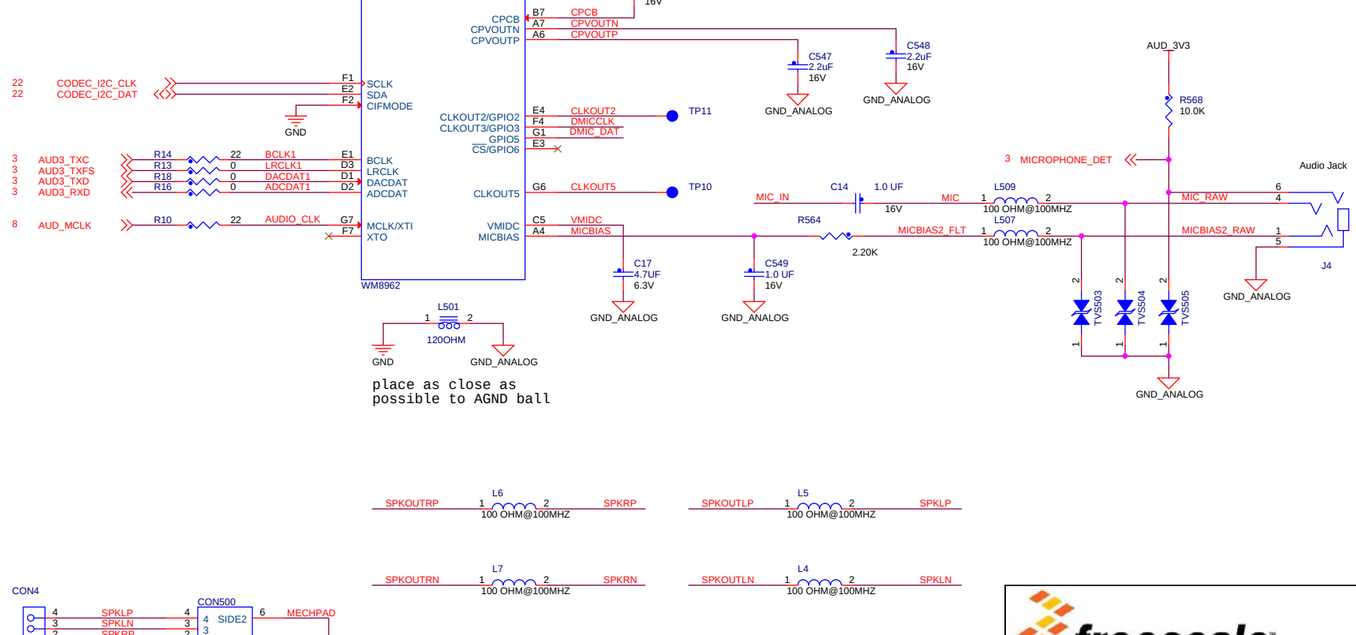
Size: C	Document Number: SOURCE:SCH-27417 PDF:SPF-27417		Rev: C5
Date: Monday, February 16, 2015	Sheet 9 of 25		







NOTE:
On Rev B4 boards, buffers U500 and U520 are removed, and a wire is added by hand connecting pins 2 and 4 together. On Rev C boards, the layout will be modified to remove the hand rework.

NOTE:
MECHPAD trace is for mechanical hold down tabs only.
There is no shield ground on this plastic connector.

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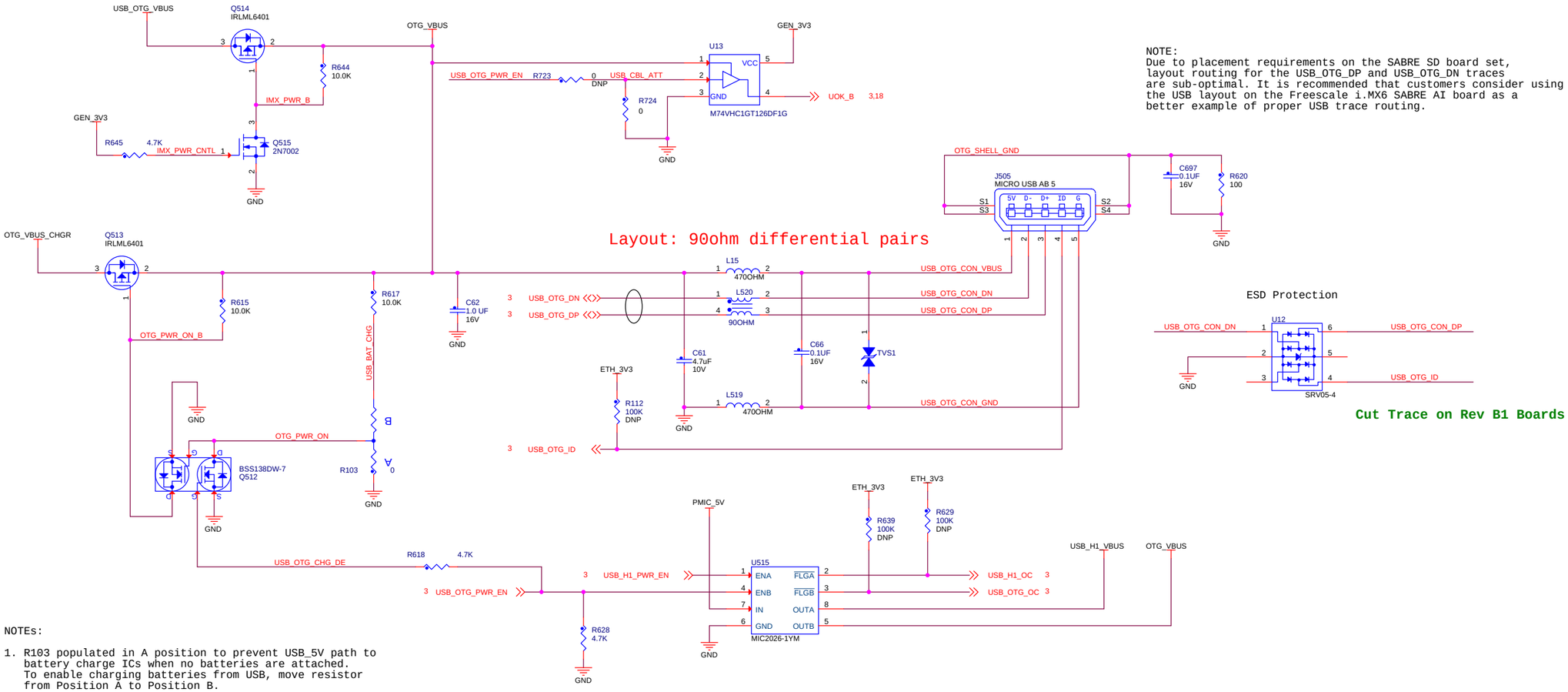
Drawing Title:	MCIMX6DL-SMART DEVICE PLATFORM
Page Title:	AUDIO
Size: C	Document Number: SOURCE:SCH-27417 PDF:SPF-27417 — Rev: C5
Date: Monday, February 16, 2015	Sheet 10 of 25



NOTEs:

1. R103 populated in A position to prevent USB_5V path to battery charge ICs when no batteries are attached. To enable charging batteries from USB, move resistor from Position A to Position B.

TRUTH TABLE
OTG_VBUS INPUT TO BATTERY CHARGERS

USB_OTG _PWR_EN	OTG_PWR _ON	OTG_PWR _ON_B	OTG_VBUS _CHGR
LOW	HIGH	LOW	POWERED
HIGH	LOW	HIGH	NOT POWERED

NOTE:
On all three pad resistor options, resistors are to be initially populated on pads 1 - 2 (Option A). Users may move resistors from their default locations as needed.

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Drawing Title:
MCIMX6DL-SMART DEVICE PLATFORM

Page Title:
USB

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 11 of 25

To Processor I/O supply

Alternate power source for processor I/O

NVCC_RGMII
VGEN1_1V5
SH23
0
ETH_VDDIO_REG
C84 1.0 UF 16V
C85 0.1UF 16V
GND

NOTE:
Solder short normally connects NVCC_RGMII to ETH_VDDIO.
To connect NVCC_RGMII to VGEN1_1V5, cut the trace between pads 1 - 2 and solder a 0 Ohm resistor between pads 2 - 3.

VGEN6_3V3
SH24
SOLDER SHORT
ETH_3V3

ETH_3V3
L18 120OHM
ETH_AVDD33
C88 1.0 UF 16V
C92 0.1UF 16V
C97 10UF 6.3V
C99 0.1UF 16V

2V5_RGMII
C96 1.0 UF 16V

DVDDL_RGMII
ETH_LX
L19 4.7UH
C91 10UF 6.3V
C93 0.1UF 16V
1.1V

Layout: High speed data lines : 50 ohms
Place R634 near the AR8031 PHY.

U516 AR8031
VDD33 AVDD33 VDDIO_REG VDDH_REG LX
DVDDL
L16 120OHM
AVDDL1 AVDDL2 AVDDL3 AVDDL4
ETH_AVDDL
C90 C89 C95 C98 0.1UF 16V

RGMII_TXCLK → GTX_CLK
RGMII_TXD0 RGMII_TXD1 RGMII_TXD2 RGMII_TXD3 → TXD0 TXD1 TXD2 TXD3
RGMII_TXEN → TX_EN
RGMII_RXCLK → R634 0 PHY_RX_CLK → RX_CLK
RGMII_RXD0 RGMII_RXD1 RGMII_RXD2 RGMII_RXD3 → RXD0 RXD1 RXD2 RXD3
RGMII_RXDV → RX_DV
SIP SIN SOP SON SD
RGMII_nRST → R659 0 PHY_RST → RST
ETH_WOL_INT → WOL_INT INT
RGMII_INT
TP18 TP25 → PPS
ENET_REF_CLK → R626 22 PHY_CLKO → CLK_25M
RGMII_MDC → MDC
MDIO
PHY_XTLO → XTLO
PHY_XTLI → XTLI
ETH_RBIAS → R166 2.37K 1% → RBIAS
GND

R161 10.0K DNP
R164 10.0K
R654 4.7K ETH_SD
R163 10.0K
R657 1.5K
Y500 25MHZ
C748 22PF
C750 22PF

NOTE:
Place R626 close to Ethernet PHY.

LED_LINK10_100 → RGMII_LED_10_100
LED_LINK1000 → RGMII_LED_1000
LED_ACT → RGMII_LED_ACT
C739 C740 C741 470PF DNP

EMI Filter Reserved
470pF are for LED

Layout: 100 ohm differential pairs

TRXP0 TRXN0 TRXP1 TRXN1 TRXP2 TRXN2 TRXP3 TRXN3
RGMII_TRXP0 RGMII_TRXN0 RGMII_TRXP1 RGMII_TRXN1 RGMII_TRXP2 RGMII_TRXN2 RGMII_TRXP3 RGMII_TRXN3

TP505 TP_404
C82 C81 C80 0.1UF 16V DNP

J7 V890-1AX1-A1
TRD1+ TRD1- TRD2+ TRD2- TRD3+ TRD3- TRD4+ TRD4-
TRDCT1/2/3/4
LEDYC LEDYA LEDGC LEDGA
GND SH1 SH2
R642 270 RGMII_LED_ACT
R640 270 RGMII_LED_10_100
RJ45_LED_ACT
RJ45_LED_10_100
R658 100
C747 0.1UF 16V
CGND3

RGMII_LED_1000
R641 270
LED_1000_O
D11 LED_ORANGE

Place LED D11 near LED for pins 11 - 12 of RJ-45 connector.
Orange LED indicates 1000 speed.

Power-on Strapping Pins

ETH_VDDIO_REG
R636 10.0K
R638 10.0K DNP

PHYADDRESS0	RGMII_RXD0	R144	10.0K DNP
PHYADDRESS1	RGMII_RXD1	R143	10.0K
MODE2[1]	RGMII_RXD2	R142	10.0K
MODE2[3]	RGMII_RXD3	R631	10.0K
MODE2[2]	PHY_RX_CLK	R146	10.0K
MODE2[0]	RGMII_RXDV	R145	10.0K
SEL_GPIO_INT (default) 0: INT 1:GPIO	RGMII_LED_1000	R141	10.0K
ANA_MOD Select the core voltage level: 0:1.1V, 1:1.2V	RGMII_LED_ACT	R140	10.0K

2V5_RGMII
R148 10.0K DNP
R147 10.0K DNP

MODE2[3:0]

(Default assemble: 0000)
1100 BaseT, RMII1;
1101 BaseT, RMII2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMII;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RGMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, RGMII, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved

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ICAP Classification: FCP:___ FIUO:___ PUBI: X

Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM

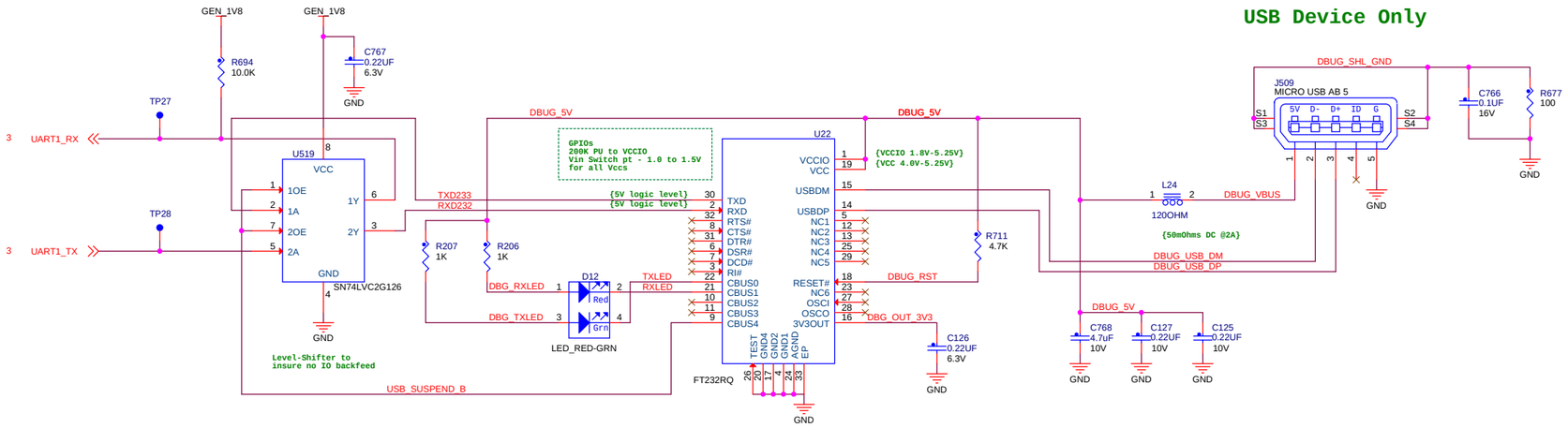
Page Title: ETHERNET

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 12 of 25

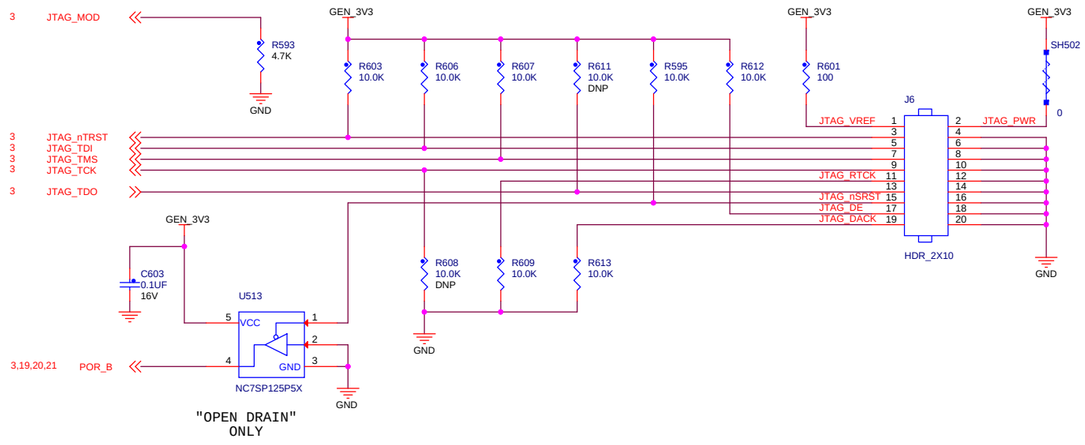
DEBUG UART TO USB CONVERSION

Library Revision - A



Drivers located at:
http://www.ftdichip.com/Products/ICs/FT232R.htm

JTAG



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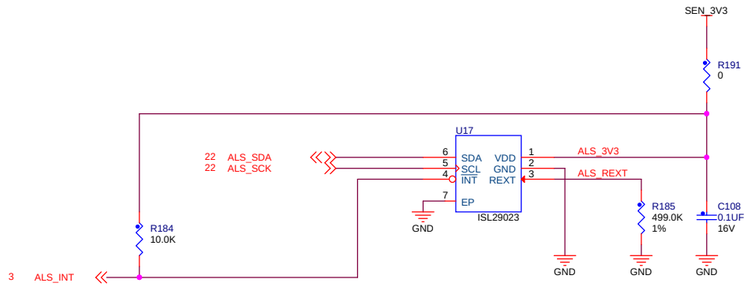
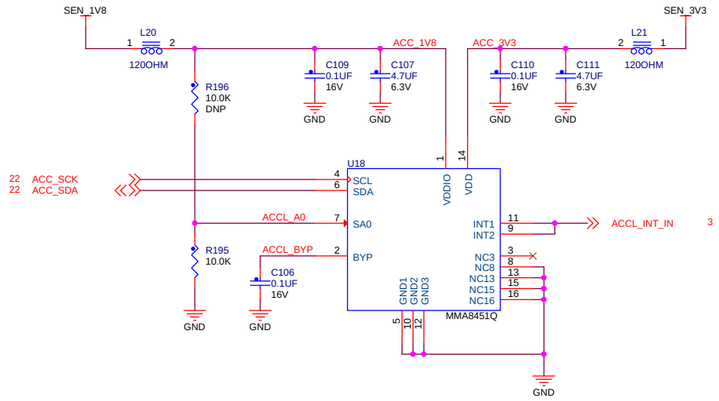
Size: C	Document Number: SOURCE:SCH-27417 PDF:SPF-27417		Rev: C5
Date: Monday, February 16, 2015		Sheet 13 of 25	

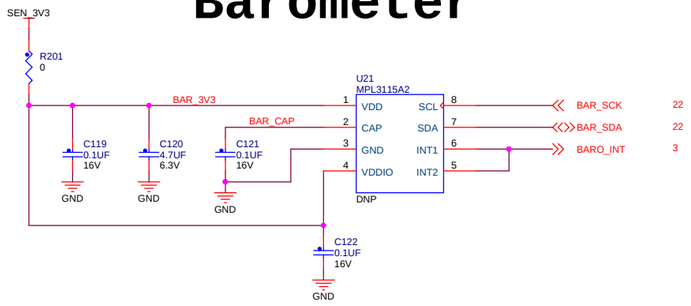
Ambient Light Sensor



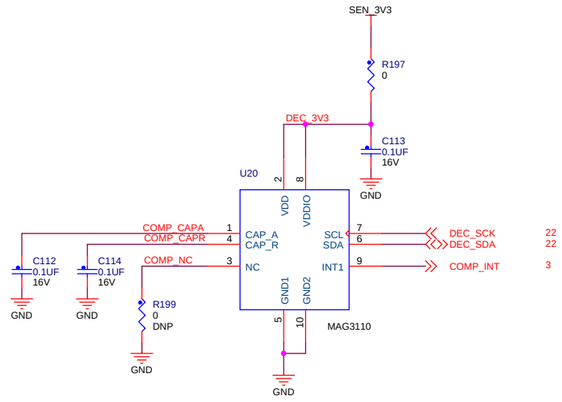
3-AXIS ACC

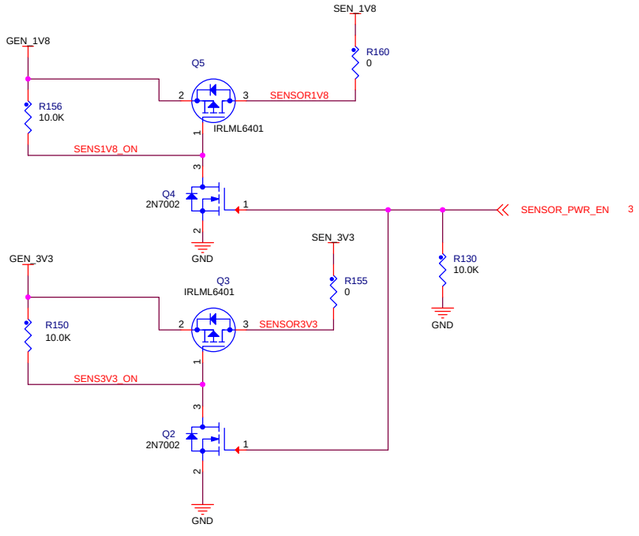


Barometer



Digital eCompass





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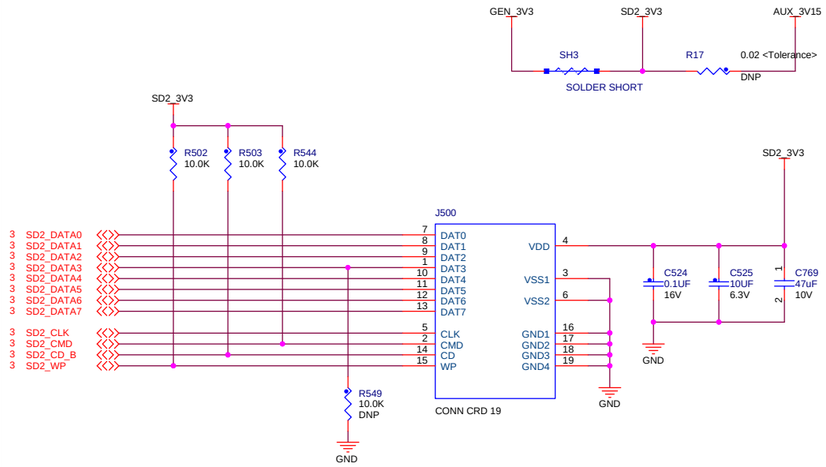
Drawing Title: **MCIMX6DL-SMART DEVICE PLATFORM**

Page Title: **SENSORS**

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 14 of 25

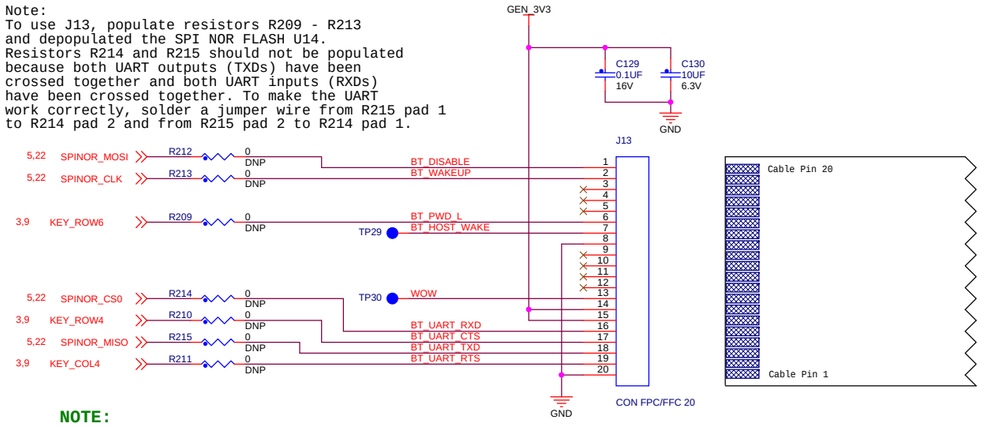
AUX SDIO CARD SOCKET



Layout:
50ohm, SD signals(SD_DATAx, SD_CMD, SD_CLK) length equal

BLUETOOTH CABLE CONNECTOR

Note:
To use J13, populate resistors R209 - R213
and depopulated the SPI NOR FLASH U14.
Resistors R214 and R215 should not be populated
because both UART outputs (TXDs) have been
crossed together and both UART inputs (RXDs)
have been crossed together. To make the UART
work correctly, solder a jumper wire from R215 pad 1
to R214 pad 2 and from R215 pad 2 to R214 pad 1.

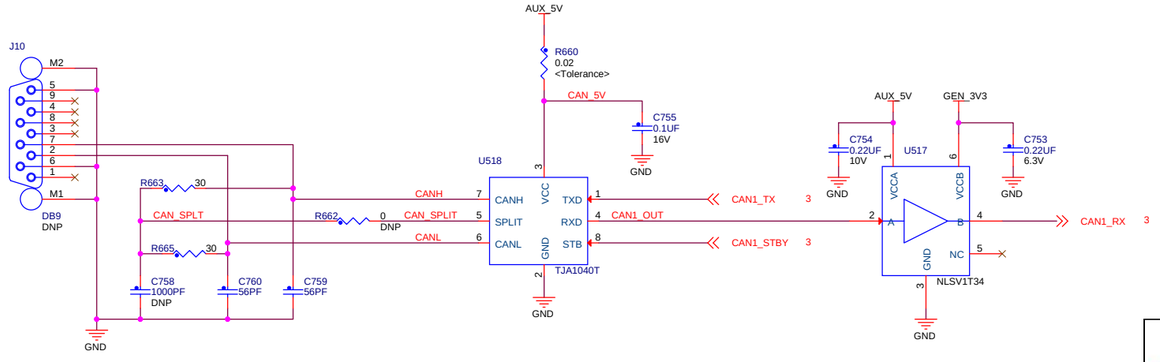


NOTE:
The AUX SDIO CARD SOCKET and the BLUETOOTH CABLE CONNECTOR have been designed and tested specifically for use with the WIFI/BT combo card SX-SDCAN-2830BT Developed and sold by Silex Technolgy. The developer may need to consult the datasheet of other WIFI solutions for compatibility with this card socket.

NOTE:
Pin 1 of the cable connector on the Smart Device board is opposite Pin 20 of the WIFI/BT module. For the FFC to lie flat, the pin order number needs to be reversed on the schematics.

NOTE:
J13 has been provided for testing the Bluetooth functionality of the SX-SDCAN-2830BT module. This part of the circuit has not yet been tested, which is why the initial boards are being shipped with isolation resistors R209 - R215 depopulated. Until fully tested, the developer assumes responsibilty for enabling J13 tor testing purposed. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

OPTIONAL CAN PINOUT



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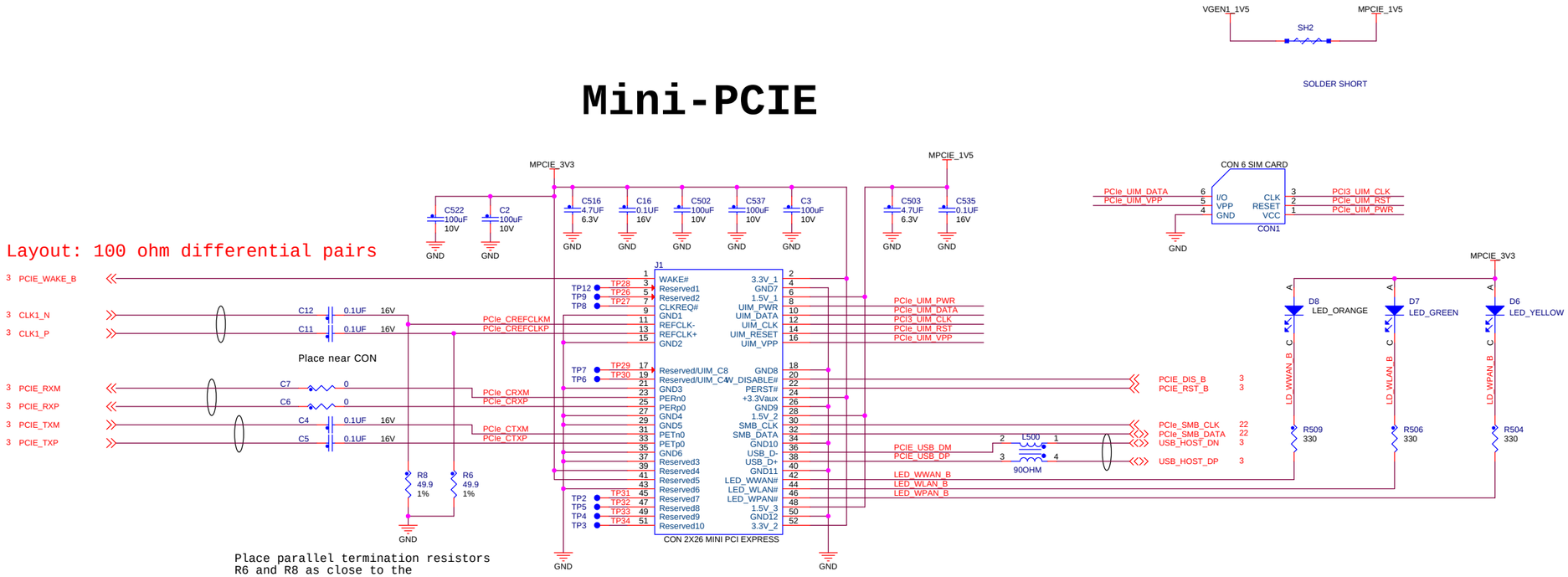
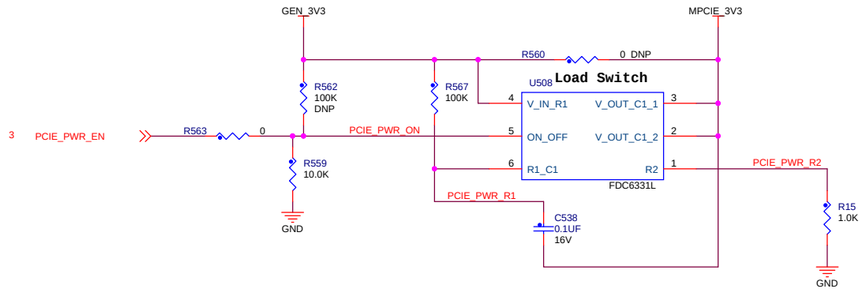
Page Title: AUX SDIO CONN, CAN			
Size C	Document Number SOURCE:SCH-27417 PDF:SPF-27417		Rev C5
Date: Monday, February 16, 2015		Sheet 15 of 25	

Mini-PCIE



NOTE:
This design assumes a normal loading on the MPCIE_3V3 rail of up to 1A. PF0100 SW2 can supply a maximum of 2A current. If more than 1A loading is desired, the designer must consider other load on the GEN_3V3 rail and depopulate other loads to allow additional loading on the MPCIE_3V3 rail. The MPCIE_1V5 rail is allowed a maximum of 100 mA.



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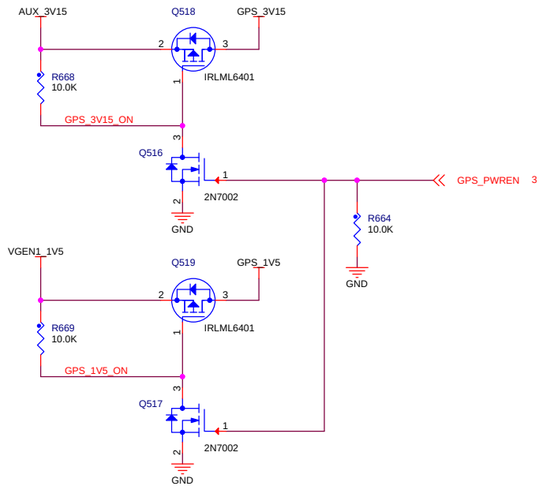
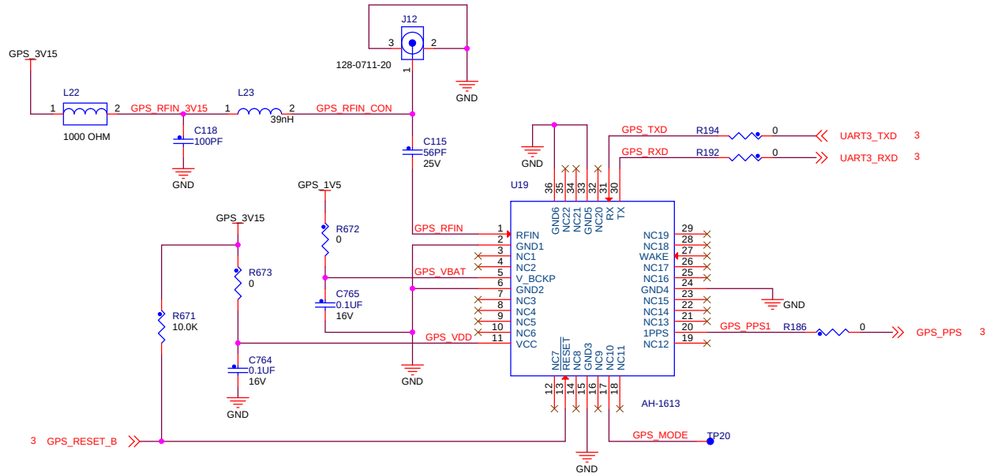
Page Title:	mPCIe CONN		
Size: C	Document Number: SOURCE:SCH-27417 PDF:SPF-27417		Rev: C5
Date: Monday, February 16, 2015		Sheet 16 of 25	

GPS Receiver





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Drawing Title:
MCIMX6DL-SMART DEVICE PLATFORM

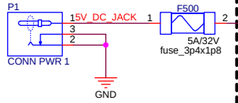
Page Title:
GPS MODULE

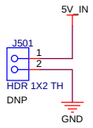
Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

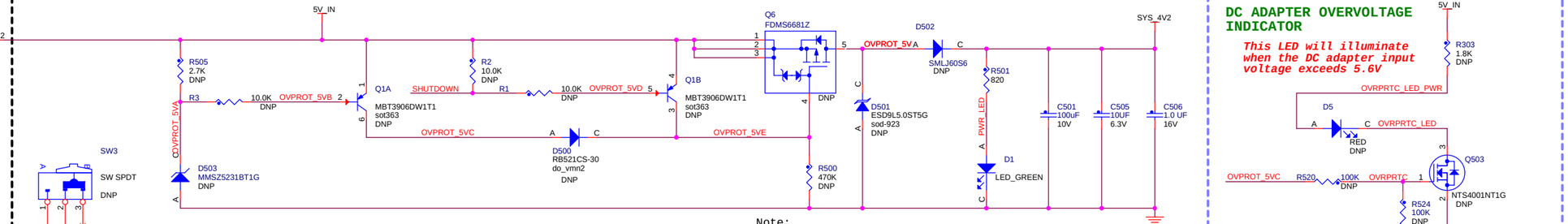
Date: Monday, February 16, 2015 Sheet 17 of 25

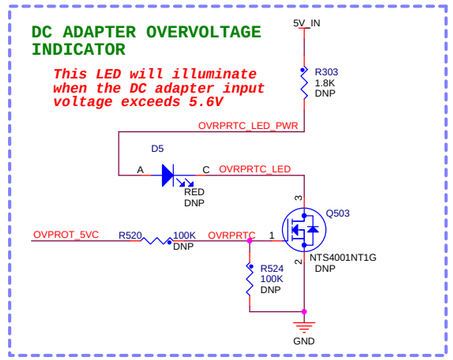
OVER VOLTAGE PROTECTION

External
Power
5 Vdc





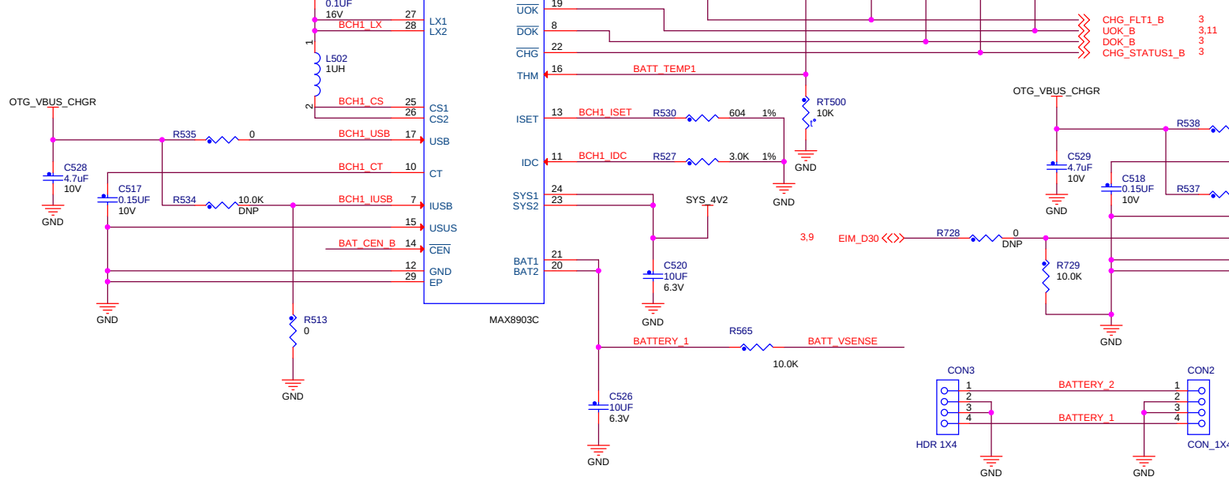




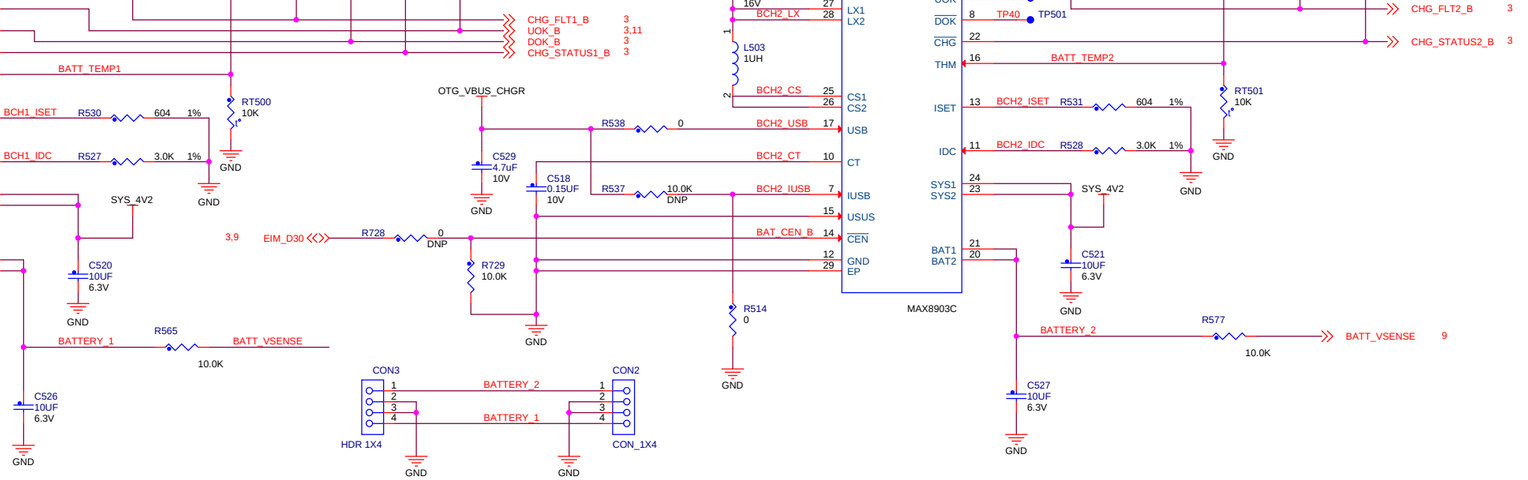
OPTION 1

Note:
Purpose for D502 is to provide voltage drop to lower input voltage below 4.5V maximum voltage level of PF0100 PMIC.

BATTERY 1 CHARGE CIRCUIT



BATTERY 2 CHARGE CIRCUIT



OPTION 2

NOTE:
Battery posts are meant for two, single cell 3.7 Li-ION batteries to be added in parallel.

Note: Populate either
Option #1 for the Smart Device Board, or
Option #2 for the Smart Device Platform

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM

Page Title: BATTERY CHARGER

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 18 of 25

PMIC LDO Outputs

PMIC Switched Outputs

PMIC Powered-ON LED indicator

PMIC Control

POWER

OPTIONAL: PMIC Power On Circuit

Note:
Bulk capacitors on VGEN1-6 are all 4.7uF for BOM consolidation purposes. Freescale recommended guidance for minimum capacitance on VGEN1, VGEN3, VGEN5, VGEN6 is 2.2uF.

NOTE:
R632 is provided for testing an alternate gating source for PMIC_5V power. The circuit has not yet been tested.

VDDOTP -

Connect TP14 to 8 volts to program PMIC OTP fuses

Note:
To turn off board "AUTO ON" feature, depopulate R30 and R31, and populate U509. This feature has not yet been tested.

Note:
PMPF0100 Pass1.0 through Pass1.2 are subject to boot issues if power is removed from the board and reapplied within ~ 2 minutes. PMPF0100 Pass2.0 will correct this issue. For more details, see the PMPF0100 ERRATA, Issue #ER19

Typical Power Requirements

	Voltage	Power Up Sequence	Current Drawn (mA)	SYS 4V2 Current (mA)	NOTES
SW1A / SW1B	1.375	1	2155	1001	
SW1C	1.375	2	1590	739	
SW2	3.3	5	653	728	
SW3A / SW3B	1.5	3	1500	760	
SW4	3.15	6	200	213	
SWBST	5.0	13	300	507	
VGEN1	1.5	9	100	0	Supplied from SW4
VGEN2	1.5	10	250	0	Supplied from SW4
VGEN3	2.8	11	70	66	
VGEN4	1.8	12	310	189	
VGEN5	2.8	10	75	71	See Note on Page 20
VGEN6	3.3	8	160	178	
VSNVS	3.0	0	0.2	0	
VREFDDR	0.75	3	10	3	
Total System Current Requirements:			4454		

SYSTEM POWER RAILS

Voltge	Rail Name	Block	Generated By	Current Capability (mA)	NOTES
5.0	PMIC_5V	USB	PF0100 SWBST	600	
		LVDS1			
		HDMI			
	AUX_5V	SATA	MAX8815	1000	
		LVDS0			
		CAN			
3.3	GEN_3V3	EMMC	PF0100 SW2	2000	NVCC_LCD NVCC_EIM0/1/2 NVCC_GPIO NVCC_SD2/3 NVCC_NANDF NAND_JTAG
		SD3			
		NOR			
		SATA			
		LVDS			
		HDMI			
		MIPI			
		mPCIe			
		SENSORS			
	VGEN6_3V3	ETH	PF0100 VGEN6	200	NVCC_ENET
3.15	AUX_3V15	EXP HDR	PF0100 SW4	1000	Supplies: VGEN1 VGEN2
		TOUCH			
		GPS			
2.8	VDDHIGH_IN	IMX6	PF0100 VGEN5	100	
	VGEN3_2V5	CAMERA	PF0100 VGEN3	100	
2.5	GEN_2V5	SATA	IMX6 VDDHIGH_CAP	TBD	NVCC_MIPI
		HDMI			
		MIPI			
		mPCIe			
1.8	GEN_1V8	AUDIO	PF0100 VGEN4	350	NVCC_SD1 NVCC_CSI
		CAMERA			
		ACC			
1.5	VGEN2_1V5	CAMERA	PF0100VGEN2	250	
	VGEN1_1V5	GPS	PF0100 VGEN1	100	
		mPCIe			
	DDR_1V5	DDR	PF0100 SW3A/B	2500	
1.375	VDDCORE	ARMCORE	PF0100 SW1A/B	2500	
	VDDSOC	VDDSOC	PF0100 SW1C	1750	
0.75	VREFDDR	DDR	PF0100 VREFDDR	10	

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ICAP Classification: FCP:___ FIUO:___ PUBI: X

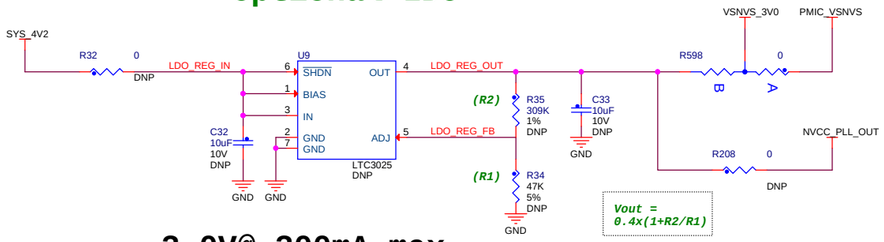
Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM

Page Title: PF0100 PMIC

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 19 of 25

Optional LDO



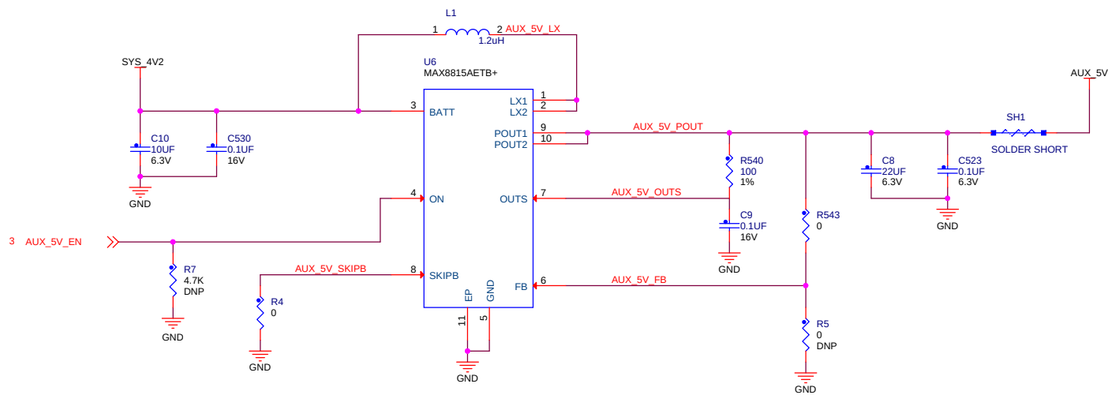
3.0V@ 300mA max

NOTE FOR VDDHIGH_IN LOADING ON VGEN5:
VDDHIGH was placed on VGEN5 early in the design as a compromise solution for a board designed primarily for software development. Validation of the i.MX6 processor has shown that operations at elevated temperatures may cause VDDHIGH_IN to require much more current than VGEN5 can supply. It is recommended for robust designs potentially operating at more extreme temperatures for VDDHIGH to be supplied from a power rail that can supply 250 mA or more.
This allows for datasheet maximum of 125 mA for internal VDDHIGH_IN loads plus 125 mA for external PHY IO loads.

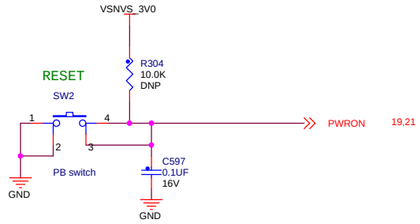
The optional LDO U9 shown on this page could be reconfigured to supply both VDDHIGH_IN and VDD_SNVS_IN loads to meet the additional current requirments

U9 is no longer required for PF0100 VSNVS issue, but may be desired for NVCC_PLL_VOUT.
It is being left in a depopulated condition. If the LDO is needed, R34 and R35 should be populated as follows:
For VSNVS (3.0V): R34 = 47K, R35 = 309K
For NVCC_PLL_OUT (1.1V): R34 = 47K, R35 = 82.5K

5.0V@1A DC2DC

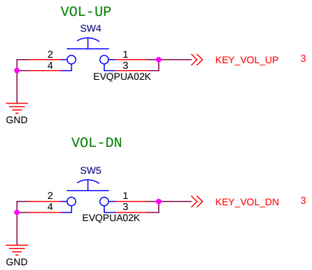


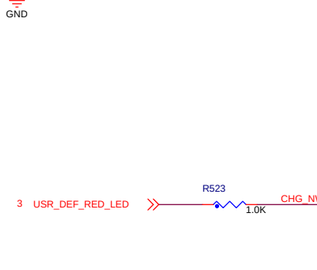
ICAP Classification:	FCP: ___ FIUO: ___ PUBI: X	
Drawing Title:	MCIMX6DL-SMART DEVICE PLATFORM	
Page Title:	AUX VOLT REG	
Size: C	Document Number: SOURCE:SCH-27417 PDF:SPF-27417	Rev: C5
Date: Monday, February 16, 2015	Sheet 20 of 25	

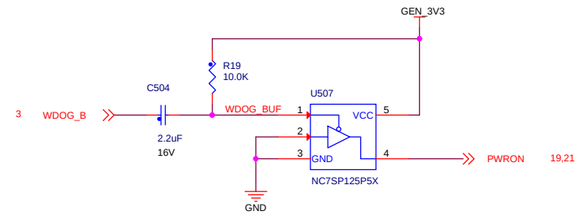


NOTE:
On Rev B4 and later designs, the RESET button is connected directly to the PWRON input of the PMIC. This will cause a complete board reset (Processor & PMIC) when the RESET button is pressed.

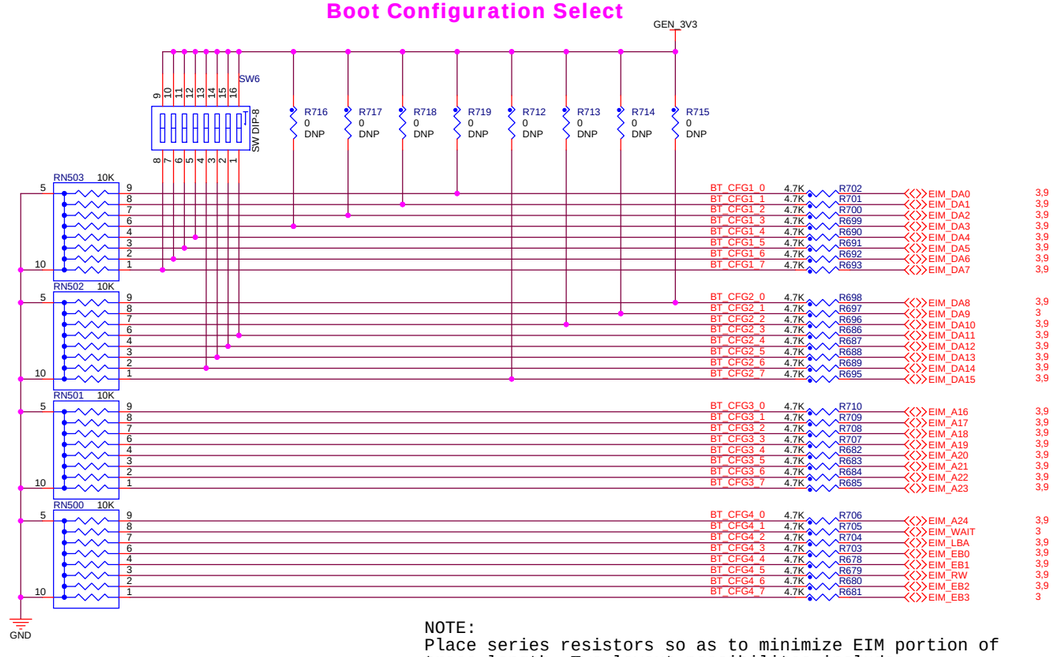
U/I KEY







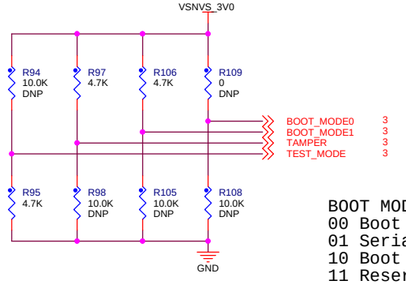
Boot Configuration Select



NOTE:
Place series resistors so as to minimize EIM portion of trace length. Two layout possibilites include:
1) As close to processor as possbile.
2) Close to other componets using EIM signals.

Boot Select Table

8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 10 = 8-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0010 = SATA Boot				X	X	X	0



BOOT MODES:
00 Boot from fuses
01 Serial downloader
10 Boot from board settings
11 Reserved

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

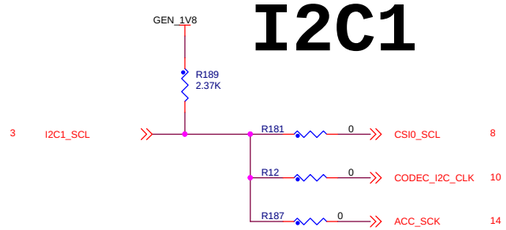
Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM

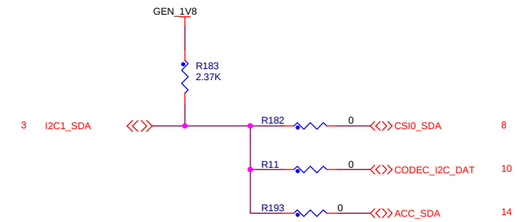
Page Title: BOOT SELECT

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 21 of 25

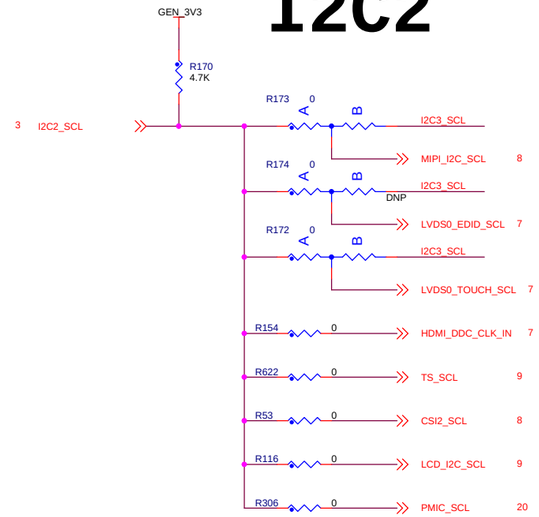
I2C1

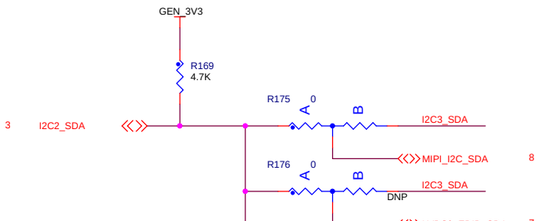




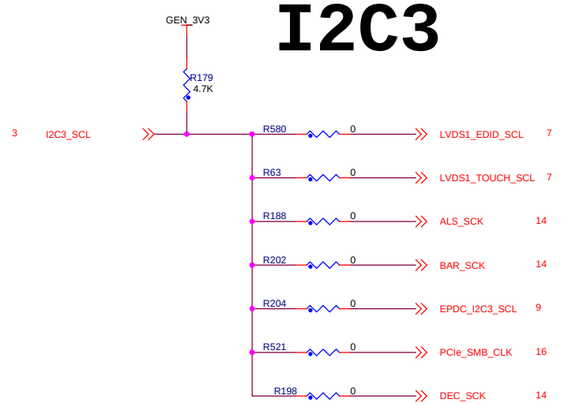
NOTE:
R183 and R189 were changed to bring I2C rise time from LOW >> HIGH within electric specification. If using a CODEC other than the one used in this design, it may be possbile to switch pull up resistors back to 4.7K.

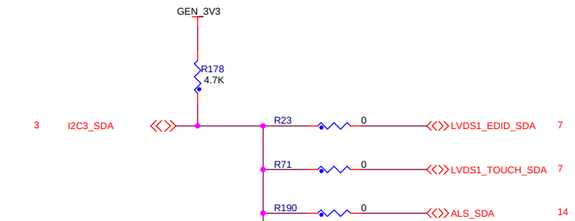
I2C2





I2C3





CSPI1

NOTE:
On all three pad resistor options, resistors are to be initially populated on pads 1 - 2 (Option A). Users may move resistors from their default locations as needed.

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM

Page Title: COMM CHANNEL STEERING

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 22 of 25

Build Option: MCIMX6Q-SDB

1.	CAN Output not populated: J10
2.	Battery Charging circuit not populated: C507, C508, C510, C511, C512, C513, C514, C515, C517, C518, C520, C521, C526, C527, C528, C529, CON2, CON3, L502, L503, R512, R513, R514, R515, R516, R518, R519, R527, R528, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R542, R565, R577, R729, RT500, RT501, U502, U503
3.	SPI NOR Flash not populated: C83, R149, R643, R646, U14
4.	MIPI Display/Camera Expansion Ports not populated: C28, C29, C30, C50, C116, C117, C123, C124, C585, C587, C588, C602, J11, J5, L25, R26, R165, R173, R175, R726, U10
5.	Audio Block Components not populated: C1, C128, C558, R569, R573, U501, U510, U521
6.	EPDC Port Connector not populated: J508
7.	Ambient Light Sensor not populated: C108, R184, R185, R188, R190, R191, U17
8.	GPS Module not populated: C115, C118, C764, C765, J12, L22, L23, Q516, Q517, Q518, Q519, R186, R192, R194, R664, R668, R669, R671, R672, R673, U19
9.	Extra Bulk Capacitors not populated: C39, C54, C68, C606, C607, C608, C609, C610, C611, C612, C673, C681
10.	BlueTooth Connector Isolation Resistors: R209, R210, R211, R212, R213, R214, R215

Build Option: MCIMX6Q-SDP MCIMX6DL-SDP

1.	CAN Output not populated: J10
2.	OverVoltage Protection circuit not populated: (OverVoltage Protection provided by battery charge ICs) D5, D500, D501, D502, D503, J501, Q1, Q6, Q503, R1, R2, R3, R303, R500, R505, R520, R524, SW3
3.	Extra Bulk Capacitors not populated: C39, C54, C68, C606, C607, C608, C609, C610, C611, C612, C673, C681
4.	BlueTooth Connector Isolation Resistors: R209, R210, R211, R212, R213, R214, R215

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Drawing Title:
MCIMX6DL-SMART DEVICE PLATFORM

Page Title:
BUILD OPTON TABLES

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 | Sheet 23 of 25

PIN MUX TABLES

Ball Name	Ball Number	IO MUX	Use
CSI0_DAT10	M1	ALT3	UART1_TXD_MUX
CSI0_DAT11	M3	ALT3	UART1_RXD_MUX
CSI0_DAT12	M2	ALT0	CSI0_D[12]
CSI0_DAT13	L1	ALT0	CSI0_D[13]
CSI0_DAT14	M4	ALT0	CSI0_D[14]
CSI0_DAT15	M5	ALT0	CSI0_D[15]
CSI0_DAT16	L4	ALT0	CSI0_D[16]
CSI0_DAT17	L3	ALT0	CSI0_D[17]
CSI0_DAT18	M6	ALT0	CSI0_D[18]
CSI0_DAT19	L6	ALT0	CSI0_D[19]
CSI0_DAT4	N1	ALT4	AUD3_TXC
CSI0_DAT5	P2	ALT4	AUD3_TXD
CSI0_DAT6	N4	ALT4	AUD3_TXFS
CSI0_DAT7	N3	ALT4	AUD3_RXD
CSI0_DAT8	N6	ALT4	I2C1_SDA
CSI0_DAT9	N5	ALT4	I2C2_SCL
CSI0_MCLK	P4	ALT0	CSI0_HSYNC
CSI0_PIXCLK	P1	ALT0	CSI0_PIXCLK
CSI0_VSYNC	N2	ALT0	CSI0_VSYNC
DI0_DISP_CLK	N19	ALT1	DI0_DISP_CLK
DI0_PIN15	N21	ALT1	DISP0_DRDT
DI0_PIN2	N25	ALT1	DISP0_HSYNCH
DI0_PIN3	N20	ALT1	DISP0_VSYNCH
DI0_PIN4	P25	ALT1	DISP0_CONTRST
DISP0_DAT0	P24	ALT1	DISP0_DAT[0]
DISP0_DAT1	P22	ALT1	DISP0_DAT[1]
DISP0_DAT10	R21	ALT1	DISP0_DAT[10]
DISP0_DAT11	T23	ALT1	DISP0_DAT[11]
DISP0_DAT12	T24	ALT1	DISP0_DAT[12]
DISP0_DAT13	R20	ALT1	DISP0_DAT[13]
DISP0_DAT14	U25	ALT1	DISP0_DAT[14]
DISP0_DAT15	T22	ALT1	DISP0_DAT[15]
DISP0_DAT16	T21	ALT1	DISP0_DAT[16]
DISP0_DAT17	U24	ALT1	DISP0_DAT[17]
DISP0_DAT18	V25	ALT1	DISP0_DAT[18]
DISP0_DAT19	U23	ALT1	DISP0_DAT[19]
DISP0_DAT2	P23	ALT1	DISP0_DAT[2]
DISP0_DAT20	U22	ALT1	DISP0_DAT[20]
DISP0_DAT21	T20	ALT1	DISP0_DAT[21]
DISP0_DAT22	V24	ALT1	DISP0_DAT[22]
DISP0_DAT23	W24	ALT1	DISP0_DAT[23]
DISP0_DAT3	P21	ALT1	DISP0_DAT[3]
DISP0_DAT4	P20	ALT1	DISP0_DAT[4]
DISP0_DAT5	R25	ALT1	DISP0_DAT[5]
DISP0_DAT6	R23	ALT1	DISP0_DAT[6]
DISP0_DAT7	R24	ALT1	DISP0_DAT[7]
DISP0_DAT8	R22	ALT1	DISP0_DAT[8]
DISP0_DAT9	T25	ALT1	DISP0_DAT[9]
EIM_D21	H20	ALT4	USB_OTG_OC
EIM_D22	E23	ALT4	USB_OTG_PWR_EN
EIM_D24	F22	ALT2	UART3_TXD_MUX
EIM_D25	G22	ALT2	UART3_RXD_MUX
EIM_D30	J20	ALT6	USB_H1_OC
ENET_MDC	V20	ALT1	MDC
ENET_MDIO	V23	ALT1	MDIO
ENET_REF_CLK	V22	ALT1	ENET_TX_CLK
ENET_RX_ER	W23	ALT0	USB_OTG_ID
GPIO_0	T5	ALT0	CLKO
GPIO_1	T4	ALT1	WDOG_B
GPIO_3	R7	ALT2	I2C3_SCL
GPIO_6	T3	ALT3	I2C3_SDA
GPIO_7	R3	ALT3	TXCAN
GPIO_8	R5	ALT3	RXCAN
GPIO_16	R2	ALT1	No-Connect
KEY_COL0	W5	ALT0	SCLK
KEY_COL1	U7	ALT0	MISO
KEY_COL3	U5	ALT4	I2C2_SCL
KEY_ROW0	V6	ALT0	CSPI1_MOSI
KEY_ROW1	U6	ALT0	CSPI1_SS0
KEY_ROW3	T7	ALT4	I2C2_SDA
KEY_ROW2	W4	ALT6	HDMI_CEC_IN

Ball Name	Ball Number	IO MUX	Use
NANDF_D4	A19	ALT1	SD2_DAT4
NANDF_D5	B18	ALT1	SD2_DAT5
NANDF_D6	E17	ALT1	SD2_DAT6
NANDF_D7	C18	ALT1	SD2_DAT7
RGMII_RD0	C24	ALT1	RGMII_RD0
RGMII_RD1	B23	ALT1	RGMII_RD1
RGMII_RD2	B24	ALT1	RGMII_RD2
RGMII_RD3	D23	ALT1	RGMII_RD3
RGMII_RX_CTL	D22	ALT1	RGMII_RX_CTL
RGMII_RXC	B25	ALT1	RGMII_RXC
RGMII_TD0	C22	ALT1	RGMII_TD0
RGMII_TD1	F20	ALT1	RGMII_TD1
RGMII_TD2	E21	ALT1	RGMII_TD2
RGMII_TD3	A24	ALT1	RGMII_TD3
RGMII_TX_CTL	C23	ALT1	RGMII_TX_CTL
RGMII_TXC	D21	ALT1	RGMII_TXC
SD1_DAT3	F18	ALT3	PWMO
SD2_CLK	C21	ALT0	SD2_CLK
SD2_CMD	F19	ALT0	SD2_CMD
SD2_DAT0	A22	ALT0	SD2_DAT0
SD2_DAT1	E20	ALT0	SD2_DAT1
SD2_DAT2	A23	ALT0	SD2_DAT2
SD2_DAT3	B22	ALT0	SD2_DAT3
SD3_CLK	D14	ALT0	SD3_CLK
SD3_CMD	B13	ALT0	SD3_CMD
SD3_DAT0	E14	ALT0	SD3_DAT0
SD3_DAT1	F14	ALT0	SD3_DAT1
SD3_DAT2	A15	ALT0	SD3_DAT2
SD3_DAT3	B15	ALT0	SD3_DAT3
SD3_DAT4	D13	ALT0	SD3_DAT4
SD3_DAT5	C13	ALT0	SD3_DAT5
SD3_DAT6	E13	ALT0	SD3_DAT6
SD3_DAT7	F13	ALT0	SD3_DAT7
SD4_CLK	E16	ALT0	SD4_CLK
SD4_CMD	B17	ALT0	SD4_CMD
SD4_DAT0	D18	ALT1	SD4_DAT0
SD4_DAT1	B19	ALT1	SD4_DAT1
SD4_DAT2	F17	ALT1	SD4_DAT2
SD4_DAT3	A20	ALT1	SD4_DAT3
SD4_DAT4	E18	ALT1	SD4_DAT4
SD4_DAT5	C19	ALT1	SD4_DAT5
SD4_DAT6	B20	ALT1	SD4_DAT6
SD4_DAT7	D19	ALT1	SD4_DAT7

Reserved For i.MX6DLS

NANDF_WP_B	E15	ALT5	DISP0_WR
EIM_RW	K20	ALT8	EPDC_SDDO7
EIM_LBA	K22	ALT8	EPDC_SDDO4
EIM_CS0	H24	ALT8	EPDC_SDDO6
EIM_EB1	K23	ALT8	EPDC_SDSHR
EIM_EB2	E22	ALT8	EPDC_SDDO5
EIM_A16	H25	ALT8	EPDC_SDDO0
EIM_A18	J22	ALT8	EPDC_PWRCTRL0
EIM_A21	H23	ALT8	EPDC_GDCLK
EIM_A22	F24	ALT8	EPDC_GDSP
EIM_A23	J21	ALT8	EPCD_GDOE
EIM_A24	F25	ALT8	EPDC_GDRL
EIM_D17	F21	ALT8	EPDC_VCOM0
EIM_D27	E25	ALT8	EPDC_SDOE
EIM_D31	H21	ALT8	EPDC_SDCLK
EIM_DA1	J25	ALT8	EPDC_SDLE
EIM_DA2	L21	ALT8	EPDC_BDR0
EIM_DA3	K24	ALT8	EPDC_BDR1
EIM_DA4	L22	ALT8	EPDC_SDCE0
EIM_DA5	L23	ALT8	EPDC_SDCE1
EIM_DA6	K25	ALT9	EPDC_SDCE2
EIM_DA10	M22	ALT8	EPDC_SDDO1
EIM_DA11	M20	ALT8	EPDC_SDDO3
EIM_DA12	M24	ALT8	EPDC_SDDO2

Ball Name	Ball Number	IO MUX	Use	GPIO Function	Direction	Active
SD1_CMD	B21	ALT5	GPIO1[18]	ACCL_INT_IN	Input	High
EIM_DA9	M21	ALT5	GPIO3[9]	ALS_INT	Input	High
NANDF_WP_B	E15	ALT5	GPIO6[9]	DISP0_WR	Output	High
NANDF_RB0	B16	ALT5	GPIO6[10]	AUX_5V_EN	Output	High
EIM_DA15	N24	ALT5	GPIO3[15]	BARO_INT	Input	High
NANDF_CS2	A17	ALT5	GPIO6[15]	CABC_EN0	Output	High
NANDF_CS3	D16	ALT5	GPIO6[16]	CABC_EN1	Output	High
GPIO_19	P5	ALT5	GPIO4[5]	CAN1_STBY	Output	High
NANDF_ALE	A16	ALT5	GPIO6[8]	CAP_TCH_INT0	Input	High
NANDF_CLE	C15	ALT5	GPIO6[7]	CAP_TCH_INT1	Input	High
EIM_A25	H19	ALT5	GPIO5[2]	CHG_FLT1_B	Input	Low
EIM_DA14	N23	ALT5	GPIO3[14]	CHG_FLT2_B	Input	Low
EIM_D23	D25	ALT5	GPIO3[23]	CHG_STATUS1_B	Input	Low
EIM_DA13	M23	ALT5	GPIO3[13]	CHG_STATUS2_B	Input	Low
KEY_COL2	W6	ALT5	GPIO4[10]	CODEC_PWR_EN	Output	High
EIM_D16	C25	ALT5	GPIO3[16]	COMP_INT	Input	High
SD1_DAT2	E19	ALT5	GPIO1[19]	CSI_PWN	Output	High
SD1_CLK	D20	ALT5	GPIO1[20]	CSI_RST_B	Output	High
SD1_DAT0	A21	ALT5	GPIO1[16]	CSI0_PWN	Output	High
SD1_DAT1	C20	ALT5	GPIO1[17]	CSI0_RST_B	Output	High
EIM_WAIT	M25	ALT5	GPIO5[0]	DI0_DO_CS	Output	High
EIM_BCLK	N22	ALT5	GPIO6[31]	DI0_D1_CS	Output	High
NANDF_CS1	C16	ALT5	GPIO6[14]	DISP0_PWR_EN	Output	High
EIM_D28	G23	ALT5	GPIO3[28]	DISP0_RD	Output	High
EIM_DA8	L24	ALT5	GPIO3[8]	DISP0_RST_B	Output	Low
NANDF_CS0	F15	ALT5	GPIO6[11]	DISP0_RST_B	Output	Low
EIM_CS1	J23	ALT5	GPIO2[24]	DOK_B	Input	Low
EIM_A17	G24	ALT5	GPIO2[21]	E_PMIC_GOOD_B	Input	Low
EIM_D20	G20	ALT5	GPIO3[20]	EPDC_PMIC_WAKEUP	Output	High
EIM_A19	G25	ALT5	GPIO2[19]	EPDC_PWRCTRL1	Output	High
EIM_A20	H22	ALT5	GPIO2[18]	EPDC_PWRCTRL2	Output	High
EIM_OE	J24	ALT5	GPIO2[25]	EPDC_PWRIRQ	Input	High
ENET_TX_EN	V21	ALT5	GPIO1[28]	ETH_WOL_INT	Input	High
EIM_D18	D24	ALT5	GPIO3[18]	GPS_PPS	Input	High
EIM_DA0	L20	ALT5	GPIO3[0]	GPS_PWREN	Output	High
EIM_EB0	K21	ALT5	GPIO2[28]	GPS_RESET_B	Output	Low
SD3_RST	D15	ALT5	GPIO7[8]	HEADPHONE_DET	Input	Low
GPIO_5	R4	ALT5	GPIO1[5]	KEY_VOL_DN	Input	Low
GPIO_4	R6	ALT5	GPIO1[4]	KEY_VOL_UP	Input	Low
KEY_COL4	T6	ALT5	GPIO4[14]	PCIE_DIS_B	Output	Low
GPIO_17	R1	ALT5	GPIO7[12]	PCIE_RST_B	Output	Low
EIM_D19	G21	ALT5	GPIO3[19]	PCIE_PWR_EN	Output	High
GPIO_18	P6	ALT5	GPIO7[13]	PMIC_INT_B	Input	Low
EIM_D29	J19	ALT5	GPIO3[29]	PWR_BTN_SNS	Input	High
ENET_CRS_DV	U21	ALT5	GPIO1[25]	RGMII_NRST	Output	High
NANDF_D2	F16	ALT5	GPIO2[2]	SD2_CD_B	Input	Low
NANDF_D3	D17	ALT5	GPIO2[3]	SD2_WP	Input	High
NANDF_D0	A18	ALT5	GPIO2[0]	SD3_CD_B	Input	Low
NANDF_D1	C17	ALT5	GPIO2[1]	SD3_WP	Input	High
EIM_EB3	F23	ALT5	GPIO2[31]	SENSOR_PWR_EN	Output	High
EIM_DA7	L25	ALT5	GPIO3[7]	KP_LOCK	Input	High
EIM_D26	E24	ALT5	GPIO3[26]	TS_INT	Input	High
ENET_RXD0	W21	ALT5	GPIO1[27]	UOK_B	Input	Low
ENET_RXD1	W22	ALT5	GPIO1[26]	RGMII_INT	Input	High
ENET_TXD0	U20	ALT5	GPIO1[30]	DISP0_WR	Output	High
ENET_TXD1	W20	ALT5	GPIO1[29]	USB_H1_PWR_EN	Output	High
GPIO_2	T1	ALT5	GPIO1[2]	USR_DEF_RED_LED	Output	High
GPIO_9	T2	ALT6	GPIO1[9]	MICROPHONE_DET	Input	Low
KEY_ROW4	V5	ALT5	GPIO4[15]	SATA_DEVSLP	Output	High
CSI0_DATA_EN	P3	ALT5	GPIO5[20]	PCIE_WAKE_B	Input	Low

I2C1 Bus (1.8V)

Peripheral	Bus Activity Level	Speed (kbps)	Addresses (hex)	Default Address (hex)
CSI Bus Camera	Low	400	Write: 0x78	Write: 0x78
Auido CODEC	Low	400	0x34, 0x36	0x34
MMA 8451Q Accelerometer	Low	400	0x3A, 0x39	0x39

I2C1_SDA = CSI0_DAT8
I2C1_SCL = CSI0_DAT9

I2C2 Bus (3.3V)

Peripheral	Bus Activity Level	Speed (kbps)	Addresses (hex)	Default Address (hex)
PF0100 PMIC	Low	400	0x08 - 0x0F	0x08
MIPI Bus Camera	Low	400	0x3C	0x3C
MIPI Bus Display	TBD	TBD	TBD	TBD
HDMI EDID	Low	100	0x50	0x50
LVDS0 EDID	Low	100	0x50	0x50
LVDS0 TOUCH SCREEN	High	400	0x82	0x82
RGB TFT LCD DISPLAY	TBD	TBD	TBD	TBD
LCD TOUCH SCREEN	Low	400	0x68, 0x69, 0x6A, 0x6B	0x68

I2C2_SDA = KEY_ROW3
I2C2_SCL = KEY_COL3

I2C3 Bus (3.3V)

Peripheral	Bus Activity Level	Speed (kbps)	Addresses (hex)	Default Address (hex)
LVDS1 EDID	Low	100	0x50	0x50
LVDS1 TOUCH SCREEN	High	400	0x82	0x82
PCIe EXP PORT	TBD	TBD	TBD	TBD
EPDC DISPLAY CARD	Low	400	0x68, 0x69, 0x6A, 0x6B	0x68
AMBIENT LIGHT SENSOR	Low	400	0x44	0x44
DIGITAL eCOMPASS	Low	400	0x0E	0x0E
BAROMETER	Low	400	0x60	0x60

I2C3_SDA = GPIO_16
I2C3_SCL = GPIO_3

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ICAP Classification: FCP:___ FIUO:___ PUBI: X

Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM

Page Title: PIN MUX TABLE

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 24 of 25

HISTORY OF TEMPORARY DEVIATIONS

TDA 4100

1. Digital microphone ANALOG DEVICES ADMP421 was used in place of WOLFSON WM7230 due to supply shortage. Affects U500 and U520.

TDA 4112

Replaced TDA 4100
1. Digital microphone ANALOG DEVICES ADMP421 was used in place of WOLFSON WM7230 due to supply shortage. Affects U500 and U520.
2. Q512 was depopulated due to schematic mistake. Removes battery charge from USB option.
3. Depopulate R30 on MCIMX6DL-SD boards only. i.MX6DL Processor configured for Smart PMIC mode. Not compatible with board design. Removes SW ability to shutdown the board.

TDA 4136

1. Solder a 0402 2.2M Ohm resistor across pins of C55. Some i.MX6Q Processors require this resistor to stabalize the 24MHz crystal circuit, in order to start up within the required time interval.

TDA 4221 (6DL) / TDA 4222 (6Q)

1. Schematic revision B3 changed DDR3 memory to MT41K128M16JT-125:K. Due to unavailability of new part, this TDA autorizes the continued use of MT41J128M16HA-15.
2. Change C540 to 1.0uF capacitor.
3. Change resistors R183 and R189 to 2.37K Ohm resistors.

TDA 4275

1. Remove buffers U500 and U520 from digital Microphone data signal. Replace with hand wire mod.
2. Add WDOG_B reset capability (UX1, RX2, CX1).
3. Add diode DX1 to EIM_D19 to allow GPIO sense of power button press.
4.Change RESET button press to connect to PMIC PWRON pin. RESET press now causes global reset.
5. Add 10K pull down resistor RX3 to SDCKE0 pin.
6. Depopulate Resistors R174 and R176 to disconnect LVDS0 EDID from I2C2 communications channel.
7. Populate Battery Conector Header CON3.
8. Populate SIM Card Connector CON1.
9. Remove U1 from BOM (in preparation for next revision MX 6 silicon).
10. On MCIMX6DL-SDP boards, populate resistor R30 with 1K Ohm resistor.

TDA 4425

1. Depopulate ferrite beads L10 and L17.
2. Populate ferrite beads L25 and L26 (wih Murata BLM18PG121SH1).

TDA 4502

1. Change R17, R21, R25, R27, R68, R85, R582, and R660 to 0.5% resistors due to parts availability.

TDA 4516

1. Change R17, R21, R25, R27, R68, R85, R582, and R660 to 1.0% resistors due to parts availability.

TDA 4538

1. U8 PMIC was installed without F0 programming (U8 not stamped F0). TDA is to program part in place.

CHANGE REVISION DEFECT TRACKING

REV:	Change:	Reference Defect Number:
B4	Removed buffers U500 and U520 from digital microphone data outputs.	ENGR00181056 ENGR00211969
B4	The Battery Charge Done LED is disconnected and R522 is depopulated. New parts RX2, CX1 and UX1 are added. Traces show required hand modifications.	ENGR00211943
B4	Optional Power On Circuit has been disabled and U511 and R578 are now DNP. A new Diode DX1 has been added to allow EIM_D29 to sense a button	ENGR00181039 ENGR00211948
B4	RESET button SW2 now connects to The PWRON pin of The PMIC.	ENGR00211979
B4	Added 10K pull down resistor RX3 to SDCKE0 trace.	ENGR00211962
B4	SIM Card Connector CON1 is now populated by default.	ENGR00224087
B4	Battery Connector Header CON3 is now populated by default.	ENGR00224089
B4	Changed resistors R174 and R176 and to depopulated by default. LVDS0 EDID will not be connected to I2C2 channel unless needed.	ENGR00211965
B4	Replaced digital microphones with Analog Devices ADMP421.	ENGR00211964
B4	Disabled USR_DEF_GRN_LED circuit. Configured GPIO_1 for WDOG_B output.	ENGR00211973
C	Q512 is Changed to populated.	ENGR00211943
C	Optional Start Up Circuit has been modified.	ENGR00181039
C	PMIC Programming Micro-Processor is removed.	ENGR00224090
C	Add DNP Input to U13 buffer for USB_OTG_PWR_EN. Buffer now powered from GEN_3V3.	ENGR00319341
C	FA_ANA and VDD_FA signals now connected to ground.	ENGR00213511
C	Added resistor options to EIM_DA7 trace to EPD connector.	ENGR00181054 ENGR00211953
C	Connected EIM_DA9 to EPDC Connector J508 to supply SDCE5 if needed.	ENGR00213510
C	Optional LDO U9 is now depopulated.	ENGR00224091
C	Added Connector J13 to support BT from SDIO Card. Connector is isolated by DNP resistors on Rev C boards.	ENGR00181035 ENGR00211946
C	Added GPIO control of Battery Charge Enable pins.	ENGR00217643
C	Changed C594 to 0.22uF, changed C31 to 47uF, added C555 as second 22uF capacitor in parallel with C546, changed C561, C562, C586 and C596 to 0.47uF. Changes made per recommendation of MMPF0100NPEP team.	ENGR00224093
C	Added additional 47uF bulk capacitor C769 to SD2 socket VDD supply.	ENGR00224094
C	Added option to route HDMI DDC comms seperate from I2C2 comms channel.	ENGR00215026
C	C597 populated to provide de-bounce to RESET circuit.	ENGR00224095
C	Depopulated C68, C612. Populated C682, C716 closer to pins.	ENGR00224096
C	Depopulated C39, C606, C607, C608, C609, C610, C673 and C681.	ENGR00224097
C	Added DNP R302 to provide alternate 5V supply path to USB_H1_VBUS.	ENGR00224098
C	Added DNP R632 to provide alternate gating of PMIC_5V source (tied to VDDSOC).	ENGR00224098
C	Added DNP L25 and L26 to provide alternate 2.8V supply path to camera modules.	ENGR00224099
C	Added TP31, TP32, TP509, and TP510 to bring out third data lane for both LVDS0 and LVDS1.	ENGR00214325 ENGR00214502
C	Change blocking capacitors C6 and C7 to Zero Ohm resistors R307 and R308. PCIe specification requires blocking capacitors to be on transmit side of	ENGR00226040
C2	Depopulate L10 and L17. Move Ferrite beads to L25 and L26	ENGR00231769
C3	Changed R97 and R106 pull up resistors to 4.7K to reduce current on VSNVS	ENGR00237171
C3	Changed R19 to 10K pull up resistor to prevent WDOG reset during POR.	ENGR00234394
C3	Added note to BlueTooth connector that RXD and TXD traces are crossed.	ENGR00239363

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX6DL-SMART DEVICE PLATFORM

Page Title: TEMPORARY DEVIATIONS

Size	Document Number	Rev
C	SOURCE:SCH-27417 PDF:SPF-27417	C5

Date: Monday, February 16, 2015 Sheet 25 of 25