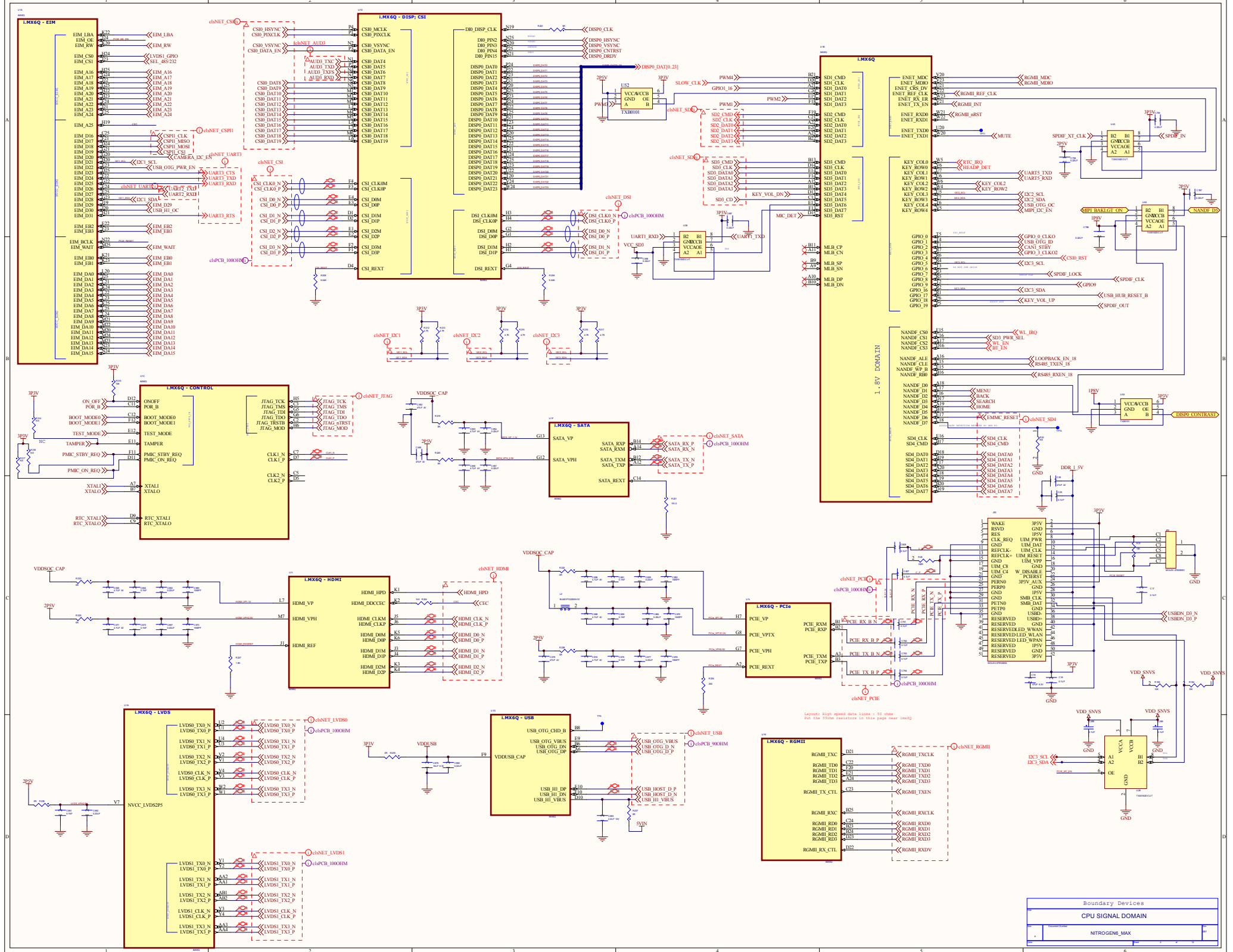
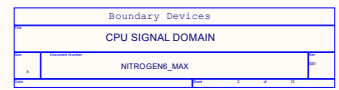
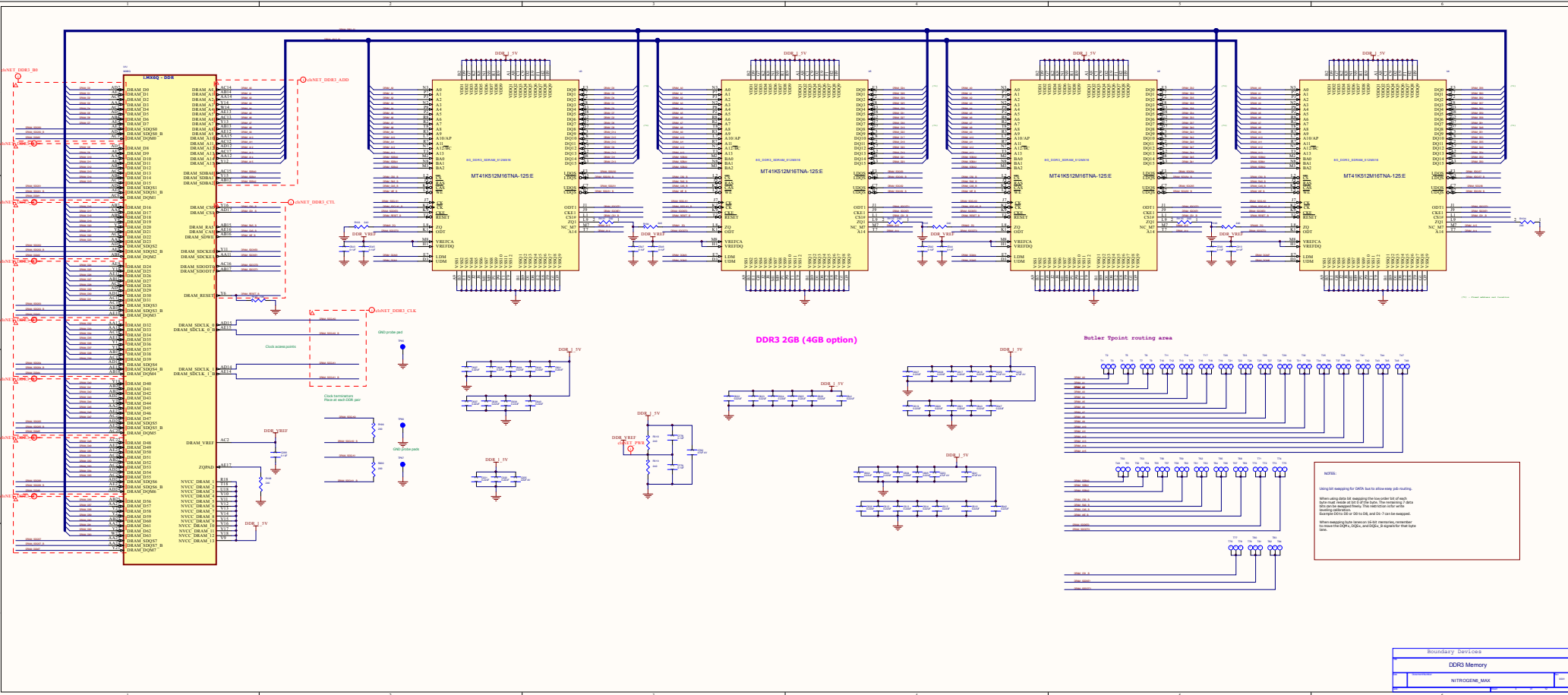


Boundary Devices	
CPU POWER DOMAIN	
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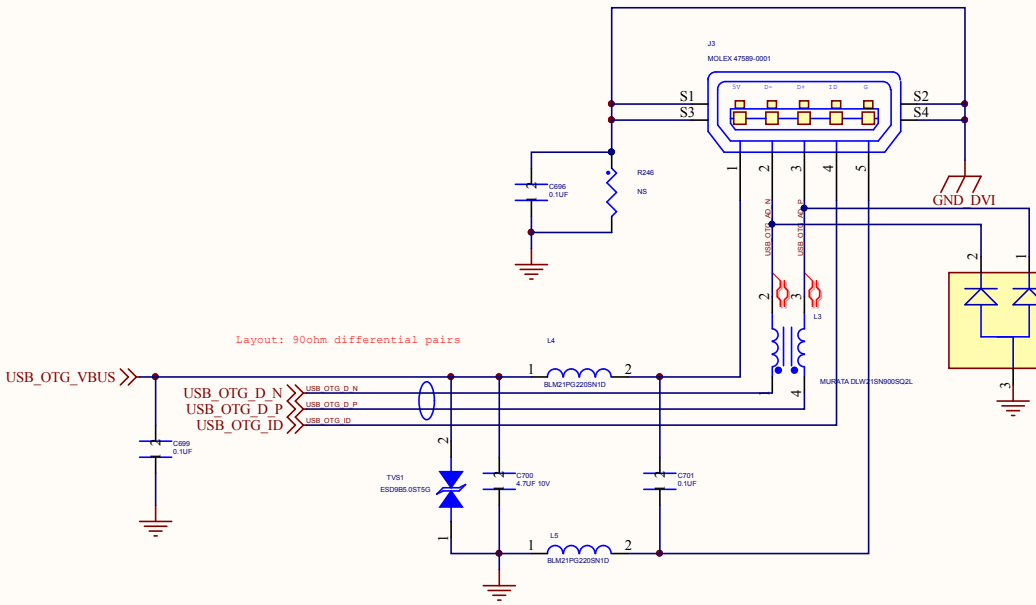
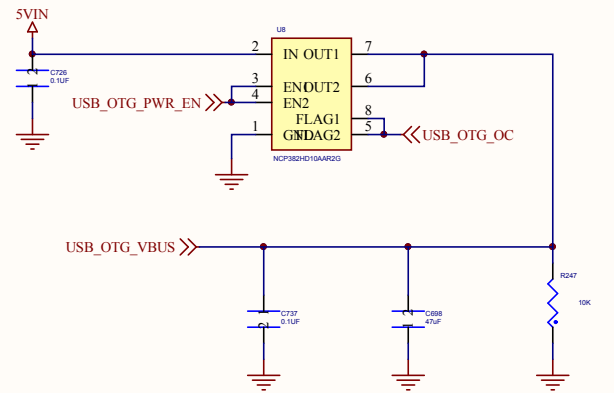
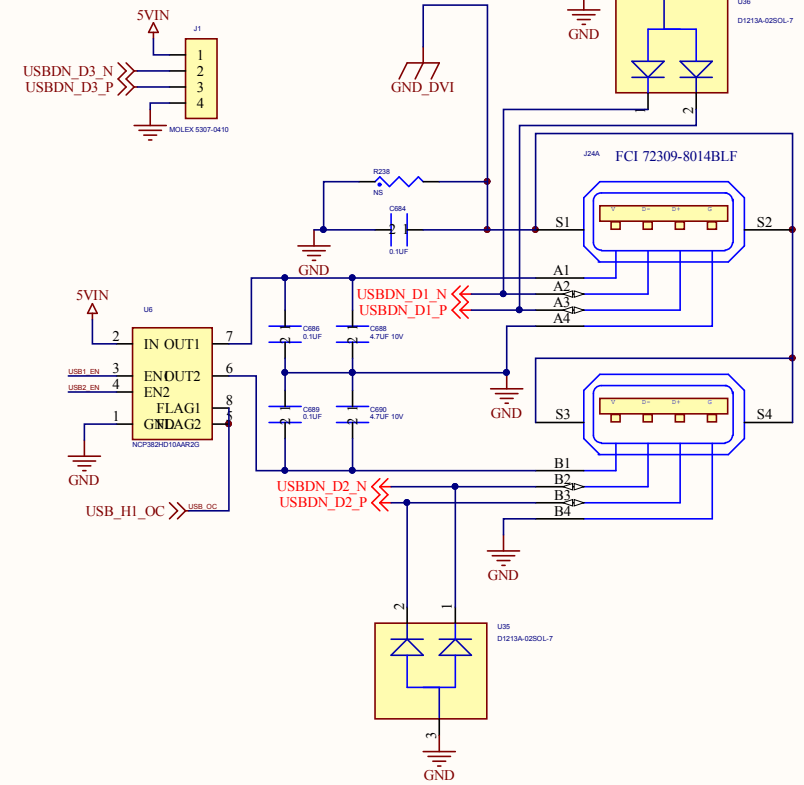
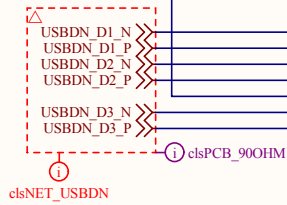
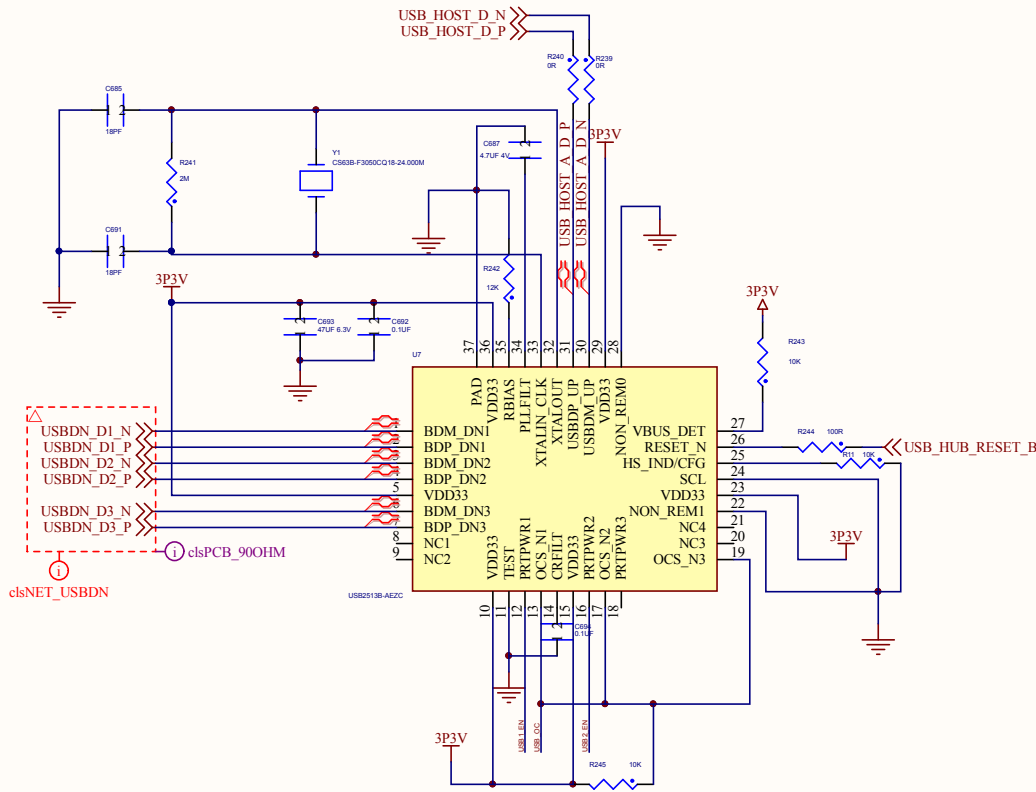


Layout: High speed data lines > 10 cmil
 Put the 350m tracewidth in this page near layout





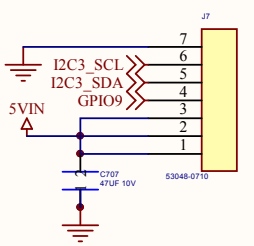
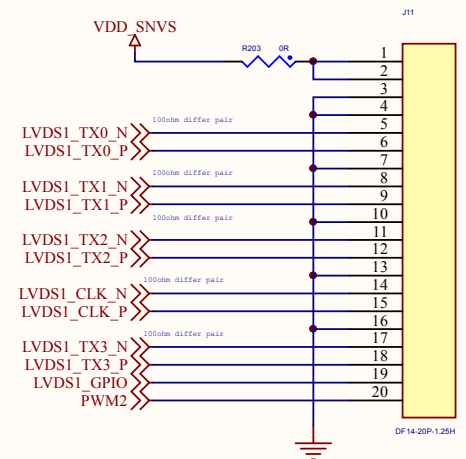
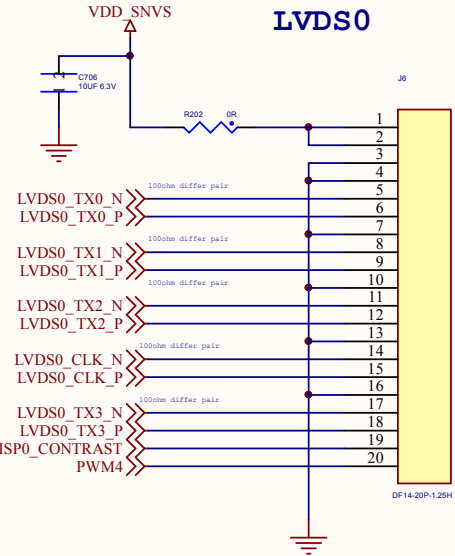
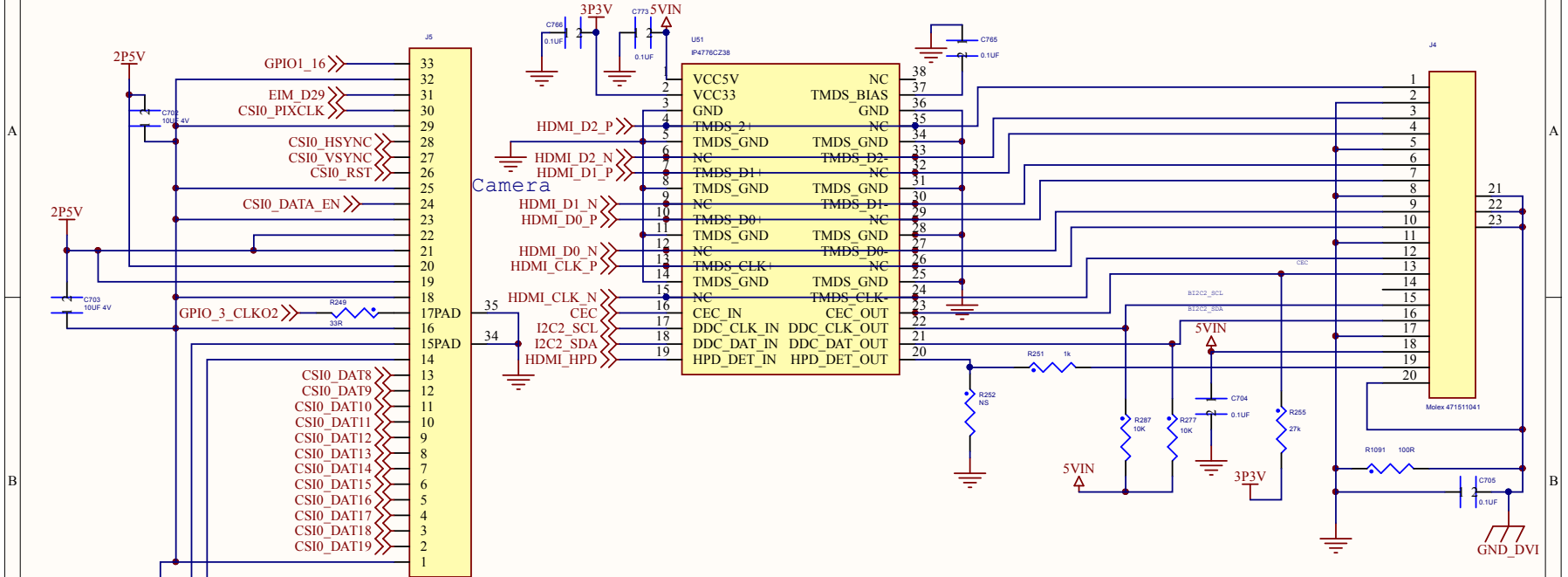
Layout: Route DIFF pairs on top layer only.



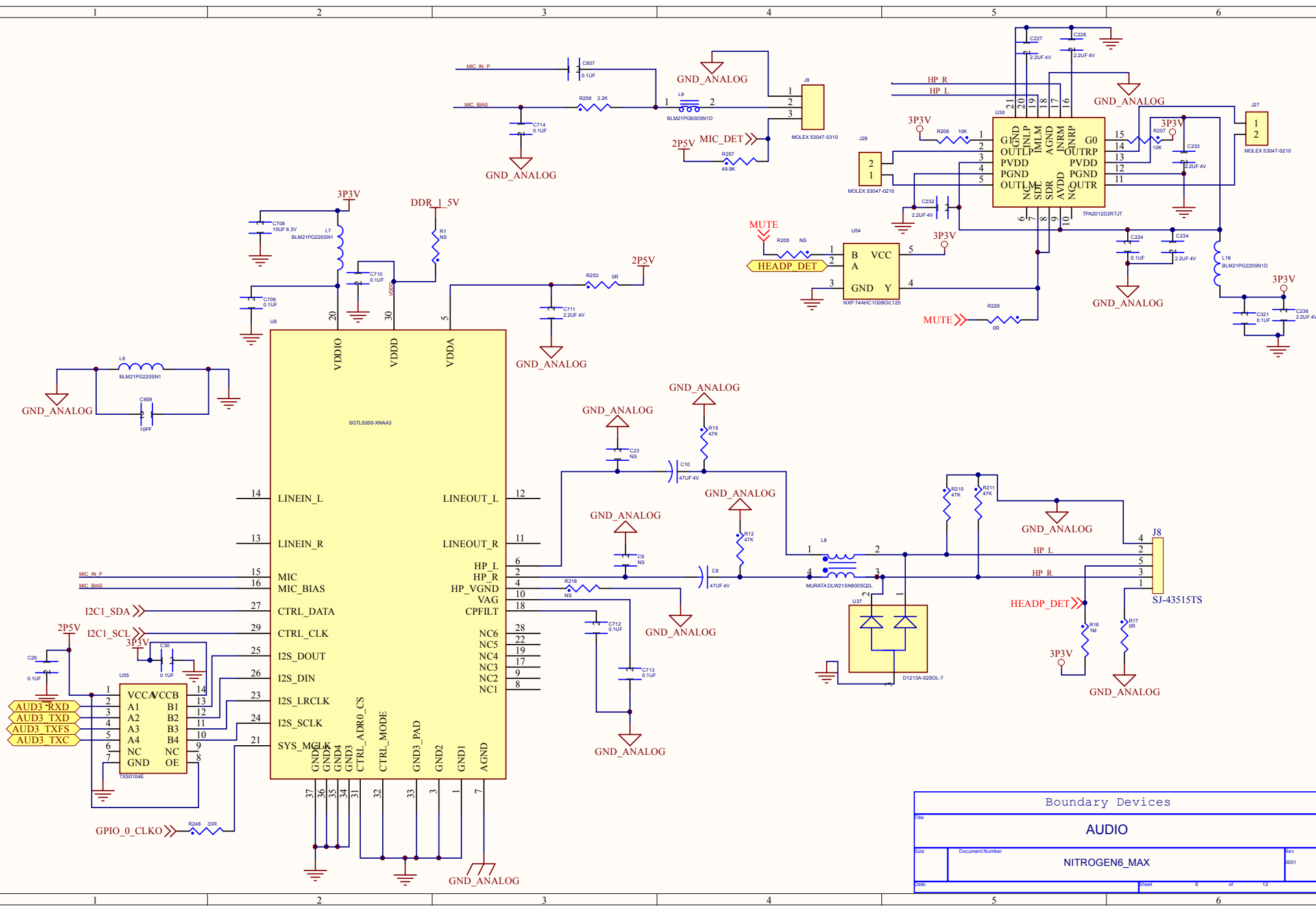
Boundary Devices			
USB HUB + OTG			
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CMOS Sensor

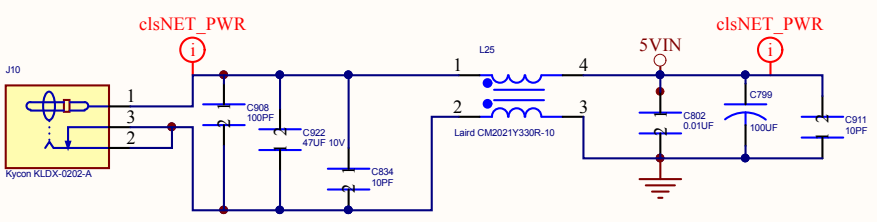
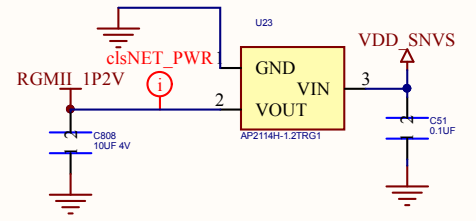
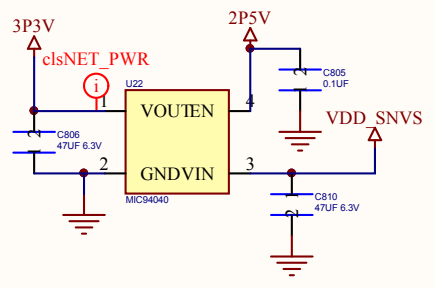
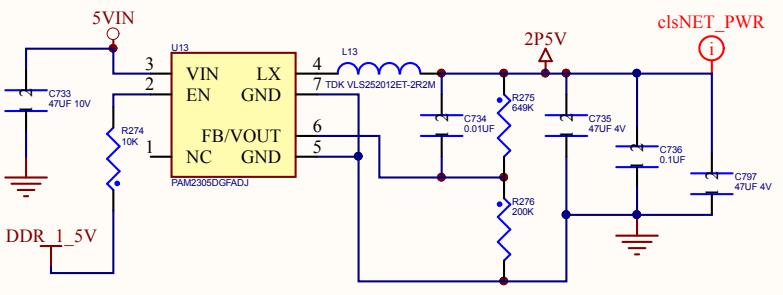
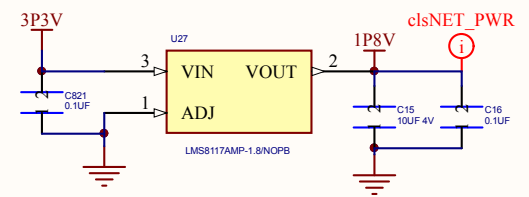
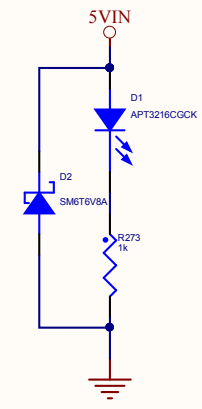
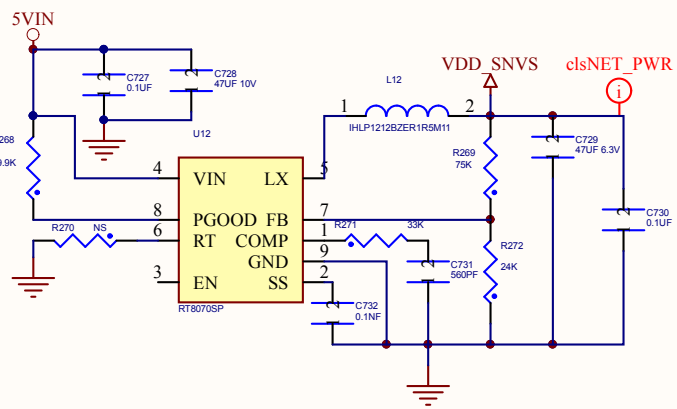
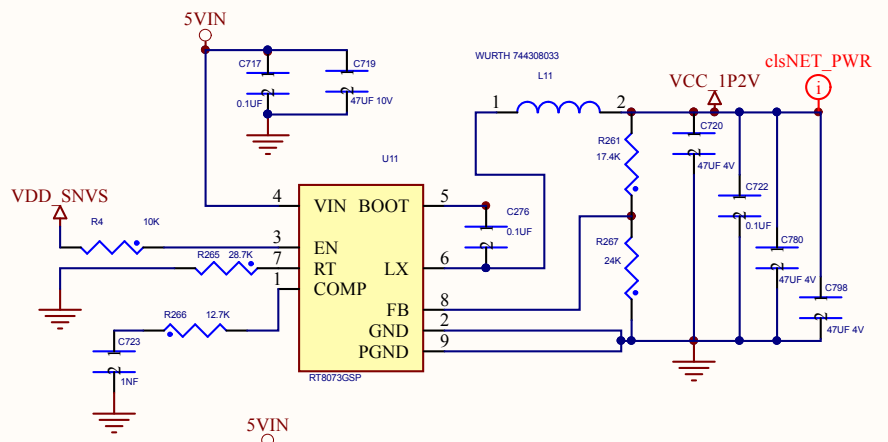
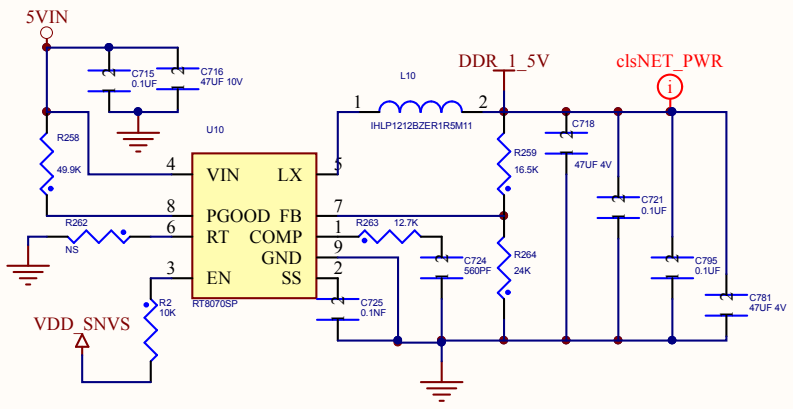
Layout: HDMI 100 ohm differential pairs



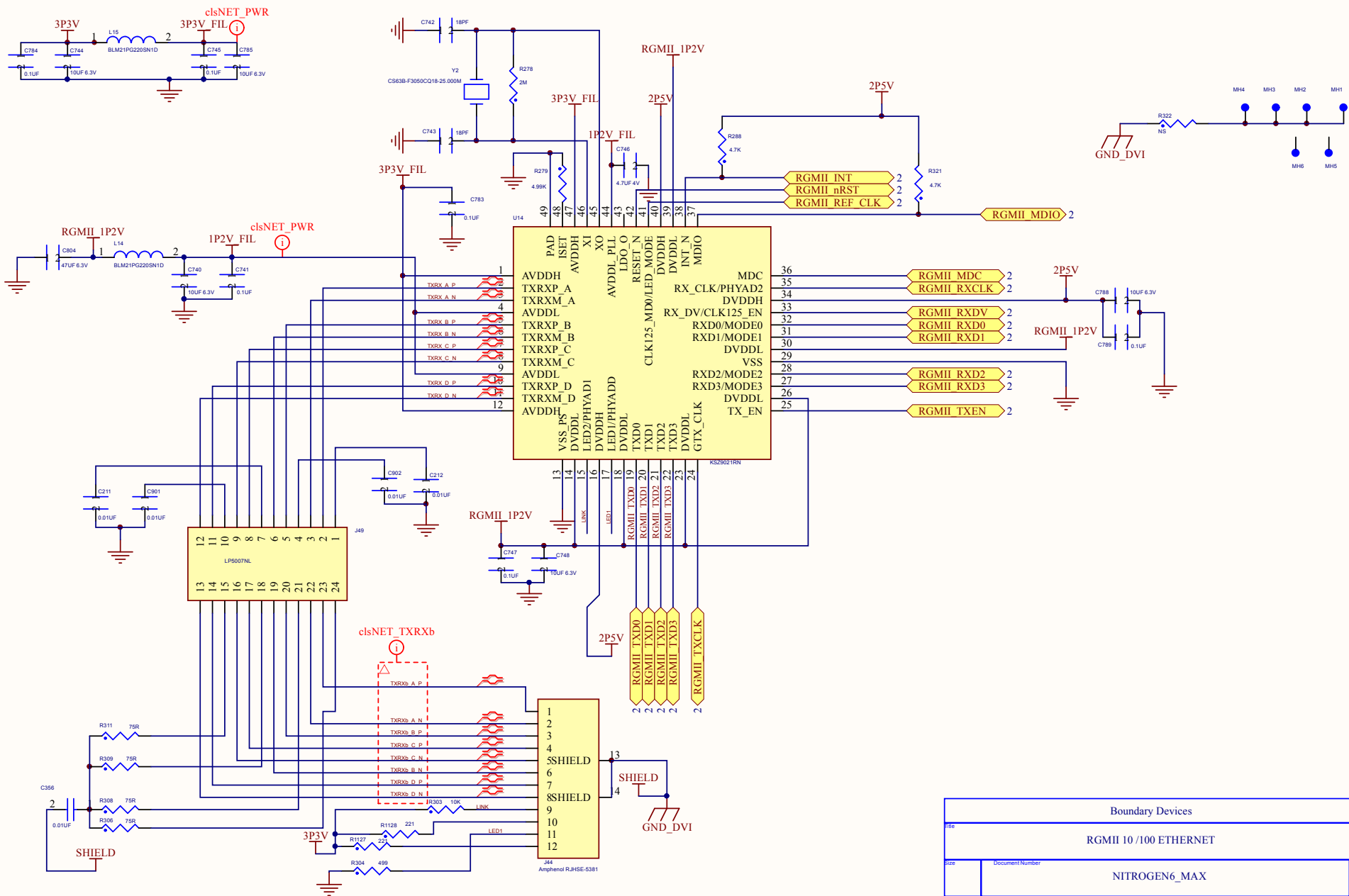
Boundary Devices			
RGB +LVDS+HDMI			
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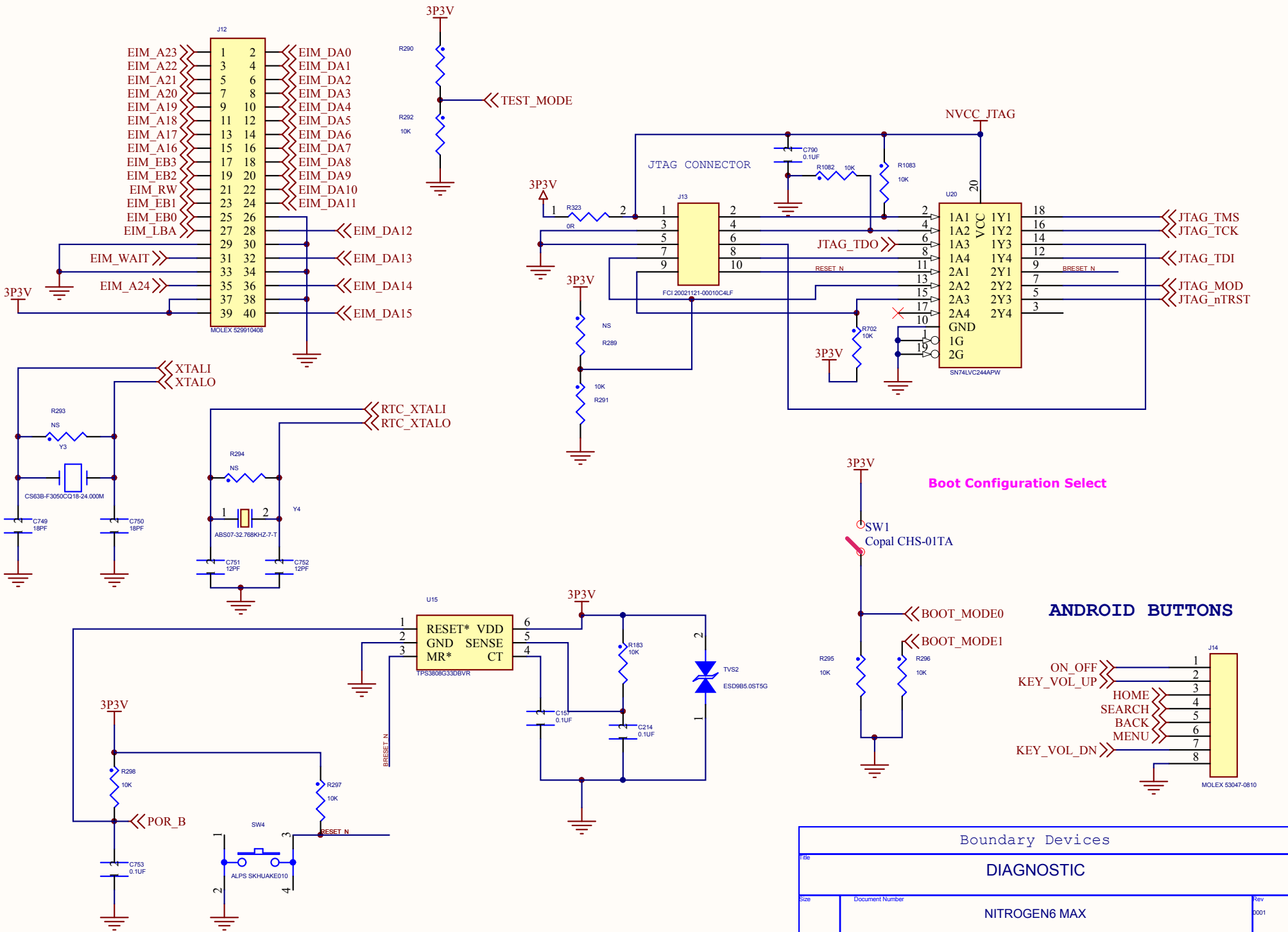
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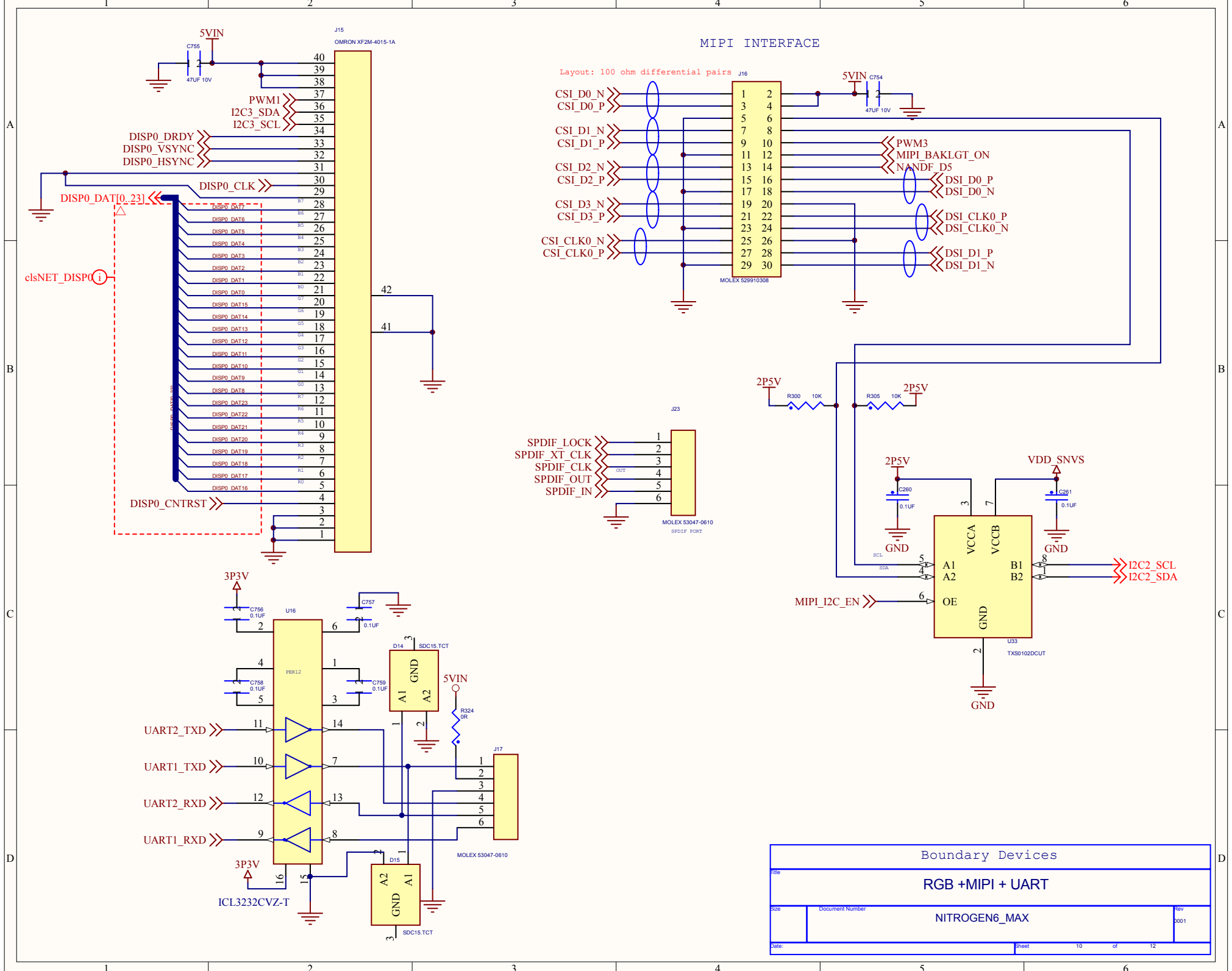
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SYSTEM POWER			
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RGMII 10/100 ETHERNET	
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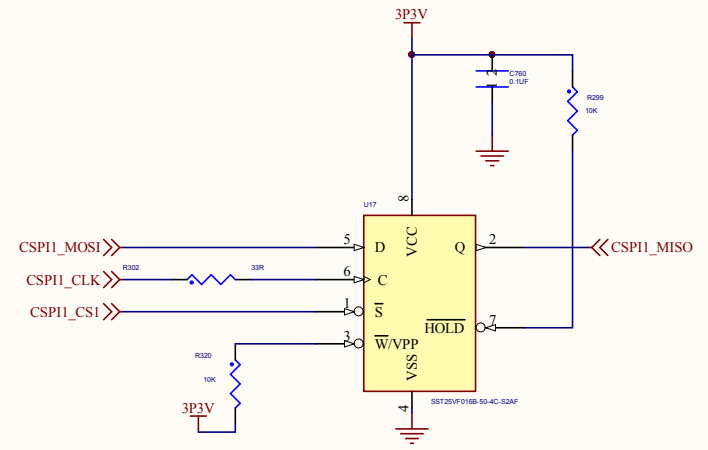
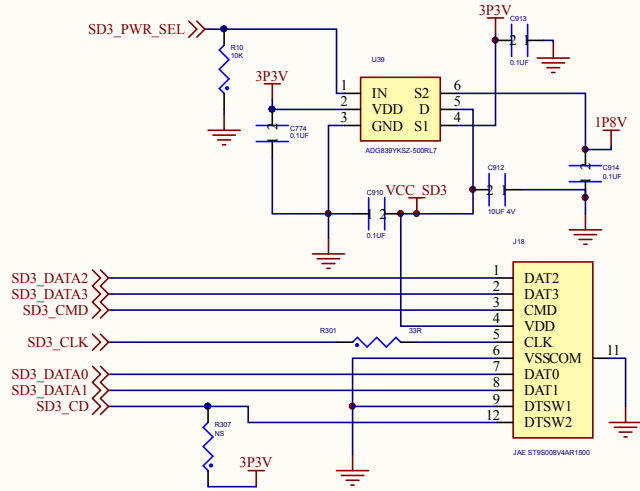


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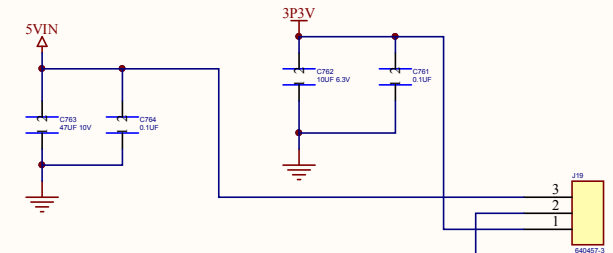
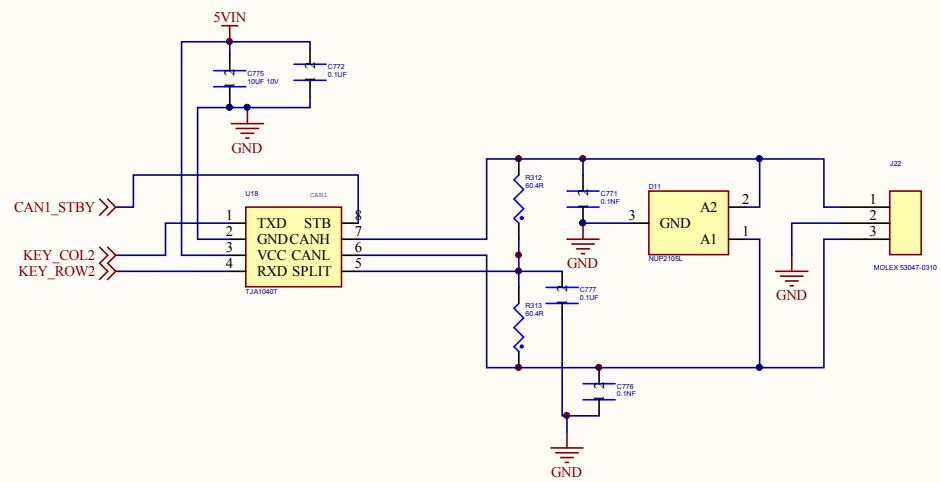
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A



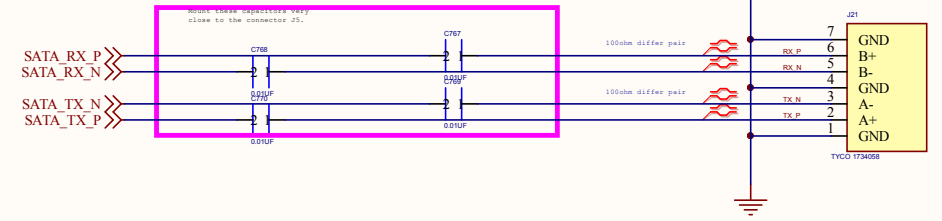
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B



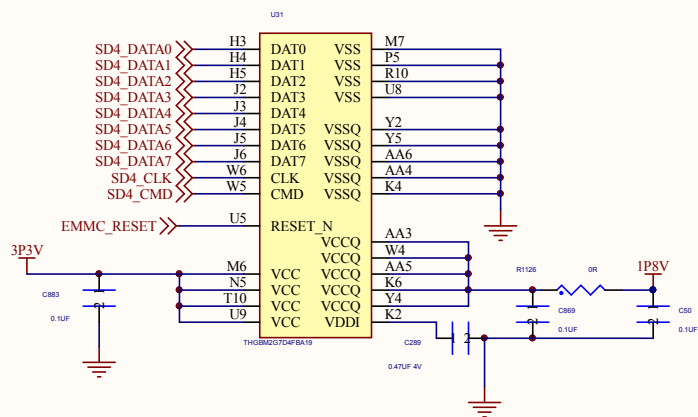
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C

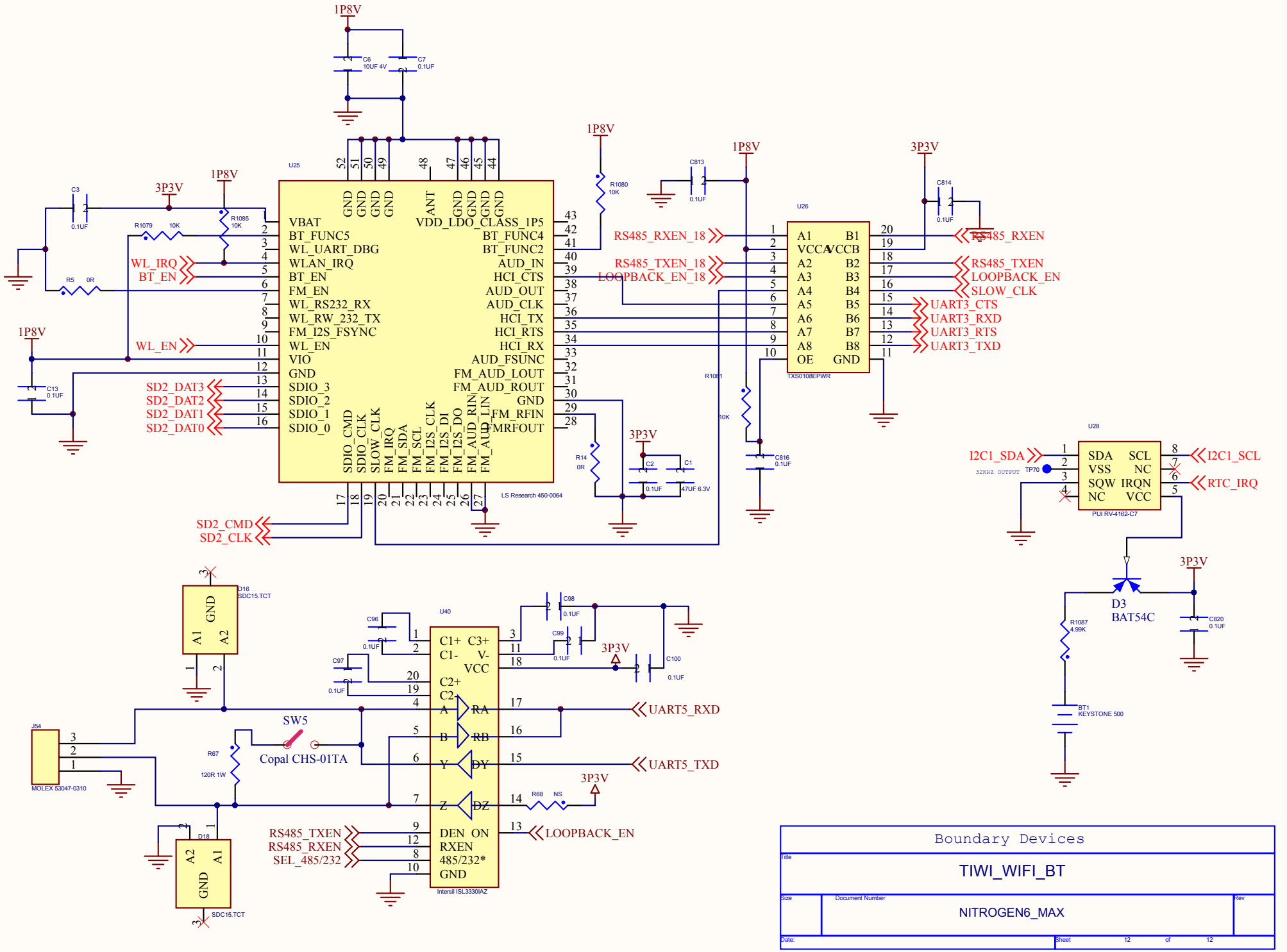


D

D



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