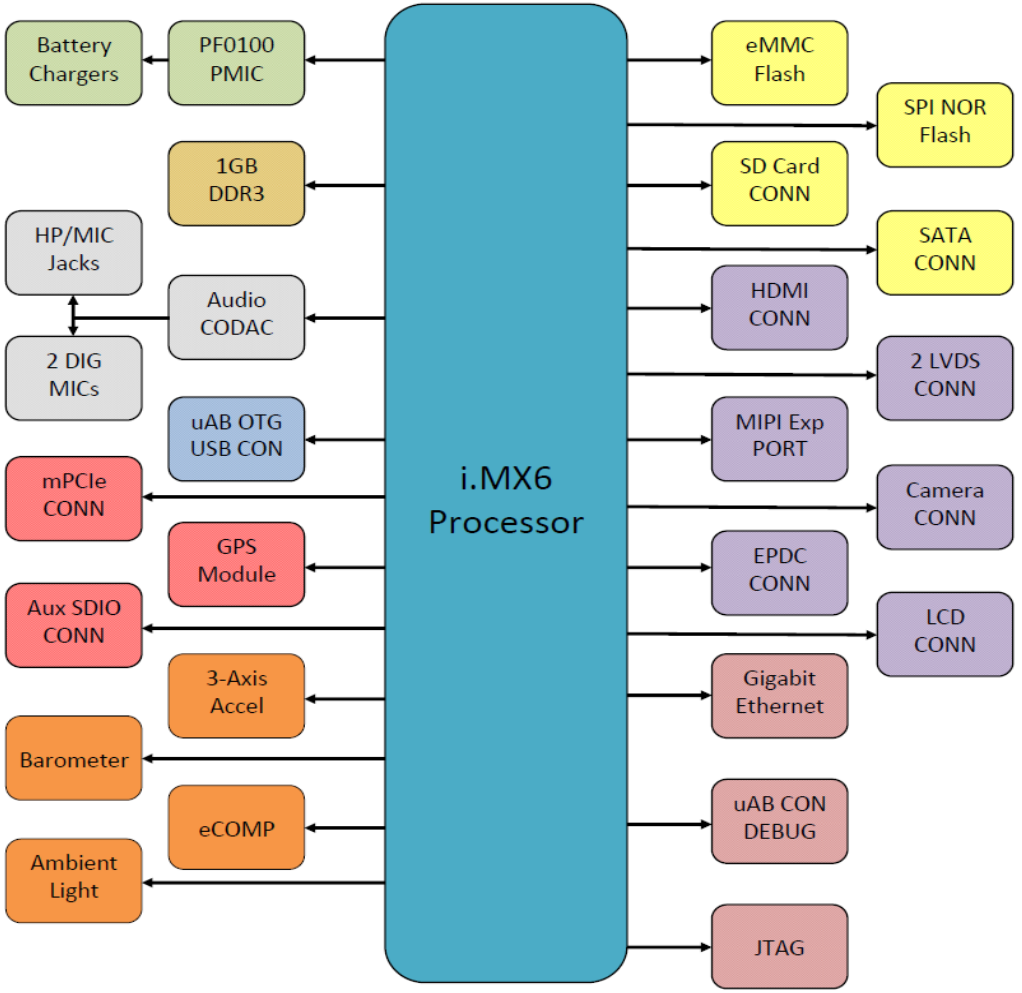
i.MX6 SMART DEVICE SYSTEM

MCIMX6Q-SDB, MCIMX6Q-SDP, MCIMX6DL-SDP

Table of Content

Smart Device System Block Diagram



GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum

2. Critical compenents that require tolerances tighter than listed in Note 1are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.

3. Interrupted lines coded with the same letter or letter combinations are electrically connected.

4. Device type number is for reference only. The number varies with the manufacturer.

5. Special signal usage:
   _B or 'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC
Current Output: ~ 5A (depending on application)
Polarity:
Inner Diameter: 2.1mm
Outer Diameter: 5.5mm

Revision History

Rev. Code	Date	Description
X1	11/02/2011	Rev X1 Draft
A	12/15/2011	Release to Prototype Phase
AX1	02/09/12	Draft Rev B Respin: - Changed Audio CODEC to WM8962 per Marketing Request. - Removed two digital microphones. Changed mics to Wolfson WM2730 per Marketing. - Connected NVCC_JTAG rail to GEN_3V3. - Added PFET Switch to SW8ST supply to isolate it from System power. - Changed HDMI Media guard to CM2020 IC to correct I2C HDMI issue. - Changed voltage sides on U9 level shifter. - Changed SW4 to 3.15V output. Moved audio 1.8V to GEN_1V8. - Changed camera 1V5 supply to VGEN2, other 1V5 loads moved to VGEN1. - Added isolation PFETs to Audio voltage supplies. - Switched USB_OTG_ID to pin ENET_RX_ER, USBOTG_OC to pin EIM2 and USBH1_OC to pin EIM_D30 to match pinmux functionality. - Added parallel termination resistors to PCIe differential clock traces. - Added next generation DEVSLP option for SATA connection. - Moved DISP0_PWR_EN to NANDF_WP_B to correct pull up voltage issue. - Deleted auxiliary 3.15V voltage regulator. - Designated several capacitors on processor core power rails as DNP. Validation proved unnecessary. - Moved I2C3 SDA from GPIO_16, This pin must be unconnected for Ethernet 1588 (time stamp) functionality to work. - Added shield ground pins to LVDS connectors. - Changed extrnal speaker capacitors to higher voltage rating. - Changed external regulator to supply 3.0V power to VSNVS. - Changed PF0100 microprocessor program circuit to DNP. - Added 5V supply to LCD expansion headers. - Connected HPOUTFB directly to Audio GND. - Connected VDDOTP to ground to boot PMIC from program settings. - Added isolation to prevent back powering board from USB when no battery present. - Back annotated Schematic to Layout. REFDES may have changed from Rev A. - Populated optional "PWRON" button circuit for use with Android. - Removed write protect on NOR Flash. - Removed LC filter circuit from external speakers. - Added an additional 2 100uF capacitors to MPCIE_3V3 next to connector. - Updated Power Rail, IOMUX, and Configuration Tables.
B	02/17/12	Release to Production
B1	04/11/12	Release to Production - Depopulated Q512 because of schematic error. - Cut trace to U12 pin 5 to prevent false USB plug in detects. - Added schematic page to detail applicable board TDAs that affect Rev B boards. - Populating CAN components U517 and U518 per Marketing Request. - Added resistor RX1 across pads for C55 to improve 24MHz clock stability. - Pull up resistors R629 and R639 have been changed to DNP.
B2	05/04/12	- Changed Marketing part number to MCIMX6Q-SDP - Changed R7, R112 and R585 to DNP - Changed C540 to "POPULATED"
B3	05/25/12	- Changed DDR3 Memory to new 1.35V capable memory MT41K128M16JT. - Changed C540 to 1.0 uF per Wolfson recommendation. - Changed R183 and R189 to 2.37K pull ups to bring I2C rise time into specification.
B4	07/18/12	- Removed buffers U580 and U520 from digital microphone data outputs. A note is added to show required hand wire modification. - The Battery Charge Done LED is disconnected and R522 is depopulated. New parts RX2, CX1 and UX1 are added. Traces show required hand modifications. - Optional Power On Circuit has been disabled and US11 and RS78 are now DNP. A new Diode DX1 has been added to allow EIM_D29 to sense a button press. - RESET button SW2 now connects to the PWRON pin of the PMIC. - Added 10K pull down resistor RX3 to SDCKE0 trace. - SIM Card Connector CON1 is now populated by default. - Battery Connector Header CON3 is now populated by default. - Changed resistors R174 and R176 and to depopulated by default. LVDS0 EDID will not be connected to I2C2 channel unless needed. - Replaced digital microphones with Analog Devices ADMP421. - Disabled USR_DEF_GRN_LED circuit. Configured GPIO_1 for WDOG_B output.
B5	09/28/12	- Changed U1 to i.MX 6 TO1.2 processor. - Changed C68 and C612 to DNP. - Populated C682 and C716 with 22uF capacitors.
C	09/12/12	- All hand wire changes made in Revision B4 are now formally made in the netlist and the layout files. - Q512 is changed to populated. - Optional Start Up circuit has been modified. - PMIC Programming Micro-Processor is removed. - CX1 capacitor is changed to C504 - DX1 diode is changed to D4 - RX1 resistor changed to R216 - RX2 resistor changed to R19 - RX3 resistor changed to R635 - UX1 buffer changed to U587 - Add DNP Input to U13 buffer for USB_OTG_PWR_EN. Buffer now powered from GEN_3V3. - FA_ANA and VDD_FA signals now connected to ground. - Added resistor options to EIM_DA7 trace to EPD connector. - Connected EIM_DA9 to EPDC connector JS08 to supply SDCE5 if needed. - Optional LDO U9 is now depopulated. - Added Connector J13 to support BT from SDIO Card through DNP resistors. - Added GPIO control of Battery Charge Enable pins through DNP resistor. - Changed C594 to 0.22uF - Changed C31 to 47uF. - Added C555 as second 22uF capacitor in parallel with C546. - Changed C561, C562, C586 and C596 to 0.47uF. - Added additional 47uF bulk capacitor C769 to SD2 socket VDD supply. - Added option to route HDMI DDC comms seperate from I2C2 comms channel. - C597 populated to provide de-bounce to RESET circuit. - Depopulated C68, C612. Populated C682, C716 closer to pins. - Depopulated C39, C606, C607, C608, C609, C610, C673 and C681. - Added DNP R302 to provide alternate 5V supply path to USB_H1_VBUS. - Added DNP R632 to provide alternate gating of PMIC_5V source (tied to VDDSOC). - Added DNP L25 and L26 to provide alternate 2.8V supply path to camera modules. - Added test pads to LVDS third data lanes to support testing with will 24-bit panels. - Changed capacitors C6 and C7 to Zero Ohm resistors R307 and R308 per PCIe Spec.
C1	09/27/12	- Changed Ref Des R307 and R308 back to C6 and C7 to match layout netlist.
C2	11/09/12	- Moved Ferrite Beads L10 and L17 to pads for L25 and L26. Camera Analog Voltage supply moved to VGEN3. - Added notes for 24MHz crystal and USB layout design. - Changed R17, R21, R25, R27, R68, R85, R582, and R660 to 1% resistors due to lead time availability issues.
C3	02/20/13	- Changed BT598 Battery Holder to new manufacturer due to parts availability. - Changed R17, R21, R25, R27, R68, R85, R582, and R660 to 0.5% resistors due to parts availability. - Changed R97 and R106 pull up resistors to 4.7 Ohm. - Changed R19 pull up resistor to 10K Ohm.

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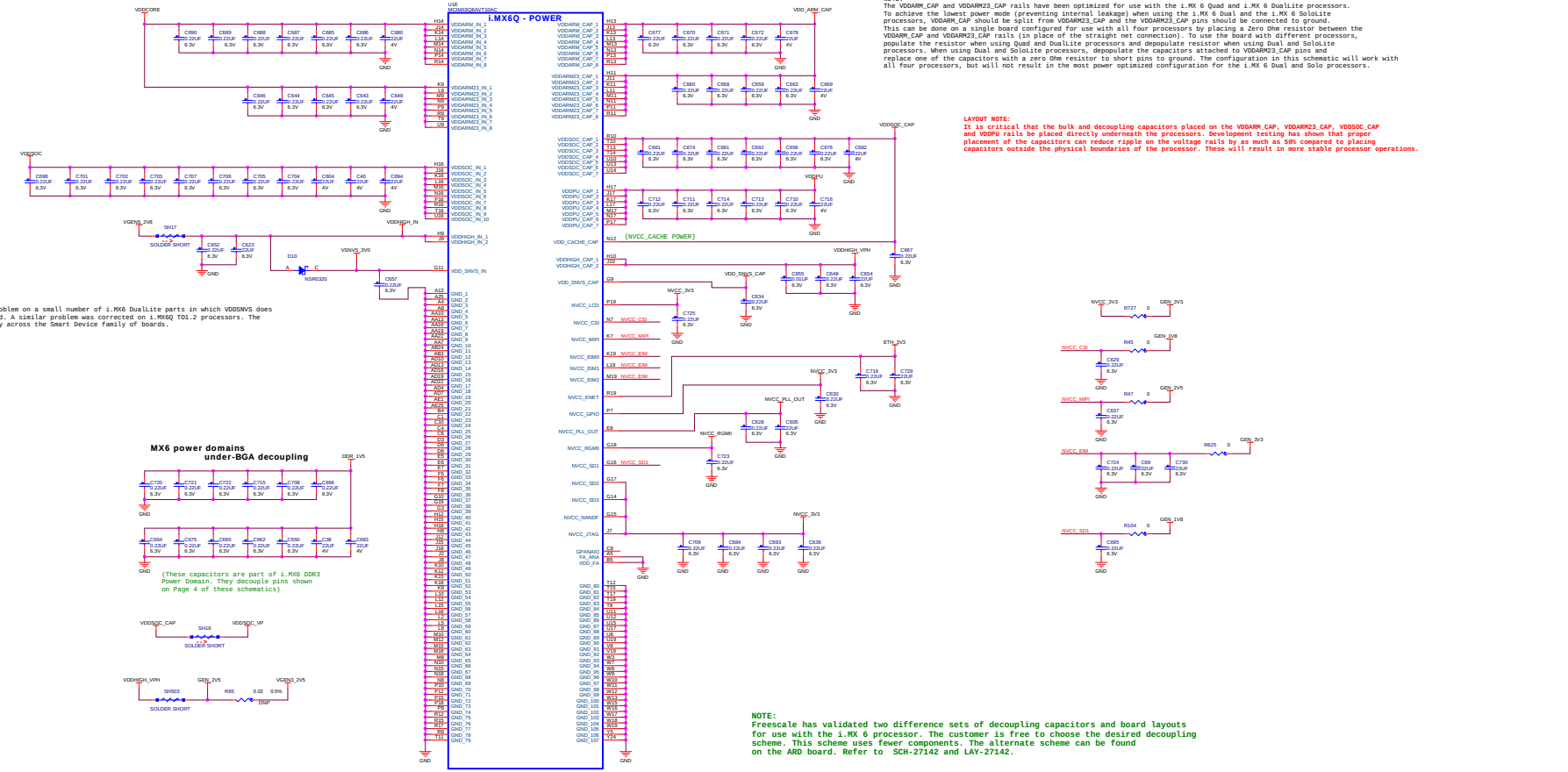
Designed by: Mark Middleton	Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM
Drawn by: Mark Middleton	Page Title: TITLE PAGE
Approved: <Approver>	Size: D; Document Number: SOURCE:SCH-27392 PDF:SPF-27392; Rev: C3
	Date: Tuesday, February 19, 2013; Sheet 1 of 25



NOTE:
Diode D10 is required to correct a problem on a small number of i.MX6 Duallite parts in which VDDSNVS does not come up when VDDHIGH_IN is applied. A similar problem was corrected on i.MX6Q T01.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

MX6 power domains under-BGA decoupling

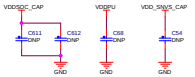
(These capacitors are part of i.MX6 DDR3 Power Domain. They decouple pins shown on Page 4 of these schematics)

NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 Duallite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and Duallite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 58% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

NOTE:
Freescale has validated two difference sets of decoupling capacitors and board layouts for use with the i.MX 6 processor. The customer is free to choose the desired decoupling scheme. This scheme uses fewer components. The alternate scheme can be found on the ARD board. Refer to SCH-27142 and LAY-27142.

Extra Bulk Capacitors



NOTE:
In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitive loading on the internal processor LDOs. The coponents/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.

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Page Title:	CPU POWER		
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SECURE HDMI COMMUNICATIONS

NOTE:
To configure SD board to run in Secure HDMI mode:
1) Depopulate R153 and R154 (schematic page 22)
   This removes HDMI comms channel from I2C2.
2) Populated R218 and R219.
   This connects HDMI comms to DDC capable pins.
3) Depopulate R168.
   This deconflicts HDMI comms from the compass interrupt.
4) Populate R217 to connect COMP_INT to processor.
   This connects COMP_INT to a different GPIO pin.
5) R167 may be left populated or depopulated as desired.

Depopulate R121, R123, R133, R138, R139, R167, R168, and R627 when using E-BOOK Card in 16-bit Data Mode.

Note:
1) R216 is required to correct a known 24MHz slow starting issue present on some iMX 6 part. Please refer to the i.MX 6 Processor Errata, issue # ERR003745 for more details.

2) Per bulletin EB830, the i.MX6 processor may drive the 24 MHz crystal up to 250 uW. Freescale recommends following the guidelines contained in the bulletin.

The HW Developer Guide contains additional information.

NVCC_LVDS2P5 also powers on-chip DDR I/O predrivers, and must be powered whether LVDS is used or not.

Extra Bulk Capacitors

NOTE:
In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitive loading on the internal processor LDOs. The components/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.

Refer to build options table for assembly options on muxed signal resistors.

NOTE:
R302 is provided for testing with an alternate power supply for USB_H1_VBUS. It has not yet been tested. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

Layout: High speed data lines : 50 ohms

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Page Title:	CPU SIGNAL
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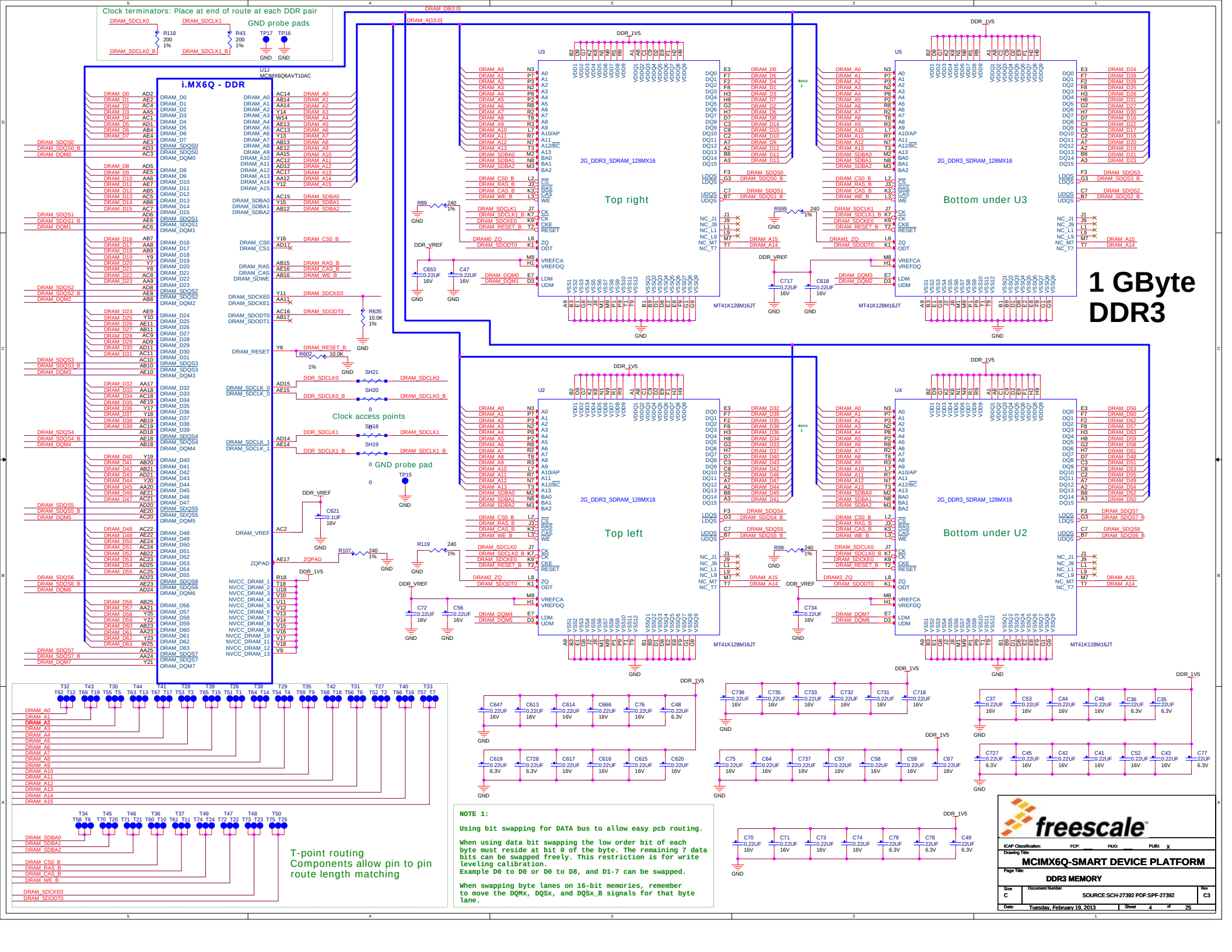
Clock terminators: Place at end of route at each DDR pair
GND probe pads
i.MX6Q - DDR
Top right
Bottom under U3
Top left
Bottom under U2
Clock access points
GND probe pad
1 GByte DDR3
T-point routing
Components allow pin to pin route length matching
NOTE 1:
Using bit swapping for DATA bus to allow easy pcb routing.
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.
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MCIMX6Q-SMART DEVICE PLATFORM
DDR3 MEMORY
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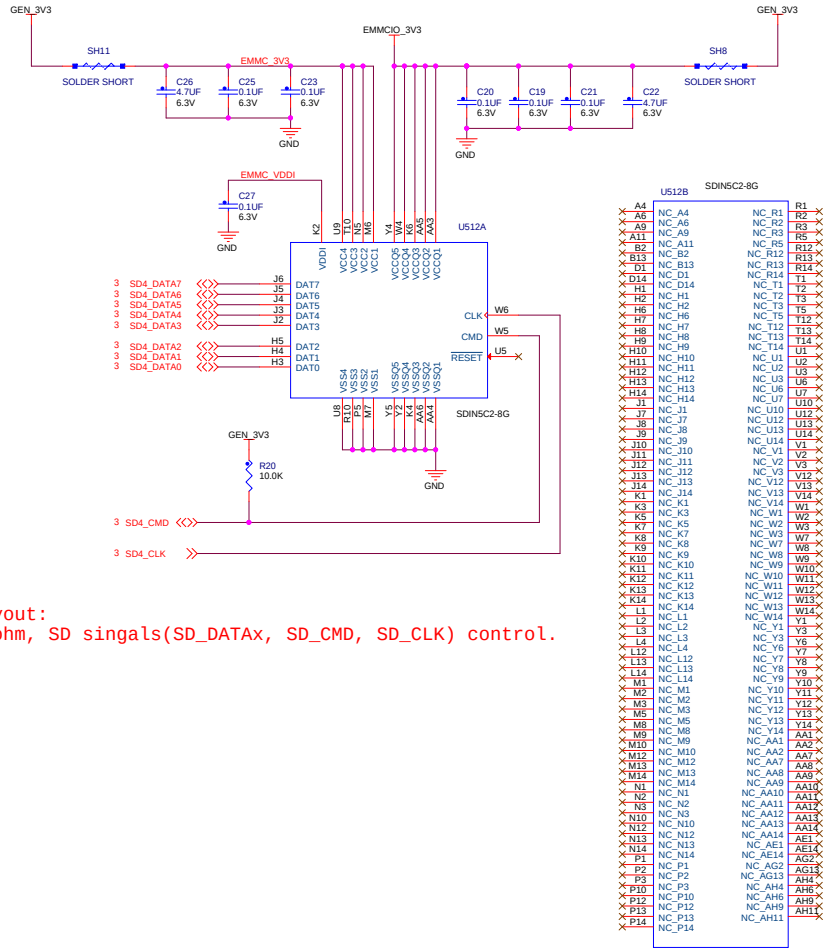
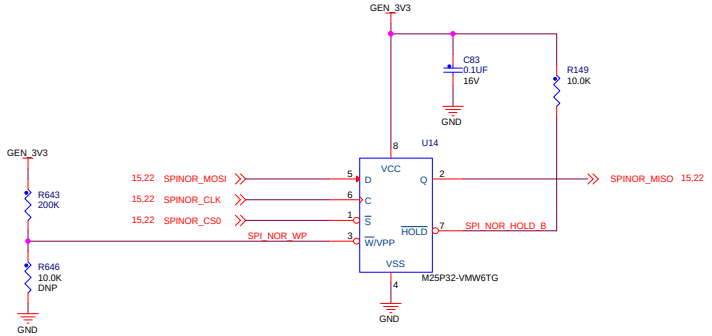
8GB eMMC MEMORY



Layout:
50ohm, SD singals(SD_DATAx, SD_CMD, SD_CLK) control.

4MB SPI NOR FLASH



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Page Title:	eMMC, SPI NOR FLASH
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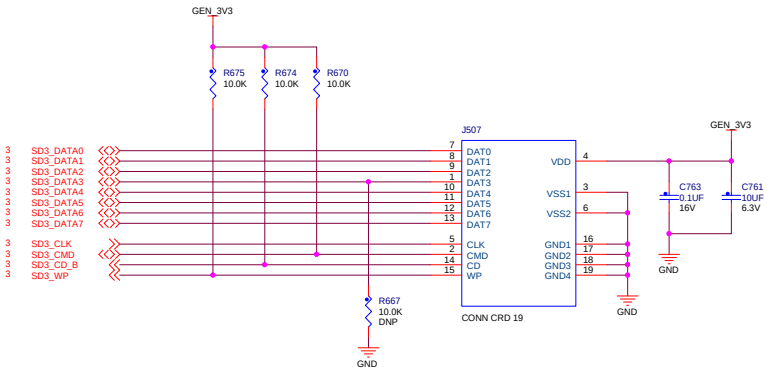
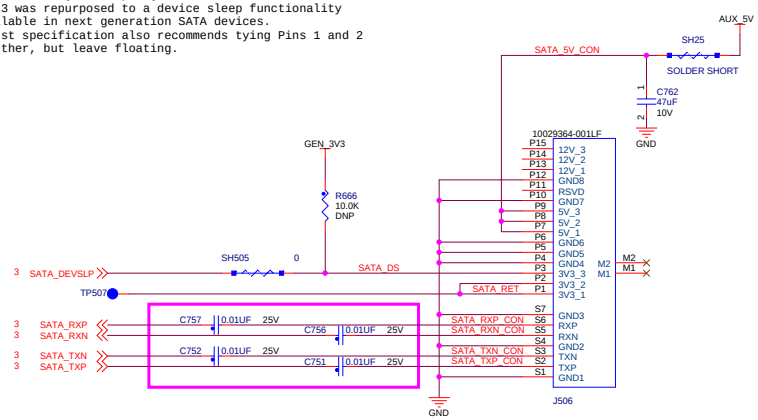
SD CARD SOCKET



Layout:
50ohm, SD signals(SD_DATAx, SD_CMD, SD_CLK) length equal

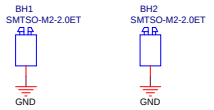
SATA CONNECTOR

NOTE:
The new SATA specification retires the 3V3 pins as they were not being used by regular sized SATA devices.
Pin 3 was repurposed to a device sleep functionality available in next generation SATA devices.
Latest specification also recommends tying Pins 1 and 2 together, but leave floating.



Layout:
1. 100ohm diff pairs, length equal
2. Mount these capacitors very close to the connector J506.

hard drive standoff



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Page Title: SD CARD, SATA

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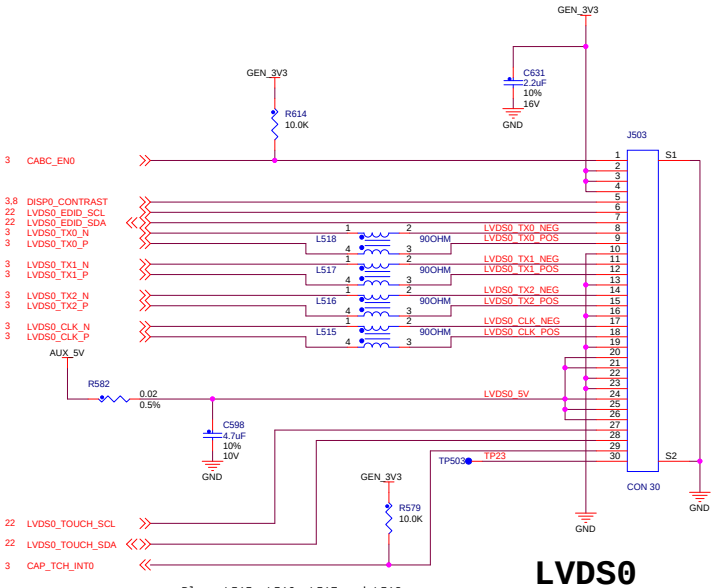
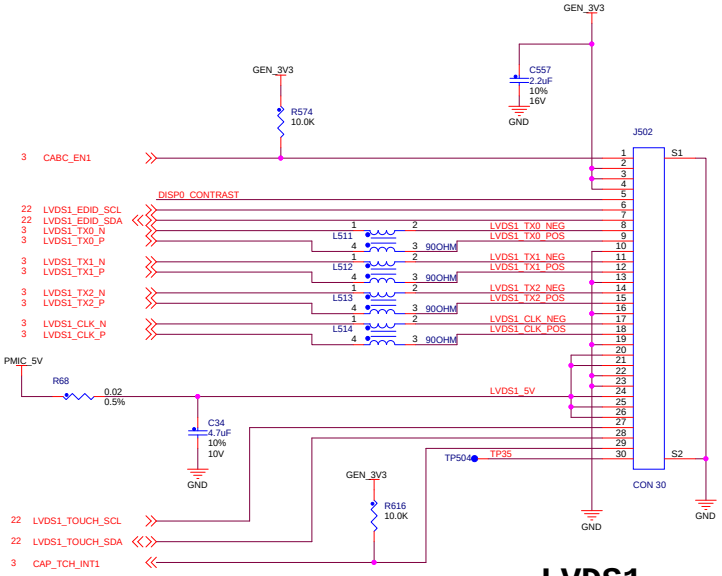
LVDS



LVDS0

Place L515, L516, L517 and L518
CMCs close to J403 connector.

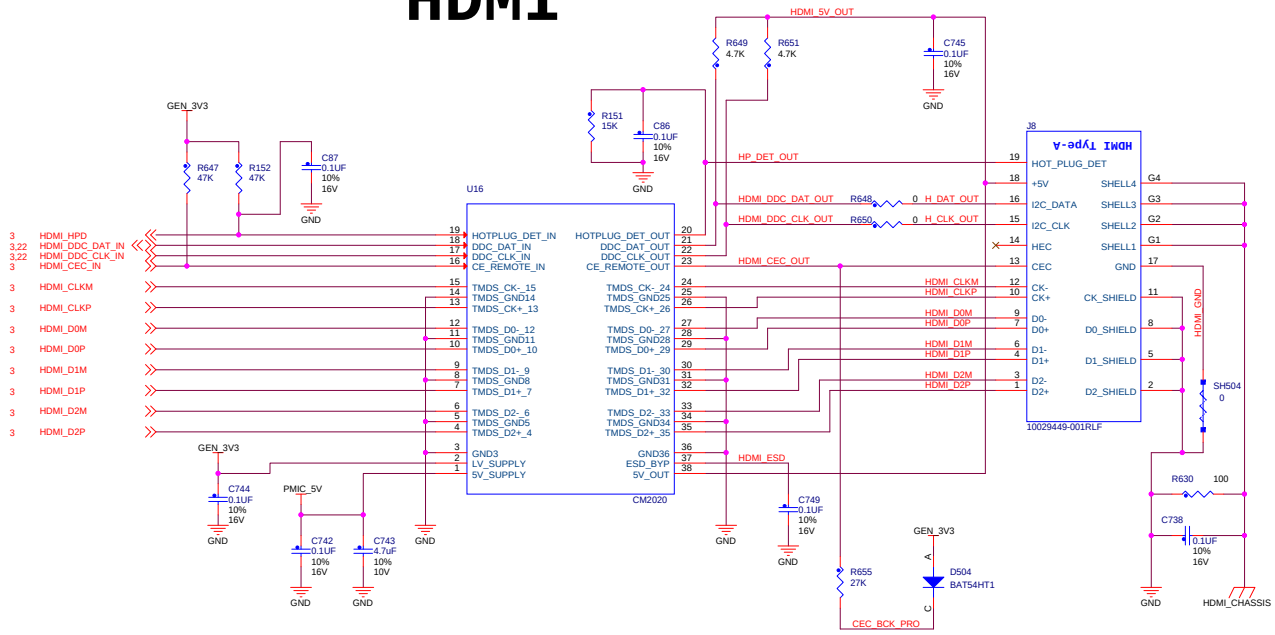


LVDS1

Place L511, L512, L513 and L514
CMCs close to J402 connector.

Layout: LVDS 100 ohm differential pairs

HDMI



Layout: HDMI 100 ohm differential pairs

NOTE:
When using HDMI, I2C2 bus is limited to 100 kHz
to read EDID values due to HDMI standards.
I2C2 bus speed should be limited to 100 kHz whenever
Hot Plug Detect is high.

LVDS Connector notes:
Pin 1: This pin is the Display Enable pin. It is used to
Enable/Disable the HannStar display.
Pin 5: This pin is the Display Brightness control. It
provides a PWM signal to the display to increase/
decrease display brightness depending on PWM
duty cycle. This signal is shared by all displays, so all
displays will change brightness together.

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Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: LVDS, HDMI

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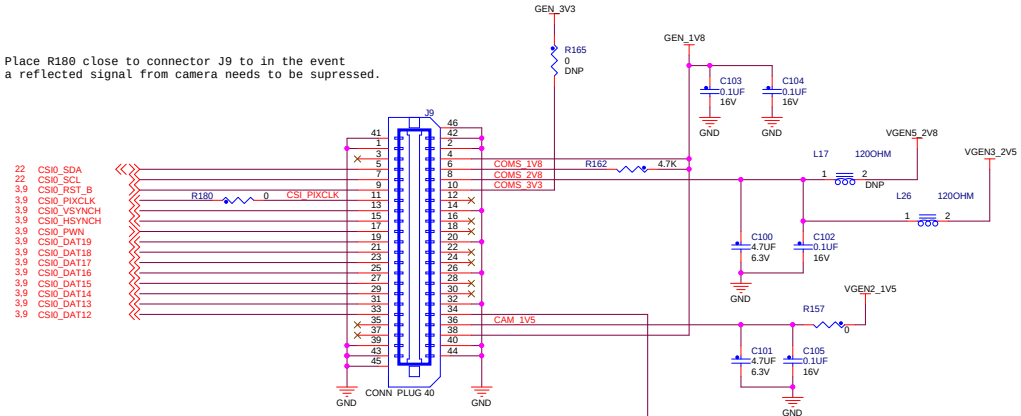
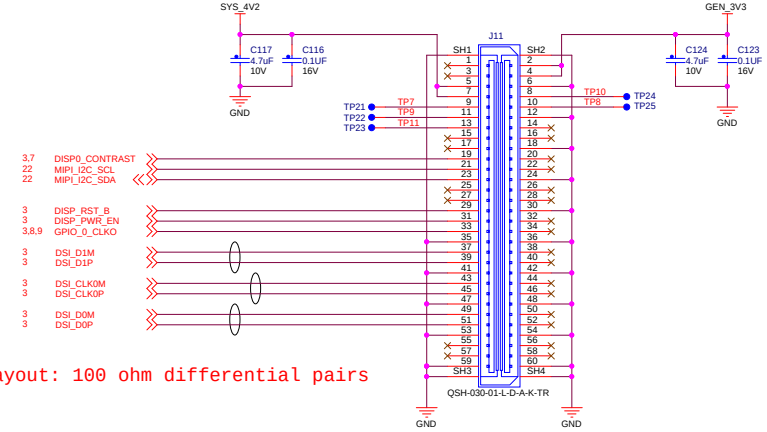
CSI CMOS Sensor
OV5642 5M Pixel

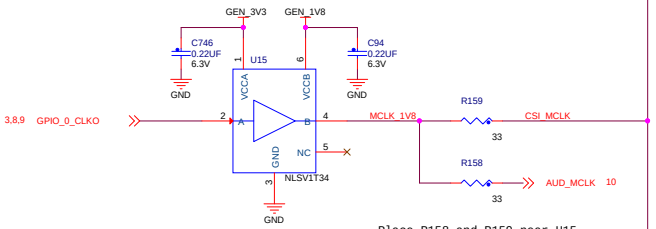


MIPI DISPLAY
EXP PORT



Layout: 100 ohm differential pairs

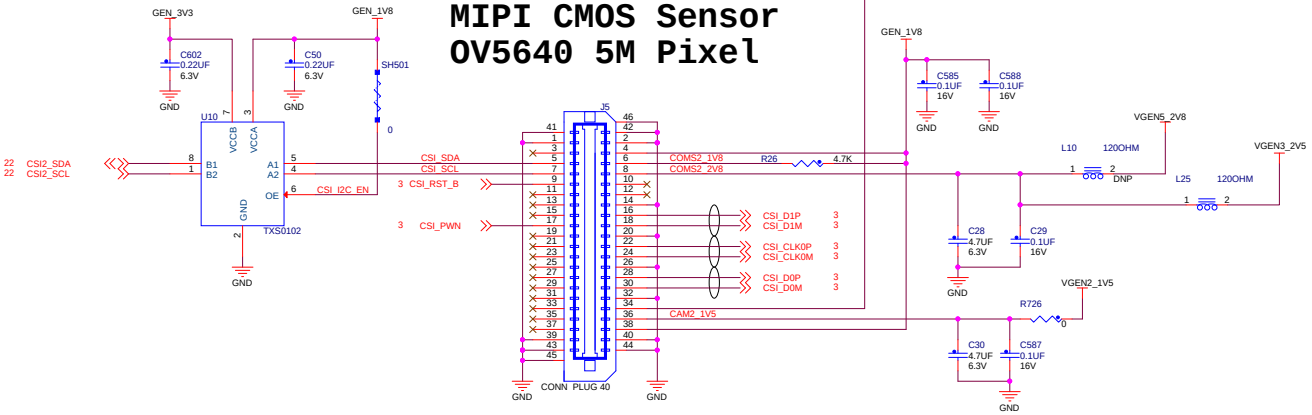
MIPI Connector



Place R158 and R159 near U15.
Acts as source termination.

NOTE:
The Camera Analog Power supply has been moved to VGEN3. Freescale SW will program VGEN3 to operate at 2.8V. L25 and L26 are now populated and L10 and L17 are depopulated. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

MIPI CMOS Sensor
OV5640 5M Pixel



Layout: 100 ohm differential pairs

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Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

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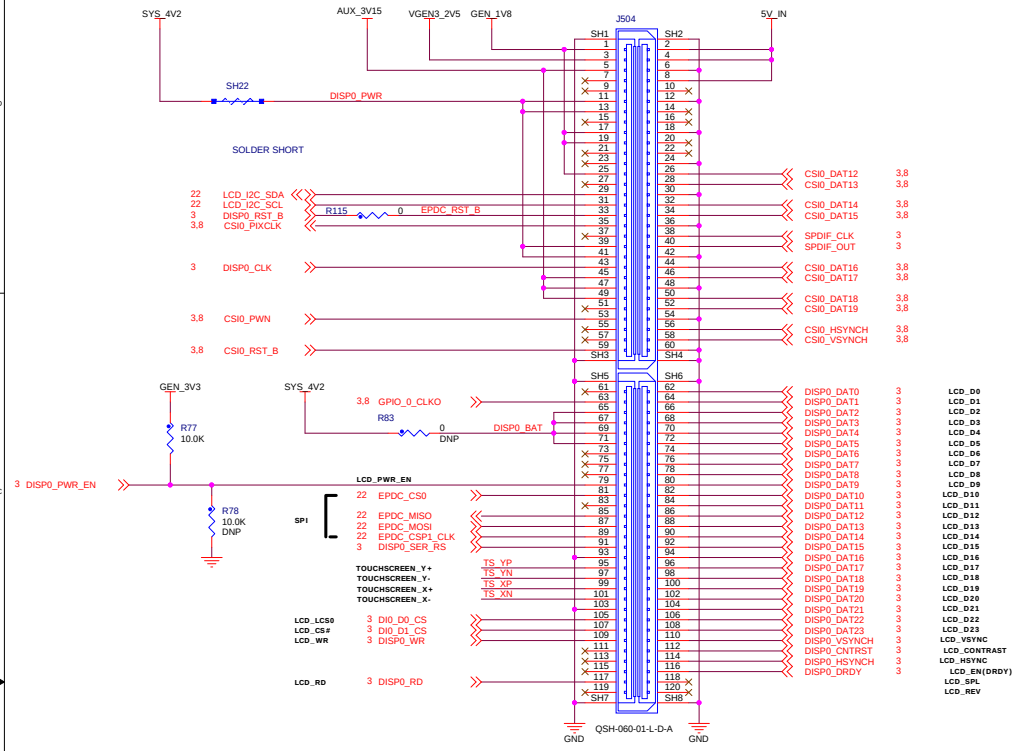
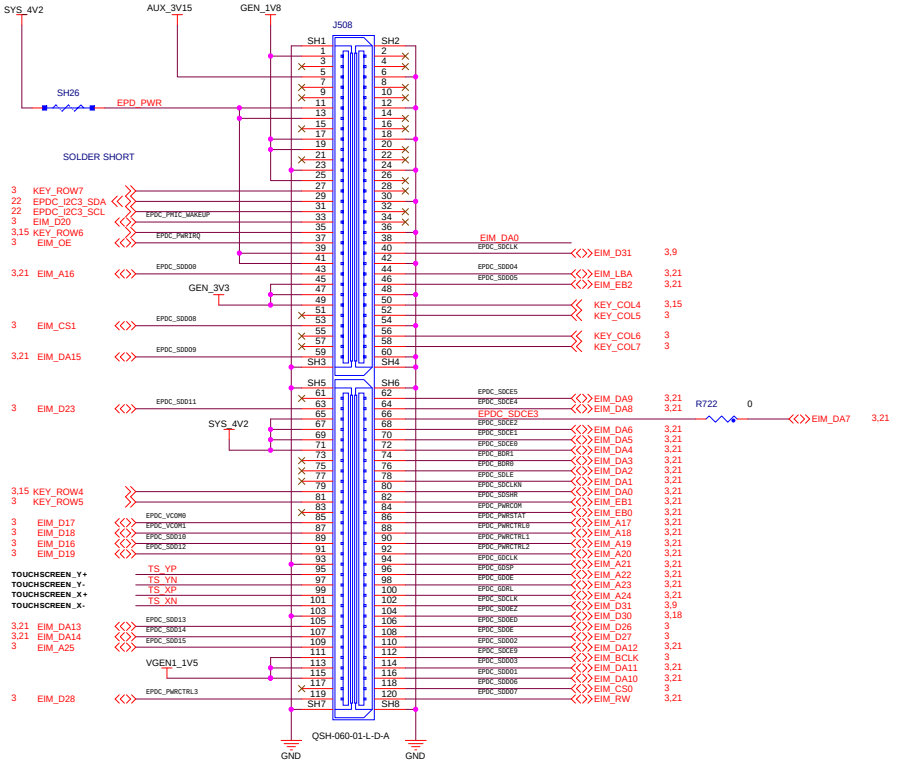
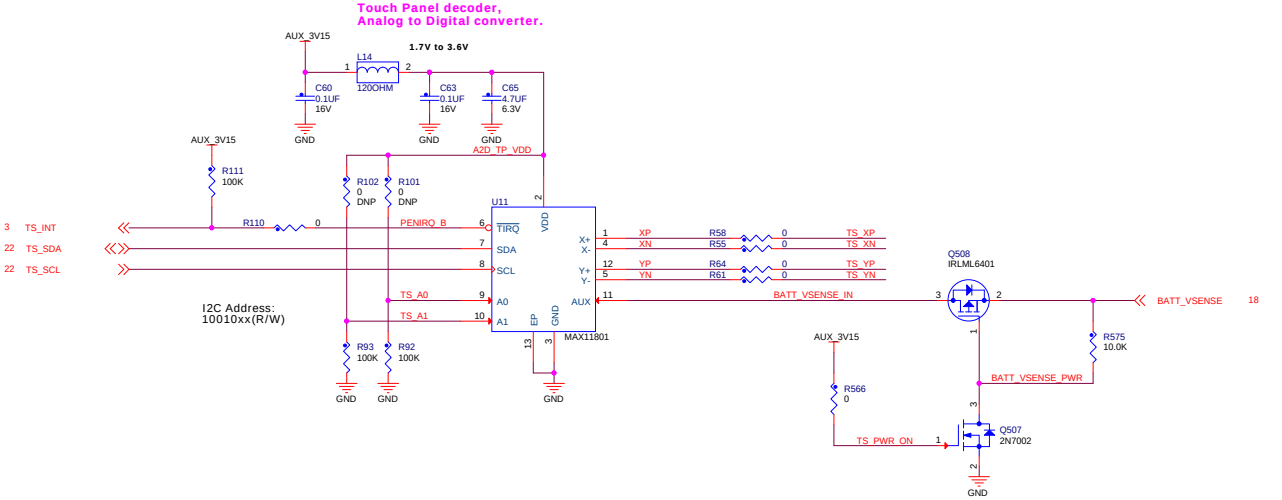
DISP0 Expansion Connector



For MX60 EPD





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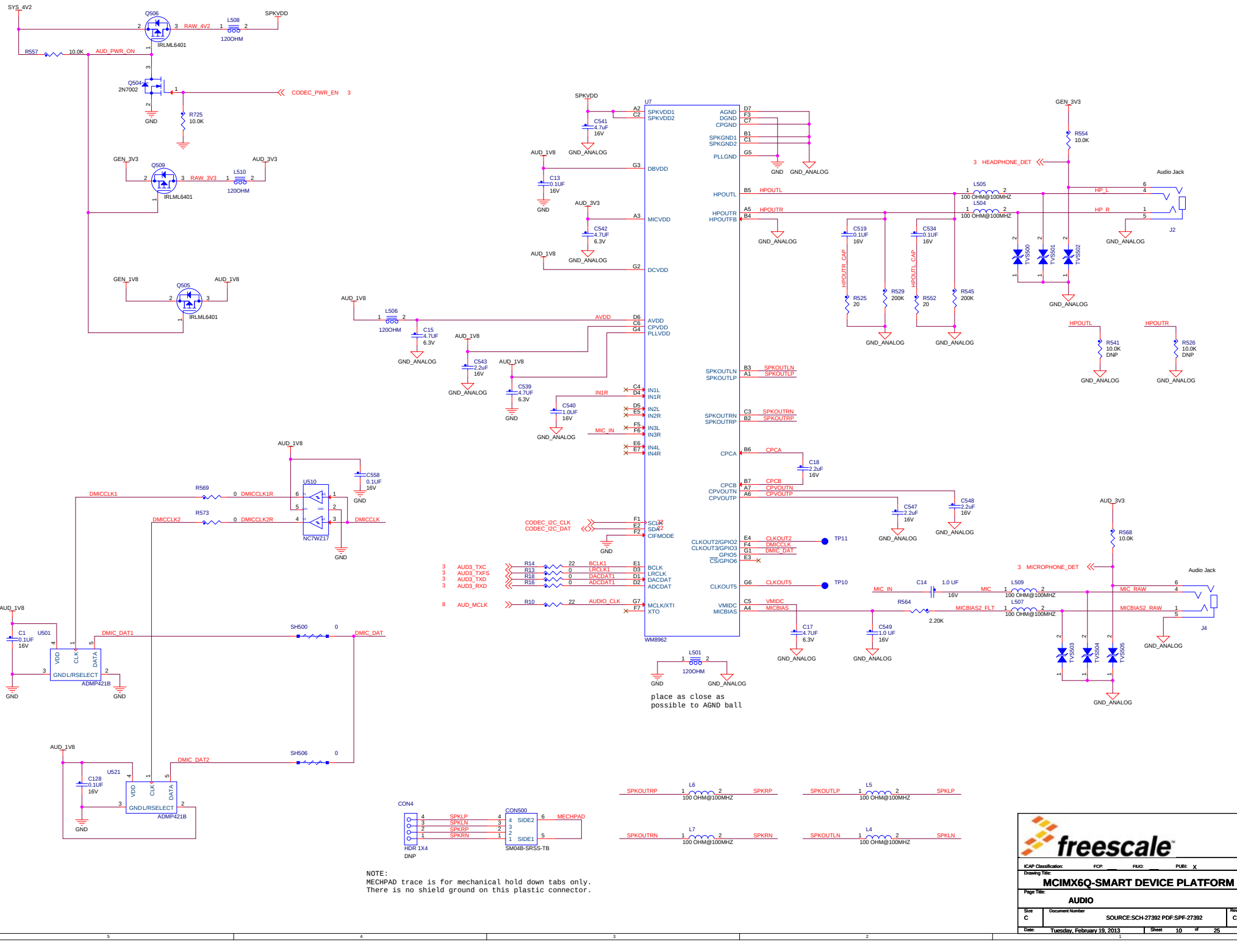
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Q506
IRLML6401
RAW_4V2
L508
120OHM
SPKVDD
R557
10.0K
AUD_PWR_ON
Q504
2N7002
CODEC_PWR_EN
R725
10.0K
GND
GEN_3V3
Q509
IRLML6401
RAW_3V3
L510
120OHM
AUD_3V3
GEN_1V8
Q505
IRLML6401
AUD_1V8
U7
SPKVDD1
SPKVDD2
DBVDD
MICVDD
DCVDD
AVDD
CPVDD
PLLVDD
IN1L
IN1R
IN2L
IN2R
IN3L
IN3R
IN4L
IN4R
SCLK
SDA
CIFMODE
BCLK
LRCLK
DACDAT
ADCDAT
MCLK/XTI
XTO
AGND
DGND
CPGND
SPKGND1
SPKGND2
PLLGND
HPOUTL
HPOUTR
HPOUTFB
SPKOUTLN
SPKOUTLP
SPKOUTRN
SPKOUTRP
CPCA
CPCB
CPVOUTN
CPVOUTP
CLKOUT2/GPIO2
CLKOUT3/GPIO3
GPIO5
CS/GPIO6
CLKOUT5
VMIDC
MICBIAS
WM8962
C541 4.7uF 16V
C13 0.1UF 16V
C542 4.7UF 6.3V
C15 4.7UF 6.3V
C543 2.2uF 16V
C539 4.7UF 6.3V
C540 1.0UF 16V
L506
120OHM
L501
120OHM
place as close as possible to AGND ball
R554 10.0K
HEADPHONE_DET
Audio Jack
J2
L505 100 OHM@100MHZ
L504 100 OHM@100MHZ
HP_L
HP_R
C519 0.1UF 16V
C534 0.1UF 16V
HPOUTR_CAP
HPOUTL_CAP
R525 20
R529 200K
R552 20
R545 200K
TVS500
TVS501
TVS502
R541 10.0K DNP
R526 10.0K DNP
C18 2.2uF 16V
C547 2.2uF 16V
C548 2.2uF 16V
TP11
TP10
C17 4.7UF 6.3V
C549 1.0 UF 16V
R564 2.20K
C14 1.0 UF 16V
L509 100 OHM@100MHZ
L507 100 OHM@100MHZ
MIC_IN
MIC
MICBIAS2_FLT
MICBIAS2_RAW
MICROPHONE_DET
R568 10.0K
J4
TVS503
TVS504
TVS505
R569 0 DMICCLK1R
R573 0 DMICCLK2R
U510
NC7WZ17
C558 0.1UF 16V
DMICCLK1
DMICCLK2
DMICCLK
U501
ADMP421B
C1 0.1UF 16V
DMIC_DAT1
SH500 0
DMIC_DAT
U521
C128 0.1UF 16V
DMIC_DAT2
SH506 0
CODEC_I2C_CLK
CODEC_I2C_DAT
AUD3_TXC
AUD3_TXFS
AUD3_TXD
AUD3_RXD
AUD_MCLK
R14 22 BCLK1
R13 0 LRCLK1
R18 0 DACDAT1
R16 0 ADCDAT1
R10 22 AUDIO_CLK
CON4
HDR 1X4
DNP
CON500
SM04B-SRSS-TB
MECHPAD
SPKLP
SPKLN
SPKRP
SPKRN
L6 100 OHM@100MHZ
L5 100 OHM@100MHZ
L7 100 OHM@100MHZ
L4 100 OHM@100MHZ
NOTE:
MECHPAD trace is for mechanical hold down tabs only.
There is no shield ground on this plastic connector.
freescale
ICAP Classification:
FCP:
FIUO:
PUBI: X
Drawing Title:
MCIMX6Q-SMART DEVICE PLATFORM
Page Title:
AUDIO
Size C
Document Number
SOURCE:SCH-27392 PDF:SPF-27392
Rev C3
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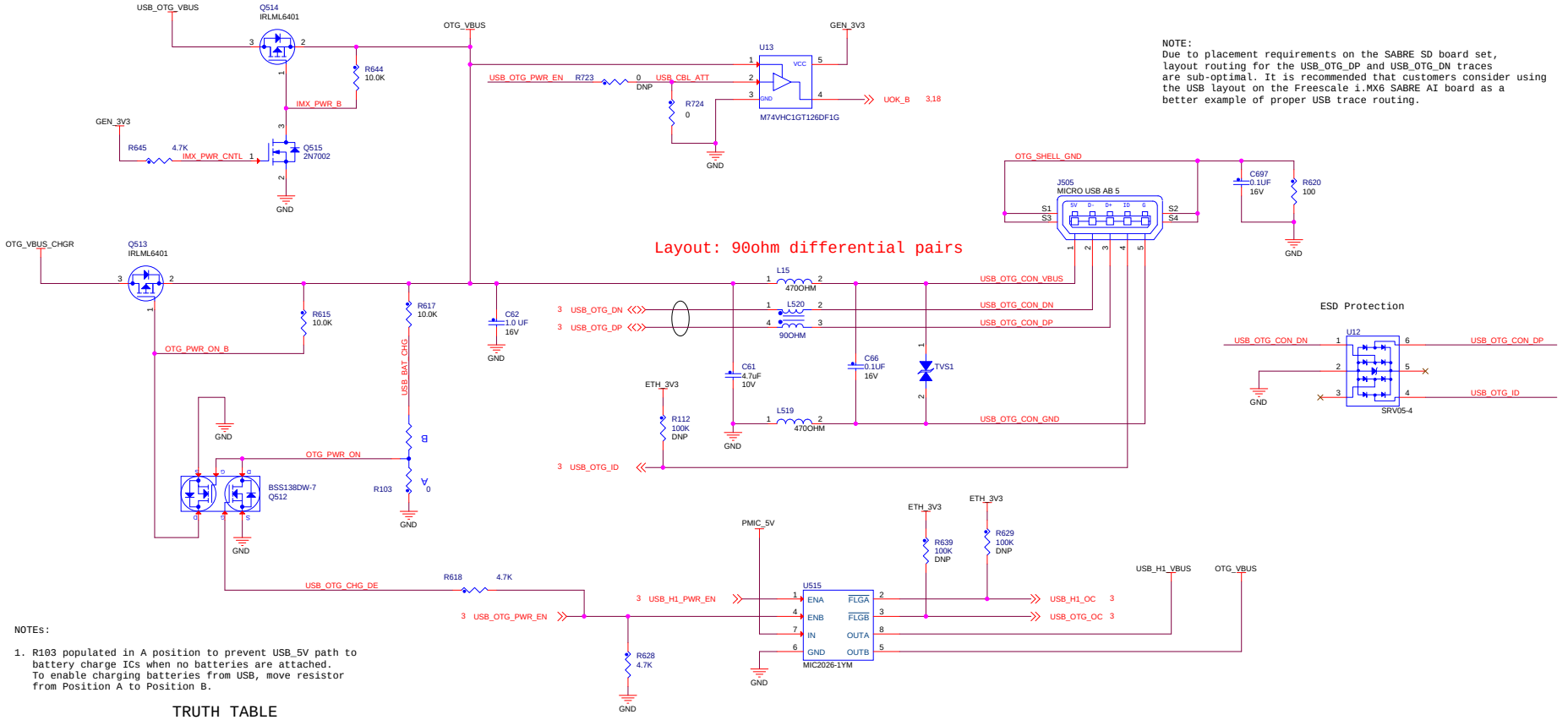

NOTEs:

1. R103 populated in A position to prevent USB_5V path to battery charge ICs when no batteries are attached. To enable charging batteries from USB, move resistor from Position A to Position B.

TRUTH TABLE

OTG_VBUS INPUT TO BATTERY CHARGERS

USB_OTG _PWR_EN	OTG_PWR _ON	OTG_PWR _ON_B	OTG_VBUS _CHGR
LOW	HIGH	LOW	POWERED
HIGH	LOW	HIGH	NOT POWERED

NOTE:
On all three pad resistor options, resistors are to be initially populated on pads 1 - 2 (Option A). Users may move resistors from their default locations as needed.

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: USB

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To Processor I/O supply

Alternate power source for processor I/O

NOTE:
Solder short normally connects NVCC_RGMII to ETH_VDDIO.
To connect NVCC_RGMII to VGEN1_1V5, cut the trace between pads 1 - 2 and solder a 0 Ohm resistor between pads 2 - 3.

Layout: High speed data lines : 50 ohms
Place R634 near the AR8031 PHY.

Layout: 100 ohm differential pairs

EMI Filter Reserved
470pF are for LED

NOTE:
Place R626 close to Ethernet PHY.

NOTE:
R657 pull up required to support AR8031 open drain MDIO pin, when AR8031 is outputting data. Pull up not required on MDC since line is only driven by i.MX 6.

Place LED D11 near LED for pins 11 - 12 of RJ-45 connector. Orange LED indicates 1000 speed.

Power-on Strapping Pins

MODE2[3:0]

(Default assemble: 0000)
1100 BaseT, RMII1;
1101 BaseT, RMII2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMII;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RGMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, RGMII, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved

PHYADDRESS0	RGMII_RXD0	R144 10.0K DNP
PHYADDRESS1	RGMII_RXD1	R143 10.0K
MODE2[1]	RGMII_RXD2	R142 10.0K
MODE2[3]	RGMII_RXD3	R631 10.0K
MODE2[2]	PHY_RX_CLK	R146 10.0K
MODE2[0]	RGMII_RXDV	R145 10.0K
SEL_GPIO_INT	RGMII_LED_1000	R141 10.0K
ANA_MOD	RGMII_LED_ACT	R140 10.0K

R636 10.0K, R638 10.0K DNP; R148 10.0K DNP, R147 10.0K DNP; 2V5_RGMII; GND

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ICAP Classification:	FCP: ___ FIUO: ___ PUBI: X
Drawing Title:	MCIMX6Q-SMART DEVICE PLATFORM
Page Title:	ETHERNET
Size: C	Document Number: SOURCE:SCH-27392 PDF:SPF-27392 Rev: C3
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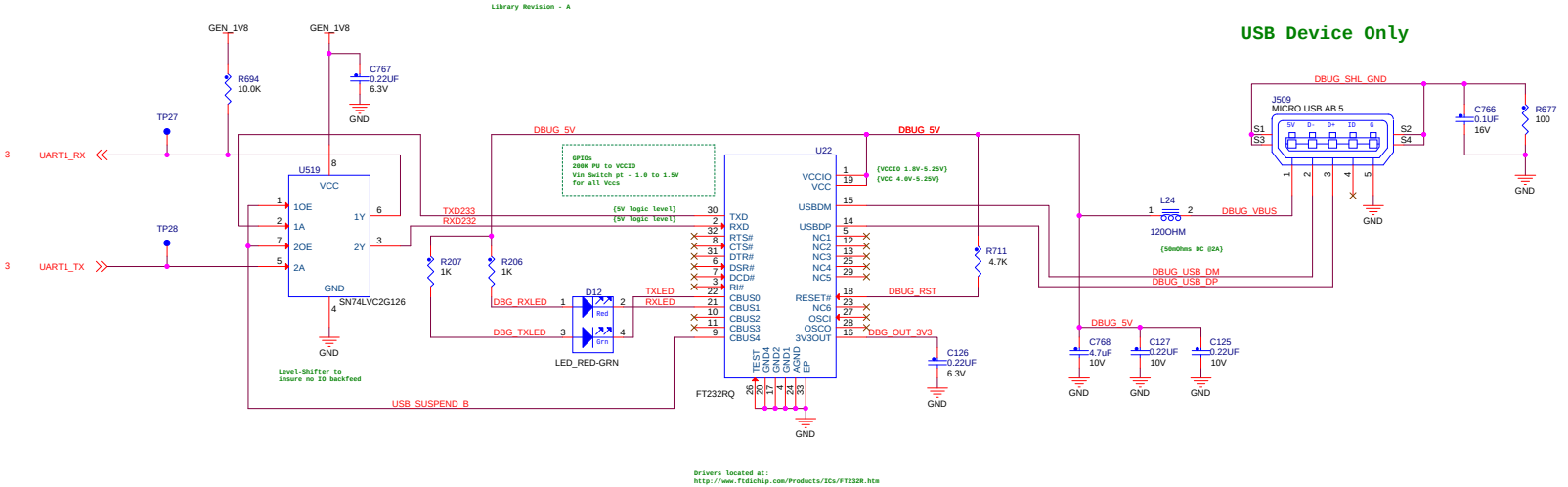
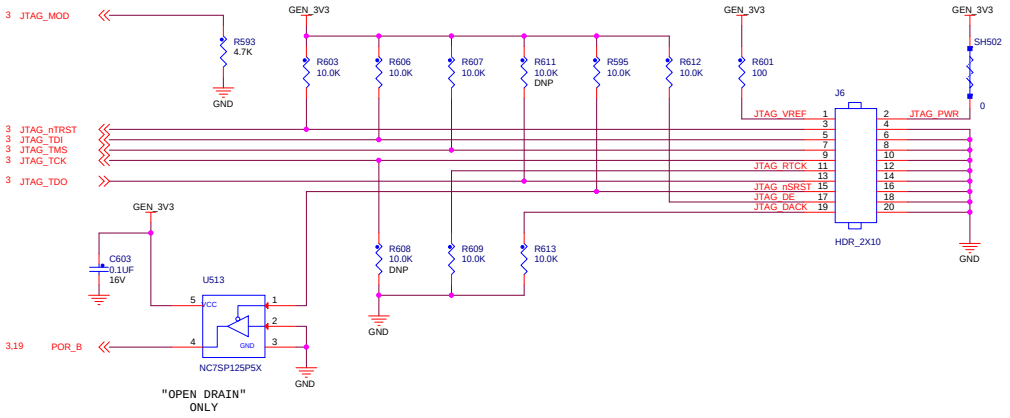
DEBUG UART TO USB CONVERSION



JTAG



freescale

ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: JTAG, DEBUG

Size	Document Number	Rev
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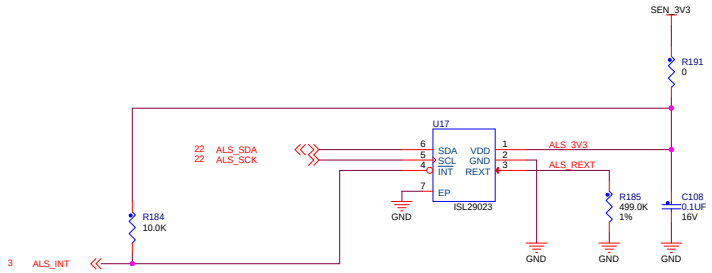
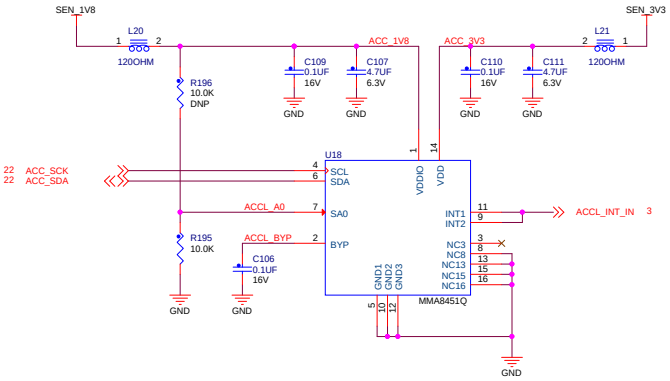
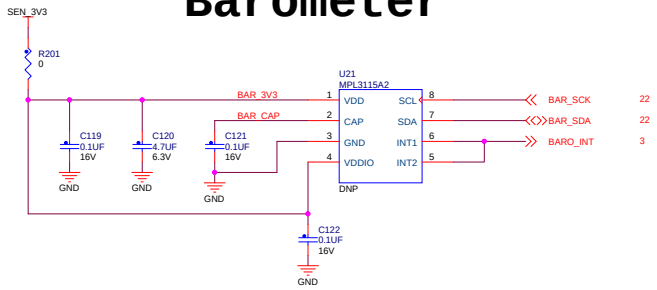
Ambient Light Sensor

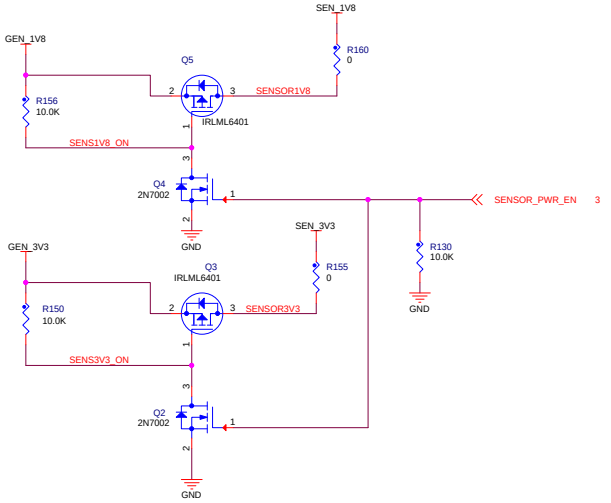


3-AXIS ACCELEROMETER

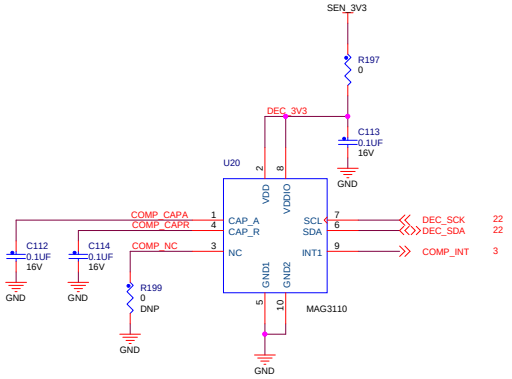


Barometer





Digital eCompass



freescale

ICAP Classification:	FCP: ___ FIUO: ___ PUBI: X	
Drawing Title:	MCIMX6Q-SMART DEVICE PLATFORM	
Page Title:	SENSORS	
Size: C	Document Number: SOURCE:SCH-27392 PDF:SPF-27392	Rev: C3
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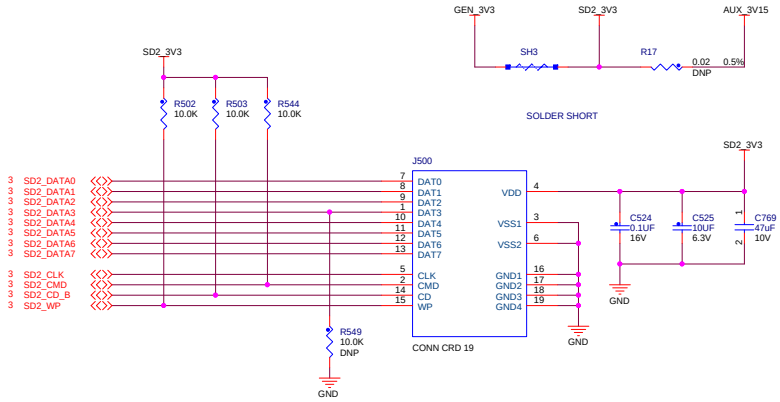
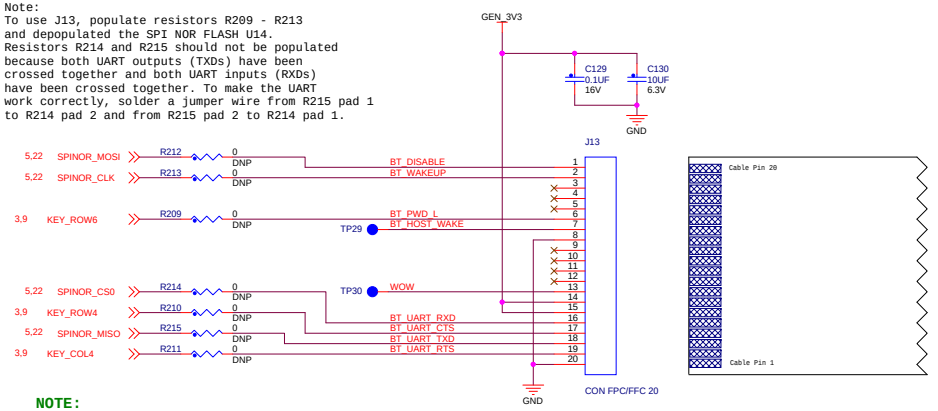
AUX SDIO CARD SOCKET



Layout:
50ohm, SD signals(SD_DATAx, SD_CMD, SD_CLK) length equal

BLUETOOTH CABLE CONNECTOR

Note:
To use J13, populate resistors R209 - R213
and depopulated the SPI NOR FLASH U14.
Resistors R214 and R215 should not be populated
because both UART outputs (TXDs) have been
crossed together and both UART inputs (RXDs)
have been crossed together. To make the UART
work correctly, solder a jumper wire from R215 pad 1
to R214 pad 2 and from R215 pad 2 to R214 pad 1.

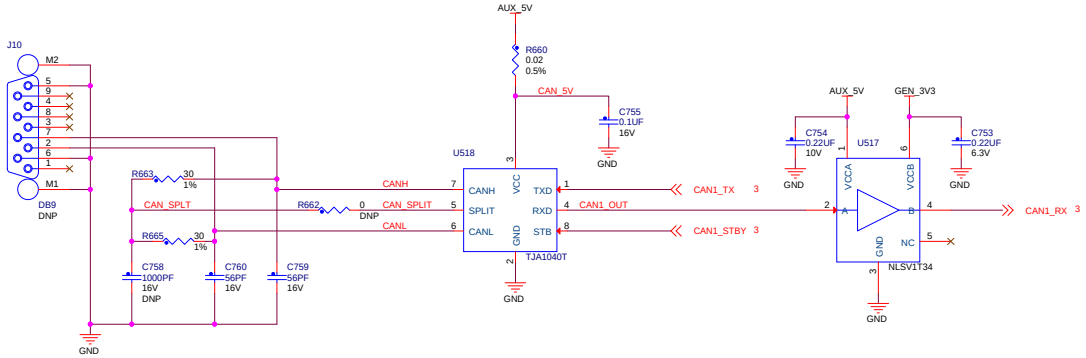


NOTE:
The AUX SDIO CARD SOCKET and the BLUETOOTH CABLE CONNECTOR have been designed and tested specifically for use with the WIFI/BT combo card SX-SDCAN-2830BT Developed and sold by Silex Technolgy. The developer may need to consult the datasheet of other WIFI solutions for compatibility with this card socket.

NOTE:
Pin 1 of the cable connector on the Smart Device board is opposite Pin 20 of the WIFI/BT module. For the FFC to lie flat, the pin order number needs to be reversed on the schematics.

NOTE:
J13 has been provided for testing the Bluetooth functionality of the SX-SDCAN-2830BT module. This part of the circuit has not yet been tested, which is why the initial boards are being shipped with isolation resistors R209 - R215 depopulated. Until fully tested, the developer assumes responsibilty for enabling J13 tor testing purposed. See the Freescale HW User Guide for the Smart Device board for details (to be published 2Q13).

OPTIONAL CAN PINOUT



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ICAP Classification:	FCP: ___ FIUO: ___ PUBI: X
Drawing Title:	MCIMX6Q-SMART DEVICE PLATFORM
Page Title:	AUX SDIO CONN, CAN
Size: C	Document Number: SOURCE:SCH-27392 PDF:SPF-27392 Rev: C3
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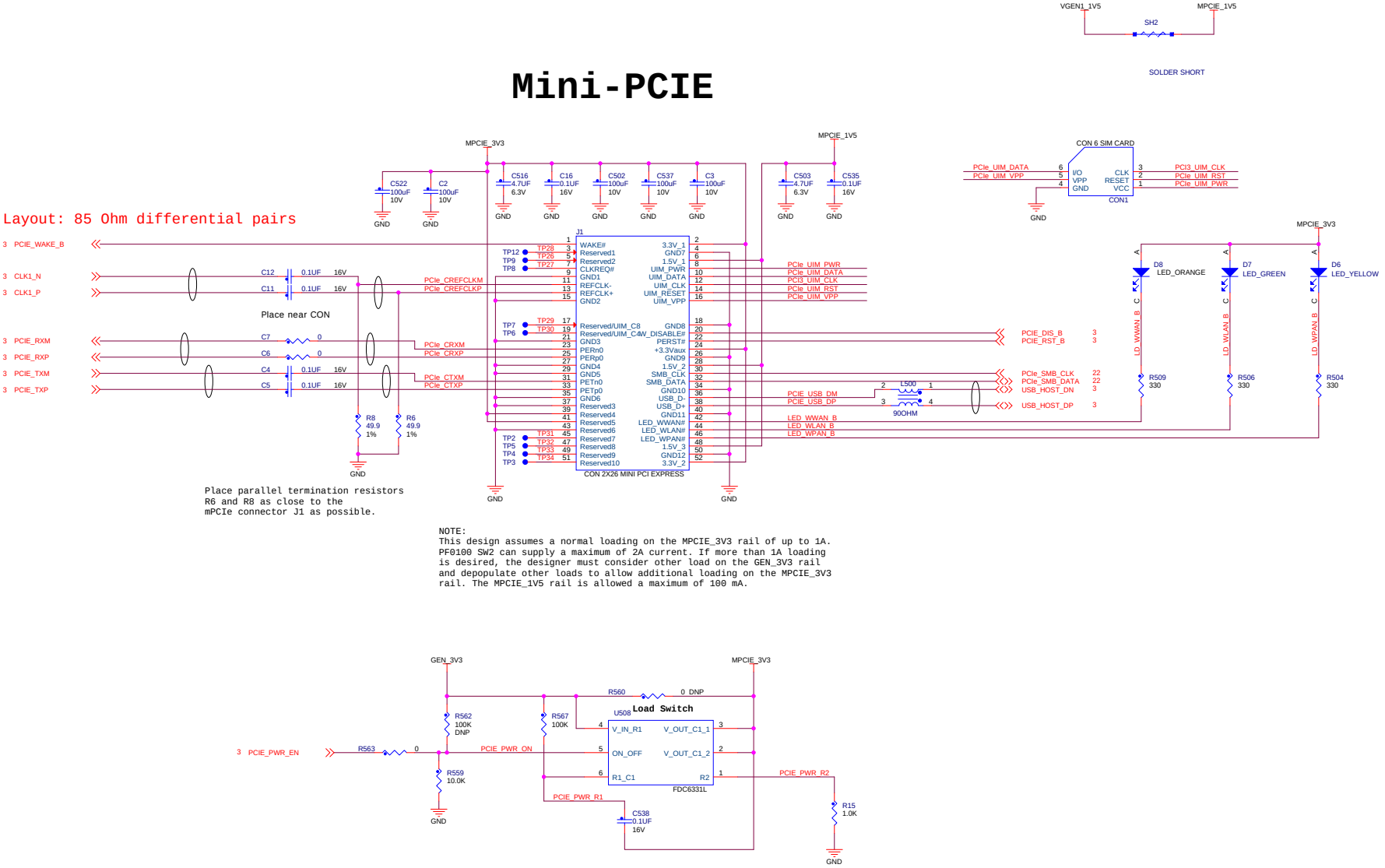
Mini-PCIE



NOTE:
This design assumes a normal loading on the MPCIE_3V3 rail of up to 1A. PF0100 SW2 can supply a maximum of 2A current. If more than 1A loading is desired, the designer must consider other load on the GEN_3V3 rail and depopulate other loads to allow additional loading on the MPCIE_3V3 rail. The MPCIE_1V5 rail is allowed a maximum of 100 mA.

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: **MCIMX6Q-SMART DEVICE PLATFORM**

Page Title: **mPCIe CONN**

Size	Document Number	Rev
C	SOURCE:SCH-27392 PDF:SPF-27392	C3

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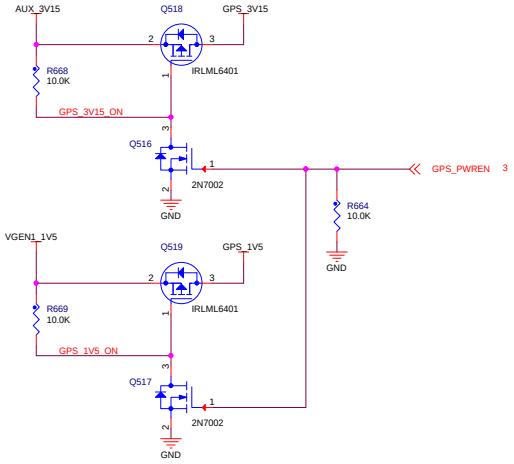
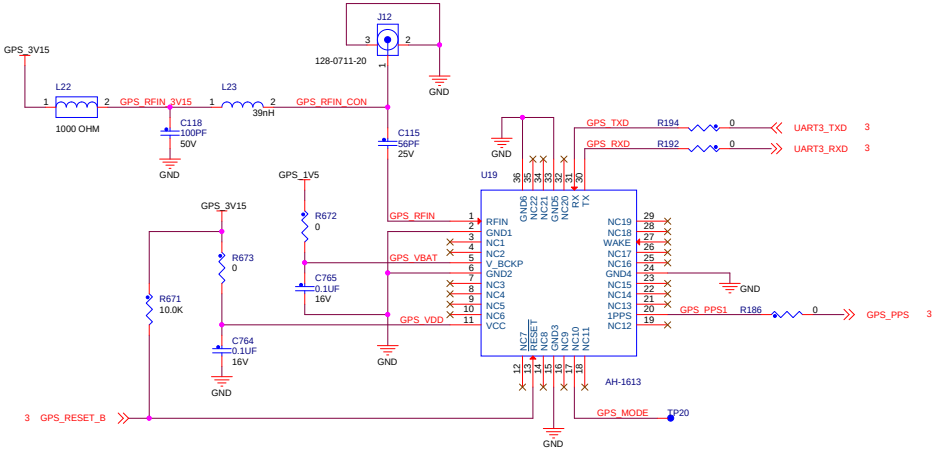
GPS Receiver





ICAP Classification:	FCP: ___	FIUO: ___	PUBI: X
Drawing Title:	MCIMX6Q-SMART DEVICE PLATFORM		
Page Title:	GPS MODULE		
Size: C	Document Number: SOURCE:SCH-27392 PDF:SPF-27392		Rev: C3
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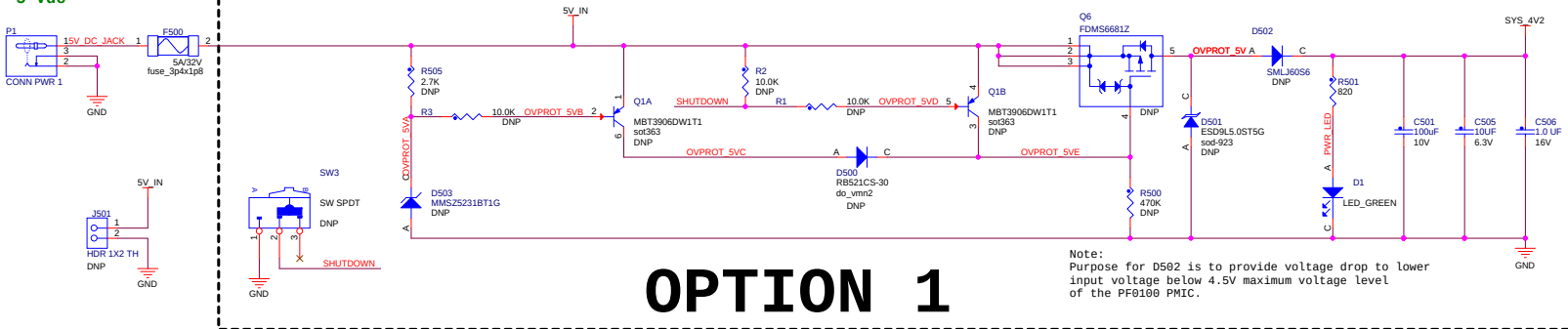
OVER VOLTAGE PROTECTION

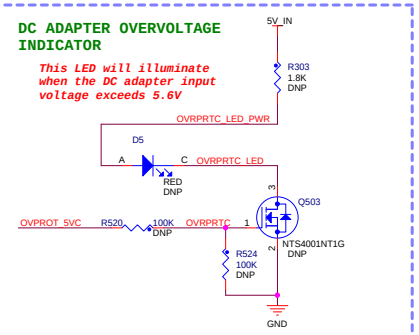
External Power 5 Vdc



Note:
Purpose for D502 is to provide voltage drop to lower input voltage below 4.5V maximum voltage level of the PF0100 PMIC.

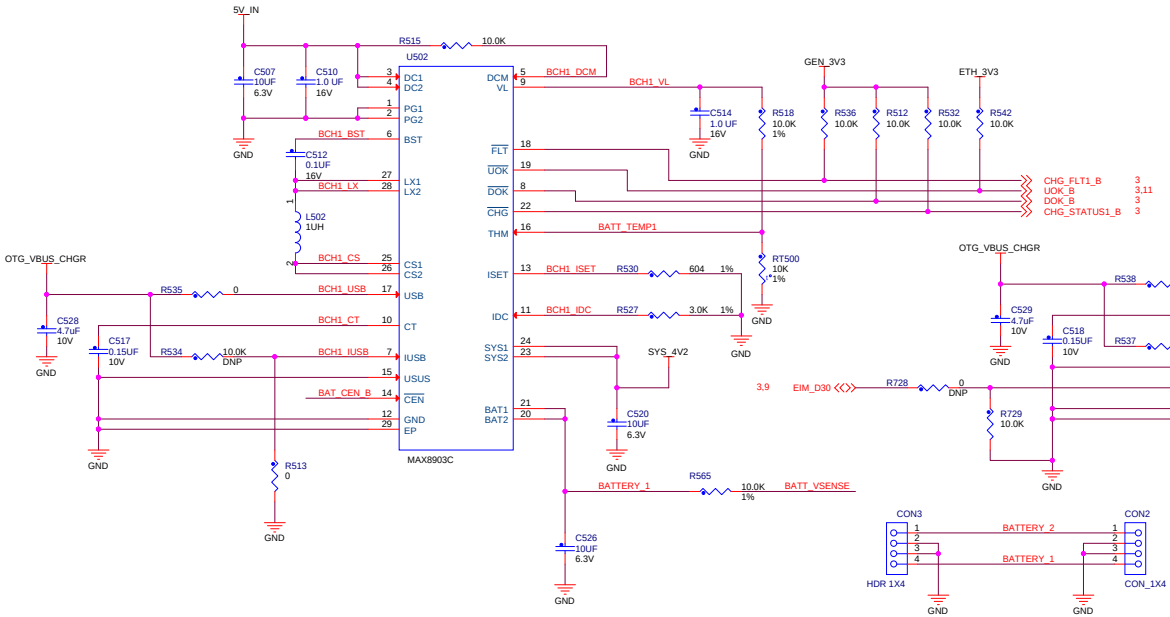
DC ADAPTER OVERVOLTAGE INDICATOR

This LED will illuminate when the DC adapter input voltage exceeds 5.6V

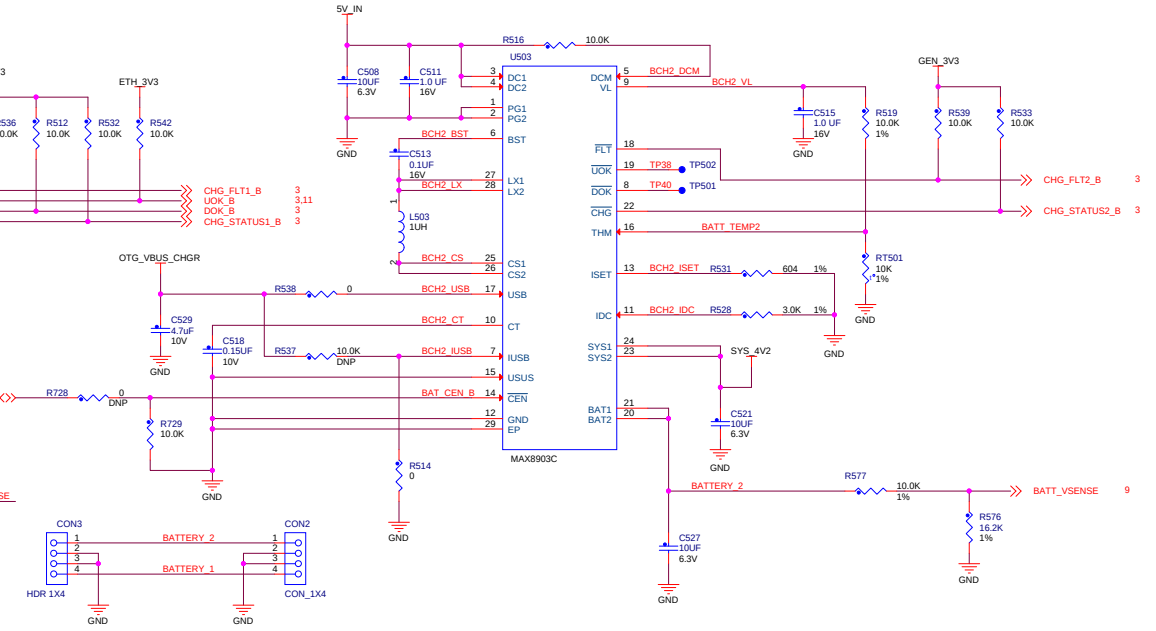


OPTION 1

BATTERY 1 CHARGE CIRCUIT



BATTERY 2 CHARGE CIRCUIT



OPTION 2

NOTE:
Battery posts are meant for two, single cell 3.7 Li-ION batteries to be added in parallel.

NOTE:
R728 is provided for testing a means to suspend battery charging so that an acurate voltage reading can be taken during the battery charge cycle. It has not yet been tested. When populating R728, R134 should be depopulated. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

Note: Populate either
Option #1 for the Smart Device Board, or
Option #2 for the Smart Device Platform

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: BATTERY CHARGER

Size	Document Number	Rev
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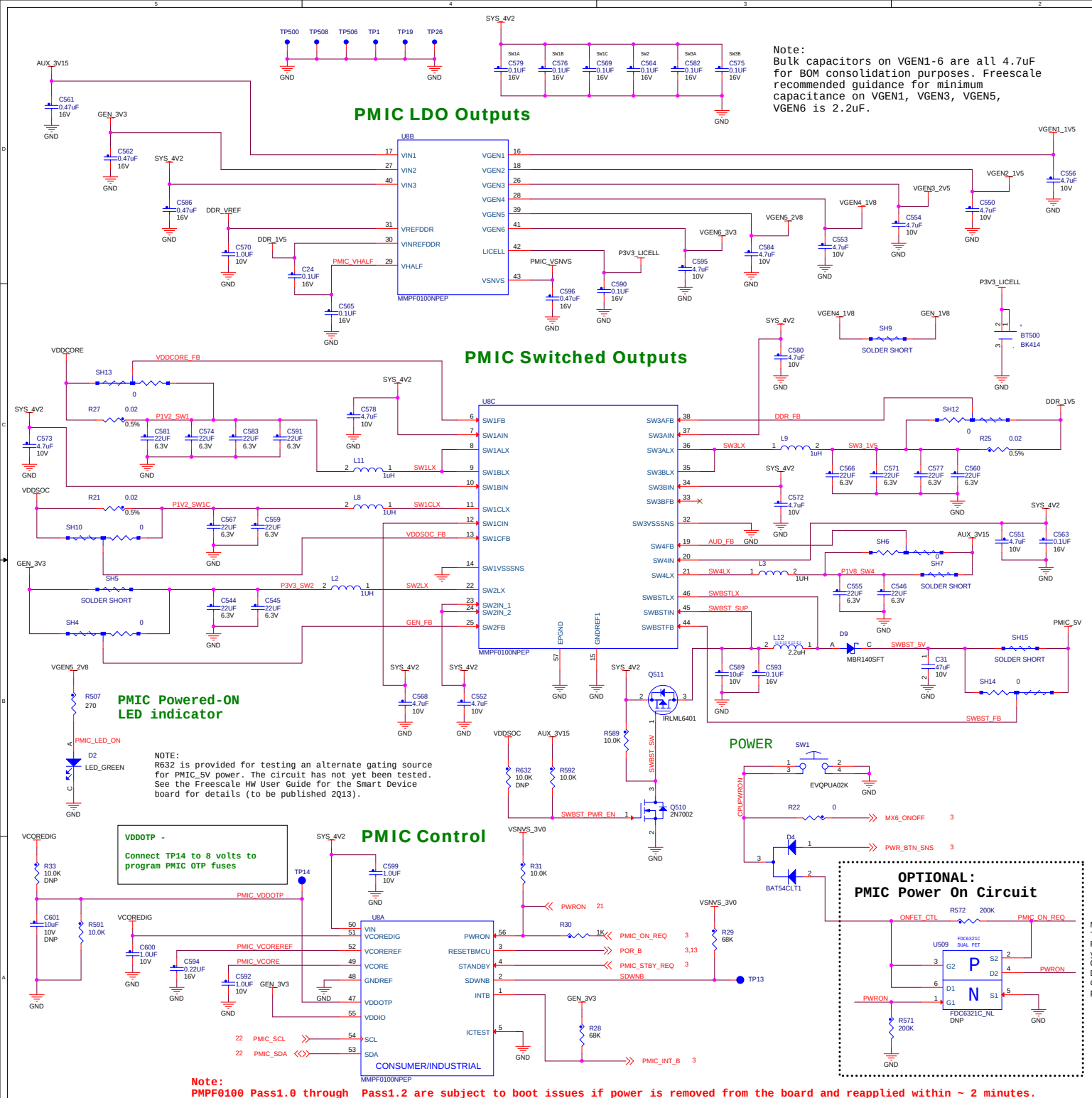

Typical Power Requirements

	Voltage	Power Up Sequence	Current Drawn (mA)	SYS 4V2 Current (mA)	NOTES
SW1A	1.375	1	2155	1001	
SW1B					
SW1C	1.375	2	1590	739	
SW2	3.3	5	653	728	
SW3A	1.5	3	1500	760	
SW3B					
SW4	3.15	6	200	213	
SWBST	5.0	13	300	507	
VGEN1	1.5	9	100	0	Supplied from SW4
VGEN2	1.5	10	250	0	Supplied from SW4
VGEN3	2.8	11	70	66	
VGEN4	1.8	12	310	189	
VGEN5	2.8	10	75	71	See Note on Page 20
VGEN6	3.3	8	160	178	
VSNVS	3.0	0	0.2	0	
VREFDDR	0.75	3	10	3	
Total System Current Requirements:			4454		

SYSTEM POWER RAILS

Voltge	Rail Name	Block	Generated By	Current Capability (mA)	NOTES
5.0	PMIC_5V	USB	PF0100 SWBST	600	
		LVDS1			
		HDMI			
	AUX_5V	SATA	MAX8815	1000	
		LVDS0			
		CAN			
3.3	GEN_3V3	EMMC	PF0100 SW2	2000	NVCC_LCD NVCC_EIM0/1/2 NVCC_GPIO NVCC_SD2/3 NVCC_NANDF NAND_JTAG
		SD3			
		NOR			
		SATA			
		LVDS			
		HDMI			
		MIPI			
		mPCIe			
		SENSORS			
	VGEN6_3V3	ETH	PF0100 VGEN6	200	NVCC_ENET
3.15	AUX_3V15	EXP HDR	PF0100 SW4	1000	Supplies: VGEN1 VGEN2
		TOUCH			
		GPS			
2.8	VDDHIGH_IN	IMX6	PF0100 VGEN5	100	
	VGEN3_2V5	CAMERA	PF0100 VGEN3	100	
2.5	GEN_2V5	SATA	IMX6 VDDHIGH_CAP	TBD	NVCC_MIPI
		HDMI			
		MIPI			
		mPCIe			
1.8	GEN_1V8	AUDIO	PF0100 VGEN4	350	NVCC_SD1 NVCC_CSI
		CAMERA			
		ACC			
1.5	VGEN2_1V5	CAMERA	PF0100VGEN2	250	
	VGEN1_1V5	GPS	PF0100 VGEN1	100	
		mPCIe			
	DDR_1V5	DDR	PF0100 SW3A/B	2500	
1.375	VDDCORE	ARMCORE	PF0100 SW1A/B	2500	
	VDDSOC	VDDSOC	PF0100 SW1C	1750	
0.75	VREFDDR	DDR	PF0100 VREFDDR	10	

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: PF0100 PMIC

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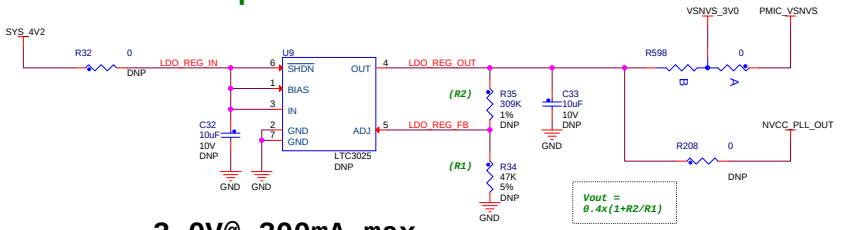
Optional LDO



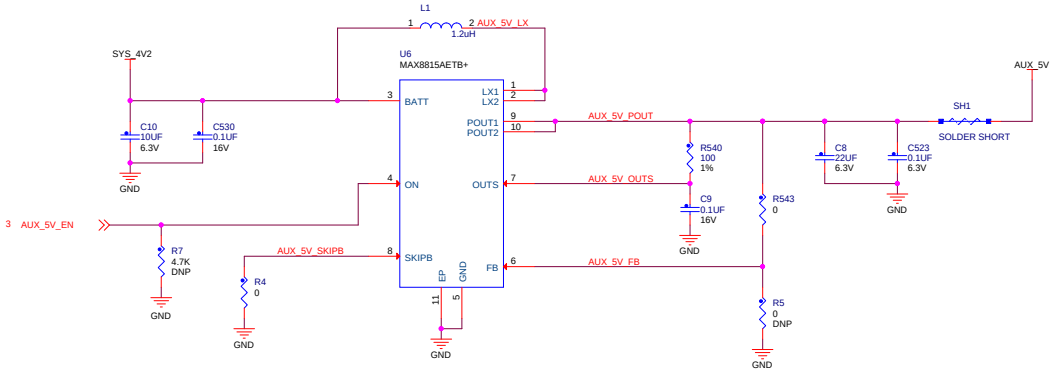
3.0V@ 300mA max

NOTE FOR VDDHIGH_IN LOADING ON VGEN5:
VDDHIGH was placed on VGEN5 early in the design as a compromise solution for a board designed primarily for software development. Validation of the i.MX6 processor has shown that operations at elevated temperatures may cause VDDHIGH_IN to require much more current than VGEN5 can supply. It is recommended for robust designs potentially operating at more extreme temperatures for VDDHIGH to be supplied from a power rail that can supply 250 mA or more.
This allows for datasheet maximum of 125 mA for internal VDDHIGH_IN loads plus 125 mA for external PHY IO loads.

The optional LDO U9 shown on this page could be reconfigured to supply both VDDHIGH_IN and VDD_SNVS_IN loads to meet the additional current requirments

U9 is no longer required for PF0100 VSNVS issue, but may be desired for NVCC_PLL_VOUT.
It is being left in a depopulated condition. If the LDO is needed, R34 and R35 should be populated as follows:
For VSNVS (3.0V): R34 = 47K, R35 = 309K
For NVCC_PLL_OUT (1.1V): R34 = 47K, R35 = 82.5K

5.0V@1A DC2DC



ICAP Classification:	FCP: ___	FIUO: ___	PUBI: X
Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM			
Page Title: AUX VOLT REG			
Size: C	Document Number: SOURCE:SCH-27392 PDF:SPF-27392		Rev: C3
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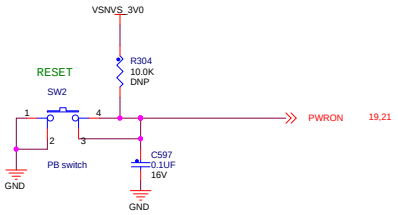
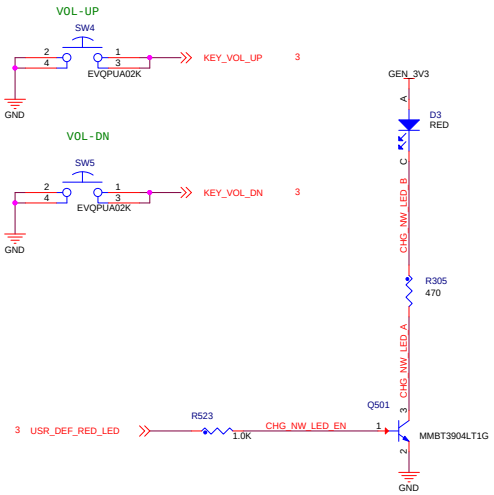
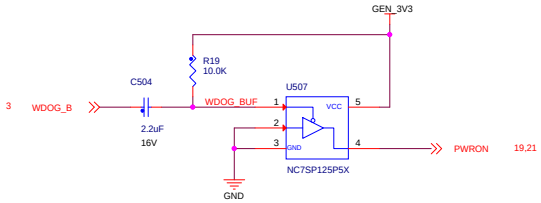


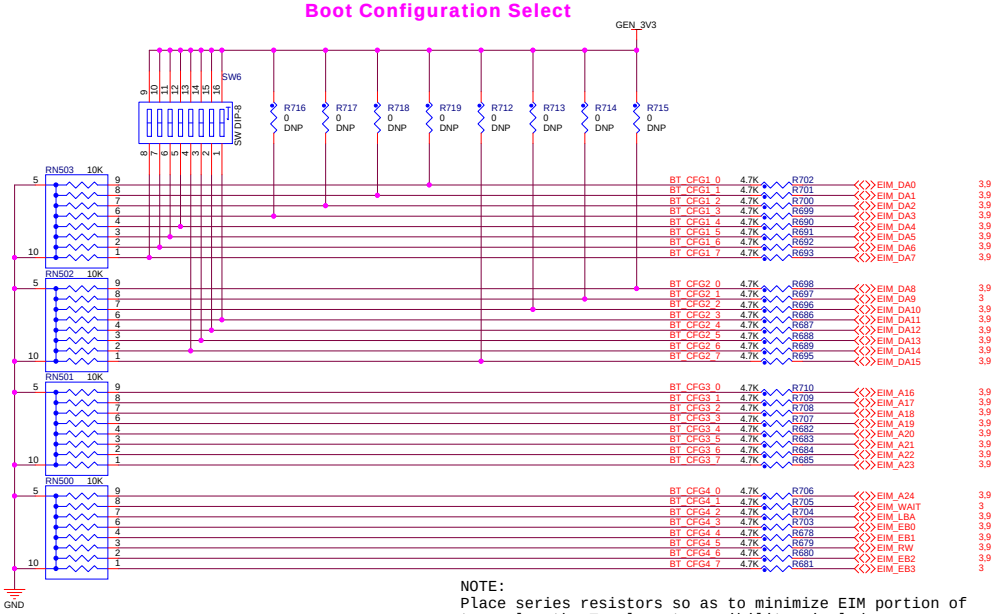
NOTE:
On Rev B4 and later designs, the RESET button is connected directly to the PWRON input of the PMIC. This will cause a complete board reset (Processor & PMIC) when the RESET button is pressed.

U/I KEY





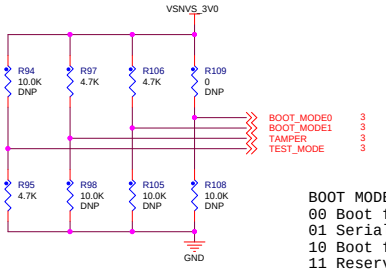
Boot Configuration Select



NOTE:
Place series resistors so as to minimize EIM portion of trace length. Two layout possibilites include:
1) As close to processor as possbile.
2) Close to other componets using EIM signals.

Boot Select Table

8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 10 = 8-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0010 = SATA Boot				X	X	X	0



BOOT MODES:
00 Boot from fuses
01 Serial downloader
10 Boot from board settings
11 Reserved

freescale

ICAP Classification: FCP: ___ FIUO: ___ PUBL: X

Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: BOOT SELECT

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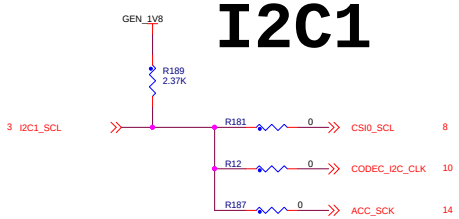
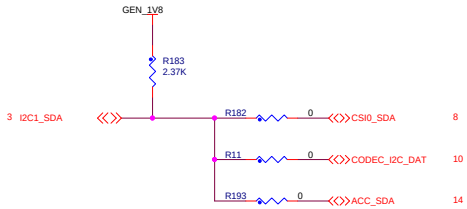
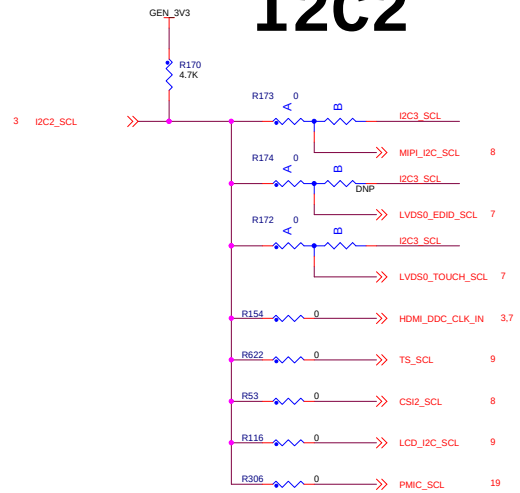
I2C1

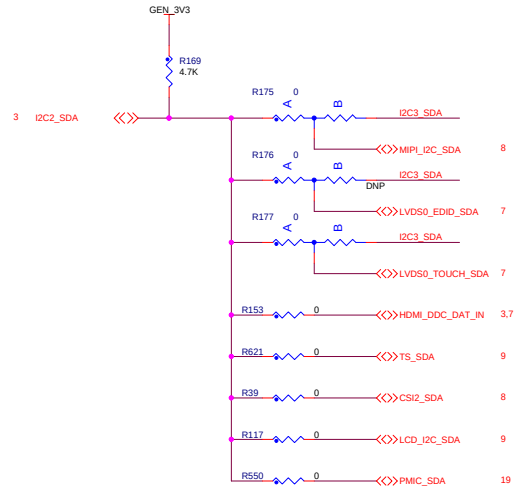




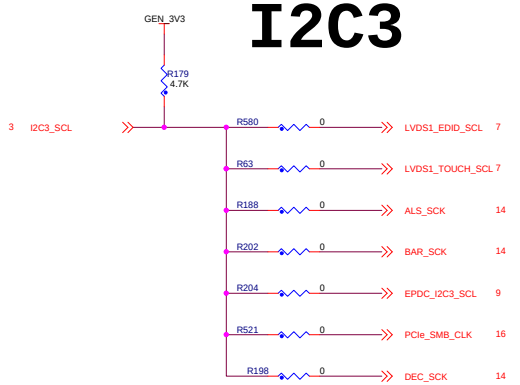
NOTE:
R183 and R189 were changed to bring I2C rise time from LOW >> HIGH within electric specification. If using a CODEC other than the one used in this design, it may be possbile to switch pull up resistors back to 4.7K.

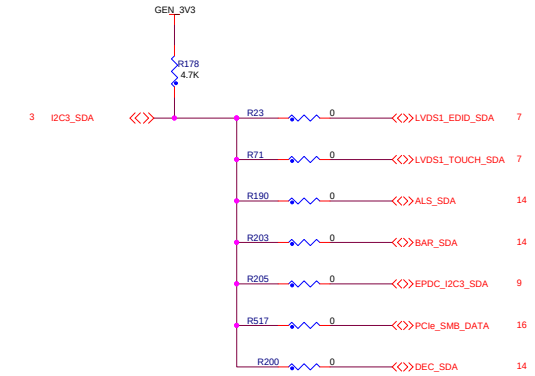
I2C2



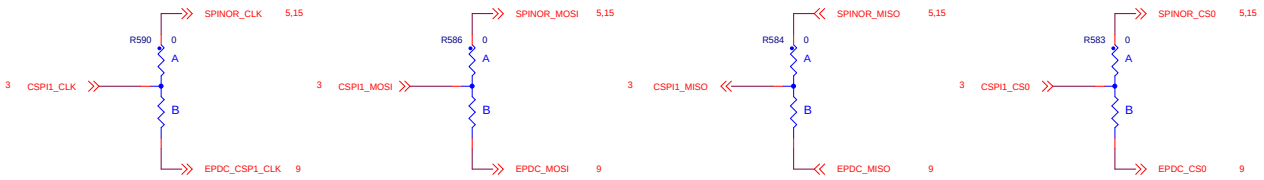


I2C3





CSPI1



NOTE:
On all three pad resistor options, resistors are to be initially populated on pads 1 - 2 (Option A). Users may move resistors from their default locations as needed.

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: COMM CHANNEL STEERING

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Build Option: MCIMX6Q-SDB

1.	CAN Output not populated: J10
2.	Battery Charging circuit not populated: C507, C508, C510, C511, C512, C513, C514, C515, C517, C518, C520, C521, C526, C527, C528, C529, CON2, CON3, L502, L503, R512, R513, R514, R515, R516, R518, R519, R527, R528, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R542, R565, R577, R729, RT500, RT501, U502, U503
3.	SPI NOR Flash not populated: C83, R149, R643, R646, U14
4.	MIPI Display/Camera Expansion Ports not populated: C28, C29, C30, C50, C116, C117, C123, C124, C585, C587, C588, C602, J11, J5, L25, R26, R165, R173, R175, R726, U10
5.	Audio Block Components not populated: C1, C128, C558, R569, R573, U501, U510, U521
6.	EPDC Port Connector not populated: J508
7.	Ambient Light Sensor not populated: C108, R184, R185, R188, R190, R191, U17
8.	GPS Module not populated: C115, C118, C764, C765, J12, L22, L23, Q516, Q517, Q518, Q519, R186, R192, R194, R664, R668, R669, R671, R672, R673, U19
9.	Extra Bulk Capacitors not populated: C39, C54, C68, C606, C607, C608, C609, C610, C611, C612, C673, C681
10.	BlueTooth Connector Isolation Resistors: R209, R210, R211, R212, R213, R214, R215

Build Option: MCIMX6Q-SDP MCIMX6DL-SDP

1.	CAN Output not populated: J10
2.	OverVoltage Protection circuit not populated: (OverVoltage Protection provided by battery charge ICs) D5, D500, D501, D502, D503, J501, Q1, Q6, Q503, R1, R2, R3, R303, R500, R505, R520, R524, SW3
3.	Extra Bulk Capacitors not populated: C39, C54, C68, C606, C607, C608, C609, C610, C611, C612, C673, C681
4.	BlueTooth Connector Isolation Resistors: R209, R210, R211, R212, R213, R214, R215

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: BUILD OPTON TABLES

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PIN MUX TABLES

Ball Name	Ball Number	IO MUX	Use
CSI0_DAT10	M1	ALT3	UART1_TXD_MUX
CSI0_DAT11	M3	ALT3	UART1_RXD_MUX
CSI0_DAT12	M2	ALT0	CSI0_D[12]
CSI0_DAT13	L1	ALT0	CSI0_D[13]
CSI0_DAT14	M4	ALT0	CSI0_D[14]
CSI0_DAT15	M5	ALT0	CSI0_D[15]
CSI0_DAT16	L4	ALT0	CSI0_D[16]
CSI0_DAT17	L3	ALT0	CSI0_D[17]
CSI0_DAT18	M6	ALT0	CSI0_D[18]
CSI0_DAT19	L6	ALT0	CSI0_D[19]
CSI0_DAT4	N1	ALT4	AUD3_TXC
CSI0_DAT5	P2	ALT4	AUD3_TXD
CSI0_DAT6	N4	ALT4	AUD3_TXFS
CSI0_DAT7	N3	ALT4	AUD3_RXD
CSI0_DAT8	N6	ALT4	I2C1_SDA
CSI0_DAT9	N5	ALT4	I2C2_SCL
CSI0_MCLK	P4	ALT0	CSI0_HSYNC
CSI0_PIXCLK	P1	ALT0	CSI0_PIXCLK
CSI0_VSYNC	N2	ALT0	CSI0_VSYNC
DI0_DISP_CLK	N19	ALT1	DI0_DISP_CLK
DI0_PIN15	N21	ALT1	DISP0_DRDT
DI0_PIN2	N25	ALT1	DISP0_HSYNCH
DI0_PIN3	N20	ALT1	DISP0_VSYNCH
DI0_PIN4	P25	ALT1	DISP0_CONTRST
DISP0_DAT0	P24	ALT1	DISP0_DAT[0]
DISP0_DAT1	P22	ALT1	DISP0_DAT[1]
DISP0_DAT10	R21	ALT1	DISP0_DAT[10]
DISP0_DAT11	T23	ALT1	DISP0_DAT[11]
DISP0_DAT12	T24	ALT1	DISP0_DAT[12]
DISP0_DAT13	R20	ALT1	DISP0_DAT[13]
DISP0_DAT14	U25	ALT1	DISP0_DAT[14]
DISP0_DAT15	T22	ALT1	DISP0_DAT[15]
DISP0_DAT16	T21	ALT1	DISP0_DAT[16]
DISP0_DAT17	U24	ALT1	DISP0_DAT[17]
DISP0_DAT18	V25	ALT1	DISP0_DAT[18]
DISP0_DAT19	U23	ALT1	DISP0_DAT[19]
DISP0_DAT2	P23	ALT1	DISP0_DAT[2]
DISP0_DAT20	U22	ALT1	DISP0_DAT[20]
DISP0_DAT21	T20	ALT1	DISP0_DAT[21]
DISP0_DAT22	V24	ALT1	DISP0_DAT[22]
DISP0_DAT23	W24	ALT1	DISP0_DAT[23]
DISP0_DAT3	P21	ALT1	DISP0_DAT[3]
DISP0_DAT4	P20	ALT1	DISP0_DAT[4]
DISP0_DAT5	R25	ALT1	DISP0_DAT[5]
DISP0_DAT6	R23	ALT1	DISP0_DAT[6]
DISP0_DAT7	R24	ALT1	DISP0_DAT[7]
DISP0_DAT8	R22	ALT1	DISP0_DAT[8]
DISP0_DAT9	T25	ALT1	DISP0_DAT[9]
EIM_D21	H20	ALT4	USB_OTG_OC
EIM_D22	E23	ALT4	USB_OTG_PWR_EN
EIM_D24	F22	ALT2	UART3_TXD_MUX
EIM_D25	G22	ALT2	UART3_RXD_MUX
EIM_D30	J20	ALT6	USB_H1_OC
ENET_MDC	V20	ALT1	MDC
ENET_MDIO	V23	ALT1	MDIO
ENET_REF_CLK	V22	ALT1	ENET_TX_CLK
ENET_RX_ER	W23	ALT0	USB_OTG_ID
GPIO_0	T5	ALT0	CLKO
GPIO_1	T4	ALT1	WDOG_B
GPIO_3	R7	ALT2	I2C3_SCL
GPIO_6	T3	ALT3	I2C3_SDA
GPIO_7	R3	ALT3	TXCAN
GPIO_8	R5	ALT3	RXCAN
GPIO_16	R2	ALT1	No-Connect
KEY_COL0	W5	ALT0	SCLK
KEY_COL1	U7	ALT0	MISO
KEY_COL3	U5	ALT4	I2C2_SCL
KEY_ROW0	V6	ALT0	CSPI1_MOSI
KEY_ROW1	U6	ALT0	CSPI1_SS0
KEY_ROW3	T7	ALT4	I2C2_SDA
KEY_ROW2	W4	ALT6	HDMI_CEC_IN

Ball Name	Ball Number	IO MUX	Use
NANDF_D4	A19	ALT1	SD2_DAT4
NANDF_D5	B18	ALT1	SD2_DAT5
NANDF_D6	E17	ALT1	SD2_DAT6
NANDF_D7	C18	ALT1	SD2_DAT7
RGMII_RD0	C24	ALT1	RGMII_RD0
RGMII_RD1	B23	ALT1	RGMII_RD1
RGMII_RD2	B24	ALT1	RGMII_RD2
RGMII_RD3	D23	ALT1	RGMII_RD3
RGMII_RX_CTL	D22	ALT1	RGMII_RX_CTL
RGMII_RXC	B25	ALT1	RGMII_RXC
RGMII_TD0	C22	ALT1	RGMII_TD0
RGMII_TD1	F20	ALT1	RGMII_TD1
RGMII_TD2	E21	ALT1	RGMII_TD2
RGMII_TD3	A24	ALT1	RGMII_TD3
RGMII_TX_CTL	C23	ALT1	RGMII_TX_CTL
RGMII_TXC	D21	ALT1	RGMII_TXC
SD1_DAT3	F18	ALT3	PWM0
SD2_CLK	C21	ALT0	SD2_CLK
SD2_CMD	F19	ALT0	SD2_CMD
SD2_DAT0	A22	ALT0	SD2_DAT0
SD2_DAT1	E20	ALT0	SD2_DAT1
SD2_DAT2	A23	ALT0	SD2_DAT2
SD2_DAT3	B22	ALT0	SD2_DAT3
SD3_CLK	D14	ALT0	SD3_CLK
SD3_CMD	B13	ALT0	SD3_CMD
SD3_DAT0	E14	ALT0	SD3_DAT0
SD3_DAT1	F14	ALT0	SD3_DAT1
SD3_DAT2	A15	ALT0	SD3_DAT2
SD3_DAT3	B15	ALT0	SD3_DAT3
SD3_DAT4	D13	ALT0	SD3_DAT4
SD3_DAT5	C13	ALT0	SD3_DAT5
SD3_DAT6	E13	ALT0	SD3_DAT6
SD3_DAT7	F13	ALT0	SD3_DAT7
SD4_CLK	E16	ALT0	SD4_CLK
SD4_CMD	B17	ALT0	SD4_CMD
SD4_DAT0	D18	ALT1	SD4_DAT0
SD4_DAT1	B19	ALT1	SD4_DAT1
SD4_DAT2	F17	ALT1	SD4_DAT2
SD4_DAT3	A20	ALT1	SD4_DAT3
SD4_DAT4	E18	ALT1	SD4_DAT4
SD4_DAT5	C19	ALT1	SD4_DAT5
SD4_DAT6	B20	ALT1	SD4_DAT6
SD4_DAT7	D19	ALT1	SD4_DAT7

Reserved For i.MX6DLS

NANDF_WP_B	E15	ALT5	DISP0_WR
EIM_RW	K20	ALT8	EPDC_SDDO7
EIM_LBA	K22	ALT8	EPDC_SDDO4
EIM_CS0	H24	ALT8	EPDC_SDDO6
EIM_EB1	K23	ALT8	EPDC_SDSHR
EIM_EB2	E22	ALT8	EPDC_SDDO5
EIM_A16	H25	ALT8	EPDC_SDDO0
EIM_A18	J22	ALT8	EPDC_PWRCTRL0
EIM_A21	H23	ALT8	EPDC_GDCLK
EIM_A22	F24	ALT8	EPDC_GDSP
EIM_A23	J21	ALT8	EPCD_GDOE
EIM_A24	F25	ALT8	EPDC_GDRL
EIM_D17	F21	ALT8	EPDC_VCOM0
EIM_D27	E25	ALT8	EPDC_SDOE
EIM_D31	H21	ALT8	EPDC_SDCLK
EIM_DA1	J25	ALT8	EPDC_SDLE
EIM_DA2	L21	ALT8	EPDC_BDR0
EIM_DA3	K24	ALT8	EPDC_BDR1
EIM_DA4	L22	ALT8	EPDC_SDCE0
EIM_DA5	L23	ALT8	EPDC_SDCE1
EIM_DA6	K25	ALT9	EPDC_SDCE2
EIM_DA10	M22	ALT8	EPDC_SDDO1
EIM_DA11	M20	ALT8	EPDC_SDDO3
EIM_DA12	M24	ALT8	EPDC_SDDO2

Ball Name	Ball Number	IO MUX	Use	GPIO Function	Direction	Active
SD1_CMD	B21	ALT5	GPIO1[18]	ACCL_INT_IN	Input	High
EIM_DA9	M21	ALT5	GPIO3[9]	ALS_INT	Input	High
NANDF_WP_B	E15	ALT5	GPIO6[9]	DISP0_WR	Output	High
NANDF_RB0	B16	ALT5	GPIO6[10]	AUX_5V_EN	Output	High
EIM_DA15	N24	ALT5	GPIO3[15]	BARO_INT	Input	High
NANDF_CS2	A17	ALT5	GPIO6[15]	CABC_EN0	Output	High
NANDF_CS3	D16	ALT5	GPIO6[16]	CABC_EN1	Output	High
GPIO_19	P5	ALT5	GPIO4[5]	CAN1_STBY	Output	High
NANDF_ALE	A16	ALT5	GPIO6[8]	CAP_TCH_INT0	Input	High
NANDF_CLE	C15	ALT5	GPIO6[7]	CAP_TCH_INT1	Input	High
EIM_A25	H19	ALT5	GPIO5[2]	CHG_FLT1_B	Input	Low
EIM_DA14	N23	ALT5	GPIO3[14]	CHG_FLT2_B	Input	Low
EIM_D23	D25	ALT5	GPIO3[23]	CHG_STATUS1_B	Input	Low
EIM_DA13	M23	ALT5	GPIO3[13]	CHG_STATUS2_B	Input	Low
KEY_COL2	W6	ALT5	GPIO4[10]	CODEC_PWR_EN	Output	High
EIM_D16	C25	ALT5	GPIO3[16]	COMP_INT	Input	High
SD1_DAT2	E19	ALT5	GPIO1[19]	CSI_PWN	Output	High
SD1_CLK	D20	ALT5	GPIO1[20]	CSI_RST_B	Output	High
SD1_DAT0	A21	ALT5	GPIO1[16]	CSI0_PWN	Output	High
SD1_DAT1	C20	ALT5	GPIO1[17]	CSI0_RST_B	Output	High
EIM_WAIT	M25	ALT5	GPIO5[0]	DI0_DO_CS	Output	High
EIM_BCLK	N22	ALT5	GPIO6[31]	DI0_D1_CS	Output	High
NANDF_CS1	C16	ALT5	GPIO6[14]	DISP0_PWR_EN	Output	High
EIM_D28	G23	ALT5	GPIO3[28]	DISP0_RD	Output	High
EIM_DA8	L24	ALT5	GPIO3[8]	DISP0_RST_B	Output	Low
NANDF_CS0	F15	ALT5	GPIO6[11]	DISP0_RST_B	Output	Low
EIM_CS1	J23	ALT5	GPIO2[24]	DOK_B	Input	Low
EIM_A17	G24	ALT5	GPIO2[21]	E_PMIC_GOOD_B	Input	Low
EIM_D20	G20	ALT5	GPIO3[20]	EPDC_PMIC_WAKEUP	Output	High
EIM_A19	G25	ALT5	GPIO2[19]	EPDC_PWRCTRL1	Output	High
EIM_A20	H22	ALT5	GPIO2[18]	EPDC_PWRCTRL2	Output	High
EIM_OE	J24	ALT5	GPIO2[25]	EPDC_PWRIRQ	Input	High
ENET_TX_EN	V21	ALT5	GPIO1[28]	ETH_WOL_INT	Input	High
EIM_D18	D24	ALT5	GPIO3[18]	GPS_PPS	Input	High
EIM_DA0	L20	ALT5	GPIO3[0]	GPS_PWREN	Output	High
EIM_EB0	K21	ALT5	GPIO2[28]	GPS_RESET_B	Output	Low
SD3_RST	D15	ALT5	GPIO7[8]	HEADPHONE_DET	Input	Low
GPIO_5	R4	ALT5	GPIO1[5]	KEY_VOL_DN	Input	Low
GPIO_4	R6	ALT5	GPIO1[4]	KEY_VOL_UP	Input	Low
KEY_COL4	T6	ALT5	GPIO4[14]	PCIE_DIS_B	Output	Low
GPIO_17	R1	ALT5	GPIO7[12]	PCIE_RST_B	Output	Low
EIM_D19	G21	ALT5	GPIO3[19]	PCIE_PWR_EN	Output	High
GPIO_18	P6	ALT5	GPIO7[13]	PMIC_INT_B	Input	Low
EIM_D29	J19	ALT5	GPIO3[29]	PWR_BTN_SNS	Input	High
ENET_CRS_DV	U21	ALT5	GPIO1[25]	RGMII_NRST	Output	High
NANDF_D2	F16	ALT5	GPIO2[2]	SD2_CD_B	Input	Low
NANDF_D3	D17	ALT5	GPIO2[3]	SD2_WP	Input	High
NANDF_D0	A18	ALT5	GPIO2[0]	SD3_CD_B	Input	Low
NANDF_D1	C17	ALT5	GPIO2[1]	SD3_WP	Input	High
EIM_EB3	F23	ALT5	GPIO2[31]	SENSOR_PWR_EN	Output	High
EIM_DA7	L25	ALT5	GPIO3[7]	KP_LOCK	Input	High
EIM_D26	E24	ALT5	GPIO3[26]	TS_INT	Input	High
ENET_RXD0	W21	ALT5	GPIO1[27]	UOK_B	Input	Low
ENET_RXD1	W22	ALT5	GPIO1[26]	RGMII_INT	Input	High
ENET_TXD0	U20	ALT5	GPIO1[30]	DISP0_WR	Output	High
ENET_TXD1	W20	ALT5	GPIO1[29]	USB_H1_PWR_EN	Output	High
GPIO_2	T1	ALT5	GPIO1[2]	USR_DEF_RED_LED	Output	High
GPIO_9	T2	ALT6	GPIO1[9]	MICROPHONE_DET	Input	Low
KEY_ROW4	V5	ALT5	GPIO4[15]	SATA_DEVSLP	Output	High
CSI0_DATA_EN	P3	ALT5	GPIO5[20]	PCIE_WAKE_B	Input	Low

I2C1 Bus (1.8V)

Peripheral	Bus Activity Level	Speed (kbps)	Addresses (hex)	Default Address (hex)
CSI Bus Camera	Low	400	Write: 0x78	Write: 0x78
Auido CODEC	Low	400	0x34, 0x36	0x34
MMA 8451Q Accelerometer	Low	400	0x3A, 0x39	0x39

I2C1_SDA = CSI0_DAT8
I2C1_SCL = CSI0_DAT9

I2C2 Bus (3.3V)

Peripheral	Bus Activity Level	Speed (kbps)	Addresses (hex)	Default Address (hex)
PF0100 PMIC	Low	400	0x08 - 0x0F	0x08
MIPI Bus Camera	Low	400	0x3C	0x3C
MIPI Bus Display	TBD	TBD	TBD	TBD
HDMI EDID	Low	100	0x50	0x50
LVDS0 EDID	Low	100	0x50	0x50
LVDS0 TOUCH SCREEN	High	400	0x82	0x82
RGB TFT LCD DISPLAY	TBD	TBD	TBD	TBD
LCD TOUCH SCREEN	Low	400	0x68, 0x69, 0x6A, 0x6B	0x68

I2C2_SDA = KEY_ROW3
I2C2_SCL = KEY_COL3

I2C3 Bus (3.3V)

Peripheral	Bus Activity Level	Speed (kbps)	Addresses (hex)	Default Address (hex)
LVDS1 EDID	Low	100	0x50	0x50
LVDS1 TOUCH SCREEN	High	400	0x82	0x82
PCIe EXP PORT	TBD	TBD	TBD	TBD
EPDC DISPLAY CARD	Low	400	0x68, 0x69, 0x6A, 0x6B	0x68
AMBIENT LIGHT SENSOR	Low	400	0x44	0x44
DIGITAL eCOMPASS	Low	400	0x0E	0x0E
BAROMETER	Low	400	0x60	0x60

I2C3_SDA = GPIO_16
I2C3_SCL = GPIO_3

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

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HISTORY OF TEMPORARY DEVIATIONS

TDA 4100

1. Digital microphone ANALOG DEVICES ADMP421 was used in place of WOLFSON WM7230 due to supply shortage. Affects U500 and U520.

TDA 4112

Replaced TDA 4100
1. Digital microphone ANALOG DEVICES ADMP421 was used in place of WOLFSON WM7230 due to supply shortage. Affects U500 and U520.
2. Q512 was depopulated due to schematic mistake. Removes battery charge from USB option.
3. Depopulate R30 on MCIMX6DL-SD boards only. i.MX6DL Processor configured for Smart PMIC mode. Not compatible with board design. Removes SW ability to shutdown the board.

TDA 4136

1. Solder a 0402 2.2M Ohm resistor across pins of C55. Some i.MX6Q Processors require this resistor to stabalize the 24MHz crystal circuit, in order to start up within the required time interval.

TDA 4221 (6DL) / TDA 4222 (6Q)

1. Schematic revision B3 changed DDR3 memory to MT41K128M16JT-125:K. Due to unavailability of new part, this TDA autorizes the continued use of MT41J128M16HA-15.
2. Change C540 to 1.0uF capacitor.
3. Change resistors R183 and R189 to 2.37K Ohm resistors.

TDA 4275

1. Remove buffers U500 and U520 from digital Microphone data signal. Replace with hand wire mod.
2. Add WDOG_B reset capability (UX1, RX2, CX1).
3. Add diode DX1 to EIM_D19 to allow GPIO sense of power button press.
4.Change RESET button press to connect to PMIC PWRON pin. RESET press now causes global reset.
5. Add 10K pull down resistor RX3 to SDCKE0 pin.
6. Depopulate Resistors R174 and R176 to disconnect LVDS0 EDID from I2C2 communications channel.
7. Populate Battery Conector Header CON3.
8. Populate SIM Card Connector CON1.
9. Remove U1 from BOM (in preparation for next revision MX 6 silicon).
10. On MCIMX6DL-SDP boards, populate resistor R30 with 1K Ohm resistor.

TDA 4425

1. Depopulate ferrite beads L10 and L17.
2. Populate ferrite beads L25 and L26
   (wih Murata BLM18PG121SH1).

TDA 4502

1. Change R17, R21, R25, R27, R68, R85, R582, and R660 to 0.5% resistors due to parts availability.

CHANGE REVISION DEFECT TRACKING

REV:	Change:	Reference Defect Number:
B4	Removed buffers U500 and U520 from digital microphone data outputs.	ENGR00181056 ENGR00211969
B4	The Battery Charge Done LED is disconnected and R522 is depopulated. New parts RX2, CX1 and UX1 are added. Traces show required hand modifications.	ENGR00211943
B4	Optional Power On Circuit has been disabled and U511 and R578 are now DNP. A new Diode DX1 has been added to allow EIM_D29 to sense a button	ENGR00181039 ENGR00211948
B4	RESET button SW2 now connects to The PWRON pin of The PMIC.	ENGR00211979
B4	Added 10K pull down resistor RX3 to SDCKE0 trace.	ENGR00211962
B4	SIM Card Connector CON1 is now populated by default.	ENGR00224087
B4	Battery Connector Header CON3 is now populated by default.	ENGR00224089
B4	Changed resistors R174 and R176 and to depopulated by default. LVDS0 EDID will not be connected to I2C2 channel unless needed.	ENGR00211965
B4	Replaced digital microphones with Analog Devices ADMP421.	ENGR00211964
B4	Disabled USR_DEF_GRN_LED circuit. Configured GPIO_1 for WDOG_B output.	ENGR00211973
C	Q512 is Changed to populated.	ENGR00211943
C	Optional Start Up Circuit has been modified.	ENGR00181039
C	PMIC Programming Micro-Processor is removed.	ENGR00224090
C	Add DNP Input to U13 buffer for USB_OTG_PWR_EN. Buffer now powered from GEN_3V3.	ENGR00319341
C	FA_ANA and VDD_FA signals now connected to ground.	ENGR00213511
C	Added resistor options to EIM_DA7 trace to EPD connector.	ENGR00181054 ENGR00211953
C	Connected EIM_DA9 to EPDC Connector J508 to supply SDCE5 if needed.	ENGR00213510
C	Optional LDO U9 is now depopulated.	ENGR00224091
C	Added Connector J13 to support BT from SDIO Card. Connector is isolated by DNP resistors on Rev C boards.	ENGR00181035 ENGR00211946
C	Added GPIO control of Battery Charge Enable pins.	ENGR00217643
C	Changed C594 to 0.22uF, changed C31 to 47uF, added C555 as second 22uF capacitor in parallel with C546, changed C561, C562, C586 and C596 to 0.47uF. Changes made per recommendation of MMPF0100NPEP team.	ENGR00224093
C	Added additional 47uF bulk capacitor C769 to SD2 socket VDD supply.	ENGR00224094
C	Added option to route HDMI DDC comms seperate from I2C2 comms channel.	ENGR00215026
C	C597 populated to provide de-bounce to RESET circuit.	ENGR00224095
C	Depopulated C68, C612. Populated C682, C716 closer to pins.	ENGR00224096
C	Depopulated C39, C606, C607, C608, C609, C610, C673 and C681.	ENGR00224097
C	Added DNP R302 to provide alternate 5V supply path to USB_H1_VBUS.	ENGR00224098
C	Added DNP R632 to provide alternate gating of PMIC_5V source (tied to VDDSOC).	ENGR00224098
C	Added DNP L25 and L26 to provide alternate 2.8V supply path to camera modules.	ENGR00224099
C	Added TP31, TP32, TP509, and TP510 to bring out third data lane for both LVDS0 and LVDS1.	ENGR00214325 ENGR00214502
C	Change blocking capacitors C6 and C7 to Zero Ohm resistors R307 and R308. PCIe specification requires blocking capacitors to be on transmit side of	ENGR00226040
C2	Depopulate L10 and L17. Move Ferrite beads to L25 and L26	ENGR00231769
C3	Changed R97 and R106 pull up resistors to 4.7K to reduce current on VSNVS	ENGR00237171
C3	Changed R19 to 10K pull up resistor to prevent WDOG reset during POR.	ENGR00234394
C3	Added note to BlueTooth connector that RXD and TXD traces are crossed.	ENGR00239363

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