Rev. 0, 11/2015

FreeRTOS™ BSP v.1.0.0 for i.MX 6SoloX Release Notes

1 Overview

These are the release notes for the FreeRTOSTM BSP 1.0.0 for the i.MX 6SoloX ARM[®] Cortex[®]-M4 core. The core of the BSP is a set of peripheral drivers.

The peripheral driver wraps the hardware register accesses into a set of stateless functional primitives that provide the building blocks for high-level applications.

The FreeRTOS BSP includes a set of example applications demonstrating the use of the peripheral drivers and some demonstrations of integrated FreeRTOS operating system (OS) v8.0.0. The FreeRTOS BSP also integrates RPMsg middleware to provide an easy-to-use multi-core communication API for i.MX product families.

Contents

1	Overview	1
2	What Is New	2
3	Development Tools	3
	Supported Development Systems	
	Release Contents	
6	FreeRTOS BSP Release Overview	6
6.	1 i.MX 6SoloX Cortex-M4 platform support	6
6.	2 Demo applications	7
6.	3 Driver examples	7
	4 Other integrated software solutions	
	Known Issues	
8	Revision History	10



2 What Is New

These are the new features for FreeRTOS BSP 1.0.0 i.MX 6SoloX:

- Added Peripheral support:
 - o i.MX 6SoloX ADC
 - o i.MX 6SoloX CCM
 - o i.MX GPIO
 - o i.MX I2C
 - o i.MX MU
 - o i.MX UART
 - o i.MX WDOG
 - o ECSPI
 - o EPIT
 - o FlexCAN
 - o Local Memory Controller (LMEM) of Cortex-M4 Core
 - o Resource Domain Control (RDC)
 - o SEMA4
- Added Multi-core communication support:
 - o RPMsg

3 Development Tools

The FreeRTOS BSP 1.0.0 was compiled and tested with these development tools:

- IAR Embedded Workbench for ARM® version 7.40.3
- Makefiles support with GCC revision 4.9-2015-q1-update from ARM Embedded
- ARM Development Studio 5 (DS-5TM) version 5.20.1 (32 bit)
- Lauterbach TRACE32 PowerView for ARM version R.2014.09.000058270

4 Supported Development Systems

This release was tested with boards and devices listed in this table.

Table 2 Supported MCU devices and development boards

Development boards	i.MX devices
i.MX 6SoloX SABRE-SD board MCIMX6SX-SDB (Rev.A)	PCIMX6X4AVM08AA
i.MX 6SoloX SABRE-Al Automotive Infotainment board MCIMX6SXAICPU2(Rev.A)	PCIMX6X4AVM08AB
Extension board MCIMXABASEV1 Rev. E for peripherals	

5 Release Contents

This table describes the release contents.

Table 3 Release contents

Deliverable	Location
Examples	<install_dir>/examples/</install_dir>
Demo applications	<install_dir>/examples/<board_name>/demo_apps/</board_name></install_dir>
Driver examples	<install_dir>/examples/<board_name>/driver_examples/</board_name></install_dir>
Documentation	<install_dir>/doc/</install_dir>
Middleware	<install_dir>/middleware/</install_dir>
RPMsg stacks	<install_dir>/middleware/multicore/open-amp/</install_dir>
Driver library, startup code and utilities	<install_dir>/platform/</install_dir>
Cortex Microcontroller Software Interface Standard (CMSIS) ARM Cortex®-M header files, DSP library source	<install_dir>/platform/CMSIS/</install_dir>
Linker control files for each supported tool chain	<install_dir>/platform/devices/<device_name>/linker/</device_name></install_dir>
SoC header files	<install_dir>/platform/devices/<device_name>/include</device_name></install_dir>
CMSIS-compliant startup code	<install_dir>/platform/ devices/<device_name>/startup/</device_name></install_dir>
Peripheral Drivers	<install_dir>/platform/drivers/</install_dir>
Utilities such as debug console	<install_dir>/platform/utilities/</install_dir>
RTOS Kernel folder	<install_dir>/rtos/</install_dir>
FreeRTOS Kernel Code	<install_dir>/rtos/FreeRTOS/</install_dir>
External tools for build and debug	<install_dir>/tools/</install_dir>

6 FreeRTOS BSP Release Overview

The FreeRTOS BSP is intended for use with Freescale's i.MX product family on the ARM Cortex-M4 core. The release consists of:

- i.MX 6SoloX ARM Cortex-M4 platform support (ARM Cortex-A9 is not supported)
- Demo applications/Driver examples
- Multi-core communication stack (RPMsg)
- FreeRTOS kernel v8.0.0
- Documentation (FreeRTOS BSP i.MX 6SoloX API Reference Manual and various user's guides)

6.1 i.MX 6SoloX Cortex-M4 platform support

The FreeRTOS BSP platform directory contains the startup code, driver libraries for peripherals, header files, linker files, and utilities such as the debug console implementation.

6.1.1 Startup code

The FreeRTOS BSP includes simple CMSIS-compliant startup code for i.MX 6SoloX which efficiently delivers the code execution to the main() function. An application can include the startup code directly in the project build environment for a cleaner project build environment.

6.1.2 Driver library

The FreeRTOS BSP provides a set of drivers for the i.MX family on-chip peripherals. The drivers are designed and implemented around the peripheral hardware blocks rather than for a specific i.MX device, and work with or without FreeRTOS OS.

The drivers are designed to wrap hardware register accesses into functional accesses. They are stateless and are intended to cover the most frequently used hardware functionality. They are written in C language, which increases the reuse of code for other products as they are designed to be initialized at runtime based on the custom configuration depending on the product. For more details, see chapter "Architectural Overview" in the *FreeRTOS BSP i.MX 6SoloX API Reference Manual* (FRTOS6XAPIRM).

6.1.3 Header files

The FreeRTOS BSP devices directory contains device-specific header files that provide direct access to the i.MX peripheral registers. Each supported i.MX device in the FreeRTOS BSP has an overall System-on-Chip (SoC) memory-mapped header file. Along with the SoC header files, the FreeRTOS BSP CMSIS directory includes common CMSIS header files for the ARM Cortex-M core and DSP library from the ARM CMSIS version 4.2 release.

6.1.4 Linker files

The FreeRTOS BSP devices directory contains linker control files (or simply linker files) for each supported tool chain and i.MX device.

6.1.5 Utilities

The utilities directory contains useful software utilities such as a debug console.

6.1.6 RDC settings

i.MX 6SoloX is a multi-core device and Resource Domain Control (RDC) could be used to grant peripheral and/or memory access permissions to each core.

The examples and demo applications in the FreeRTOS BSP make use of RDC to allocate peripheral access permission. When running the ARM Cortex-A9 application with FreeRTOS BSP example/demo, it is important to respect the reserved peripheral. FreeRTOS BSP application has reserved peripherals that are used only by ARM Cortex-M4, and any access from ARM Cortex-A9 on those peripherals may cause the program to hang.

The default RDC setting is:

- ARM Cortex-M4 core is assigned to RDC domain 1, and ARM Cortex-A9 and other bus masters use the default assignment (RDC domain 0)
- Every example/demo has its specific RDC setting in its hardware_init.c. Most of them are set to exclusive access.

The user of this package can remove or change the RDC settings in the example/demo or in his application.

6.2 Demo applications

The demo applications demonstrate the usage of the drivers to create integrated software solutions on i.MX 6SoloX.

6.3 Driver examples

The driver examples demonstrate the usage of drivers on bare metal environment.

6.4 Other integrated software solutions

The FreeRTOS BSP is designed for easy integration with other software solutions such as FreeRTOS OS and RPMsg multi-core communication.

6.4.1 RTOS

The FreeRTOS BSP is pre-integrated and tested with the FreeRTOS OS (<u>www.freertos.org</u>) v8.0.0.

As the drivers have no dependency on FreeRTOS OS, it's easy to upgrade FreeRTOS OS. Just download new version of FreeRTOS OS and replace the rtos/FreeRTOS folder.

6.4.2 RPMSG

A multi-core communication stack RPMsg is integrated with FreeRTOS BSP and can be used to communicate with the i.MX ARM Cortex-A9 core. The stack is from the github project OpenAMP (github.com/OpenAMP/open-amp) and has been ported on i.MX 6SoloX with some API extension. The stack can be running in bare metal program and in FreeRTOS application. Besides the RPMsg API, no other feature from OpenAMP is included in this release. For more information, see the OpenAMP manuals under <install_dir>/middleware/multicore/open-amp/docs.

7 Known Issues

Table 4 Known issues

Issue	Workaround
The u-boot on Cortex-A9 cannot load Cortex-M4 image from SD Card to M4's Tightly Coupled Memory (TCM) directly. This is a hardware limitation.	Load M4 image from SD Card to OCRAM or DDR first and then copy image from OCRAM or DDR to M4's TCM.

8 Revision History

This table summarizes revisions to this document.

Revision number	Date	Substantial changes
0	11/2015	Initial release.

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