戻る

Although the address of register is same but different from the internal structure.
(There is a description in several places in the manual, but different content)

アドレス	レジスタ名	Width	Access	記載箇所(リファレンスマニュアル内)
20E_C004	**Channel Interrupts (SDMAARM_INTR)**	32	w1c	55.8 ARM Platform Memory Map and Control Register Definitions
	Channel Interrupts (SDMABP_INTR)	32	w1c	55.9 BP Memory Map and Control Register Definitions
	Highest Pending Channel Register (SDMACORE_NCR)	32	R	55.10 SDMA Internal (Core) Memory Map and Internal Register Definitions
20E_C00C	**Channel Start (SDMAARM_HSTART)**	32	R/W	55.8 ARM Platform Memory Map and Control Register Definitions
	Channel Start (SDMABP_DSTART)	32	R	55.9 BP Memory Map and Control Register Definitions
	OnCE Event Cell Address Register B (SDMACORE_EAB)	32	R/W	55.10 SDMA Internal (Core) Memory Map and Internal Register Definitions
20E_C018	**Channel ARM platform Override (SDMAARM_HOSTOVR)**	32	R/W	55.8 ARM Platform Memory Map and Control Register Definitions
	OnCE Real-Time Buffer (SDMACORE_RTB)	32	R/W	55.10 SDMA Internal (Core) Memory Map and Internal Register Definitions
20E_C01C	**Channel Event Pending (SDMAARM_EVTPEND)**	32	w1c	55.8 ARM Platform Memory Map and Control Register Definitions
	Channel 0 Boot Address (SDMACORE_MCHN0ADDR)	32	R	55.10 SDMA Internal (Core) Memory Map and Internal Register Definitions
261_80BC	**DP Common Configuration Async 1 Flow Register (IPU_DP_COM_CONF_ASYNC1)**	32	R/W	38.5 IPU Memory Map/Register Definition
	DP Debug Control Register (IPU_DP_DEBUG_CNT)	32	R/W	38.5 IPU Memory Map/Register Definition
261_80C0	**DP Graphic Window Control Async 1 Flow Register (IPU_DP_GRAPH_WIND_CTRL_ASYNC1)**	32	R/W	38.5 IPU Memory Map/Register Definition
	DP Debug Status Register (IPU_DP_DEBUG_STAT)	32	R	38.5 IPU Memory Map/Register Definition

Example) register of address 0x20EC004

55.8.2 Channel Interrupts (SDMAARM_INTR)

Address: 20E_C000h base + 4h offset = 20E_C004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	HI[31:0]																															
W	w1c																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDMAARM_INTR field descriptions

Field	Description
HI[31:0]	The ARM platform Interrupts register contains the 32 HI[i] bits. If any bit is set, it will cause an interrupt to the ARM platform. This register is a "write-ones" register to the ARM platform. When the ARM platform sets a bit in this register the corresponding HI[i] bit is cleared. The interrupt service routine should clear individual channel bits when their interrupts are serviced, failure to do so will cause continuous interrupts. The SDMA is responsible for setting the HI[i] bit corresponding to the current channel when the corresponding `done` instruction is executed.

Channel Interrupts (SDMABP_INTR)

55.9.2 Channel Interrupts (SDMABP_INTR)

Address: 20E_C000h base + 4h offset = 20E_C004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DI																															
W	w1c																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDMABP_INTR field descriptions

Field	Description
DI	The BP Interrupts register contains the 32 DI[i] bits. If any bit is set, it will cause an interrupt to the BP. • This register is a "write-ones" register to the BP. When the BP sets a bit in this register, the corresponding DI[i] bit is cleared. • The interrupt service routine should clear individual channel bits when their interrupts are serviced; failure to do so will cause continuous interrupts. • The SDMA is responsible for setting the DI[i] bit corresponding to the current channel when the corresponding `done` instruction is executed.

Highest Pending Channel Register (SDMACORE_NCR)

55.10.4 Highest Pending Channel Register (SDMACORE_NCR)

Address: 20E_C000h base + 4h offset = 20E_C004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																											NCR				
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDMACORE_NCR field descriptions

Field	Description
31–5 Reserved	This read-only field is reserved and always has the value 0.
NCR	Contains the number of the pending channel that the scheduler has selected to run next.