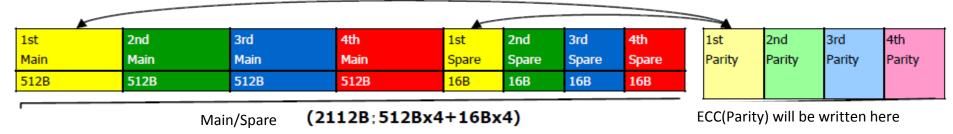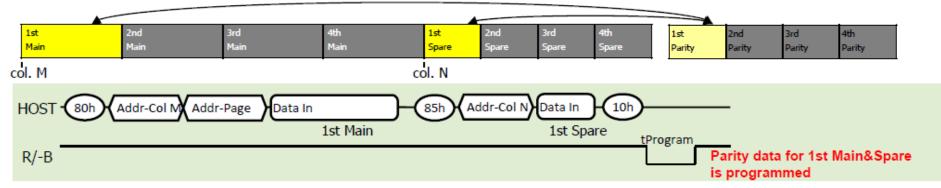# Do not "Partial page programing"

- ECC data will be created for 16B spare area and 512B Main area, in 24nm BENAND.

- As for the combination of Main and Spare, please see the below 'Page assignment'

24nm BENAND Page Assignment

1st Main	2nd Main	3rd Main	4th Main	1st Spare	2nd Spare	3rd Spare	4th Spare		1st Parity	2nd Parity	3rd Parity	4th Parity
512B	512B	512B	512B	16B	16B	16B	16B					

Main/Spare **(2112B : 512Bx4+16Bx4)**   ECC(Parity) will be written here

- Because an ECC data will be created for Main/Spare area, Main/Spare data should be written at a time.

1st Data (Main & Spare) is programmed by using Column Address Change mode: OK

1st Main	2nd Main	3rd Main	4th Main	1st Spare	2nd Spare	3rd Spare	4th Spare		1st Parity	2nd Parity	3rd Parity	4th Parity

col. M   col. N

HOST — (80h) — (Addr-Col M) — (Addr-Page) — (Data In) — (85h) — (Addr-Col N) — (Data In) — (10h)

1st Main   1st Spare

R/-B   tProgram

Parity data for 1st Main&Spare is programmed

- For the below sequence, partial page programming, causes uncorrectable-error.

- Case-1) Writing Main, then writing Spare.
  - The error occurs even if user writes additionally to Spare after writing user data.

- Case-2) Writing Spare, then writing Main.
  - The error occurs even if one writes user data after writing Spare after Erase.