

TM CARRIER BOARD Sechamtic v3.0

Bpmmaster Design Confidential

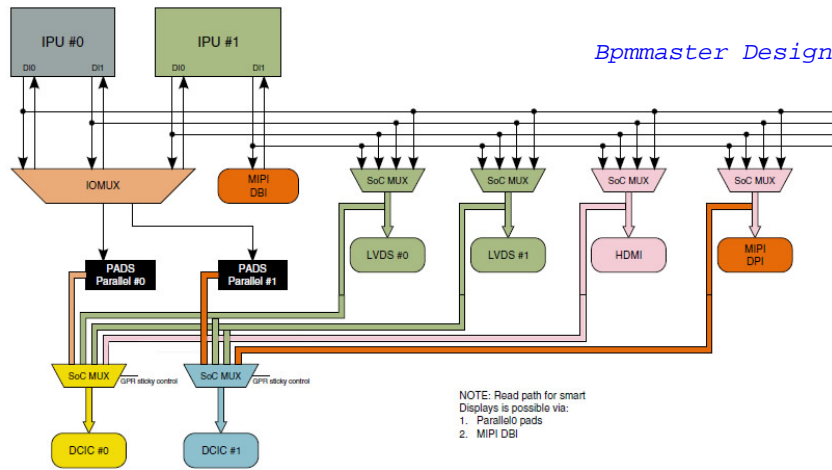


Figure 9-2. Display port muxing scheme

MX 6x Framebuffer and Display Device Software Architecture

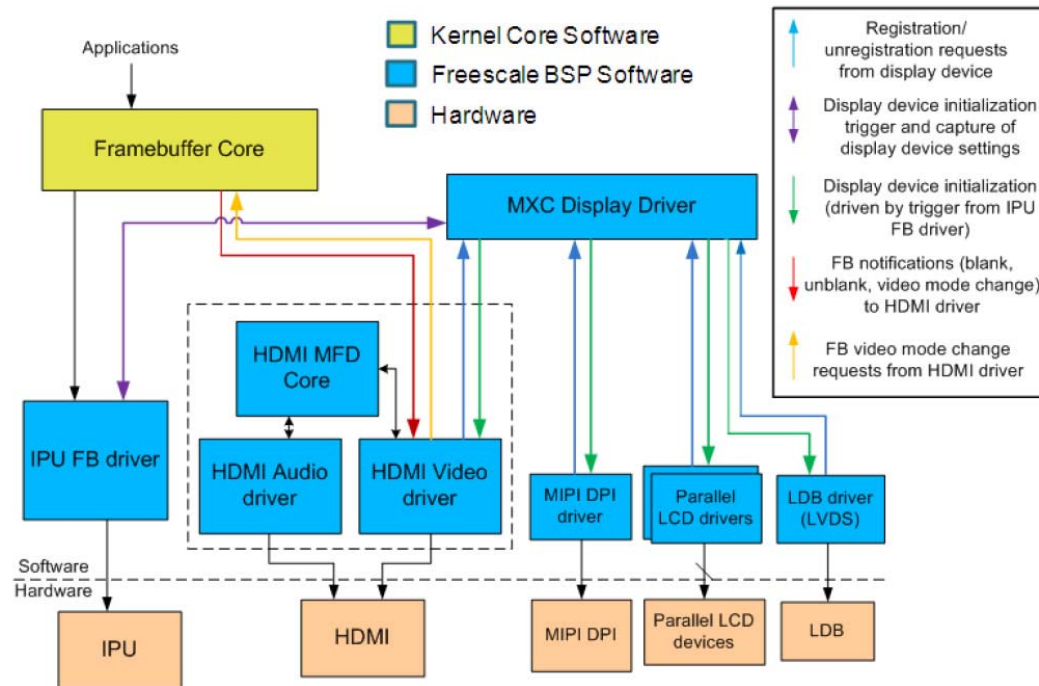
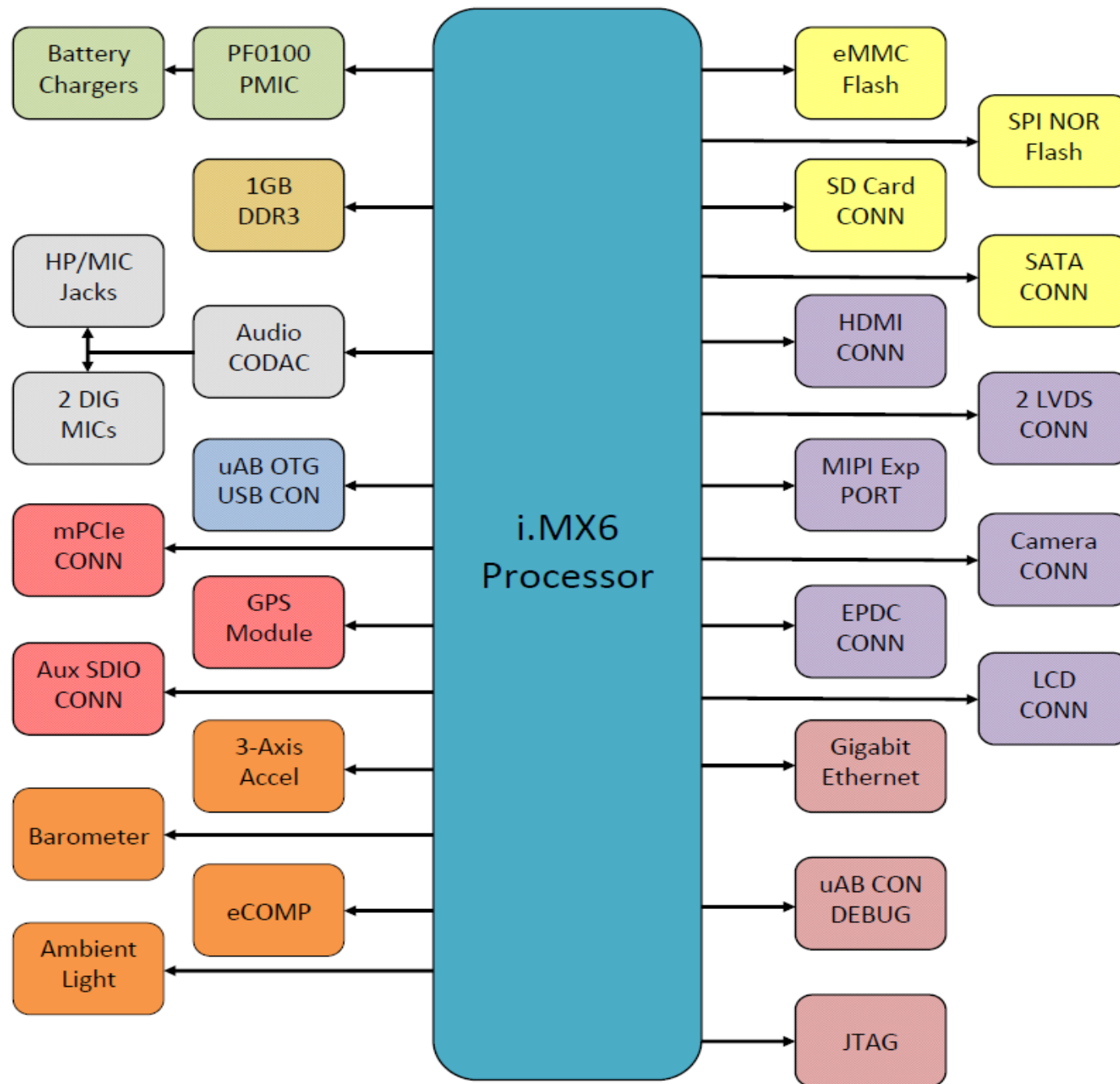


Figure 11-3. HDMI Video SW Architecture

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Smart Device System Block Diagram

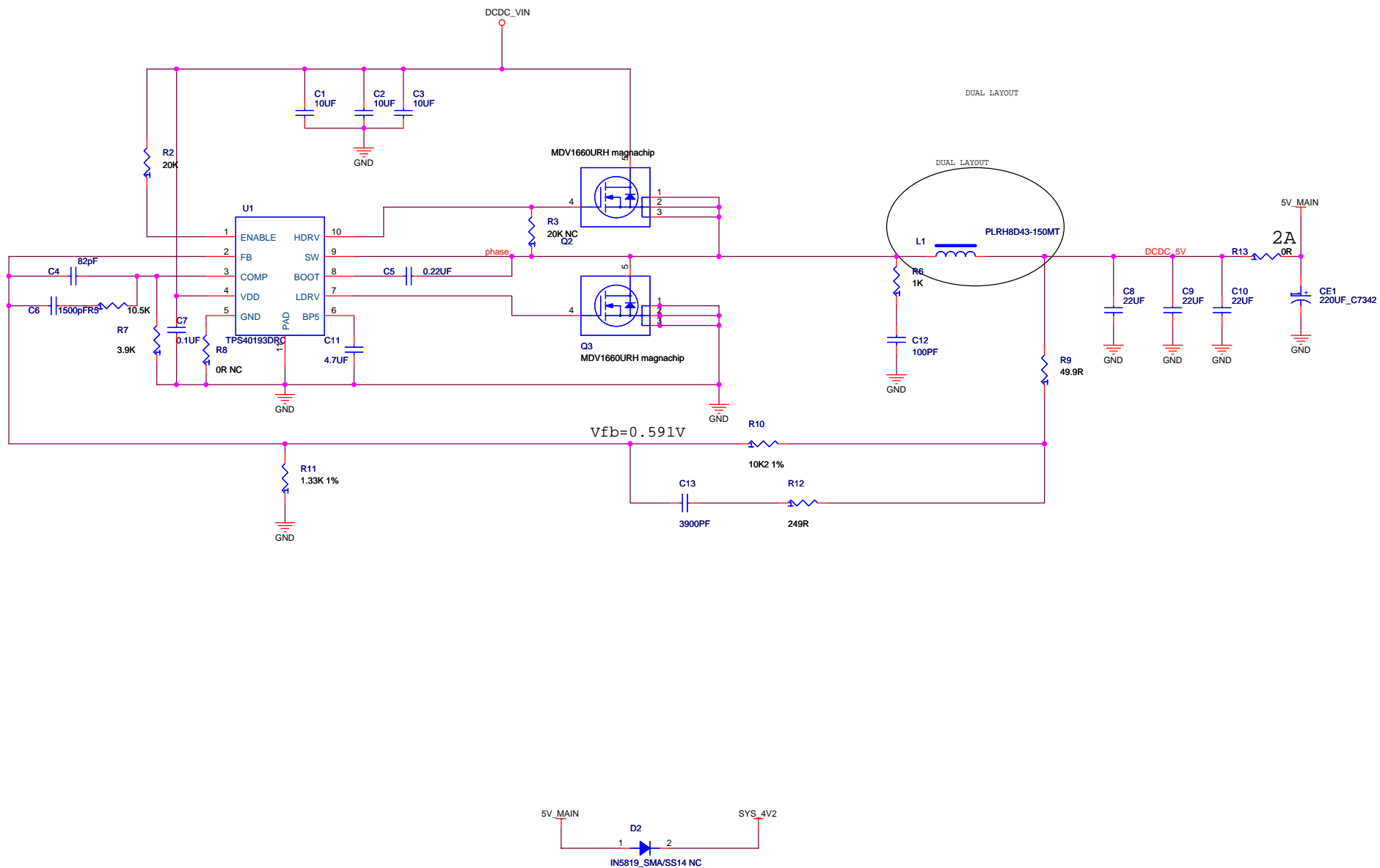


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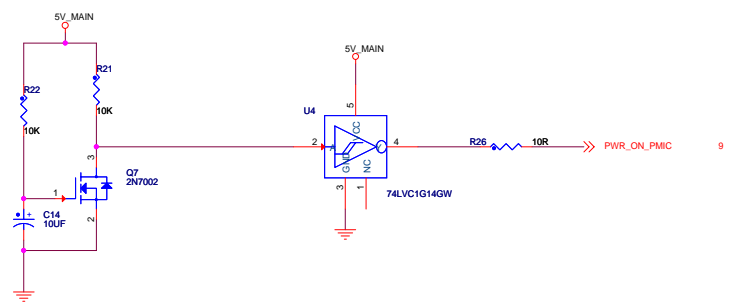
DATE	VER.	COMMENT
2013-05	V1.0	INITIAL VER.
2013-10-10	V2.0	1. LVDS 背光 电压、LVDS 电压 改为独立控制， 电压改为 12V, 或 24V 2. LINE OUT 增加 12V 输出， 支持 大功率功放 3. USB 差分阻抗 调整为 90欧 4. 增加 sd 卡支持 5. 增加 CAN 总线支持 6. 增加 miniPCIE 支持 3G , WIFI, SSD 等 SC6Q888YM10AC Difference: <ul style="list-style-type: none"> - SATA - PCIE - DSI

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静态 无电流输出时 有18-6 =1.2mA

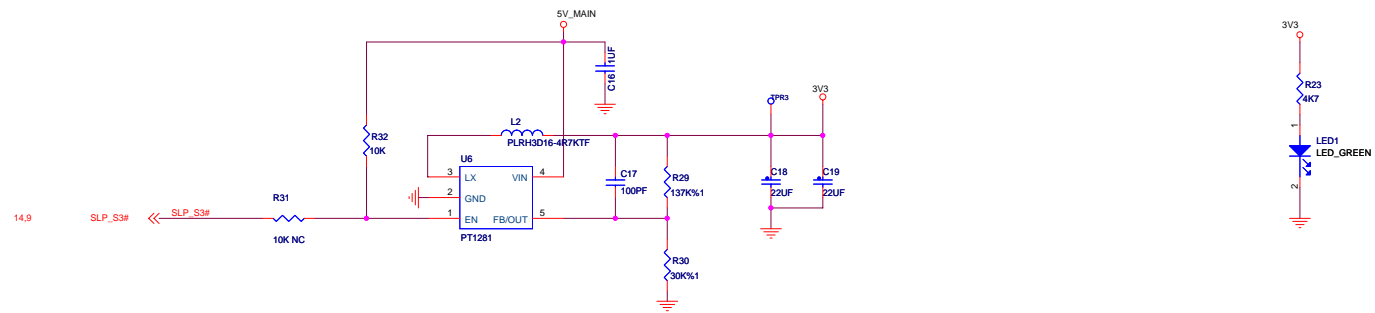


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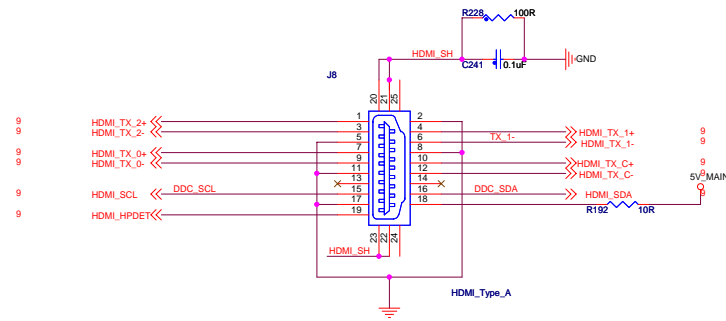
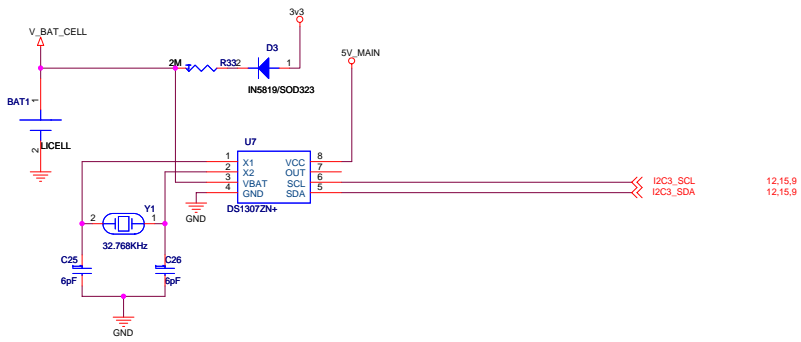


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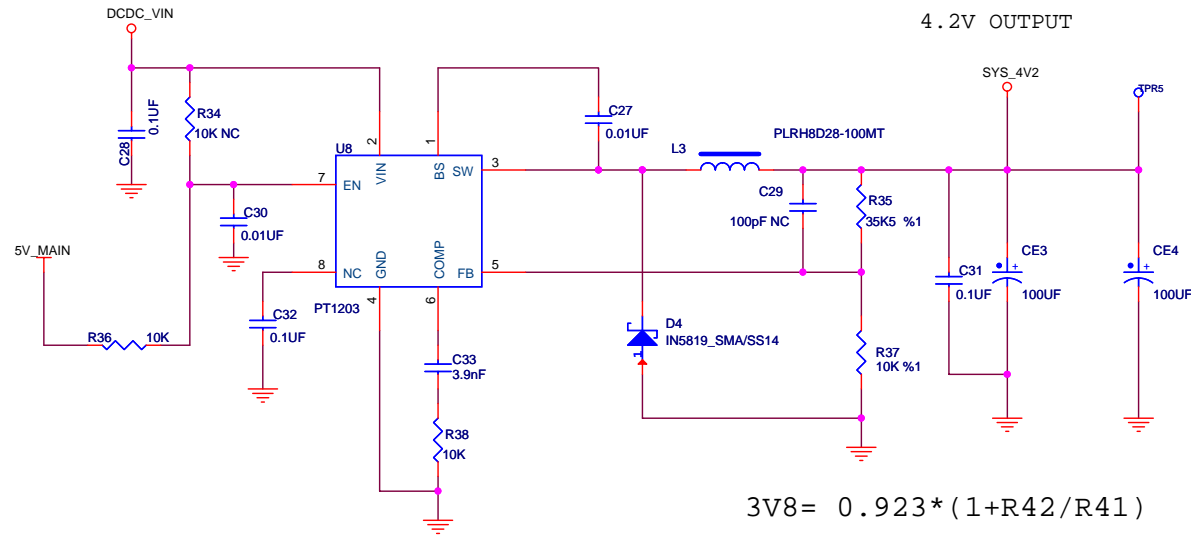
3. 3V OUTPUT



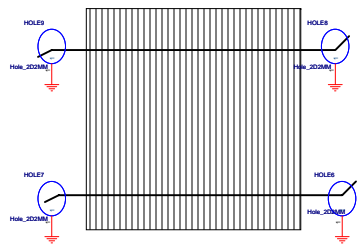
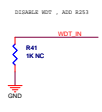
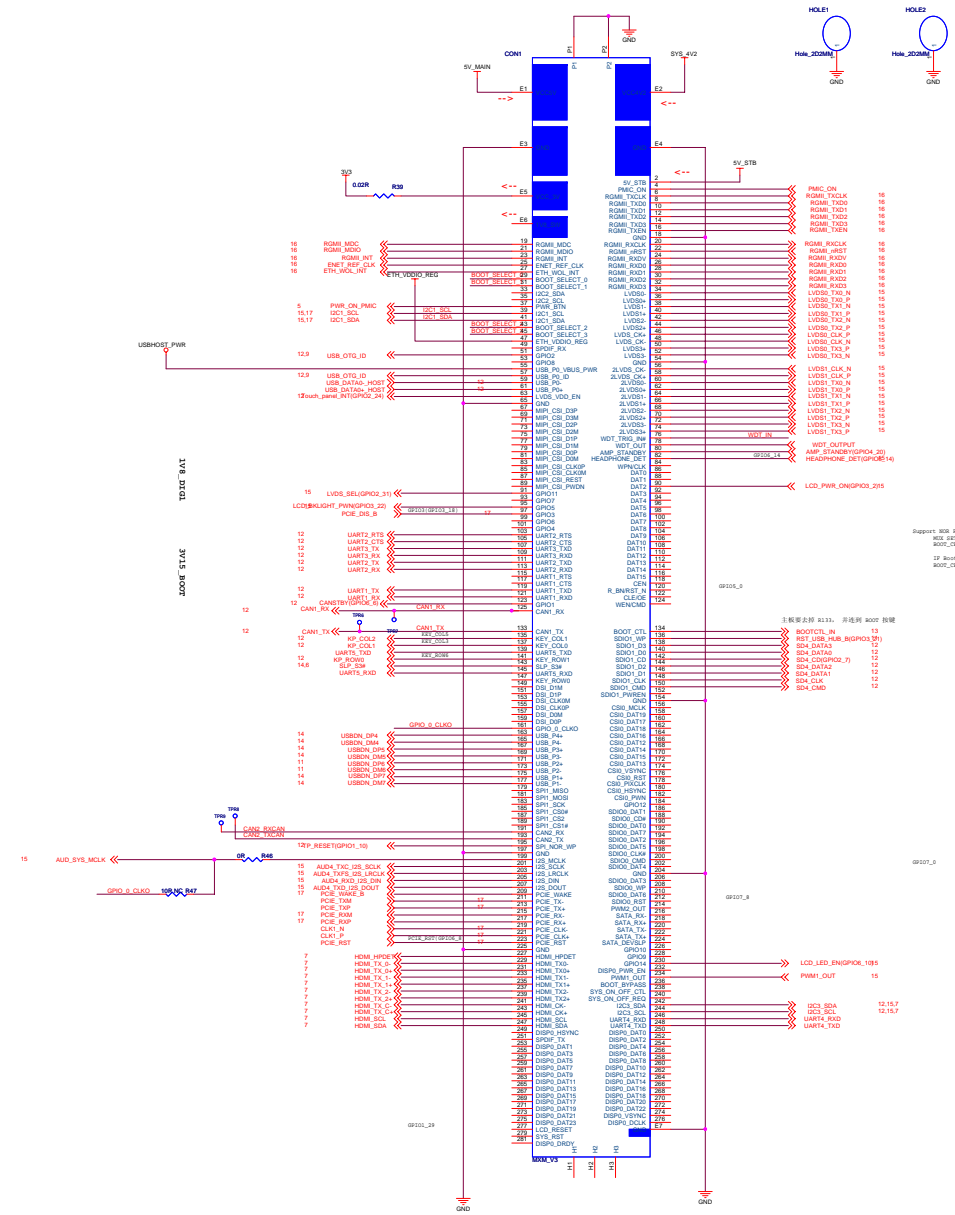
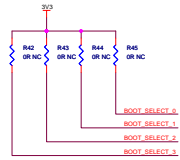
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Support ROM FLASH, DATA/Address HEX32
 KEY: 00000000
 ROM: 0002174100
 12 Base From ROM: 0000
 ROM: 0002174100000

3 載入部 0000 0000 非選択 BOOT 制御

00207_0

00207_0

00207_0

00207_0

00207_0

00207_0

00207_0

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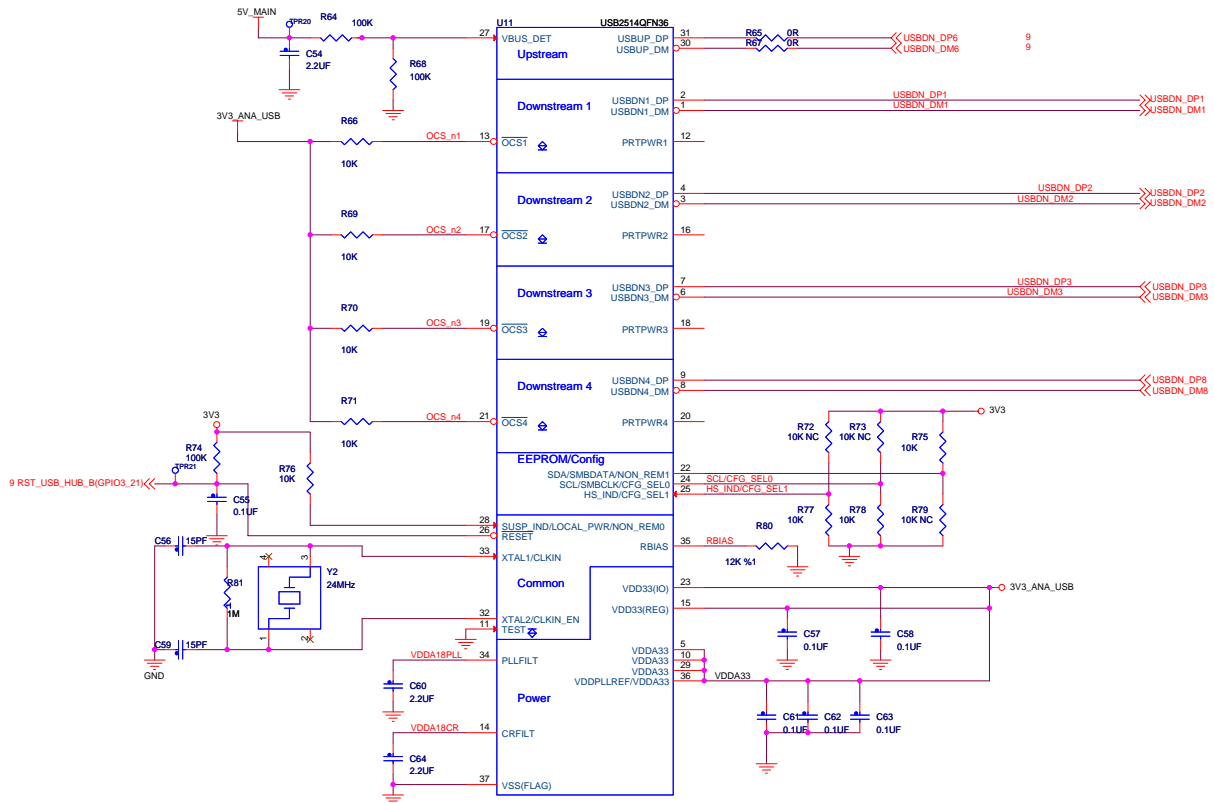
00207_0

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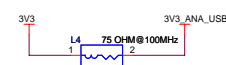
00207_0



USB PORT (9.7 板用)

连接 3G

连接 USB 转 NET

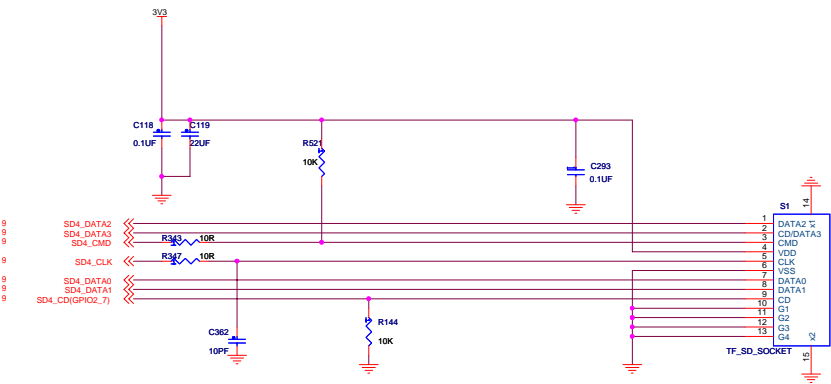
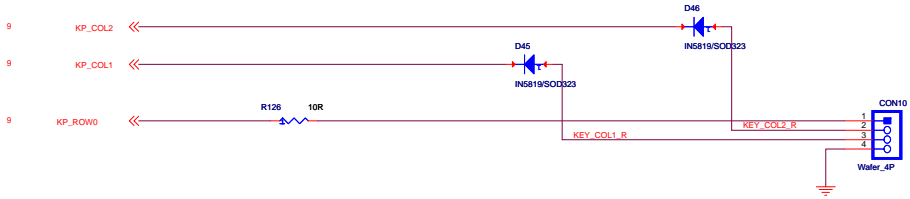
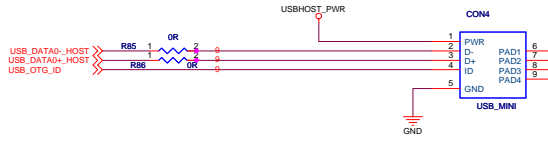
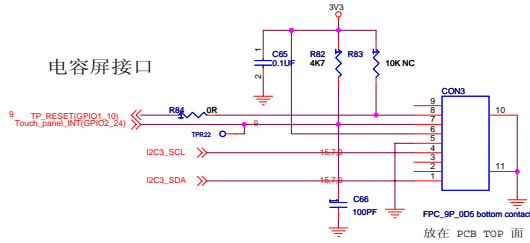


Internal Defaults

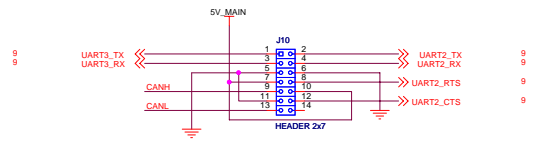
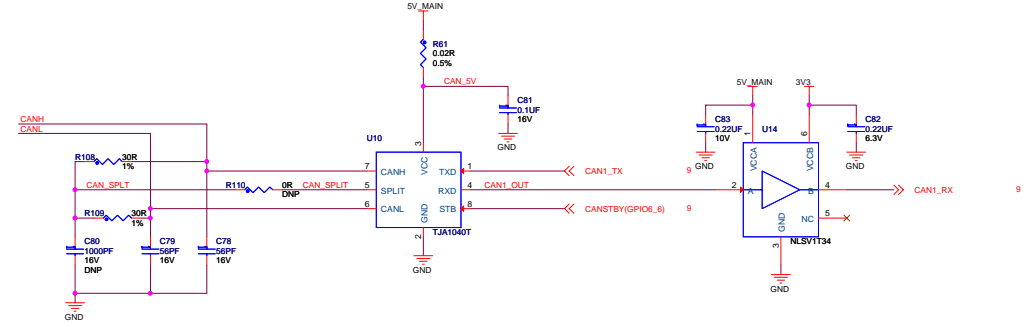
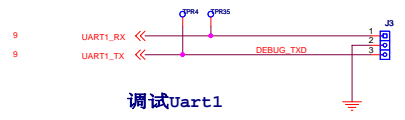
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电容屏

电容屏接口

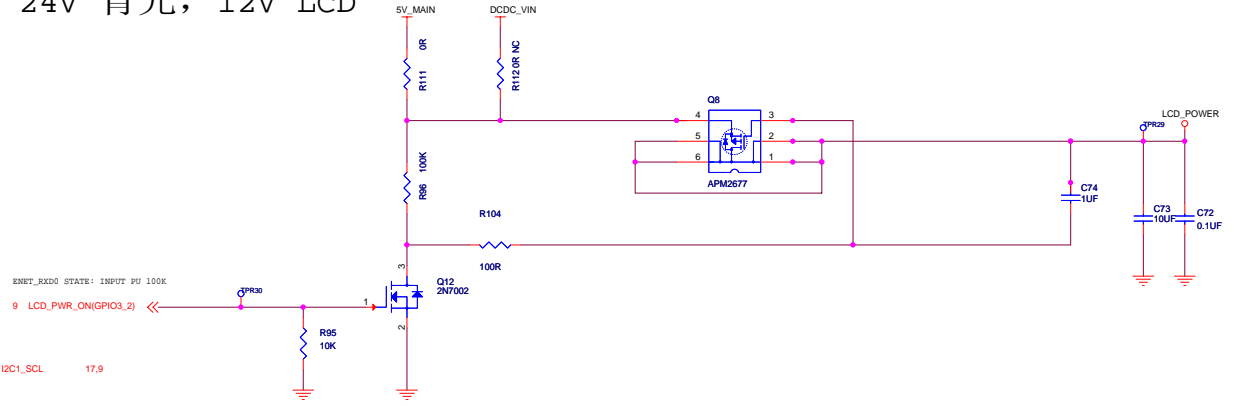
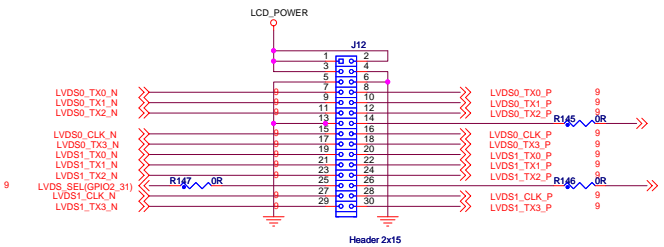


调试Uart1



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兼容 24V 背光, 12V LCD

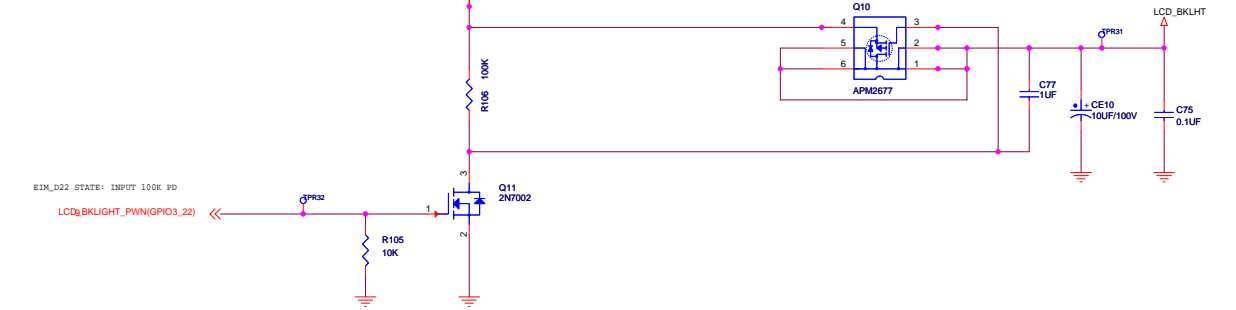


ENET_RXD0 STATE: INPUT PU 100K
 9 LCD_PWR_ON(GPIO3_2) <<< R95 10K

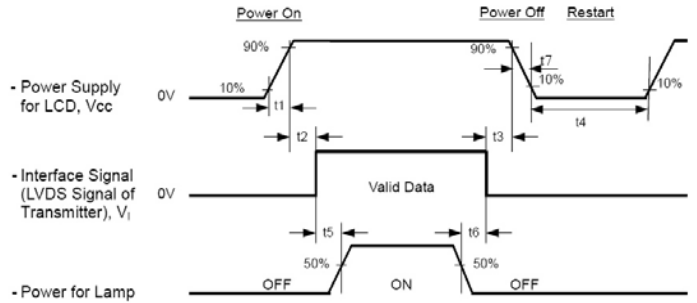
I2C1_SCL 17.9
 I2C1_SDA 17.9

3.5A 电流

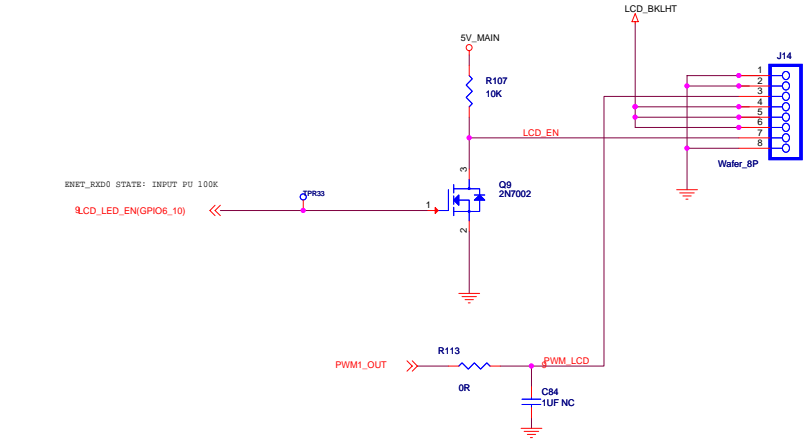
3.5A 电流



ENET_D22 STATE: INPUT 100K PD
 LCD_BKLIGHT_PWM(GPIO3_22) <<< R105 10K



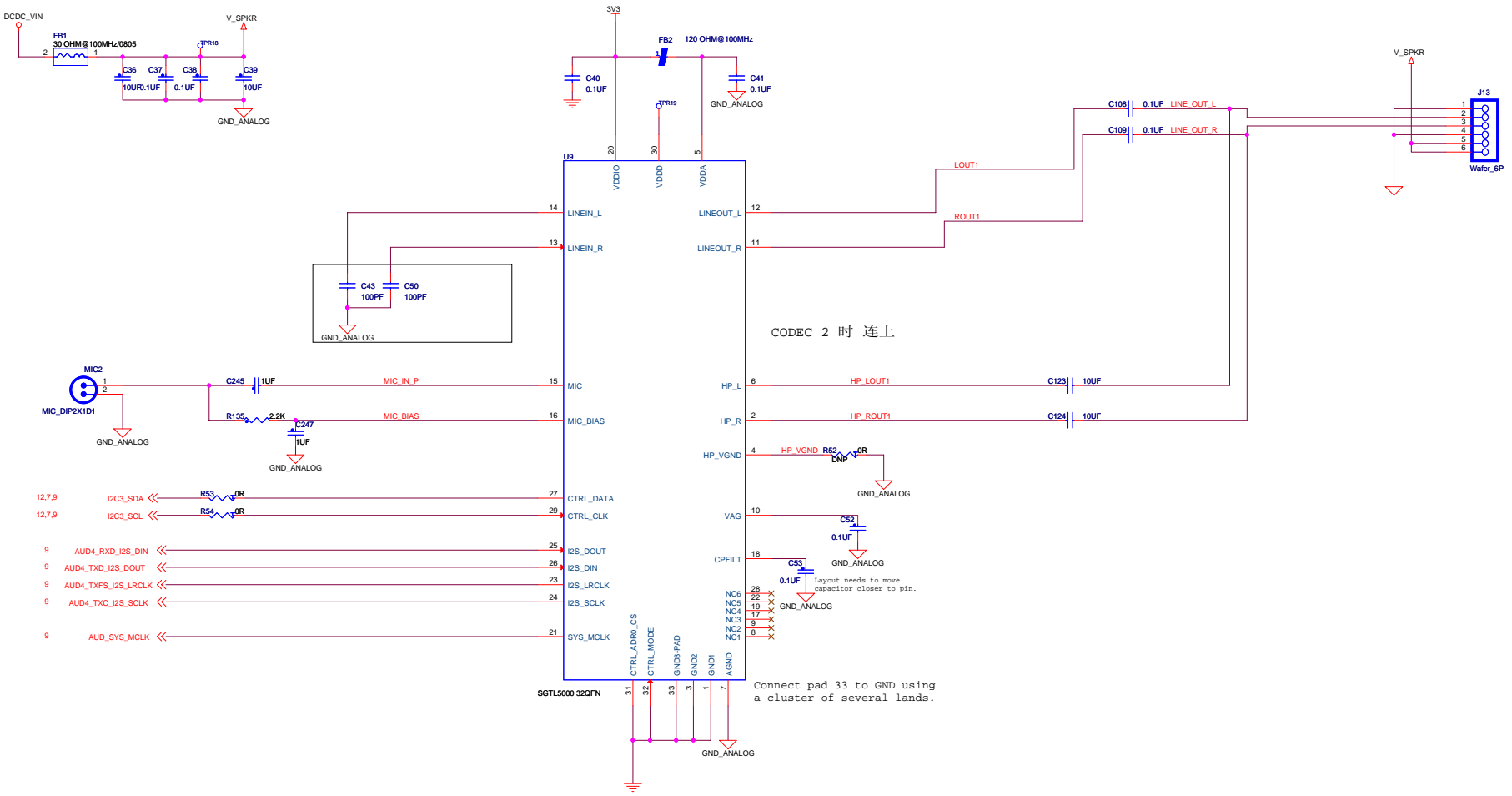
- Timing Specifications:
- 0.5 < t1 ≤ 10 msec
 - 0 < t2 ≤ 50 msec
 - 0 < t3 ≤ 50 msec
 - t4 ≤ 500 msec
 - t5 ≤ 450 msec
 - t6 ≤ 90 msec
 - 5 ≤ t7 ≤ 100 msec



ENET_RXD0 STATE: INPUT PU 100K
 LCD_LED_EN(GPIO6_10) <<< R113 0R

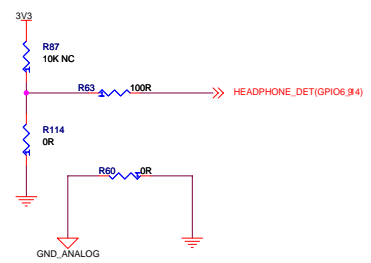
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Audio CODEC and Audio Power Amplifier



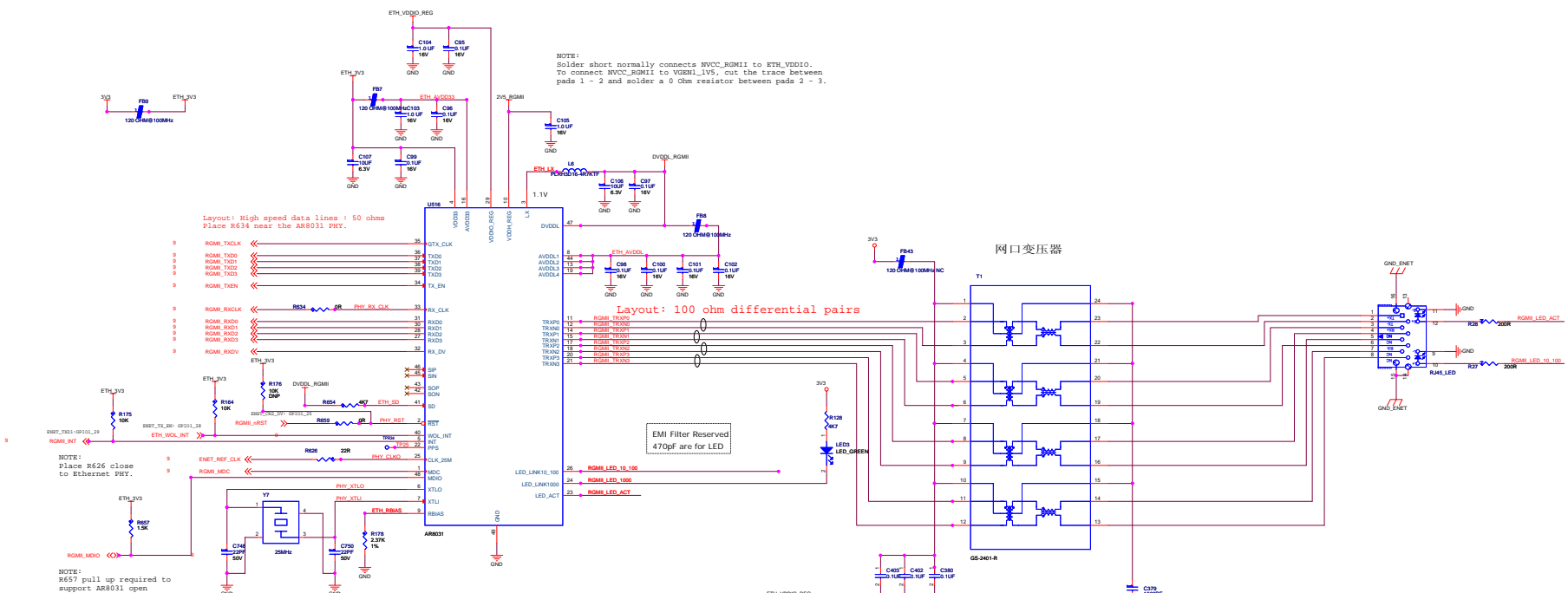
CODEC 2 吋 连上

Connect pad 33 to GND using a cluster of several lands.



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NOTE:
Solder short normally connects MVCC_RGMII to ETH_VDDIO.
To connect MVCC_RGMII to VDDEN1_VV5, cut the trace between
pads 1 - 2 and solder a 0 Ohm resistor between pads 2 - 3.



Layout: High speed data lines : 50 ohms
Place R634 near the AR8031 PHY.

Layout: 100 ohm differential pairs

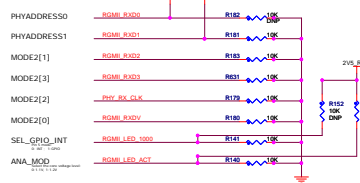
EMI Filter Reserved
470pF are for LED

NOTE:
Place R626 close to Ethernet PHY.

NOTE:
R657 pull up required to support AR8031 open drain MDIO pin, when AR8031 is outputting data. Pull up not required on MDIO since line is only driven by i.MX 6.

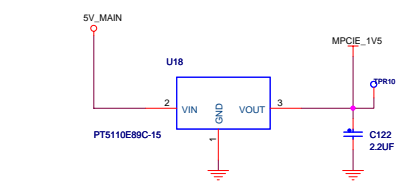
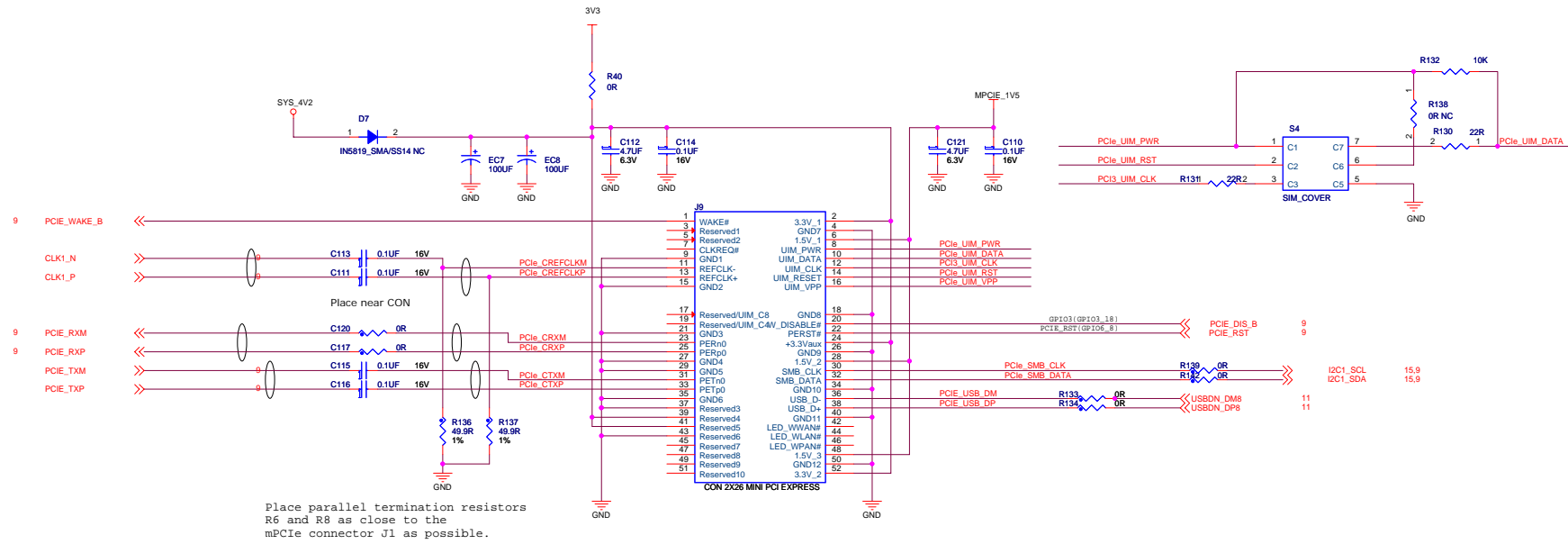
Power-on Strapping Pins

MODE2[3:0]
(Default assemble: 0000)
1100 BaseT, RMI1;
1101 BaseT, RMI2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMII;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RGMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, TRANS, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved



Mini-PCIE

Layout: 100 Ohm differential pairs



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