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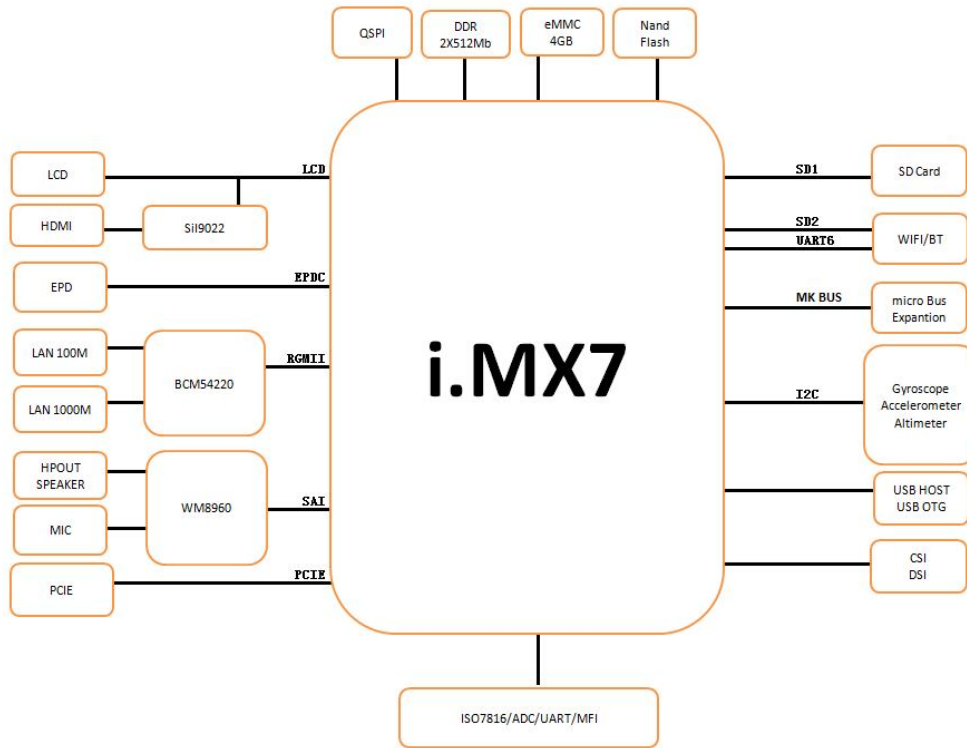
# MCIMX7D-SABRE

## Revision History

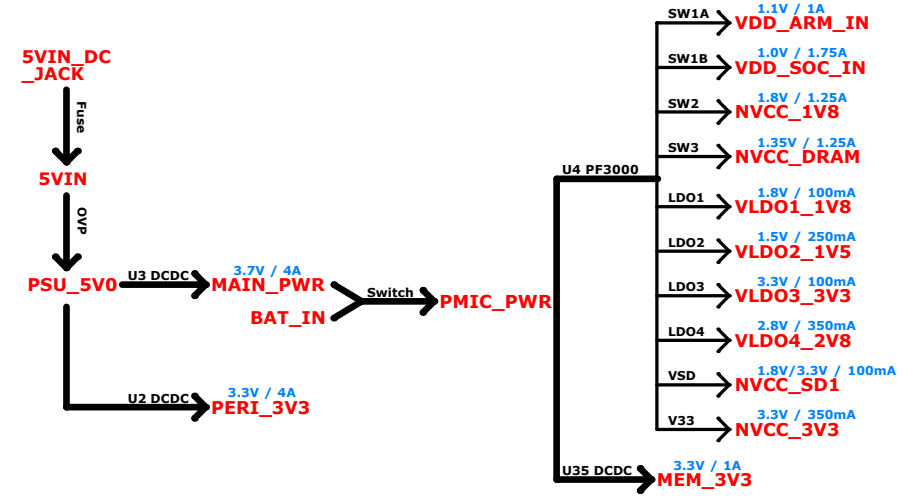
Rev. Code	Date	Description
B	22/09/2015	Initial Draft
B1	21/01/2016	<ul style="list-style-type: none"> <li>- Changed Q8 from 2N7002 to MMBT3904.</li> <li>- Reconnection U43 SW with the anode of D25.</li> <li>- DNF the capacitor:C6,C121.</li> <li>- Changed the power of JTAG from PERI_3V3 to VLD03_3V3.</li> <li>- PCIE                             <ul style="list-style-type: none"> <li>DNF the resistor:R605,R606,R607,R608.</li> <li>Changed C442 and C443 to 0ohm resistor (R632,R633).</li> <li>Add 49.9 1% 0402 resistors (R634,R635) on PCIE_REFCLKOUT_P/N to GND.</li> </ul> </li> <li>- Add the mosfet Q36 on the NET "CSI_PWDN".</li> <li>- Add blocking capacitor(C458,C459) Before the terminal resistor.</li> <li>- Add Schottky diode(D26) to isolate POR_B with JTAG interface.</li> <li>- Use the LDO U44 instead of Q11.</li> <li>- Add the 0ohm resistor(R641) connect the pin CCM_CLK2 to GND.</li> <li>- Add the U45 to match electrical level.</li> </ul>
C	28/01/2016	<ul style="list-style-type: none"> <li>- Changed the revision from "B1" to "C".</li> <li>- Delete the capacitors C312 and C314.</li> <li>- Add several GND test points TP68--TP75 around the DDR3.</li> <li>- Changed connectors type of the J29&amp;J30</li> </ul>

		<b>Multimedia Application Division, Wireless &amp; Mobile System Group</b>	
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<small>ICAP Classification:</small> FCP:		<small>FLUG: PUB:</small>	
<small>Designer:</small>	<small>Drawing Title:</small> <b>MCIMX7D-SABRE</b>		
<small>Drawn by:</small>	<small>Page Title:</small> <b>01 Title Sheet</b>		
<small>Approved:</small> <small>&lt;Approver&gt;</small>	<small>Size:</small> A2	<small>Document Number:</small> SOURCE:SCH-28590:SPF-28590	<small>Rev:</small> C
<small>Date:</small> Monday, February 01, 2016		<small>Sheet:</small> 1 of 23	

# MCIMX7D-SABRE Block Diagram



# Power Distribution Diagram

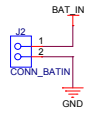


**freescale**

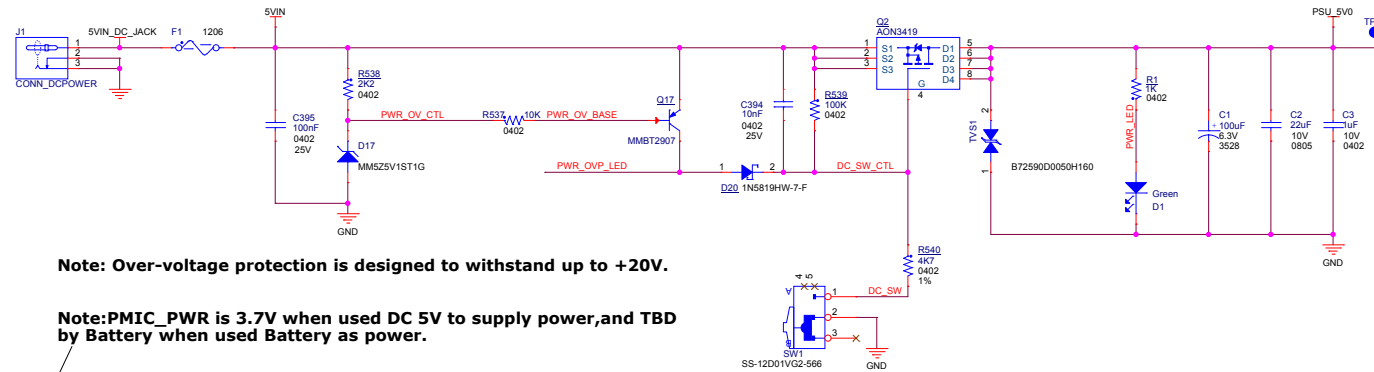
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 Page Title: **02 Block Diagram**

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# BATTERY IN



# 5V DC POWER

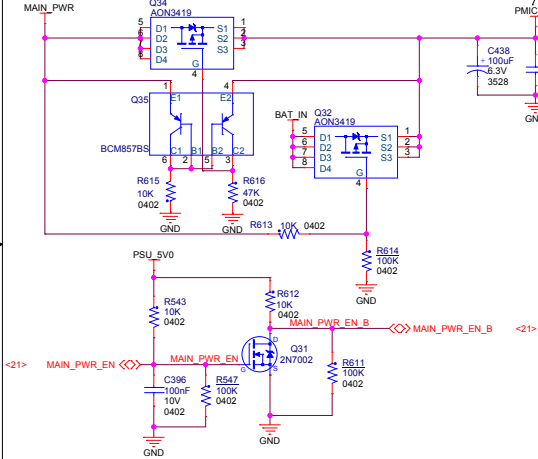


Note: Over-voltage protection is designed to withstand up to +20V.

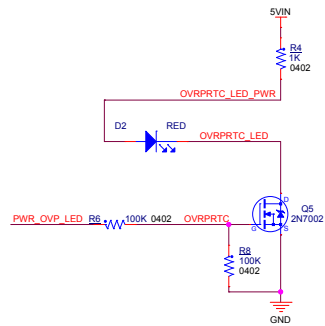
Note: PMIC\_PWR is 3.7V when used DC 5V to supply power, and TBD by Battery when used Battery as power.

# OVER VOLTAGE PROTECTION

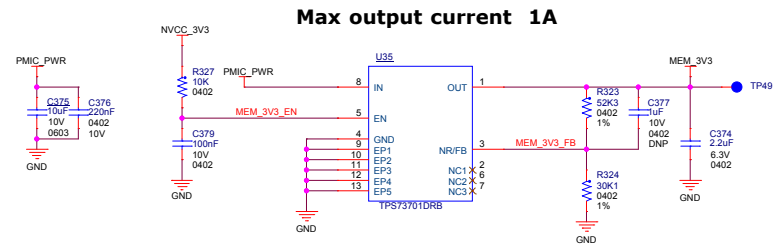
# POWER SWITCH



# OVER VOLTAGE INTICATOR



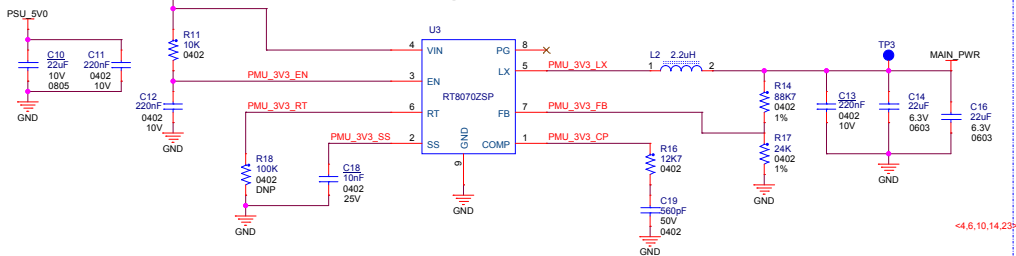
# MEM\_3V3



Max output current 1A

# PMIC POWER IN

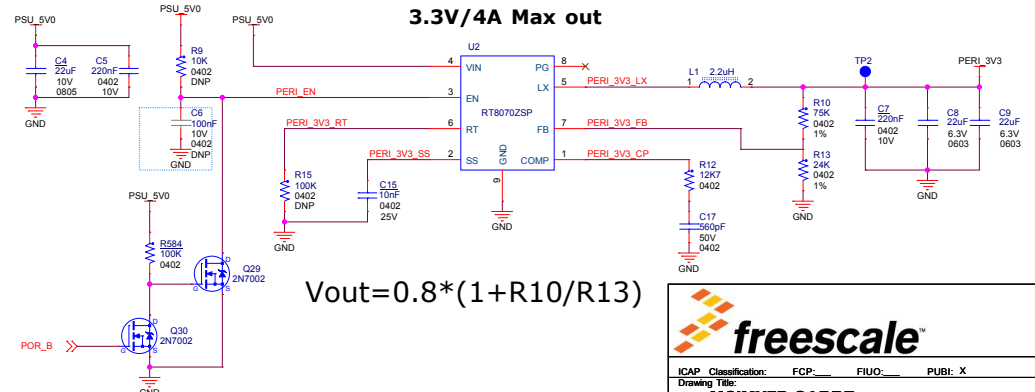
3.7V/4A Max out



$$V_{out} = 0.8 * (1 + R14/R17)$$

# 3V3 PERI

3.3V/4A Max out

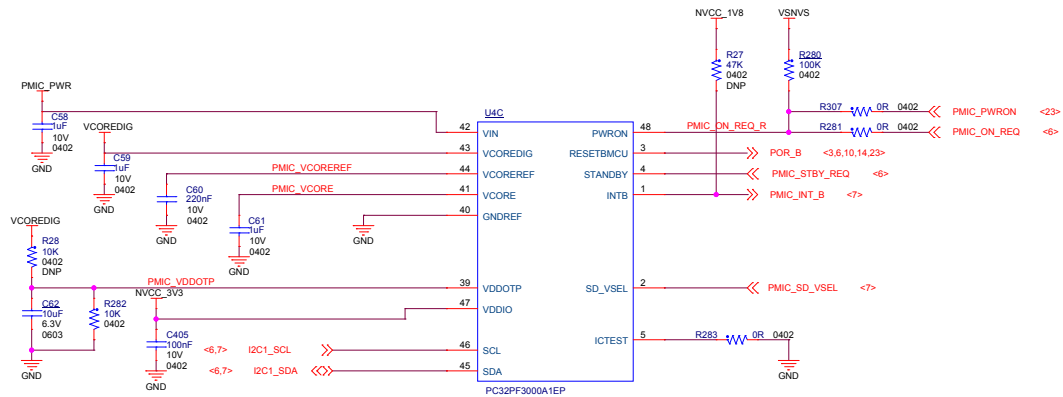
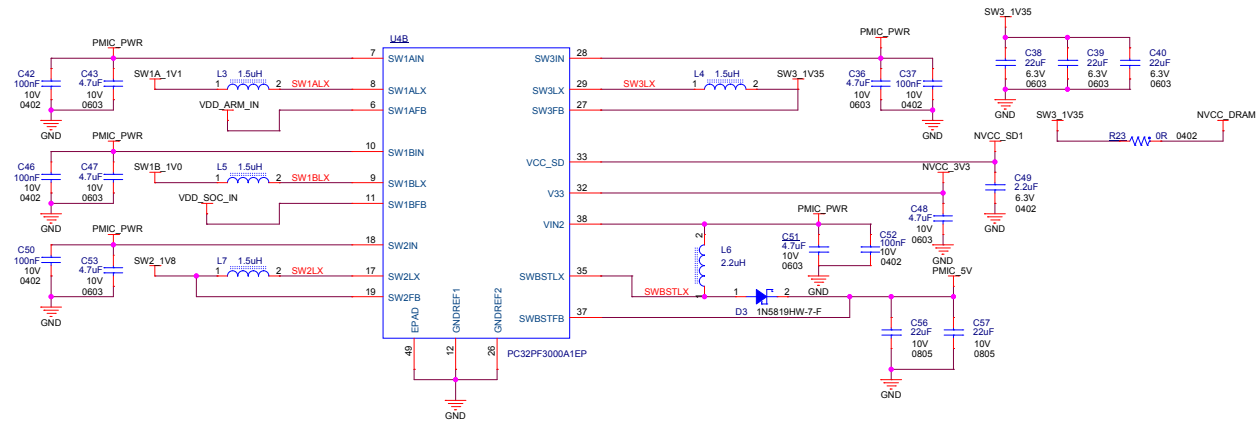
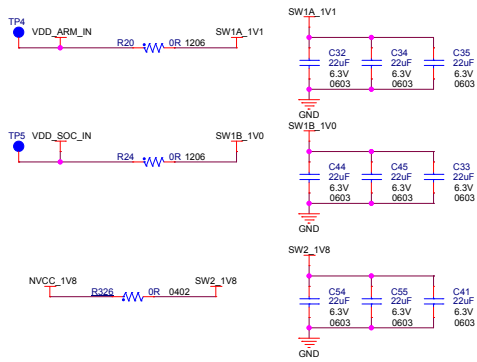
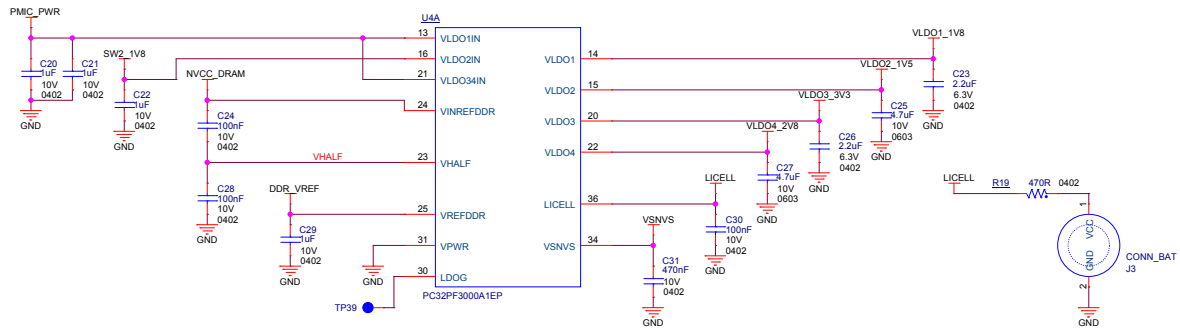


$$V_{out} = 0.8 * (1 + R10/R13)$$

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 Drawing Title: **MCIMX7D-SABRE**  
 Page Title: **03 Main Power**

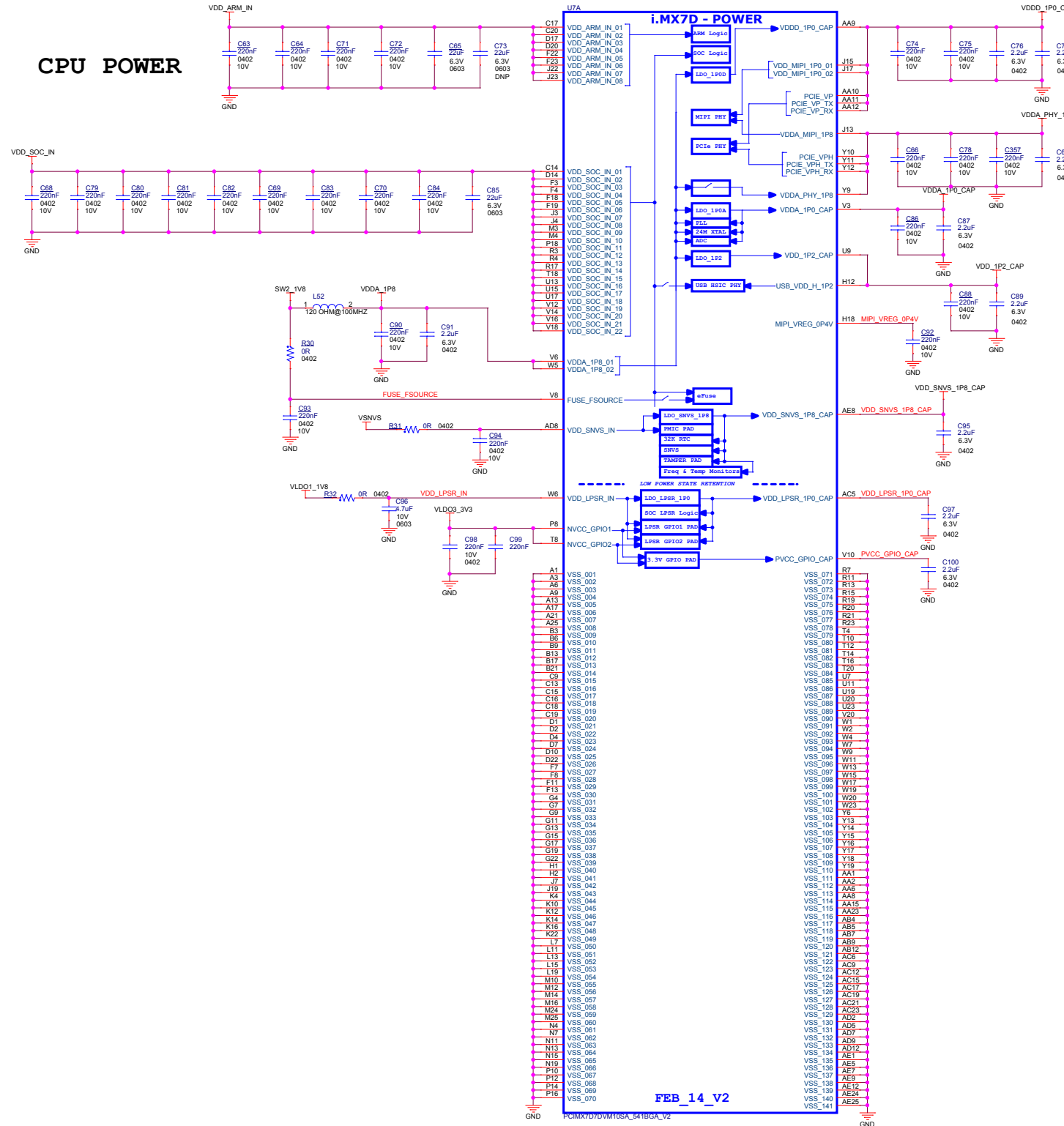
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# PMIC



ICAP Classification: FCP: _____ FIUO: _____ PUBI: X			
Drawing Title: <b>MCIMX7D-SABRE</b>			
Page Title: <b>04 PMIC</b>			
Size C	Document Number	SOURCE: SCH-28590-SPF-28590	Rev C
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# CPU POWER



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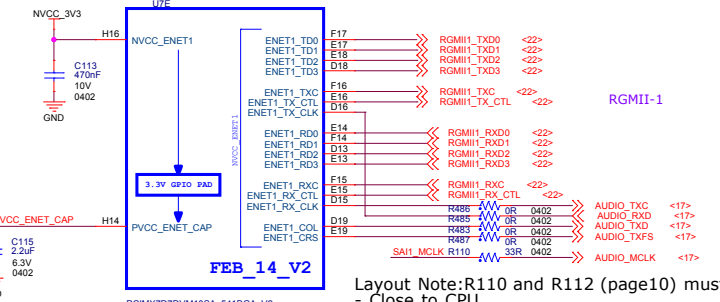
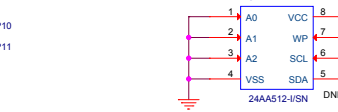
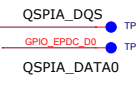
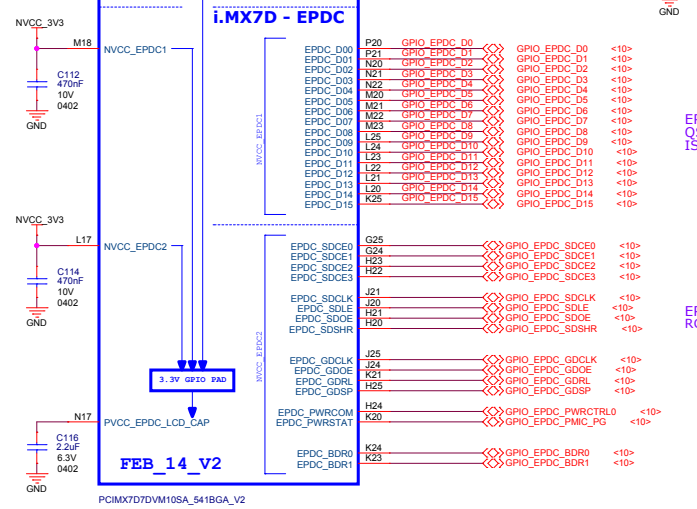
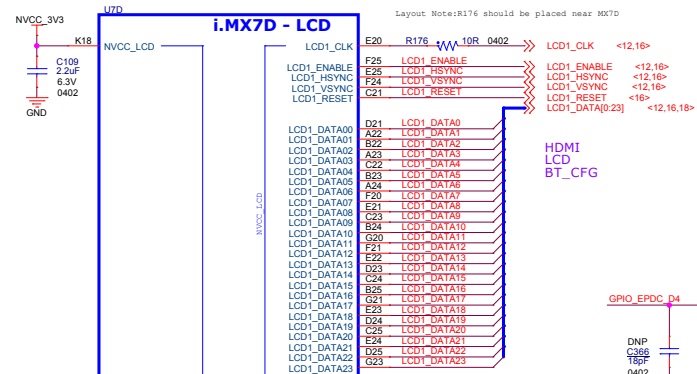
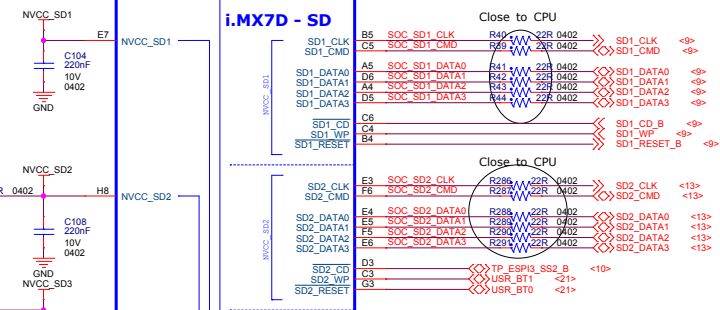
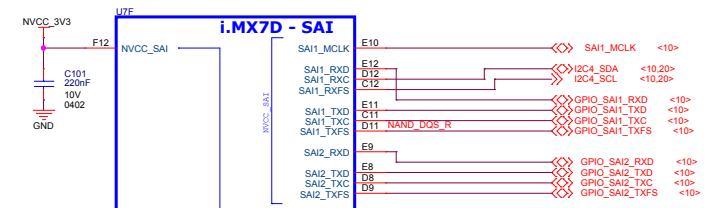
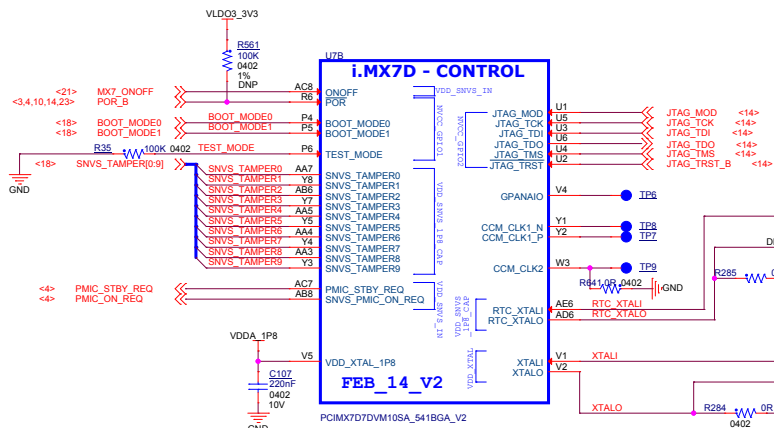
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Drawing Title:  
**MCIMX7D-SABRE**

Page Title:  
**05 CPU Power**

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Layout Note: R110 and R112 (page10) must - Close to CPU - Close to each other, to make sure the stub is as short as possible.

I2C4 MFI/Codect/CSI/DS1  
MicroBus Sensor\_INT  
EPDC Touch  
NAND  
MicroBus TP

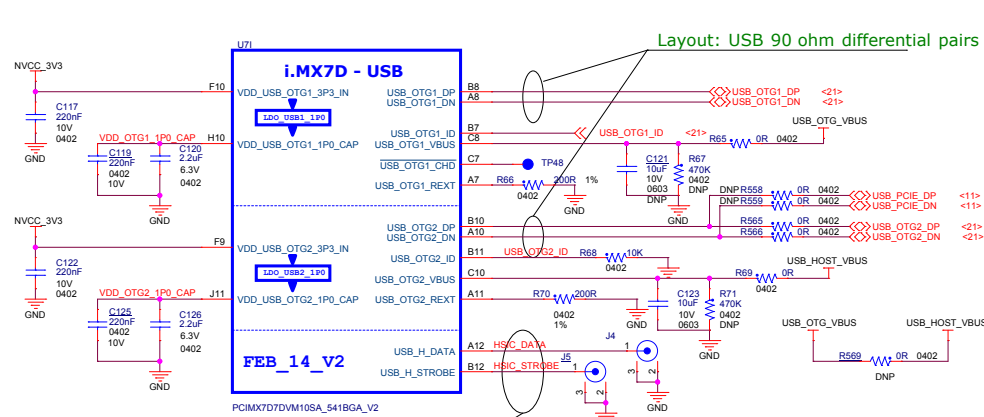
SD3.0

WiFi/BT

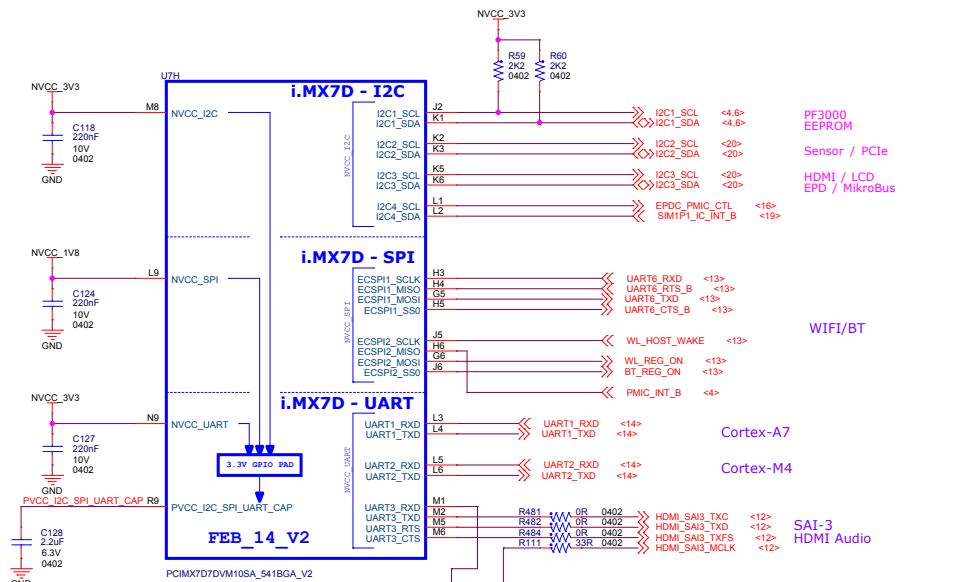
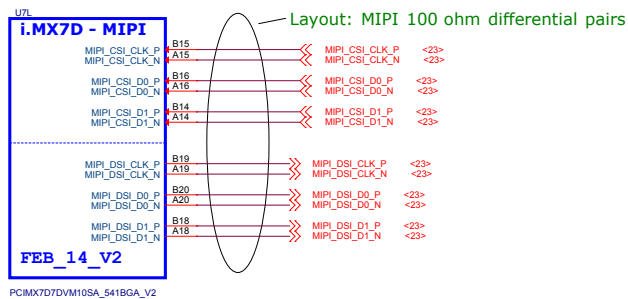
eMMC5.0  
NAND

**freescale**

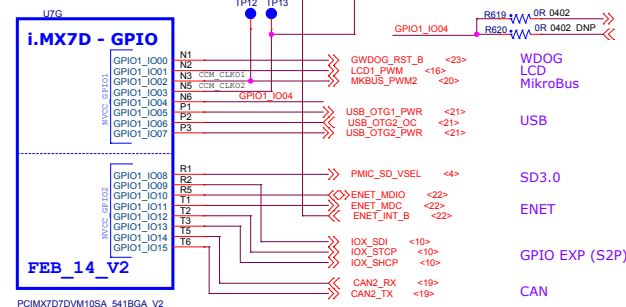
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 Page Title: **06 CPU Signal 1**  
 Date: Thursday, January 28, 2016 Sheet 6 of 23



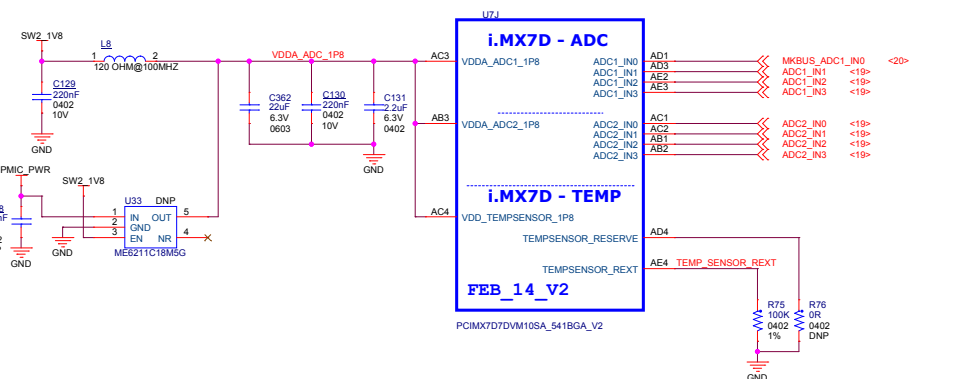
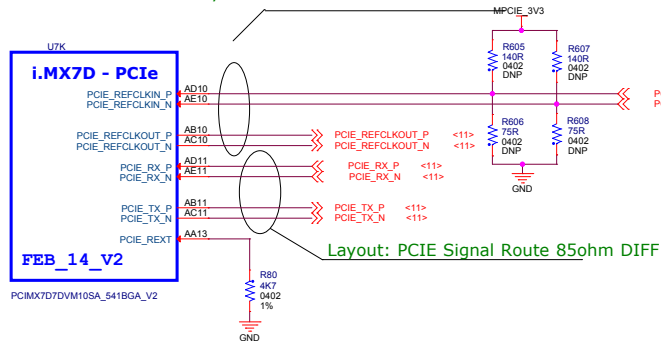
Layout: Route 50 ohm



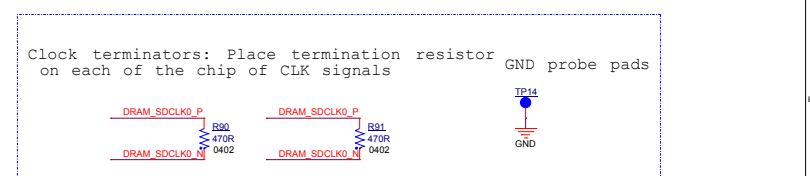
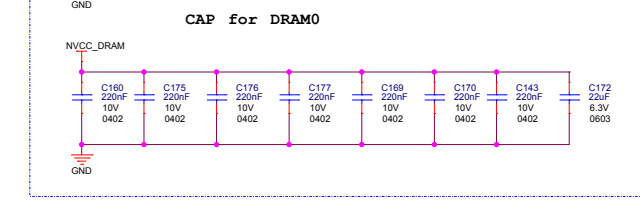
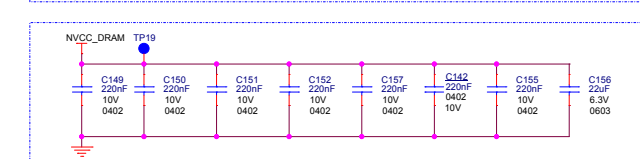
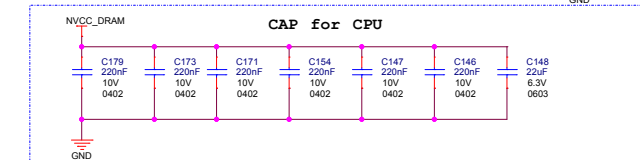
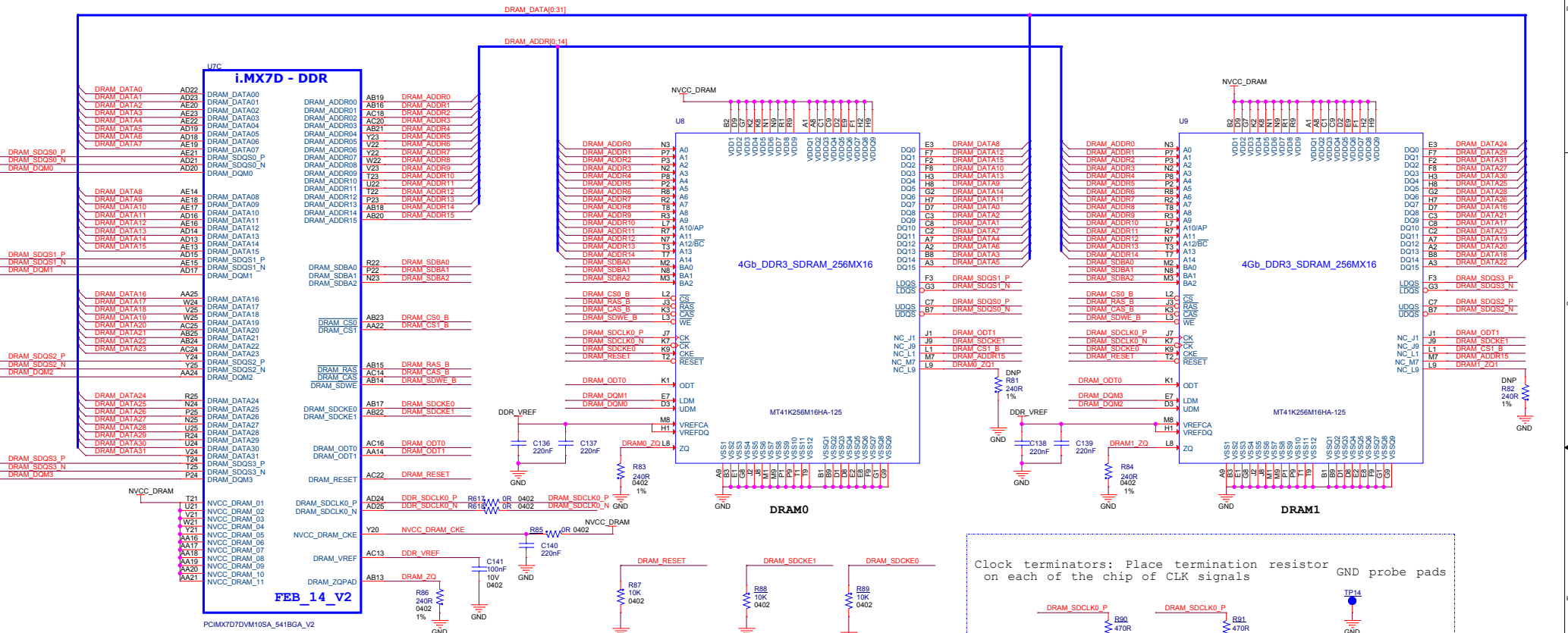
Note:GPIO\_IO04 is used as EPDC/ENET2 in default.



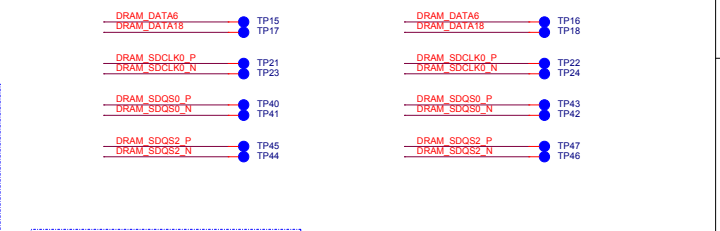
Layout: PCIe REF Clock Route 100ohm DIFF



# DDR



**Note: test points for signal integrity measurement**  
Place near the i.MX7D side Place near the DDR3L side

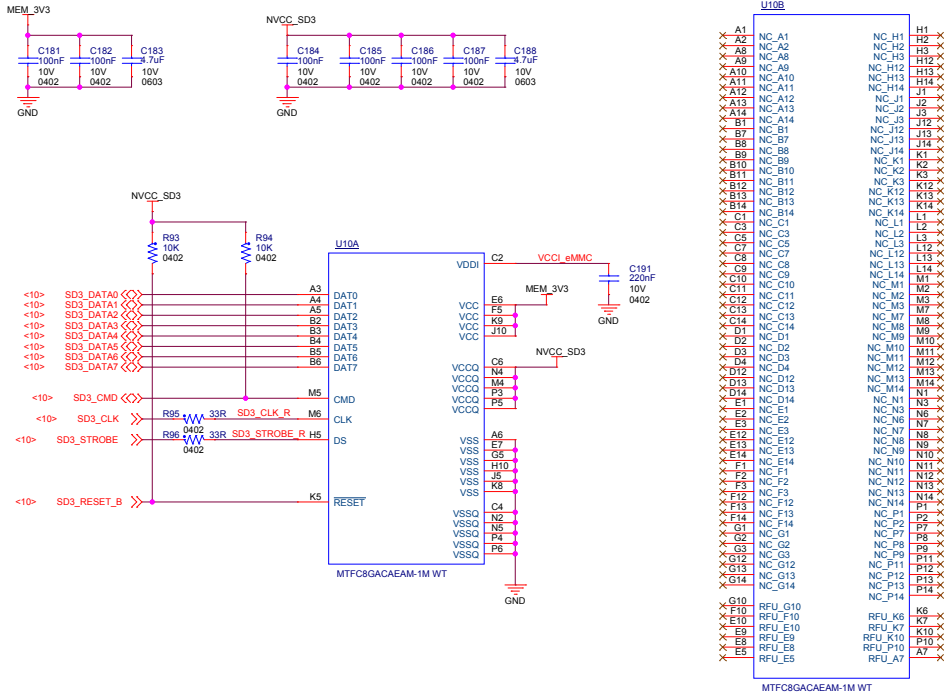


**ICAP Classification:** FCP:\_\_\_ FIUO:\_\_\_ PUBI: X  
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**Page Title:** **08 DDR3 Memory**

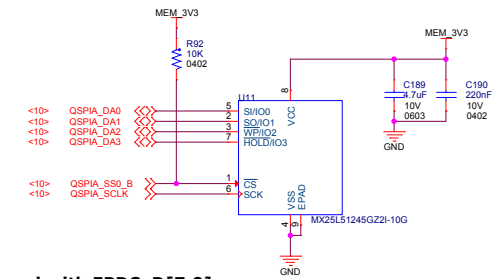
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# eMMC 5.0

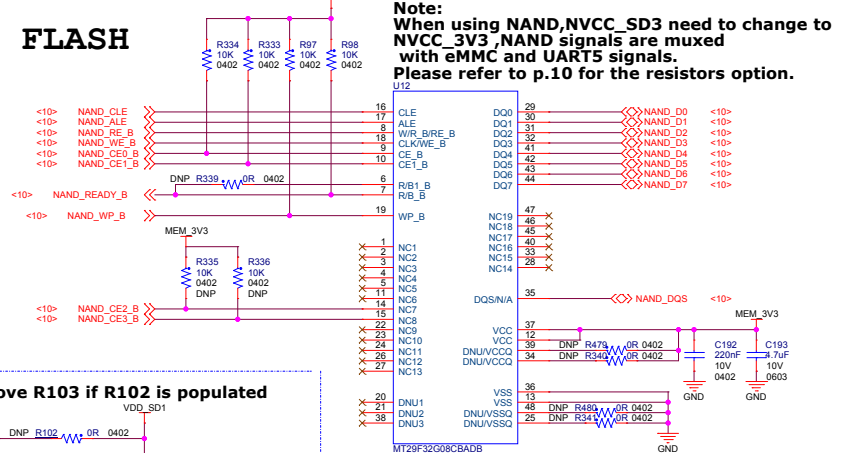


# QSPI NOR FLASH



**Note:**  
QSPI signals are muxed with EPDC\_D[7:0]  
When using QSPI:  
de-populate R388-R391, R396-R399  
populate R392-R395, R299, R300

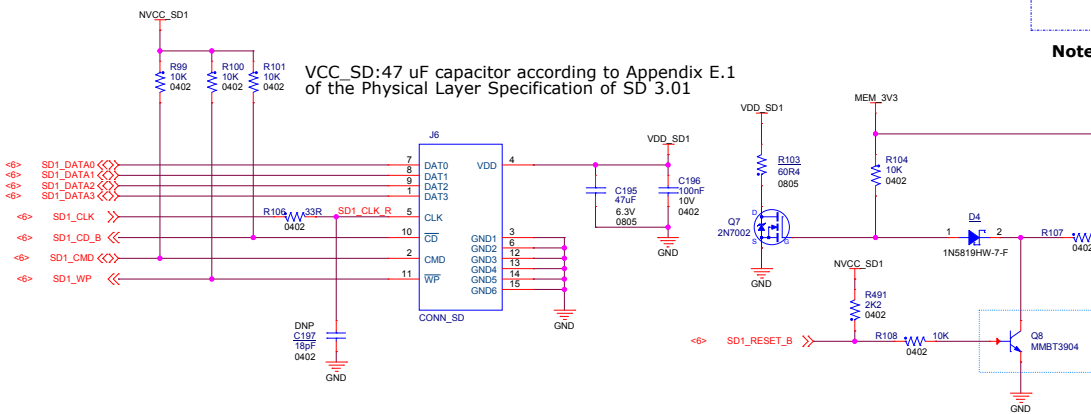
# NAND FLASH



**Note:**  
When using NAND, NVCC\_SD3 need to change to NVCC\_3V3, NAND signals are muxed with eMMC and UART5 signals. Please refer to p.10 for the resistors option.

**Note:** Remove R103 if R102 is populated

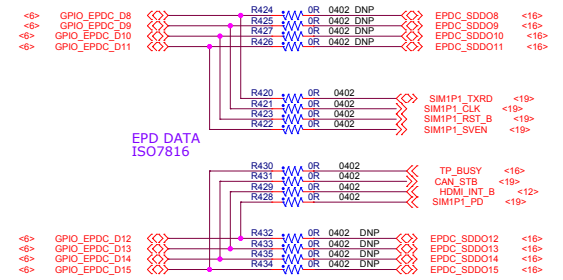
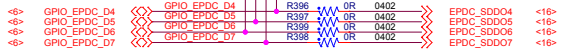
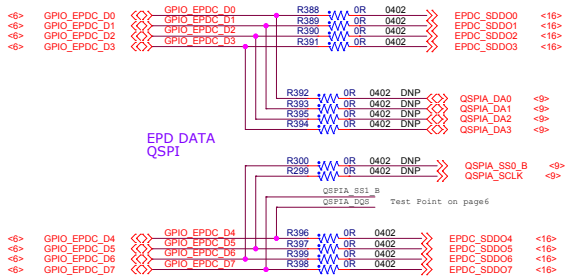
# SD CARD



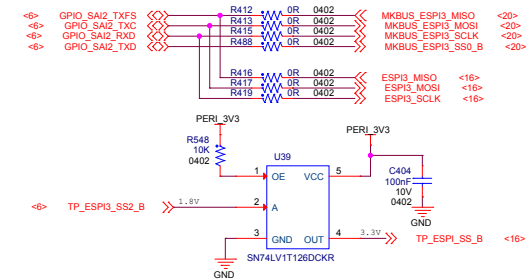
VCC\_SD: 47 uF capacitor according to Appendix E.1 of the Physical Layer Specification of SD 3.01

**freescale**  
 ICAP Classification: FCP: FUIO: PUBI: X  
 Drawing Title: MCIMX7D-SABRE  
 Page Title: 09 eMMC/NAND/QSPI/SD  
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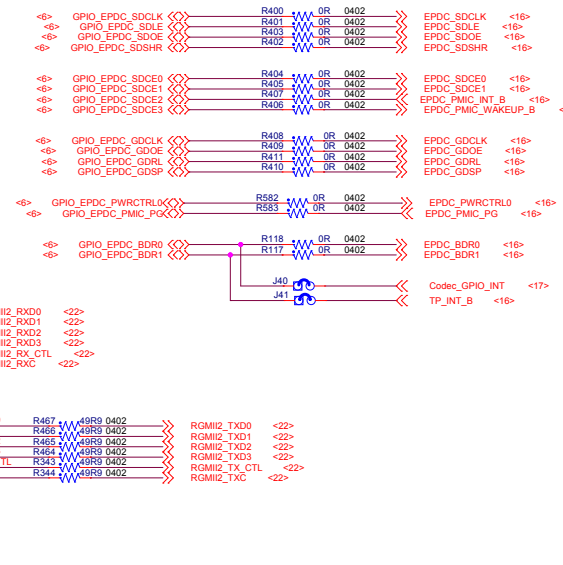
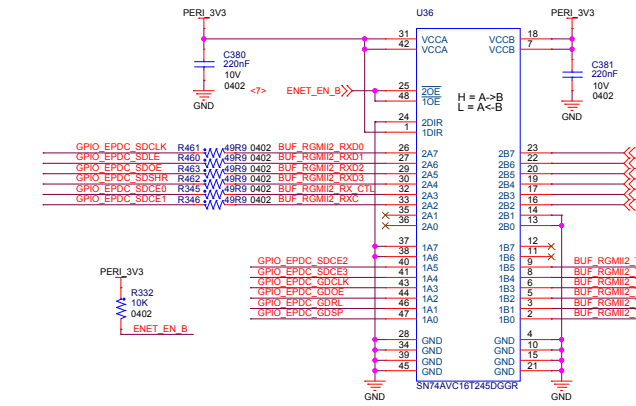
# EPD PIN MUX



# SAI2 PIN MUX

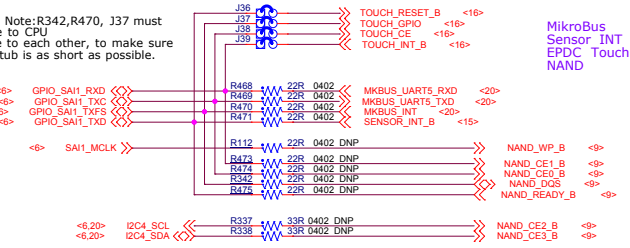


# EPD CTL RGMII-2



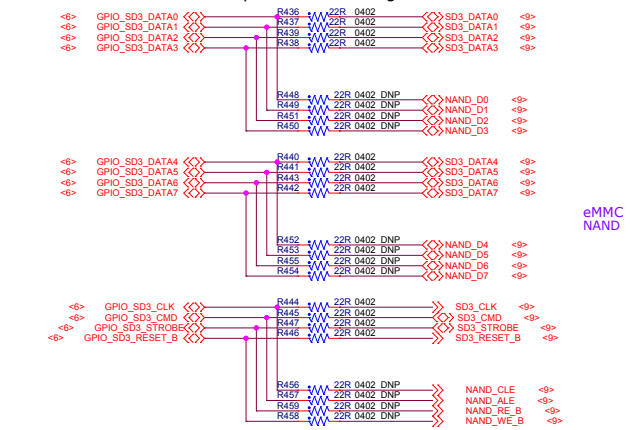
# SAI1 PIN MUX

Layout Note: R342, R470, J37 must close to CPU  
- Close to CPU  
- Close to each other, to make sure the stub is as short as possible.

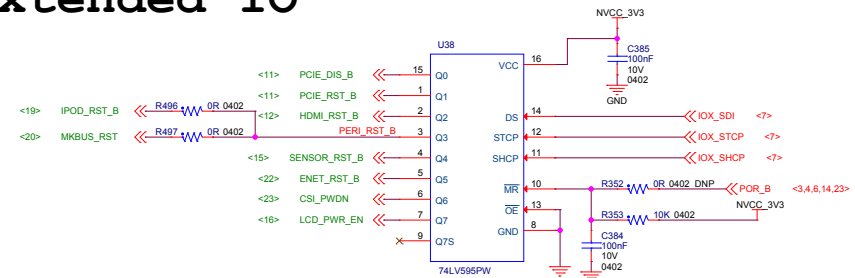


# SD3/NAND PIN MUX

Layout Note: NAND and SD resistor must close to the CPU for source impedance matching



# Extended IO



**freescale**

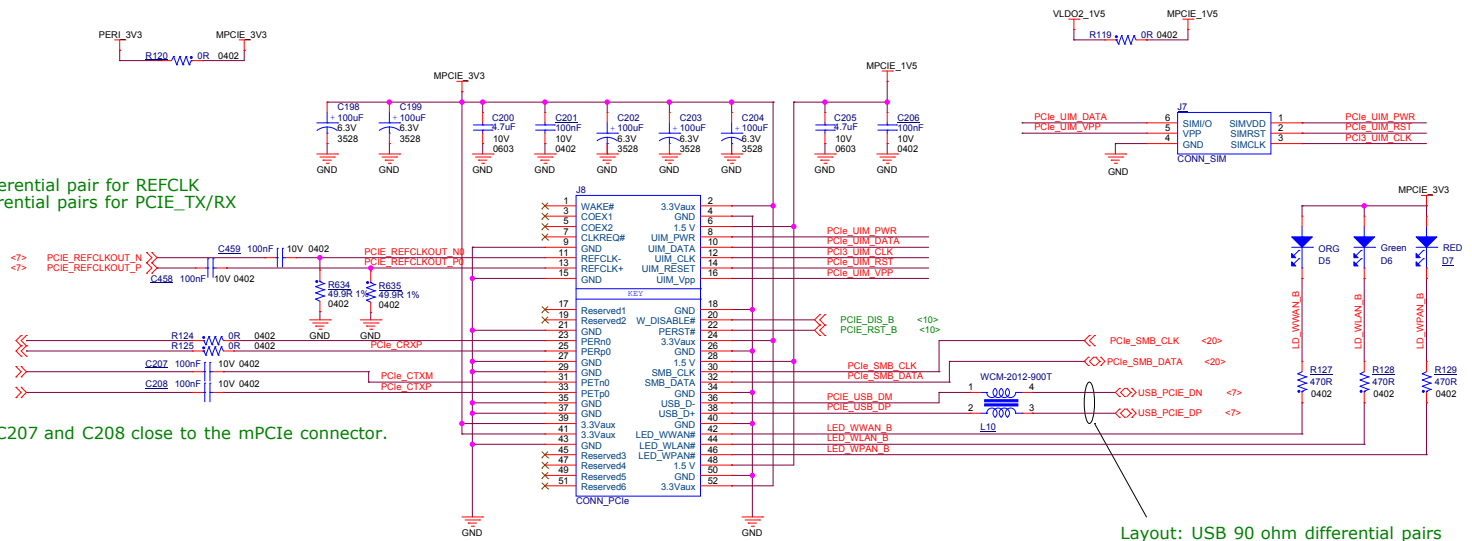
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Drawing Title: **MCIMX7D-SABRE**

Page Title: **10 Pin MUX**

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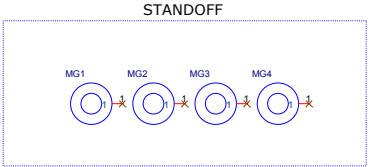
# Mini-PCIE



Layout: 100 ohm differential pair for REFCLK  
 Layout: 85 ohm differential pairs for PCIe\_TX/RX

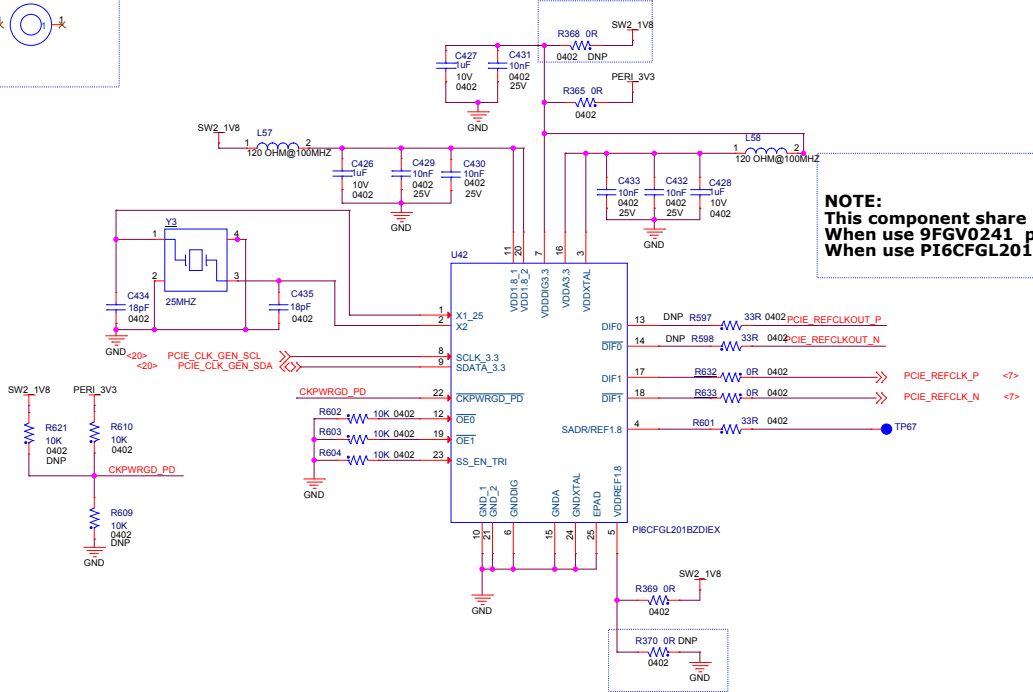
Layout: Place C207 and C208 close to the mPCIe connector.

Layout: USB 90 ohm differential pairs



**NOTE:**  
 This design assumes a normal loading on the MPCIE\_3V3 rail of up to 1A.  
 The MPCIE\_1V5 rail is allowed a maximum of 250 mA.

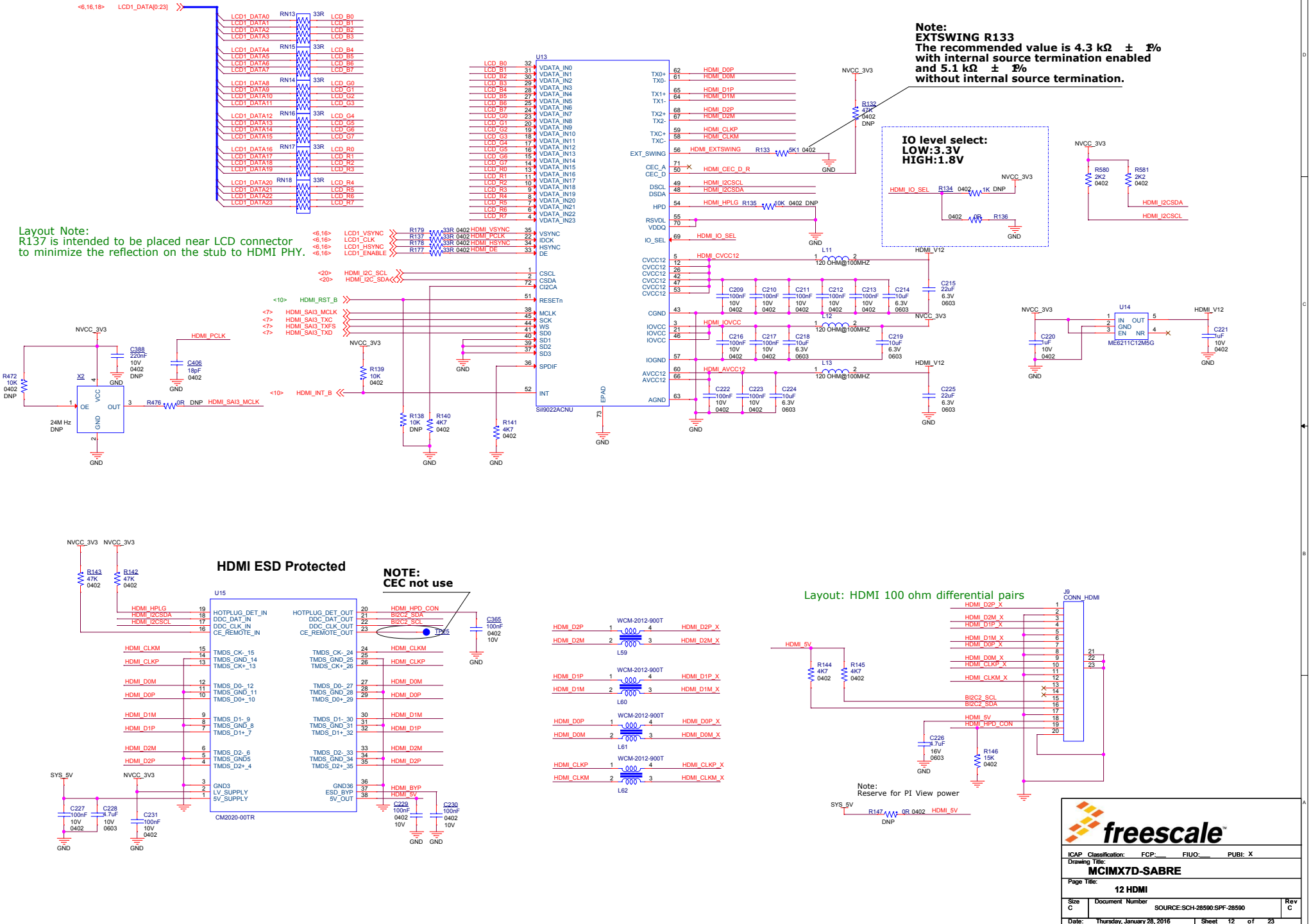
**NOTE:**  
 This component share PCB package  
 When use 9FGV0241 populate R368 & R370, de-populate R365 & R369.  
 When use PI6FCGL201BZDIEIX populate R365 & R369, de-populate R368 & R370 (default).



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ICAP Classification: FCP: _____ FIUO: _____ PUBI: X			
Drawing Title: <b>MCIMX7D-SABRE</b>			
Page Title: <b>11 Mini PCIe</b>			
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# HDMI Transceiver



**Note:**  
**EXTSWING R133**  
 The recommended value is  $4.3\text{ k}\Omega \pm 1\%$   
 with internal source termination enabled  
 and  $5.1\text{ k}\Omega \pm 1\%$   
 without internal source termination.

**IO level select:**  
**LOW:3.3V**  
**HIGH:1.8V**

**Layout Note:**  
 R137 is intended to be placed near LCD connector  
 to minimize the reflection on the stub to HDMI PHY.

**NOTE:**  
 CEC not use

**Layout:** HDMI 100 ohm differential pairs

**Note:**  
 Reserve for PI View power

**freescale**

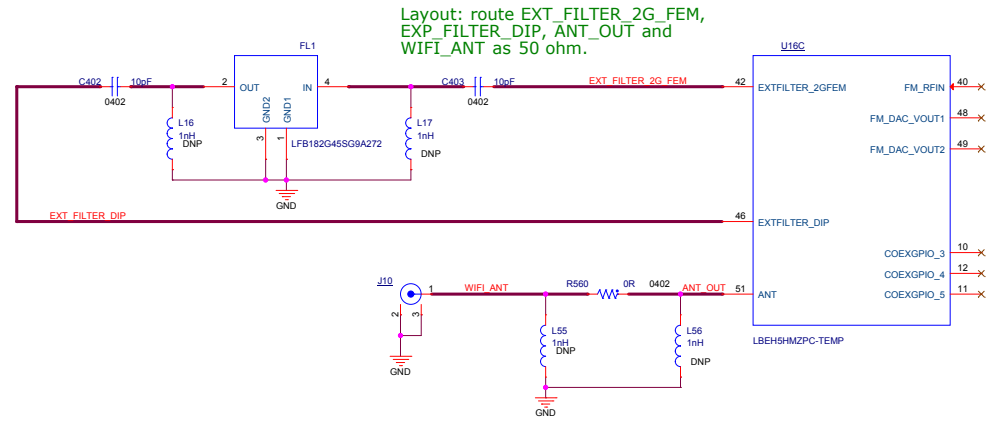
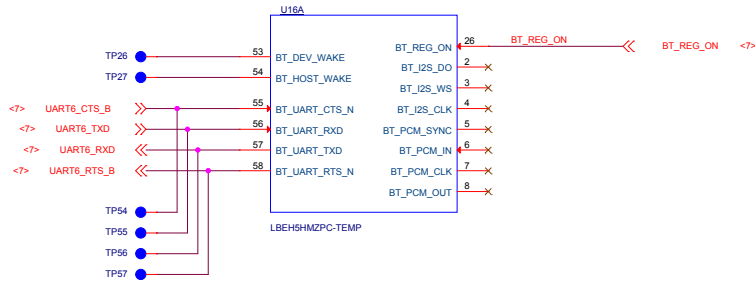
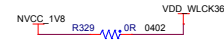
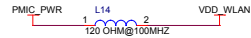
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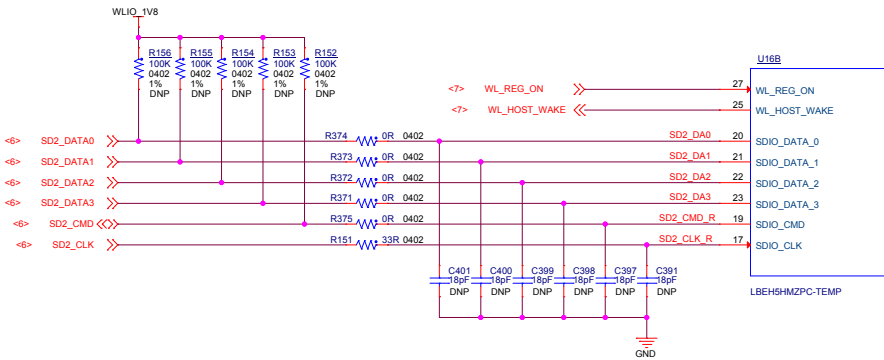
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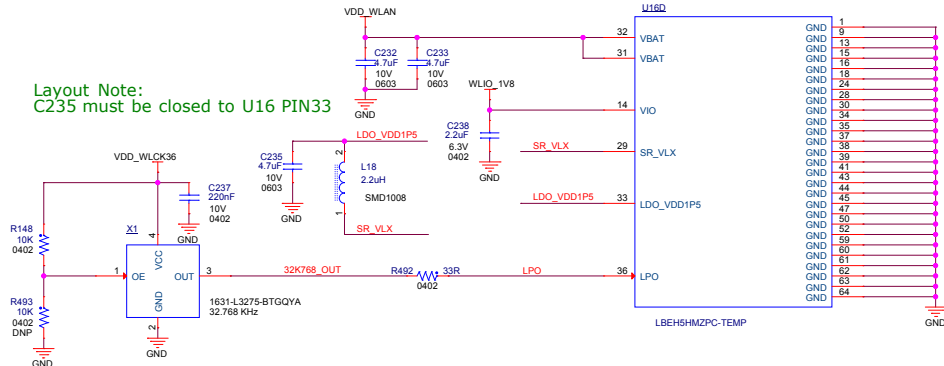
# WiFi/BT



Layout: route EXT\_FILTER\_2G\_FEM, EXP\_FILTER\_DIP, ANT\_OUT and WIFI\_ANT as 50 ohm.

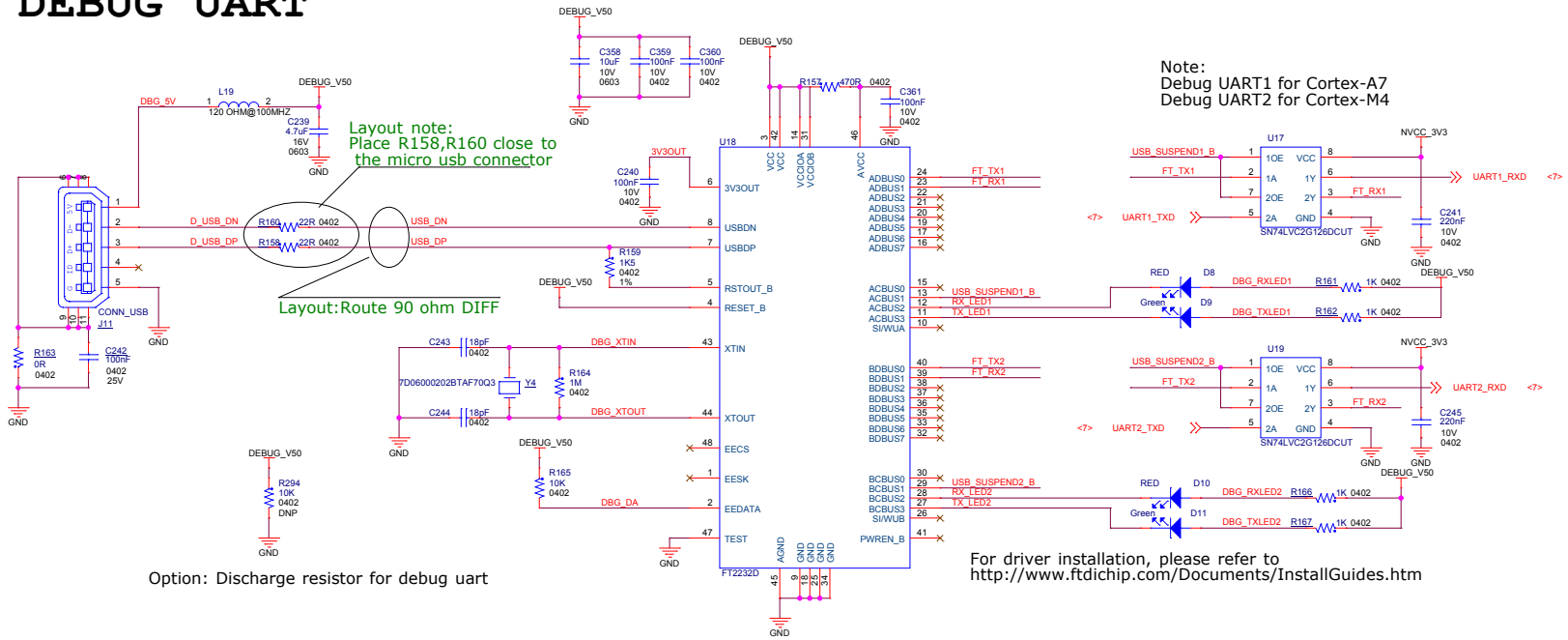


Layout Note: C235 must be closed to U16 PIN33

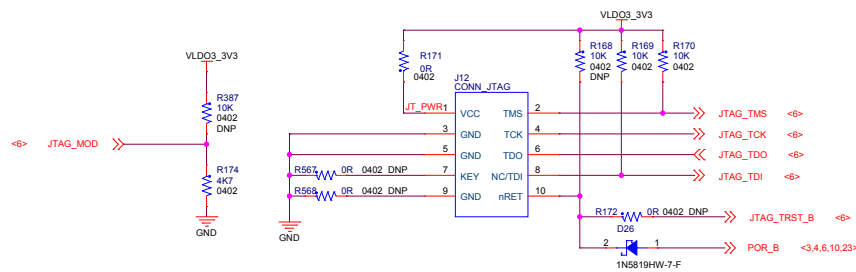


**ICAP Classification:** FCP: FUIO: PUBI: X  
**Drawing Title:** MCIMX7D-SABRE  
**Page Title:** 13 WiFi/BT  
**Size C** | **Document Number** SOURCE:SCH-28590-SPF-28590 | **Rev C**  
**Date:** Thursday, January 28, 2016 | **Sheet** 13 **of** 23

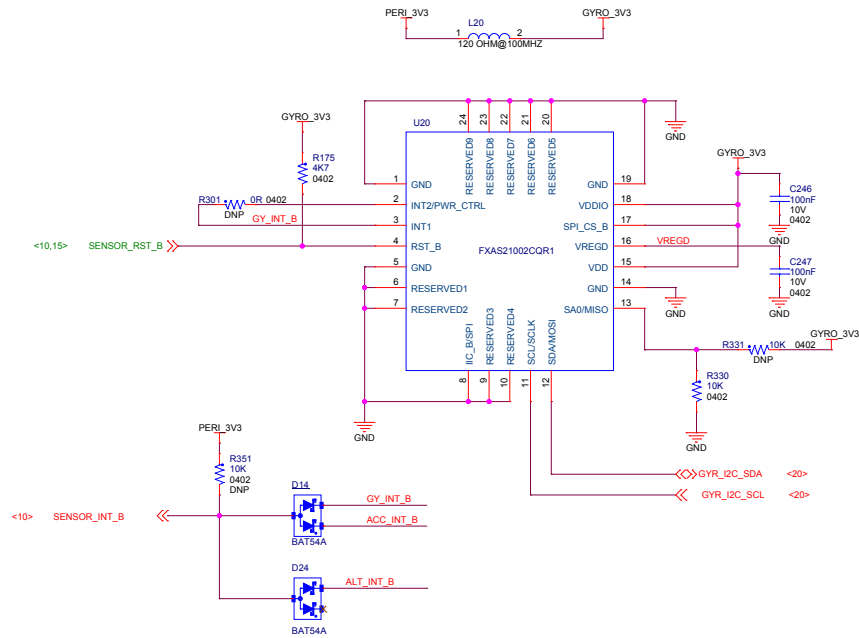
# DEBUG UART



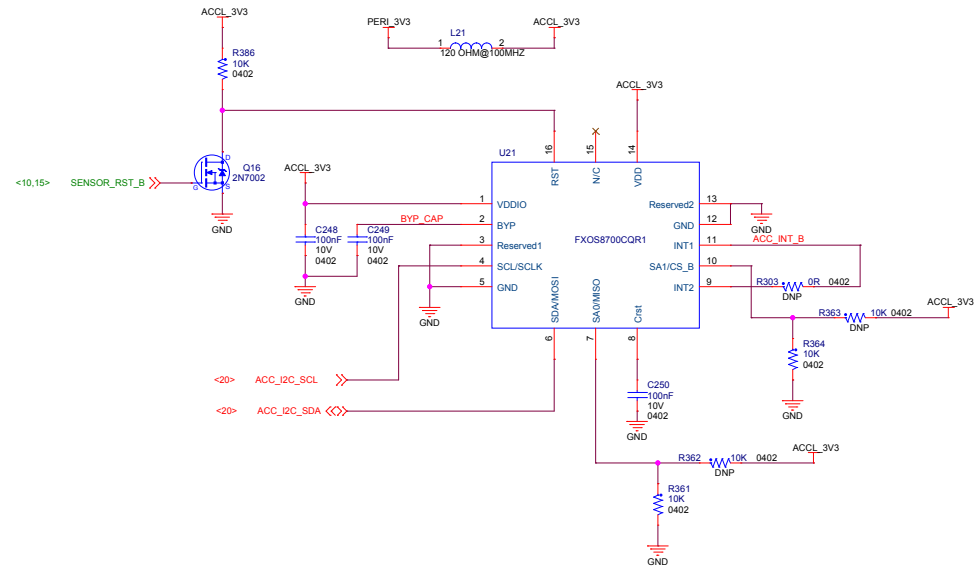
# JTAG



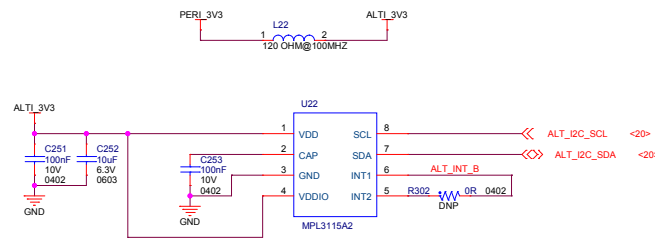
# Gyroscope



# Accelerometer & Magnetometer

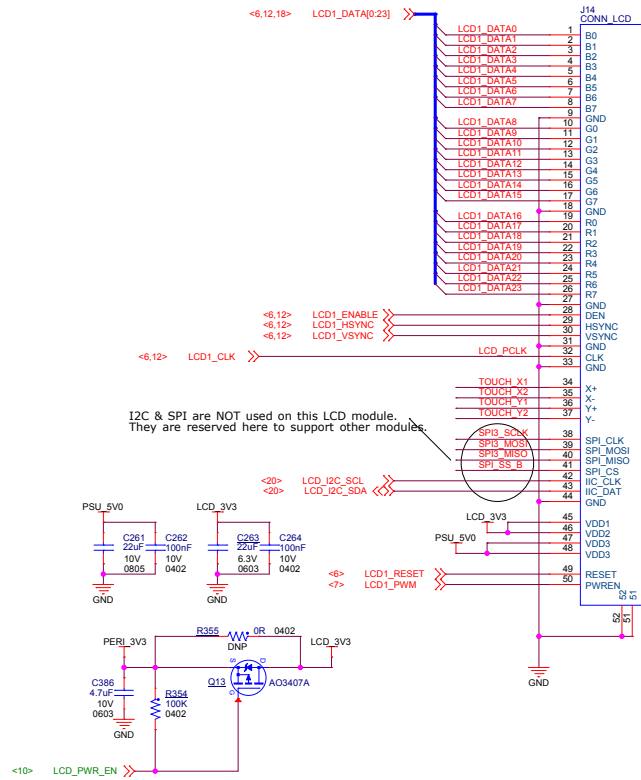


# Barometer/Altimeter



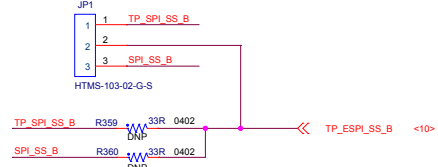
# LCD

LCD8000-43T from Embest

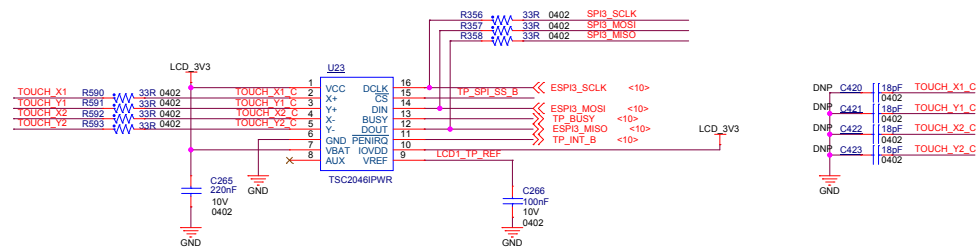
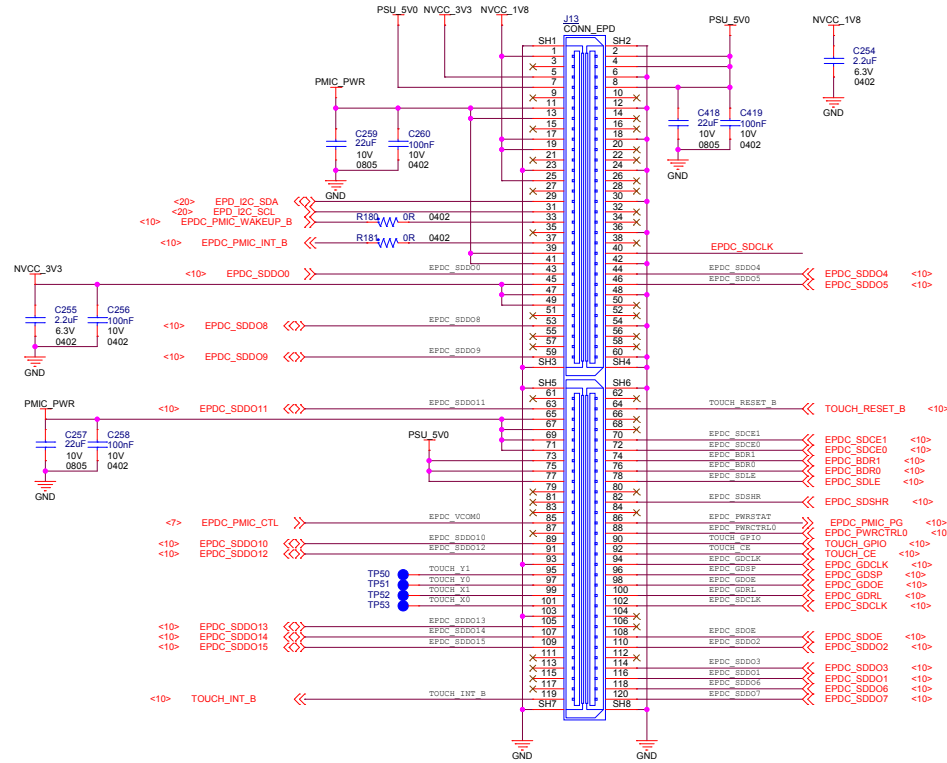


I2C & SPI are NOT used on this LCD module. They are reserved here to support other modules.

Note:  
TP\_SPI\_SS\_B default



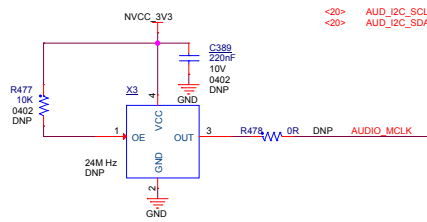
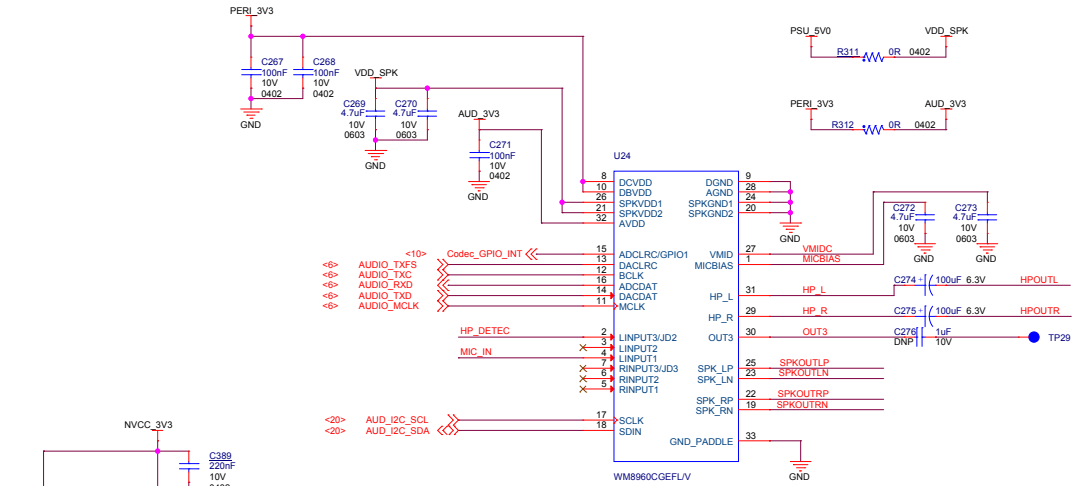
# EPD



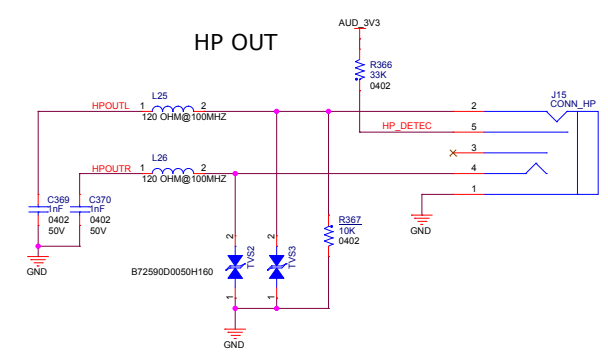
ICAP Classification: FCP: _____ FIUO: _____ PUBI: X			
<b>MCIMX7D-SABRE</b>			
Page Title: <b>16 LCD/EPD</b>			
Size C	Document Number SOURCE: SCH-28590-SPF-28590	Rev C	
Date: Thursday, January 28, 2016		Sheet 16 of 23	



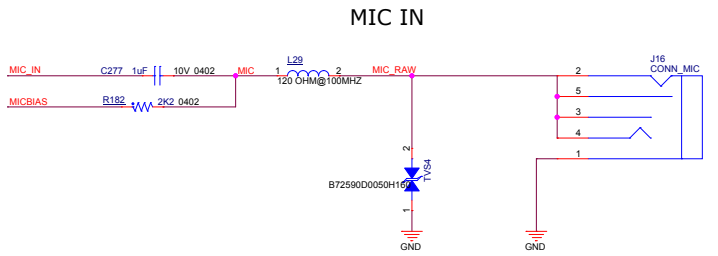
# AUDIO



Speaker Out



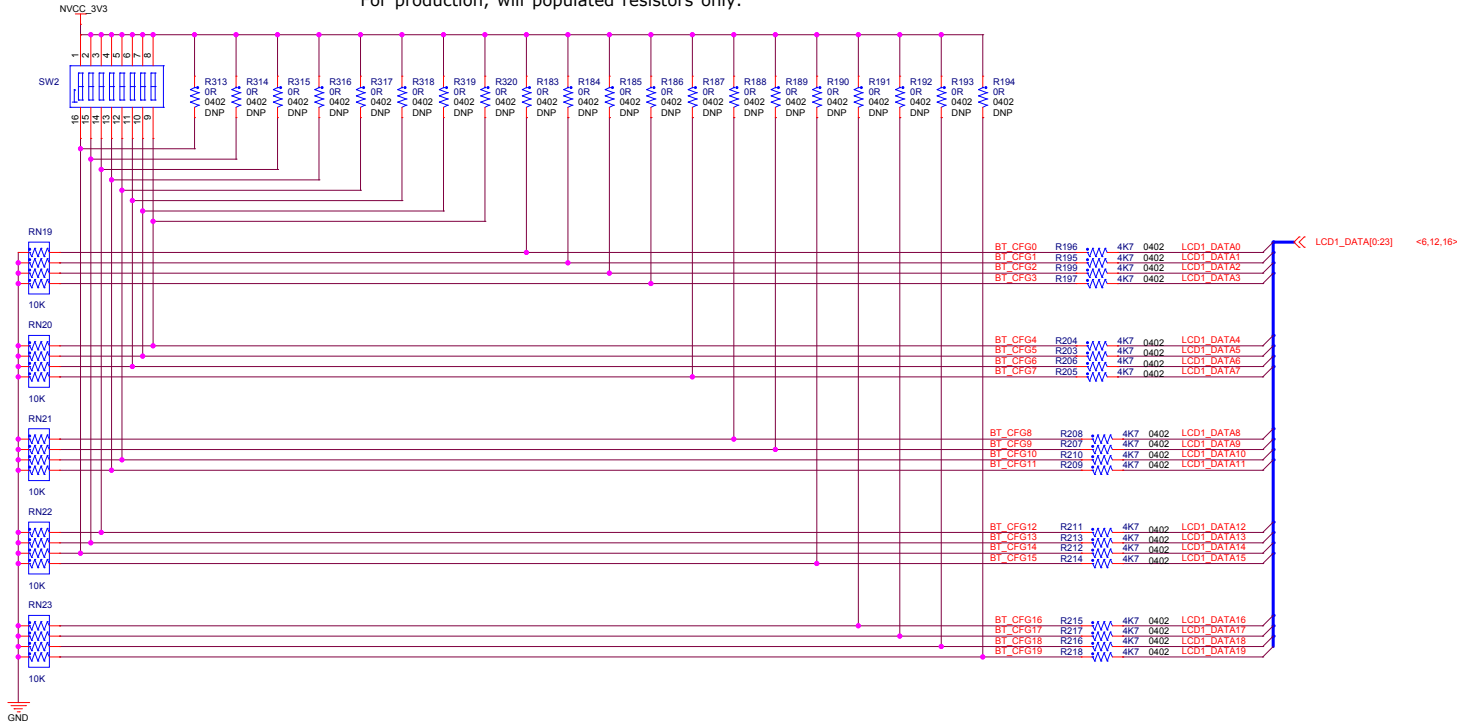
HP OUT



MIC IN

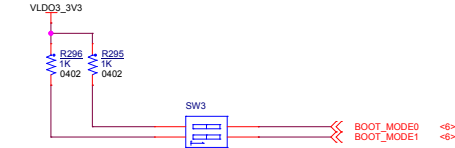
# Boot Config

SW2 will be populated on pro.  
For production, will populated resistors only.



# BOOT MODE

BOOT_MODE	[1]	[0]
FUSES	0	0
Serial Downloader	0	1
INTERNAL BOOT	1	0
TEST MODE	1	1

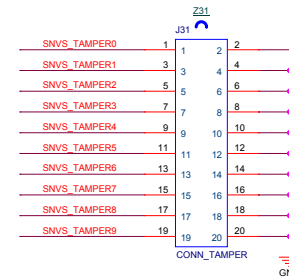
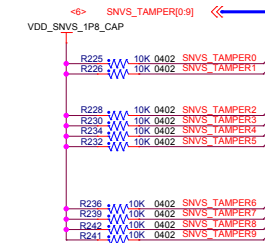


# BOOT TABLE

SW2

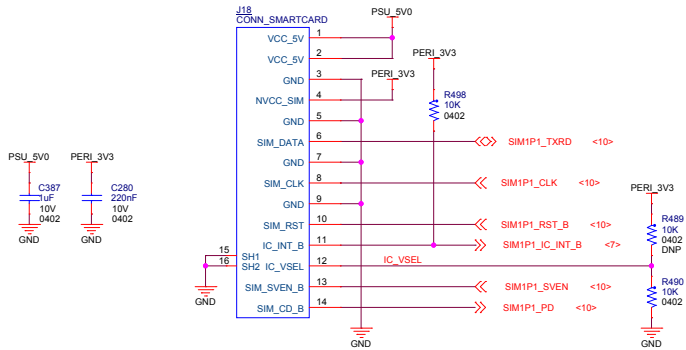
	1	2	3	4	5	6	7	8
	BT_CFG[14]	BT_CFG[13]	BT_CFG[12]	BT_CFG[11]	BT_CFG[10]	BT_CFG[6]	BT_CFG[5]	BT_CFG[4]
001 = SD/eSD Boot						0	0	Bus Width: 0 - 1-bit 1 - 4-bit
010 = MMC/eMMC Boot				Port Select: 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3				Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4)
011 = NAND Boot				Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		0
100 = QSPI Boot				0	0	0	0	0

# TAMPER



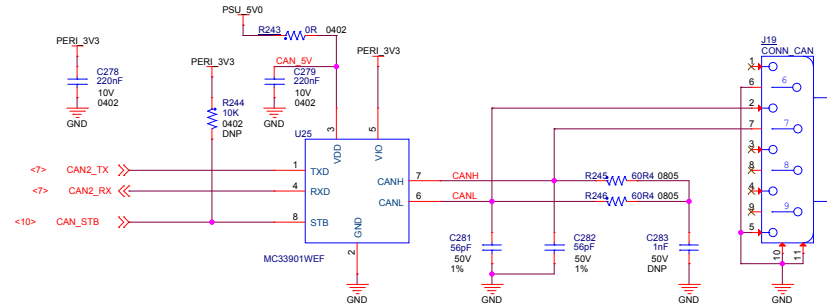
# ISO7816

Connector J18 is compatible with SCH-28609\_B.

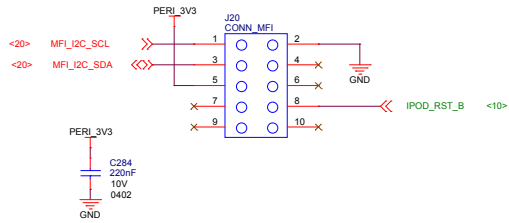


**Add a note:**  
**IC\_VSEL**  
**L: Card VCC = 3V**  
**H: Card VCC = 1.8V**

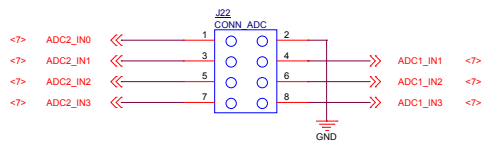
# CAN



# MFI

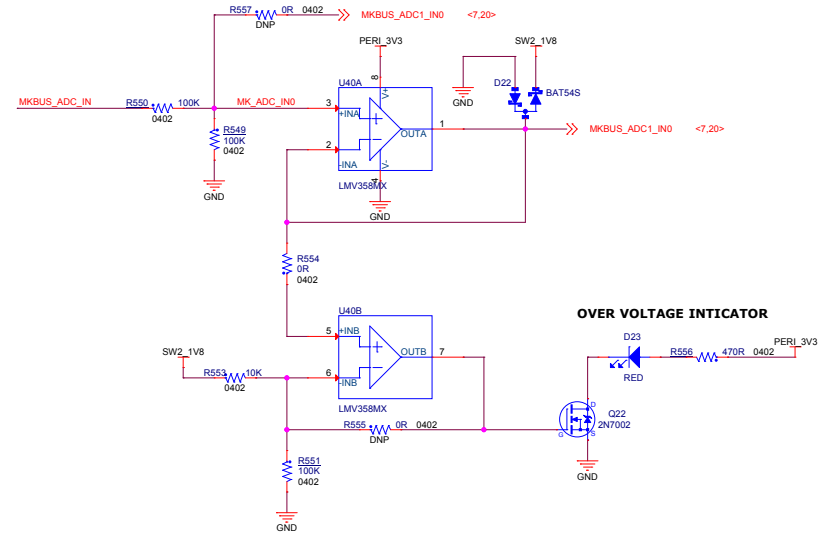
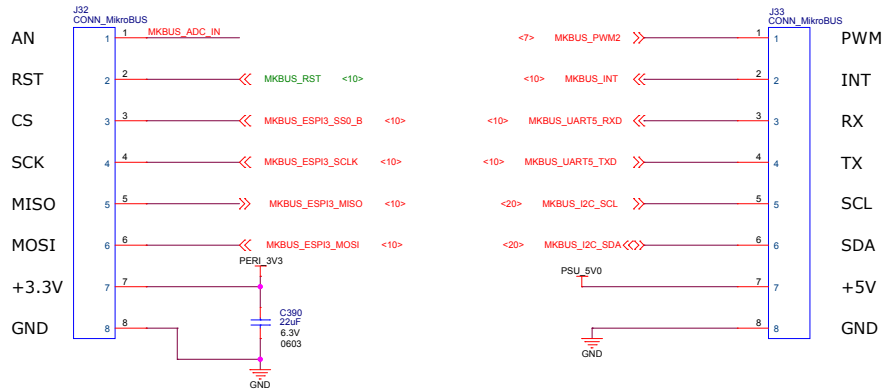


# ADC

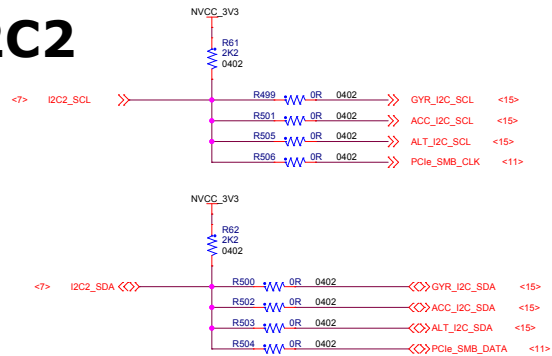


# MikroBUS

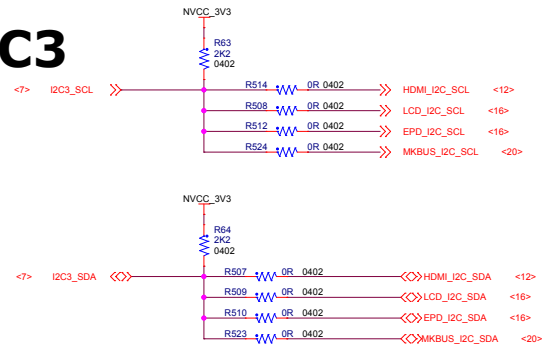
<http://www.mikroe.com/>



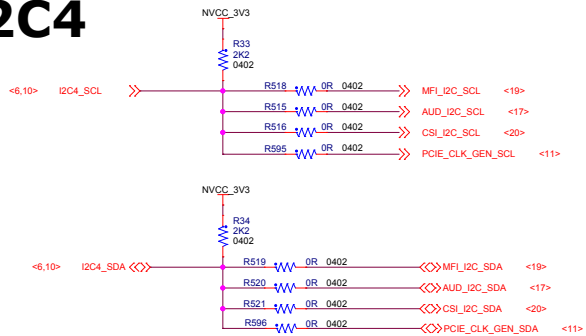
## I2C2



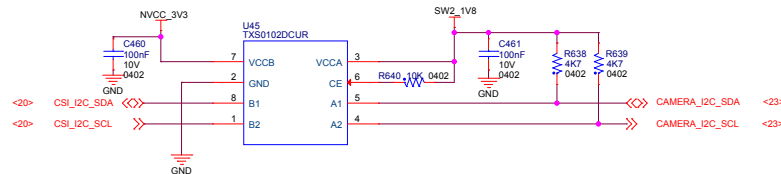
## I2C3



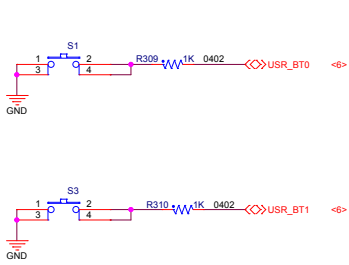
## I2C4



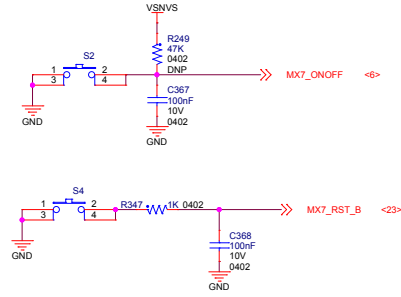
Note: Pull-up resistor must be sized to meet the signal rise times and also the V<sub>il</sub> spec of all the bus components. Due to board loadings this resistor was reduced. Validate your design, with the largest allowable resistor to reduce current consumption.



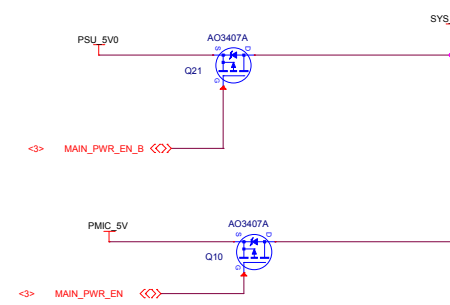
# User Button



# Power Botton

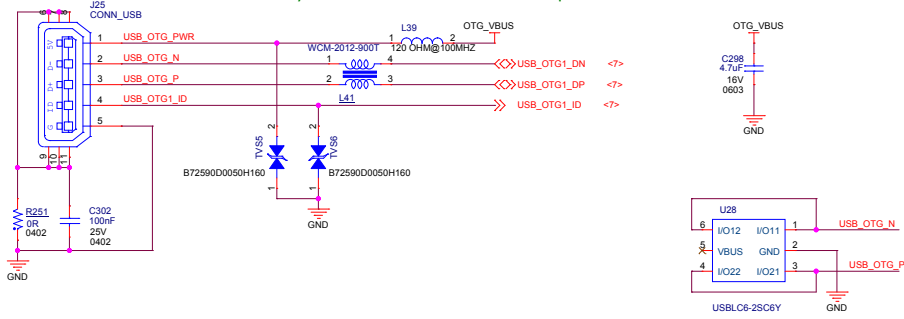


# 5V Power Switch



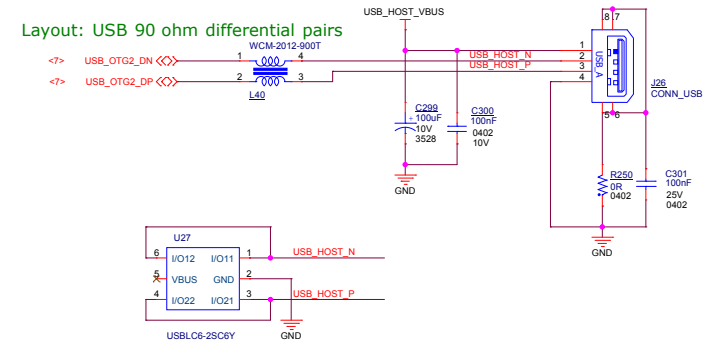
# USB OTG

Layout: USB 90 ohm differential pairs



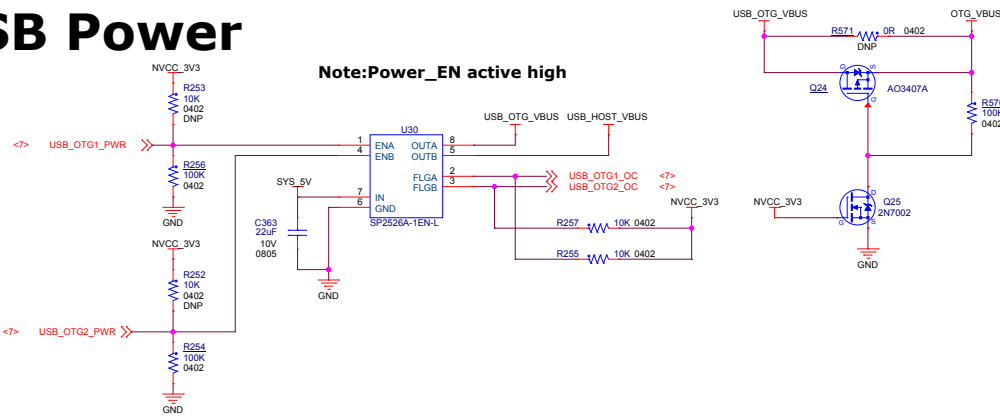
# USB HOST

Layout: USB 90 ohm differential pairs

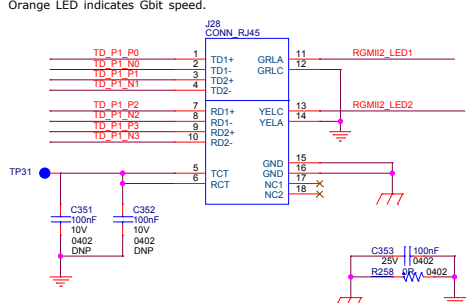
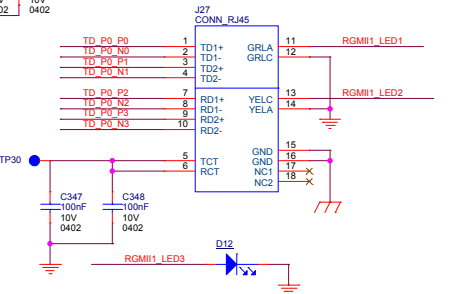
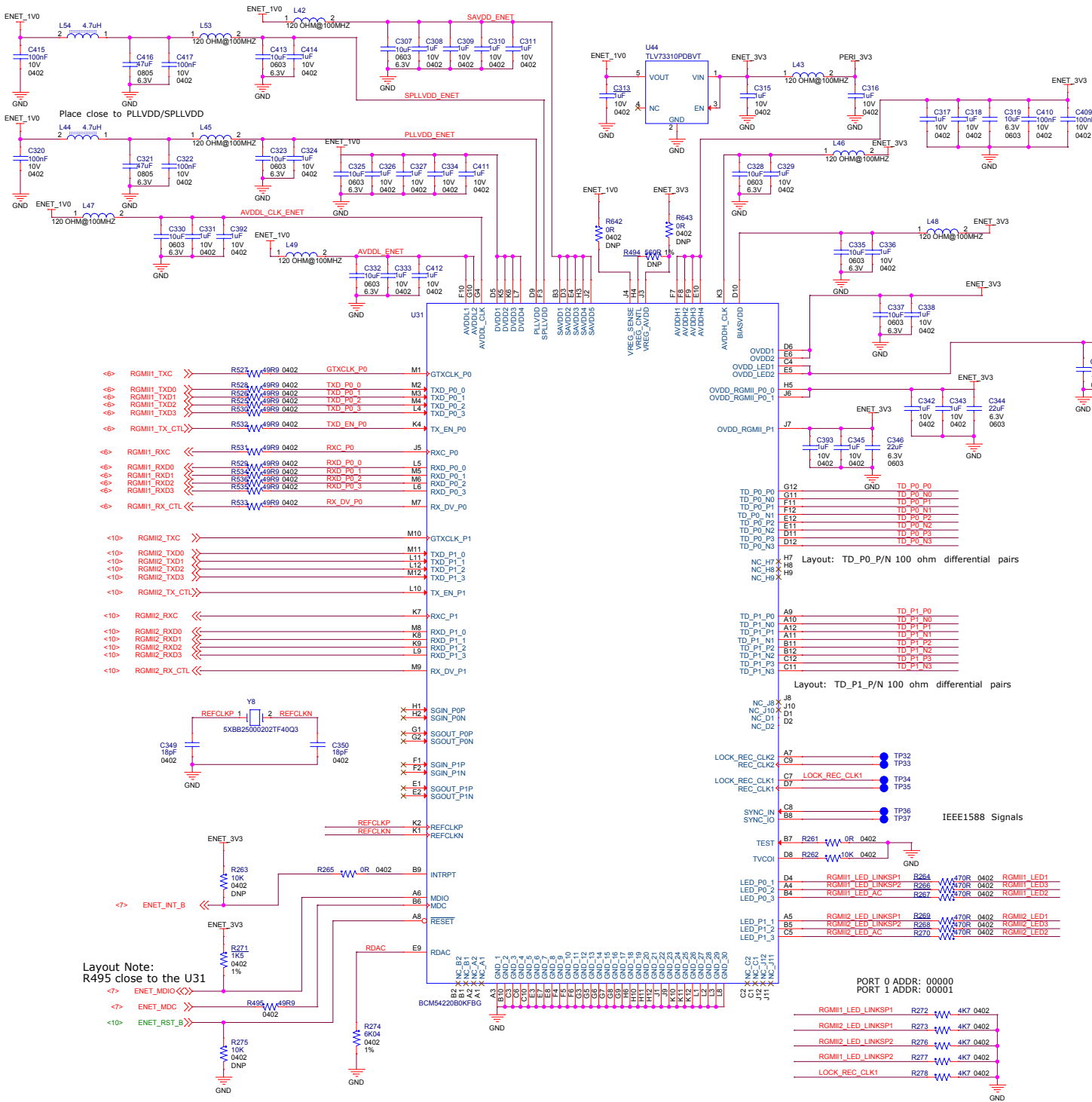


# USB Power

Note: Power\_EN active high



# Ethernet



Layout: TD\_P0\_P/N 100 ohm differential pairs

Layout: TD\_P1\_P/N 100 ohm differential pairs

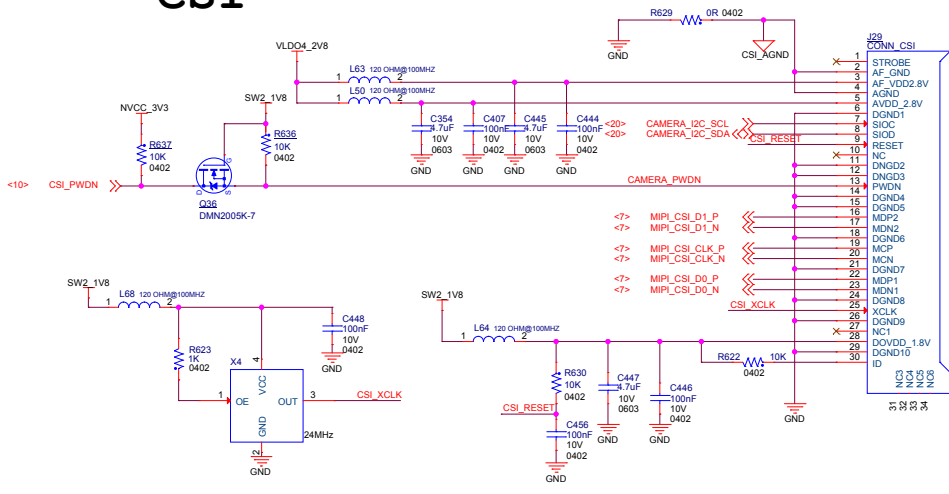
IEEE1588 Signals

PORT 0 ADDR: 00000  
PORT 1 ADDR: 00001

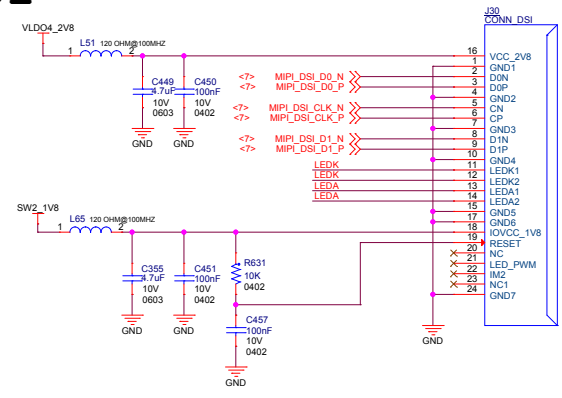
- RGMII\_LED\_LINKSP1 R272 4K7 0402
- RGMII2\_LED\_LINKSP1 R273 4K7 0402
- RGMII2\_LED\_LINKSP2 R276 4K7 0402
- RGMII\_LED\_LINKSP2 R277 4K7 0402
- LOCK\_REC\_CLK1 R278 4K7 0402



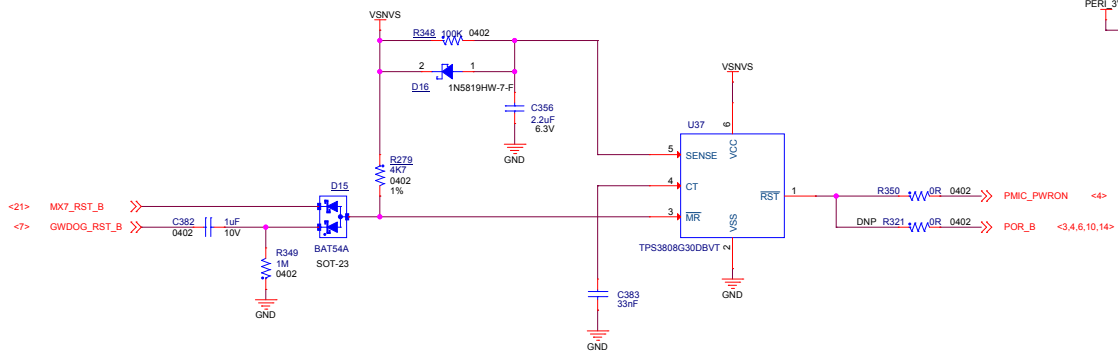
# CSI



# DSI

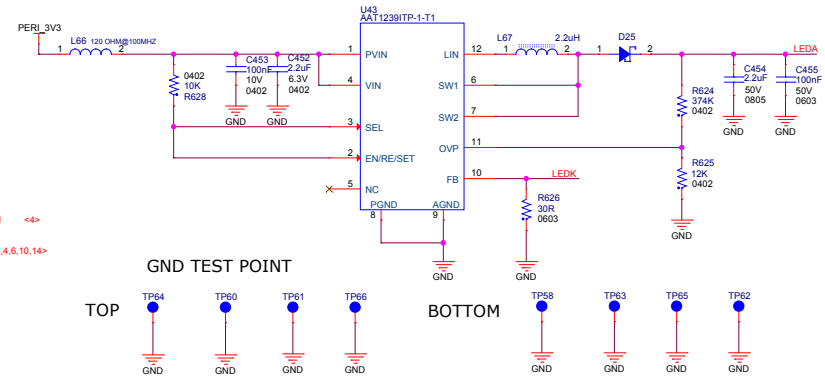


# WATCH DOG

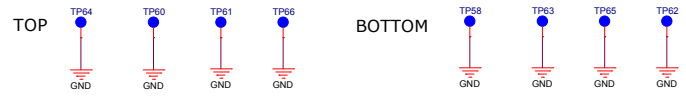


# LED BKL POWER

NOTE:  
Used R626=30R set the maximum led current is 20mA.



GND TEST POINT



**freescale**

ICAP Classification: FCP:\_\_\_ FIUO:\_\_\_ PUBI: X  
 Drawing Title: **MCIMX7D-SABRE**  
 Page Title: **23 DSI/CSI**  
 Size C Document Number SOURCE: SCH-28590-SPF-28590 Rev C  
 Date: Monday, February 01, 2016 Sheet 23 of 23