4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.11.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 68 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 68. Camera Input Signal Cross Reference, Format, and Bits Per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 2 cycles	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
IPUx_CSIx_DATA00	—	—	—	—	—	—	—	0	C[0]
IPUx_CSIx_DATA01	—	—	—	—	—	—	—	0	C[1]
IPUx_CSIx_DATA02	—	—	—	—	—	—	—	C[0]	C[2]
IPUx_CSIx_DATA03	—	—	—	—	—	—	—	C[1]	C[3]
IPUx_CSIx_DATA04	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
IPUx_CSIx_DATA05	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
IPUx_CSIx_DATA06	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
IPUx_CSIx_DATA07	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
IPUx_CSIx_DATA08	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
IPUx_CSIx_DATA09	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
IPUx_CSIx_DATA10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
IPUx_CSIx_DATA11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
IPUx_CSIx_DATA12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]

Table 68. Camera Input Signal Cross Reference, Format, and Bits Per Cycle (continued)

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 2 cycles	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
IPUx_CSIx_ DATA13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
IPUx_CSIx_ DATA14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
IPUx_CSIx_ DATA15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
IPUx_CSIx_ DATA16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
IPUx_CSIx_ DATA17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
IPUx_CSIx_ DATA18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
IPUx_CSIx_ DATA19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

1 IPUx_CSIx stands for IPUx_CSI0 or IPUx_CSI1

2 The MSB bits are duplicated on LSB bits implementing color extension

3 The two MSB bits are duplicated on LSB bits implementing color extension

4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).

5 RGB 16 bits— Supported in two ways: (1) As a “generic data” input, with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.

6 YCbCr 16 bits— Supported as a “generic-data” input, with no on-the-fly processing.

7 YCbCr 16 bits— Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).

8 YCbCr, 20 bits, supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.11.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.11.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the IPUx_CSIx_VSYNC and IPUx_CSIx_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is IPUx_CSIx_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering IPUx_CSIx_VSYNC and IPUx_CSIx_HSYNC signals for internal use. On BT.656 one component per cycle is received over the IPUx_CSIx_DATA_EN bus. On BT.1120 two components per cycle are received over the IPUx_CSIx_DATA_EN bus.