i.MX53 START Linux Reference Manual

Part Number: 924-76374
Rev. 1
09/2011

freescale™
semiconductor

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

ARM POWERED®

freescale™ semiconductor

About This Book

The Linux Board Support Package (BSP) represents a porting of the Linux Operating System (OS) to the i.MX processors and its associated reference boards. The BSP supports many hardware features on the platforms and most of the Linux OS features that are not dependent on any specific hardware feature.

Audience

This document is targeted to individuals who will port the i.MX Linux BSP to customer-specific products. The audience is expected to have a working knowledge of the Linux 2.6 kernel internals, driver models, and i.MX processors.

Conventions

This document uses the following notational conventions:

- `Courier monospaced type` indicate commands, command parameters, code examples, and file and directory names.
- *Italic* type indicates replaceable command or function parameters.
- **Bold** type indicates function names.

Definitions, Acronyms, and Abbreviations

The following table defines the acronyms and abbreviations used in this document.

Definitions and Acronyms

Term	Definition
ADC	Asynchronous Display Controller
address translation	Address conversion from virtual domain to physical domain
API	Application Programming Interface
ARM®	Advanced RISC Machines processor architecture
AUDMUX	Digital audio MUX—provides a programmable interconnection for voice, audio, and synchronous data routing between host serial interfaces and peripheral serial interfaces
BCD	Binary Coded Decimal
bus	A path between several devices through data lines
bus load	The percentage of time a bus is busy
CODEC	Coder/decoder or compression/decompression algorithm—used to encode and decode (or compress and decompress) various types of data
CPU	Central Processing Unit—generic term used to describe a processing core
CRC	Cyclic Redundancy Check—Bit error protection method for data communication
CSI	Camera Sensor Interface
DFS	Dynamic Frequency Scaling

Definitions and Acronyms (continued)

Term	Definition
DMA	Direct Memory Access—an independent block that can initiate memory-to-memory data transfers
DPM	Dynamic Power Management
DRAM	Dynamic Random Access Memory
DVFS	Dynamic Voltage Frequency Scaling
EMI	External Memory Interface—controls all IC external memory accesses (read/write/erase/program) from all the masters in the system
Endian	Refers to byte ordering of data in memory. Little endian means that the least significant byte of the data is stored in a lower address than the most significant byte. In big endian, the order of the bytes is reversed
EPIT	Enhanced Periodic Interrupt Timer—a 32-bit set and forget timer capable of providing precise interrupts at regular intervals with minimal processor intervention
FCS	Frame Checker Sequence
FIFO	First In First Out
FIPS	Federal Information Processing Standards—United States Government technical standards published by the National Institute of Standards and Technology (NIST). NIST develops FIPS when there are compelling Federal government requirements such as for security and interoperability but no acceptable industry standards
FIPS-140	Security requirements for cryptographic modules—Federal Information Processing Standard 140-2(FIPS 140-2) is a standard that describes US Federal government requirements that IT products should meet for Sensitive, but Unclassified (SBU) use
Flash	A non-volatile storage device similar to EEPROM, where erasing can be done only in blocks or the entire chip.
Flash path	Path within ROM bootstrap pointing to an executable Flash application
Flush	Procedure to reach cache coherency. Refers to removing a data line from cache. This process includes cleaning the line, invalidating its VBR and resetting the tag valid indicator. The flush is triggered by a software command
GPIO	General Purpose Input/Output
hash	Hash values are produced to access secure data. A hash value (or simply hash), also called a message digest, is a number generated from a string of text. The hash is substantially smaller than the text itself, and is generated by a formula in such a way that it is extremely unlikely that some other text produces the same hash value.
I/O	Input/Output
ICE	In-Circuit Emulation
IP	Intellectual Property
IPU	Image Processing Unit —supports video and graphics processing functions and provides an interface to video/still image sensors and displays
IrDA	Infrared Data Association—a nonprofit organization whose goal is to develop globally adopted specifications for infrared wireless communication
ISR	Interrupt Service Routine
JTAG	JTAG (IEEE Standard 1149.1) A standard specifying how to control and monitor the pins of compliant devices on a printed circuit board
Kill	Abort a memory access
KPP	KeyPad Port—16-bit peripheral used as a keypad matrix interface or as general purpose input/output (I/O)

Definitions and Acronyms (continued)

Term	Definition
line	Refers to a unit of information in the cache that is associated with a tag
LRU	Least Recently Used—a policy for line replacement in the cache
MMU	Memory Management Unit—a component responsible for memory protection and address translation
MPEG	Moving Picture Experts Group—an ISO committee that generates standards for digital video compression and audio. It is also the name of the algorithms used to compress moving pictures and video
MPEG standards	Several standards of compression for moving pictures and video: • MPEG-1 is optimized for CD-ROM and is the basis for MP3 • MPEG-2 is defined for broadcast video in applications such as digital television set-top boxes and DVD • MPEG-3 was merged into MPEG-2 • MPEG-4 is a standard for low-bandwidth video telephony and multimedia on the World-Wide Web
MQSPI	Multiple Queue Serial Peripheral Interface—used to perform serial programming operations necessary to configure radio subsystems and selected peripherals
MSHC	Memory Stick Host Controller
NAND Flash	Flash ROM technology—NAND Flash architecture is one of two flash technologies (the other being NOR) used in memory cards such as the Compact Flash cards. NAND is best suited to flash devices requiring high capacity data storage. NAND flash devices offer storage space up to 512-Mbyte and offers faster erase, write, and read capabilities over NOR architecture
NOR Flash	See NAND Flash
PCMCIA	Personal Computer Memory Card International Association—a multi-company organization that has developed a standard for small, credit card-sized devices, called PC Cards. There are three types of PCMCIA cards that have the same rectangular size (85.6 by 54 millimeters), but different widths
physical address	The address by which the memory in the system is physically accessed
PLL	Phase Locked Loop—an electronic circuit controlling an oscillator so that it maintains a constant phase angle (a lock) on the frequency of an input, or reference, signal
RAM	Random Access Memory
RAM path	Path within ROM bootstrap leading to the downloading and the execution of a RAM application
RGB	The RGB color model is based on the additive model in which Red, Green, and Blue light are combined to create other colors. The abbreviation RGB comes from the three primary colors in additive light models
RGBA	RGBA color space stands for Red Green Blue Alpha. The alpha channel is the transparency channel, and is unique to this color space. RGBA, like RGB, is an additive color space, so the more of a color placed, the lighter the picture gets. PNG is the best known image format that uses the RGBA color space
RNGA	Random Number Generator Accelerator—a security hardware module that produces 32-bit pseudo random numbers as part of the security module
ROM	Read Only Memory
ROM bootstrap	Internal boot code encompassing the main boot flow as well as exception vectors
RTIC	Real-Time Integrity Checker—a security hardware module
SCC	SeCurity Controller—a security hardware module
SDMA	Smart Direct Memory Access

Definitions and Acronyms (continued)

Term	Definition
SDRAM	Synchronous Dynamic Random Access Memory
SoC	System on a Chip
SPBA	Shared Peripheral Bus Arbiter—a three-to-one IP-Bus arbiter, with a resource-locking mechanism
SPI	Serial Peripheral Interface—a full-duplex synchronous serial interface for connecting low-/medium-bandwidth external devices using four wires. SPI devices communicate using a master/slave relationship over two data lines and two control lines: *Also see SS, SCLK, MISO, and MOSI*
SRAM	Static Random Access Memory
SSI	Synchronous-Serial Interface—standardized interface for serial data transfer
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter—asynchronous serial communication to external devices
UID	Unique ID–a field in the processor and CSF identifying a device or group of devices
USB	Universal Serial Bus—an external bus standard that supports high speed data transfers. The USB 1.1 specification supports data transfer rates of up to 12 Mb/s and USB 2.0 has a maximum transfer rate of 480 Mbps. A single USB port can be used to connect up to 127 peripheral devices, such as mice, modems, and keyboards. USB also supports Plug-and-Play installation and hot plugging
USBOTG	USB On The Go—an extension of the USB 2.0 specification for connecting peripheral devices to each other. USBOTG devices, also known as dual-role peripherals, can act as limited hosts or peripherals themselves depending on how the cables are connected to the devices, and they also can connect to a host PC
word	A group of bits comprising 32-bits

Suggested Reading

The following documents contain information that supplements this guide:

- i.MX53 Multimedia Applications Processor Reference Manual

Contents

Contents

Contents

Contents

Contents

Contents

Contents

Contents

Contents

Chapter 29
Security Drivers

Contents

Contents

Contents

Figures

Figures

Figure Number	Title	Page Number

Tables

Tables

Chapter 1
Introduction

The i.MX family Linux Board Support Package (BSP) supports the Linux Operating System (OS) on the following processor:

- i.MX53 Applications Processor

The purpose of this software package is to support Linux on the i.MX family of Integrated Circuits (ICs) and their associated platforms (START). It provides the necessary software to interface the standard open-source Linux kernel to the i.MX hardware. The goal is to enable Freescale customers to rapidly build products based on i.MX devices that use the Linux OS.

The BSP is not a platform or product reference implementation. It does not contain all of the product-specific drivers, hardware-independent software stacks, Graphical User Interface (GUI) components, Java Virtual Machine (JVM), and applications required for a product. Some of these are made available in their original open-source form as part of the base kernel.

The BSP is not intended to be used for silicon verification. While it can play a role in this, the BSP functionality and the tests run on the BSP do not have sufficient coverage to replace traditional silicon verification test suites.

1.1 Software Base

The i.MX BSP is based on version 2.6.35 of the Linux kernel from the official Linux kernel web site (http://www.kernel.org). It is enhanced with the features provided by Freescale.

1.2 Features

Table 1-1 describes the features supported by the Linux BSP for specific platforms.

Table 1-1. Linux BSP Supported Features

Feature	Description	Chapter Source	Applicable Platform
Machine Specific Layer			
MSL	Machine Specific Layer (MSL) supports interrupts, Timer, Memory Map, GPIO/IOMUX, SPBA, SDMA. • Interrupts (AITC/AVIC): The Linux kernel contains common ARM code for handling interrupts. The MSL contains platform-specific implementations of functions for interfacing the Linux kernel to the interrupt controller. • Timer (GPT): The General Purpose Timer (GPT) is set up to generate an interrupt as programmed to provide OS ticks. Linux facilitates timer use through various functions for timing delays, measurement, events, alarms, high resolution timer features, and so on. Linux defines the MSL timer API required for the OS-tick timer and does not expose it beyond the kernel tick implementation. • GPIO/EDIO/IOMUX: The GPIO and EDIO components in the MSL provide an abstraction layer between the various drivers and the configuration and utilization of the system, including GPIO, IOMUX, and external board I/O. The IO software module is board-specific, and resides in the MSL layer as a self-contained set of files. I/O configuration changes are centralized in the GPIO module so that changes are not required in the various drivers. • SPBA: The Shared Peripheral Bus Arbiter (SPBA) provides an arbitration mechanism among multiple masters to allow access to the shared peripherals. The SPBA implementation under MSL defines the API to allow different masters to take or release ownership of a shared peripheral.	Chapter 2, “Machine Specific Layer (MSL)”	All
SDMA API	The Smart Direct Memory Access (SDMA) API driver controls the SDMA hardware. It provides an API to other drivers for transferring data between MCU, DSP and peripherals. The SDMA controller is responsible for transferring data between the MCU memory space, peripherals, and the DSP memory space. The SDMA API allows other drivers to initialize the scripts, pass parameters and control their execution. SDMA is based on a microRISC engine that runs channel-specific scripts.	Chapter 3, “Smart Direct Memory Access (SDMA) API”	i.MX53

Table 1-1. Linux BSP Supported Features (continued)

Feature	Description	Chapter Source	Applicable Platform
Power Management Drivers			
Low-level PM Drivers	The low-level power management driver is responsible for implementing hardware-specific operations to meet power requirements and also to conserve power on the development platforms. Driver implementations are often different for different platforms. It is used by the DPM layer.	”Chapter 19, “Low-level Power Management (PM) Driver”	i.MX53
CPU Frequency Scaling	The CPU frequency scaling device driver allows the clock speed of the CPUs to be changed on the fly.	Chapter 21, “CPU Frequency Scaling (CPUFREQ) Driver”	i.MX53
DVFS	The Dynamic Voltage Frequency Scaling (DVFS) device driver allows simple dynamic voltage frequency scaling. The frequency of the core clock domain and the voltage of the core power domain can be changed on the fly with all modules continuing their normal operations.	Chapter 20, “Dynamic Voltage Frequency Scaling (DVFS) Driver”	i.MX53
DA9053	This chapter introduces the information about PMIC DA9053	Chapter 5, “DA9053 PMIC Driver	i.MX53
Multimedia Drivers			
IPU	The Image Processing Unit (IPU) is designed to support video and graphics processing functions and to interface with video/still image sensors and displays. The IPU driver is a self-contained driver module in the Linux kernel. It contains a custom kernel-level API to manipulate logical channels. A logical channel represents a complete IPU processing flow. The IPU driver includes a frame buffer driver, a V4L2 device driver, and low-level IPU drivers.	Chapter 10, “Image Processing Unit (IPU) Drivers”	i.MX53
TVE	This driver provides the support of i.MX TVE modules.	Chapter 11, “TV encoder (TVE) Driver”	i.MX53
VGA	This driver provides the support of i.MX VGA module.	Chapter 12, “TVE-VGA Driver”	i.MX53
HDMI	This driver provides the support of SII902x HDMI chip.	Chapter 13, “HDMI Driver”	i.MX53
Dual Display	This chapter introduces the basic infromation about dual display	Chapter 14, “i.MX5 Dual Display”	i.MX53
V4L2 Output	The Video for Linux 2 (V4L2) output driver uses the IPU post-processing functions for video output. The driver implements the standard V4L2 API for output devices.	Chapter 15, “Video for Linux Two (V4L2) Driver”	i.MX53
VPU	The Video Processing Unit (VPU) is a multi-standard video decoder and encoder that can perform decoding and encoding of various video formats.	Chapter 18, “Video Processing Unit (VPU) Driver”	i.MX53
AMD GPU	The Graphics Processing Unit (GPU) is a graphics accelerator targeting embedded 2D/3D graphics applications.	Chapter 16, “Graphics Processing Unit (GPU)”	i.MX53

Table 1-1. Linux BSP Supported Features (continued)

Feature	Description	Chapter Source	Applicable Platform
X-Windows	This chapter introduces X-Window support on i.MX5	Chapter 17, “X Windows Acceleration	i.MX53
Sound Drivers			
ALSA Sound	The Advanced Linux Sound Architecture (ALSA) is a sound driver that provides ALSA and OSS compatible applications with the means to perform audio playback and recording functions. ALSA has a user-space component called ALSAlib that can extend the features of audio hardware by emulating the same in software (user space), such as resampling, software mixing, snooping, and so on. The ASoC Sound driver supports stereo codec playback and capture through SSI.	Chapter 23, “Advanced Linux Sound Architecture (ALSA) System on a Chip (ASoC) Sound Driver”	i.MX53
S/PDIF	The S/PDIF driver is designed under the Linux ALSA subsystem. It implements one playback device for Tx and one capture device for Rx.	Chapter 24, “The Sony/Philips Digital Interface (S/PDIF) Driver”	i.MX53
Memory Drivers			
SATA	The SATA AHCI driver is based on the LIBATA layer of the block device infrastructure of the Linux kernel	Chapter 26, “SATA Driver”	i.MX53
Input Device Drivers			
Networking Drivers			
FEC	The FEC Driver performs the full set of IEEE 802.3/Ethernet CSMA/CD media access control and channel interface functions. The FEC requires an external interface adaptor and transceiver function to complete the interface to the Ethernet media. It supports half or full-duplex operation on 10 Mbps- or 100 Mbps-related Ethernet networks.	Chapter 30, “Fast Ethernet Controller (FEC) Driver”	i.MX53
Bus Drivers			
I^2C	The I^2C bus driver is a low-level interface that is used to interface with the I^2C bus. This driver is invoked by the I^2C chip driver; it is not exposed to the user space. The standard Linux kernel contains a core I^2C module that is used by the chip driver to access the bus driver to transfer data over the I^2C bus. This bus driver supports: • Compatibility with the I^2C bus standard • Bit rates up to 400 Kbps • Standard I^2C master mode • Power management features by suspending and resuming I^2C.	Chapter 31, “Inter-IC (I2C) Driver”	i.MX53

Table 1-1. Linux BSP Supported Features (continued)

Feature	Description	Chapter Source	Applicable Platform
CSPI	The low-level Configurable Serial Peripheral Interface (CSPI) driver interfaces a custom, kernel-space API to both CSPI modules. It supports the following features: • Interrupt-driven transmit/receive of SPI frames • Multi-client management • Priority management between clients • SPI device configuration per client	Chapter 32, "Configurable Serial Peripheral Interface (CSPI) Driver"	i.MX53
MMC/SD/SDIO - eSDHC	The MMC/SD/SDIO Host driver implements the standard Linux driver interface to eSDHC.	Chapter 27, "MMC/SD/SDIO Host Driver"	i.MX53
UART Drivers			
MXC UART	The Universal Asynchronous Receiver/Transmitter (UART) driver interfaces the Linux serial driver API to all of the UART ports. A kernel configuration parameter gives the user the ability to choose the UART driver and also to choose whether the UART should be used as the system console.	Chapter 4, "Universal Asynchronous Receiver/Transmitter (UART) Driver"	i.MX53
General Drivers			
USB	The USB driver implements a standard Linux driver interface to the ARC USB-OTG controller.	Chapter 9, "ARC USB Driver"	i.MX53
SRTC	The SRTC driver is designed to support MXC Secure RTC module to keep the time and date	Chapter 33, "Secure Real Time Clock (SRTC) Driver"	i.MX53
WatchDog	The Watchdog Timer module protects against system failures by providing an escape from unexpected hang or infinite loop situations or programming errors. This WDOG implements the following features: • Generates a reset signal if it is enabled but not serviced within a predefined time-out value • Does not generate a reset signal if it is serviced within a predefined time-out value	Chapter 34, "Watchdog (WDOG) Driver"	i.MX53
MXC PWM driver	The MXC PWM driver provides the interfaces to access MXC PWM signals	Chapter 36, "Pulse-Width Modulator (PWM) Driver"	i.MX53
Accelerometer	This chapter describe MMA8450 Accelerometer driver.	Chapter 37, "MMA8451 Accelerometer Driver	i.MX53
Bootloaders			
uBoot	uBoot is an open source boot loader.	See uBoot User guide.	i.MX53
GUI			
OProfile	OProfile is a system-wide profiler for Linux systems, capable of profiling all running code at low overhead.	Chapter 37, "OProfile"	i.MX53

Chapter 2
Machine Specific Layer (MSL)

The Machine Specific Layer (MSL) provides the Linux kernel with the following machine-dependent components:

- Interrupts including GPIO
- Timer
- Memory map
- General Purpose Input/Output (GPIO) including IOMUX
- Smart Direct Memory Access (SDMA)
- Direct Memory Access (DMA)

These modules are normally available in the following directory:

```
<ltib_dir>/rpm/BUILD/linux/arch/arm/mach-mx5 for MX5 platform
```

The header files are implemented under the following directory:

```
<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/include/mach
```

The MSL layer contains not only the modules common to all the boards using the same processor, such as the interrupts and timer, but it also contains modules specific to each board, such as the memory map. The following sections describe the basic hardware and software operation and the software interfaces for MSL modules. First, the common modules, such as Interrupts and Timer are discussed. Next, the board-specific modules, such as Memory Map and General Purpose Input/Output (GPIO) (including IOMUX) are detailed. Because of the complexity of the SDMA module, its design is explained in Chapter 3, “Smart Direct Memory Access (SDMA) API.”

Each of the following sections contains an overview of the hardware operation. For more information, see the corresponding device documentation.

2.1 Interrupts

The following sections explain the hardware and software operation of interrupts on the device.

2.1.1 Interrupt Hardware Operation

The Interrupt Controller controls and prioritizes a maximum of 128 internal and external interrupt sources. Each source can be enabled or disabled by configuring the Interrupt Enable Register or using the Interrupt Enable/Disable Number Registers. When an interrupt source is enabled and the corresponding interrupt source is asserted, the Interrupt Controller asserts a normal or a fast interrupt request depending on the associated Interrupt Type Register setting.

Interrupt Controller registers can only be accessed in supervisor mode. The Interrupt Controller interrupt requests are prioritized in the order of fast interrupts, and normal interrupts in order of highest priority level, then highest source number with the same priority. There are sixteen normal interrupt levels for all interrupt sources, with level zero being the lowest priority. The interrupt levels are configurable through

eight normal interrupt priority level registers. Those registers, along with the Normal Interrupt Mask Register, support software-controlled priority levels for normal interrupts and priority masking.

2.1.2 Interrupt Software Operation

For ARM-based processors, normal interrupt and fast interrupt are two different exception types. The exception vector addresses can be configured to start at low address (`0x0`) or high address (`0xFFFF0000`). The ARM Linux implementation chooses the high vector address model.

The following file has a description of the ARM interrupt architecture.

```
<ltib_dir>/rpm/BUILD/linux/Documentation/arm/Interrupts
```

The software provides a processor-specific interrupt structure with callback functions defined in the `irq_chip` structure and exports one initialization function, which is called during system startup.

2.1.3 Interrupt Features

The interrupt implementation supports the following features:

- Interrupt Controller interrupt disable and enable
- Functions required by the Linux interrupt architecture as defined in the standard ARM interrupt source code (mainly the `<ltib_dir>/rpm/BUILD/linux/arch/arm/kernel/irq.c` file)

2.1.4 Interrupt Source Code Structure

The interrupt module is implemented in the following file:

```
<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/tzic.c
```

There are also two header files (located in the include directory specified at the beginning of this chapter):

```
hardware.h
irqs.h
```

Table 2-1 lists the source files for interrupts.

Table 2-1. Interrupt Files

File	Description
hardware.h	Register descriptions
irqs.h	Declarations for number of interrupts supported
tzic.c	Actual interrupt functions for TZIC modules

2.1.5 Interrupt Programming Interface

The machine-specific interrupt implementation exports a single function. This function initializes the Interrupt Controller hardware and registers functions for interrupt enable and disable from each interrupt source. This is done with the global structure `irq_desc` of type `struct irq_desc`. After the initialization,

the interrupt can be used by the drivers through the `request_irq()` function to register device-specific interrupt handlers.

In addition to the native interrupt lines supported from the Interrupt Controller, the number of interrupts is also expanded to support GPIO interrupt. This allows drivers to use the standard interrupt interface supported by ARM Linux, such as the `request_irq()` and `free_irq()` functions.

2.2 Timer

The Linux kernel relies on the underlying hardware to provide support for both the system timer (which generates periodic interrupts) and the dynamic timers (to schedule events). After the system timer interrupt occurs, it does the following:

- Updates the system uptime
- Updates the time of day
- Reschedules a new process if the current process has exhausted its time slice
- Runs any dynamic timers that have expired
- Updates resource usage and processor time statistics

The timer hardware on most i.MX platforms consists of either Enhanced Periodic Interrupt Timer (EPIT) or general purpose timer (GPT) or both. GPT is configured to generate a periodic interrupt at a certain interval (every 10 ms) and is used by the Linux kernel.

2.2.1 Timer Hardware Operation

The General Purpose Timer (GPT) has a 32 bit up-counter. The timer counter value can be captured in a register using an event on an external pin. The capture trigger can be programmed to be a rising or falling edge. The GPT can also generate an event on `ipp_do_cmpout` pins, or can produce an interrupt when the timer reaches a programmed value. It has a 12-bit prescaler providing a programmable clock frequency derived from multiple clock sources.

2.2.2 Timer Software Operation

The timer software implementation provides an initialization function that initializes the GPT with the proper clock source, interrupt mode and interrupt interval. The timer then registers its interrupt service routine and starts timing. The interrupt service routine is required to service the OS for the purposes mentioned in Section 2.2, “Timer.” Another function provides the time elapsed as the last timer interrupt.

2.2.3 Timer Features

The timer implementation supports the following features:

- Functions required by Linux to provide the system timer and dynamic timers.
- Generates an interrupt every 10 ms.

2.2.4 Timer Source Code Structure

The timer module is implemented in the `arch/arm/plat-mxc/time.c` file.

2.3 Memory Map

A predefined virtual-to-physical memory map table is required for the device drivers to access to the device registers since the Linux kernel is running under the virtual address space with the Memory Management Unit (MMU) enabled.

2.3.1 Memory Map Hardware Operation

The MMU, as part of the ARM core, provides the virtual to physical address mapping defined by the page table. For more information, see the *ARM Technical Reference Manual* (TRM) from ARM Limited.

2.3.2 Memory Map Software Operation

A table mapping the virtual memory to physical memory is implemented for i.MX platforms as defined in the `<ltib_dir>/rpm/BUILD/linux/arch/arm/mach-mx5/mm.c` file.

2.3.3 Memory Map Features

The Memory Map implementation programs the Memory Map module to creates the physical to virtual memory map for all the I/O modules.

2.3.4 Memory Map Source Code Structure

The Memory Map module implementation is in `mm.c` under the platform-specific MSL directory. The `hardware.h` header file is used to provide macros for all the IO module physical and virtual base addresses and physical to virtual mapping macros. All of the memory map source code is in the in the following directories:

```
<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/include/mach
<ltib_dir>/rpm/BUILD/linux/arch/arm/mach-mx5
```

Table 2-2 lists the source file for the memory map.

Table 2-2. Memory Map Files

File	Description
mm.c	Memory map definition file

2.3.5 Memory Map Programming Interface

The Memory Map is implemented in the `mm.c` file to provide the map between physical and virtual addresses. It defines an initialization function to be called during system startup.

2.4 IOMUX

The limited number of pins of highly integrated processors can have multiple purposes. The IOMUX module controls a pin usage so that the same pin can be configured for different purposes and can be used by different modules. This is a common way to reduce the pin count while meeting the requirements from various customers. Platforms that do not have the IOMUX hardware module can do pin muxing through the GPIO module.

The IOMUX module provides the multiplexing control so that each pin may be configured either as a functional pin or as a GPIO pin. A functional pin can be subdivided into either a primary function or alternate functions. The pin operation is controlled by a specific hardware module. A GPIO pin, is controlled by the user through software with further configuration through the GPIO module. For example, the `UART1_TXD` pin might have the following functions:

- `UART1_TXD`–internal UART1 Transmit Data. This is the primary function of this pin.
- `GPIO6[6]`—alternate mode 1
- `USBPHY1 DATAOUT[14]`—alternate mode 7

If the hardware modes are chosen at the system integration level, this pin is dedicated only to that purpose and cannot be changed by software. Otherwise, the IOMUX module needs to be configured to serve a particular purpose that is dictated by the system (board) design. If the pin is connected to an external UART transceiver and therefore to be used as the UART data transmit signal, it should be configured as the primary function. If the pin is connected to an external Ethernet controller for interrupting the ARM core, then it should be configured as GPIO input pin with interrupt enabled. Again, be aware that the software does not have control over what function a pin should have. The software only configures pin usage according to the system design.

2.4.1 IOMUX Hardware Operation

The IOMUX controller registers are briefly described here. For detailed information, refer to the pin multiplexing section of the IC Reference Manual.

- SW_MUX_CTL—Selects the primary or alternate function of a pin. Also enables loopback mode when applicable.
- SW_SELECT_INPUT—Controls pin input path. This register is only required when multiple pads drive the same internal port.
- SW_PAD_CTL—Control pad slew rate, driver strength, pull-up/down resistance, and so on.

2.4.2 IOMUX Software Operation

The IOMUX software implementation provides an API to set up pin functionality and pad features.

2.4.3 IOMUX Features

The IOMUX implementation programs the IOMUX module to configure the pins that are supported by the hardware.

2.4.4 IOMUX Source Code Structure

Table 2-3 lists the source files for the IOMUX module. The files are in the directory:

`<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc`

Table 2-3. IOMUX Files

File	Description
iomux-v3.c	IOMUX function implementation
include/mach/iomux-mx53.h	Pin definitions in the iomux pins

2.4.5 IOMUX Programming Interface

The IOMUX API is in arch/arm/plat-mxc/include/mach/iomux-v3.h. Read the comments at the head of this file to understand the iomux scheme.

2.5 General Purpose Input/Output (GPIO)

The GPIO module provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, the pin state (high or low) can be controlled by writing to an internal register. When configured as an input, the pin input state can be read from an internal register.

2.5.1 GPIO Software Operation

The general purpose input/output (GPIO) module provides an API to configure the i.MX processor external pins and a central place to control the GPIO interrupts.

The GPIO utility functions should be called to configure a pin instead of directly accessing the GPIO registers. The GPIO interrupt implementation contains functions, such as the interrupt service routine (ISR) registration/un-registration and ISR dispatching once an interrupt occurs. All driver-specific GPIO setup functions should be made during device initialization in the MSL layer to provide better portability and maintainability. This GPIO interrupt is initialized automatically during the system startup.

If a pin is configured as GPIO by the IOMUX, the state of the pin should also be set since it is not initialized by a dedicated hardware module.

2.5.1.1 API for GPIO

The GPIO implementation supports the following features:

- An API for registering an interrupt service routine to a GPIO interrupt. This is made possible as the number of interrupts defined by `NR_IRQS` is expanded to accommodate all the possible GPIO pins that are capable of generating interrupts. The macro `IOMUX_TO_IRQ_V3()` or `gpio_to_irq()` is used to convert GPIO pin to irq number,
- Functions to set an IOMUX pin, named `mxc_iomux_v3_setup_pad()`. If a pin is used as GPIO, another set of request/free function calls are provided, named `gpio_request()` and `gpio_free()`. The user should check the return value of the request calls to see if the pin has already been

reserved before modifying the pin state. The free function calls should be made when the pin is not needed. Furthermore, functions `gpio_direction_input()` and `gpio_direction_output()` are provided to set GPIO when it's used as input or output. See the API document and `Documentation/gpio.txt` for more details.

2.5.2 GPIO Features

This GPIO implementation supports the following features:

- Implements the functions for accessing the GPIO hardware modules
- Provides a way to control GPIO signal direction and GPIO interrupts

2.5.3 GPIO Source Code Structure

GPIO driver is implemented based on general gpiolib framework. The MSL-layer codes defines and registers gpio_chip instances for each bank of on-chip GPIOs, in the following files, located in the directories indicated at the beginning of this chapter:

Table 2-4. GPIO Files

File	Description
gpio.h	GPIO public header file
gpio.c	Function implementation

2.5.4 GPIO Programming Interface

For more information, see the API documents and `Documentation/gpio.txt` for the programming interface.

Chapter 3
Smart Direct Memory Access (SDMA) API

3.1 Overview

The Smart Direct Memory Access (SDMA) API driver controls the SDMA hardware. It provides an API to other drivers for transferring data between MCU memory space and the peripherals. It supports the following features:

- Loading channel scripts from the MCU memory space into SDMA internal RAM
- Loading context parameters of the scripts
- Loading buffer descriptor parameters of the scripts
- Controlling execution of the scripts
- Callback mechanism at the end of script execution

3.2 Hardware Operation

The SDMA controller is responsible for transferring data between the MCU memory space and peripherals and includes the following features.

- Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels
- Powered by a 16-bit Instruction-Set microRISC engine
- Each channel executes specific script
- Very fast context-switching with two-level priority based preemptive multi-tasking
- 4 Kbytes ROM containing startup scripts (that is, boot code) and other common utilities that can be referenced by RAM-located scripts
- 8 Kbyte RAM area is divided into a processor context area and a code space area used to store channel scripts that are downloaded from the system memory.

3.3 Software Operation

The driver provides an API for other drivers to control SDMA channels. SDMA channels run dedicated scripts, according to peripheral and transfer types. The SDMA API driver is responsible for loading the scripts into SDMA memory, initializing the channel descriptors, and controlling the buffer descriptors and SDMA registers.

Complete support for SDMA is provided in three layers (see Figure):

- I.API
- Linux DMA API
- TTY driver or DMA-capable drivers, such as ATA, SSI and the UART driver.

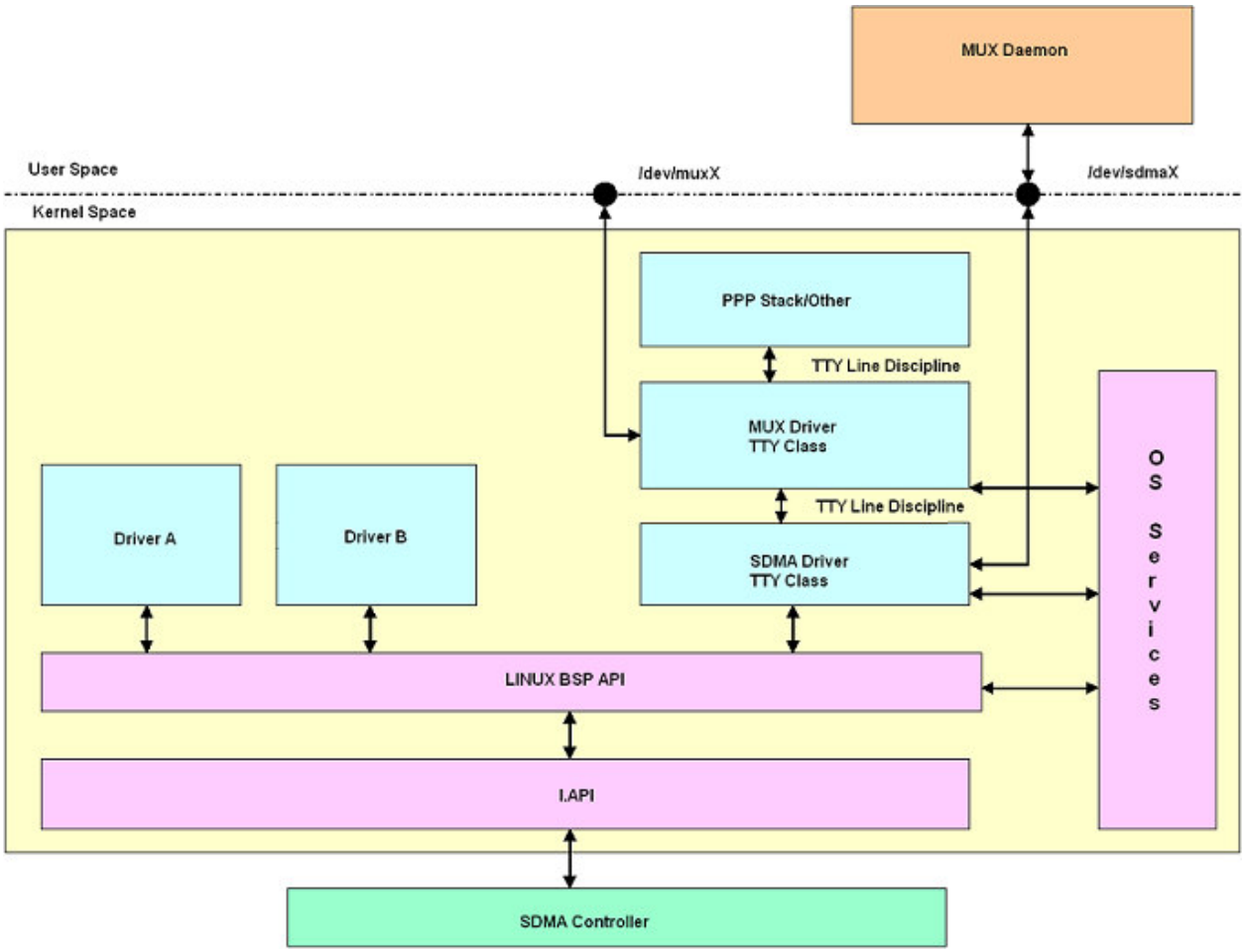


Figure 3-1. SDMA Block Diagram

The first two layers are part of the MSL and customized for each platform. I.API is the lowest layer and it interfaces with the Linux DMA API with the SDMA controller. The Linux DMA API interfaces other drivers (for example, MMC/SD, Sound) with the SDMA controller through the I.API.

Table 3-1 provides a list of drivers that use SDMA and the number of SDMA physical channels used by each driver. A driver can specify the SDMA channel number that it wishes to use (static channel allocation) or can have the SDMA driver provide a free SDMA channel for the driver to use (dynamic channel allocation). For dynamic channel allocation, the list of SDMA channels is scanned from channel 32 to channel 1. On finding a free channel, that channel is allocated for the requested DMA transfers.

Table 3-1. SDMA Channel Usage

Driver Name	Number of SDMA Channels	SDMA Channel Used
SDMA CMD	1	Static Channel allocation—uses SDMA channels 0
SSI	2 per device	Dynamic channel allocation

Table 3-1. SDMA Channel Usage (continued)

Driver Name	Number of SDMA Channels	SDMA Channel Used
UART	2 per device	Dynamic channel allocation
SPDIF	2 per device	Dynamic channel allocation

3.4 Source Code Structure

The source file, `sdma.h` (header file for SDMA API) is available in the directory `/<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/include/mach`.

Table 3-2 shows the source files available in the directory, `/<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/sdma`.

Table 3-2. SDMA API Source Files

File	Description
sdma.c	SDMA API functions
sdma_malloc.c	SDMA functions to get memory that allows DMA
iapi/	iAPI source files

Table 3-3 shows the header files available in the directory, `/<ltib_dir>/rpm/BUILD/linux/arch/arm/mach-mx5/`.

Table 3-3. SDMA Script Files

File	Description
sdma_script_code_mx53.h	SDMA RAM scripts

3.5 Menu Configuration Options

The following Linux kernel configuration option is provided for this module. To get to this options, use the `./ltib -c` command when located in the `<ltib dir>`. On the screen displayed, select **Configure the Kernel** and exit. When the next screen appears, select the following option to enable this module:

- CONFIG_MXC_SDMA_API—This is the configuration option for the SDMA API driver. In menuconfig, this option is available under

  System type > Freescale MXC implementations > MX5x Options: > Use SDMA API.

  By default, this option is Y.
- CONFIG_SDMA_IRAM—This is the configuration option to support Internal RAM as SDMA buffer or control structures. This option is available under System type > Freescale MXC implementations > MX5x Options > Use Internal RAM for SDMA transfer.

3.6 Programming Interface

The module implements custom API and partially standard DMA API. Custom API is needed for supporting non-standard DMA features such as loading scripts, interrupts handling and DVFS control. Standard API is supported partially. It can be used along with custom API functions only. Refer to the API document for more information on the functions implemented in the driver (in the doxygen folder of the documentation package).

3.7 Usage Example

Refer to one of the drivers from Table 3-1 that uses the SDMA API driver for a usage example.

Chapter 4
Universal Asynchronous Receiver/Transmitter (UART) Driver

The low-level UART driver interfaces the Linux serial driver API to all the UART ports. It has the following features:

- Interrupt-driven and SDMA-driven transmit/receive of characters
- Standard Linux baud rates up to 4 Mbps
- Transmit and receive characters with 7-bit and 8-bit character lengths
- Transmits one or two stop bits
- Supports `TIOCMGET` IOCTL to read the modem control lines. Only supports the constants `TIOCM_CTS` and `TIOCM_CAR`, plus `TIOCM_RI` in `DTE` mode only
- Supports `TIOCMSET` IOCTL to set the modem control lines. Supports the constants `TIOCM_RTS` and `TIOCM_DTR` only
- Odd and even parity
- XON/XOFF software flow control. Serial communication using software flow control is reliable when communication speeds are not too high and the probability of buffer overruns is minimal
- CTS/RTS hardware flow control—both interrupt-driven software-controlled hardware flow and hardware-driven hardware-controlled flow
- Send and receive break characters through the standard Linux serial API
- Recognizes frame and parity errors
- Ability to ignore characters with break, parity and frame errors
- Get and set UART port information through the `TIOCGSSERIAL` and `TIOCSSERIAL` TTY IOCTL. Some programs like `setserial` and `dip` use this feature to make sure that the baud rate was set properly and to get general information on the device. The UART type should be set to 52 as defined in the `serial_core.h` header file.
- Serial IrDA
- Power management feature by suspending and resuming the URT ports
- Standard TTY layer IOCTL calls

All the UART ports can be accessed through the device files `/dev/ttymxc0` through `/dev/ttymxc4`, where `/dev/ttymxc0` refers to UART 1. Autobaud detection is not supported.

4.1 Hardware Operation

Refer to the *i.MX53 Multimedia Applications Processor Reference Manual* to determine the number of UART modules available in the device. Each UART hardware port is capable of standard RS-232 serial communication and has support for IrDA 1.0. Each UART contains a 32-byte transmitter FIFO and a 32-half-word deep receiver FIFO. Each UART also supports a variety of maskable interrupts when the data level in each FIFO reaches a programmed threshold level and when there is a change in state in the modem signals. Each UART can be programmed to be in DCE or DTE mode.

4.2 Software Operation

The Linux OS contains a core UART driver that manages many of the serial operations that are common across UART drivers for various platforms. The low-level UART driver is responsible for supplying information such as the UART port information and a set of control functions to this core UART driver. These functions are implemented as a low-level interface between the Linux OS and the UART hardware. They cannot be called from other drivers or from a user application. The control functions used to control the hardware are passed to the core driver through a structure called `uart_ops`, and the port information is passed through a structure called `uart_port`. The low level driver is also responsible for handling the various interrupts for the UART ports, and providing console support if necessary.

Each UART can be configured to use DMA for the data transfer. These configuration options are provided in the `mxc_uart.h` header file. The user can specify the size of the DMA receive buffer. The minimum size of this buffer is 512 bytes. The size should be a multiple of 256. The driver breaks the DMA receive buffer into smaller sub-buffers of 256 bytes and registers these buffers with the DMA system. The DMA transmit buffer size is fixed at 1024 bytes. The size is limited by the size of the Linux UART transmit buffer (1024).

The driver requests two DMA channels for the UARTs that need DMA transfer. On a receive transaction, the driver copies the data from the DMA receive buffer to the TTY Flip Buffer.

While using DMA to transmit, the driver copies the data from the UART transmit buffer to the DMA transmit buffer and sends this buffer to the DMA system. The user should use hardware-driven hardware flow control when using DMA data transfer. For more information, see the Linux documentation on the serial driver in the kernel source tree.

The low-level driver supports both interrupt-driven software-controlled hardware flow control and hardware-driven hardware flow control. The hardware flow control method can be configured using the options provided in the header file. The user has the capability to de-assert the CTS line using the available IOCTL calls. If the user wishes to assert the CTS line, then control is transferred back to the receiver, as long as the driver has been configured to use hardware-driven hardware flow control.

4.3 Driver Features

The UART driver supports the following features:

- Baud rates up to 4 Mbps
- Recognizes frame and parity errors only in interrupt-driven mode; does not recognize these errors in DMA-driven mode
- Sends, receives, and appropriately handles break characters
- Recognizes the modem control signals
- Ignores characters with frame, parity, and break errors if requested to do so
- Implements support for software and hardware flow control (software-controlled and hardware-controlled)
- Get and set the UART port information; certain flow control count information is not available in hardware-driven hardware flow control mode
- Implements support for Serial IrDA

- Power management
- Interrupt-driven and DMA-driven data transfer

4.4 Source Code Structure

Table 4-1 shows the UART driver source files that are available in the directory:
`<ltib_dir>/rpm/BUILD/linux/drivers/serial`.

Table 4-1. UART Driver Files

File	Description
mxc_uart.c	Low level driver
serial_core.c	Core driver that is included as part of standard Linux
mxc_uart_reg.h	Register values
mxc_uart_early.c	Source file to support early serial console for UART

Table 4-2 shows the header files associated with the UART driver.

Table 4-2. UART Global Header Files

File	Description
<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/include/mach/mxc_uart.h	UART header that contains UART configuration data structure definitions

The source files, `serial.c and serial.h`, are associated with the UART driver that is available in the directory: `<ltib_dir>/rpm/BUILD/linux/arch/arm/mach-mx5` The source file contains UART configuration data and calls to register the device with the platform bus.

4.5 Configuration

This section discusses configuration options associated with Linux, chip configuration options, and board configuration options.

4.5.1 Menu Configuration Options

The following Linux kernel configuration options are provided for this module. To get to these options, use the `./ltib -c` command when located in the `<ltib dir>`. On the screen displayed, select **Configure the Kernel** and exit. When the next screen appears, select the following options to enable this module:

- CONFIG_SERIAL_MXC—Used for the UART driver for the UART ports. In menuconfig, this option is available under

  Device Drivers > Character devices > Serial drivers > MXC Internal serial port support.

  By default, this option is Y.
- CONFIG_SERIAL_MXC_CONSOLE—Chooses the Internal UART to bring up the system console. This option is dependent on the CONFIG_SERIAL_MXC option. In the menuconfig this option is available under

Device Drivers > Character devices > Serial drivers > MXC Internal serial port support > Support for console on a MXC/MX27/MX21 Internal serial port.

By default, this option is Y.

4.5.2 Source Code Configuration Options

This section details the chip configuration options and board configuration options.

4.5.2.1 Chip Configuration Options

The chip-specific configuration options are provided in
`<ltib_dir>/rpm/BUILD/linux/arch/arm/mach-mx5/serial.c`

4.5.2.2 Board Configuration Options

For *i.MX53*, the board specific configuration options for the driver is set within
`<ltib_dir>/rpm/BUILD/linux/arch/arm/mach-mx5/serial.h`

4.6 Programming Interface

The UART driver implements all the methods required by the Linux serial API to interface with the UART port. The driver implements and provides a set of control methods to the Linux core UART driver. For more information about the methods implemented in the driver, see the API document.

4.7 Interrupt Requirements

The UART driver interface generates many kinds of interrupts. The highest interrupt rate is associated with transmit and receive interrupt.

The system requirements are listed in Table 4-3.

Table 4-3. UART Interrupt Requirements

Parameter	Equation	Typical	Worst Case
Rate	(BaudRate/(10))*(1/Rxtl + 1/(32–Txtl))	5952/sec	300000/sec
Latency	320/BaudRate	5.6 ms	213.33 µs

The baud rate is set in the `mxcuart_set_termios` function. The typical values are based on a baud rate of 57600 with a receiver trigger level (Rxtl) of one and a transmitter trigger level (Txtl) of two. The worst case is based on a baud rate of 1.5 Mbps (maximum supported by the UART interface) with an Rxtl of one and a Txtl of 31. There is also an undetermined number of handshaking interrupts that are generated but the rates should be an order of magnitude lower.

Chapter 5
DA9053 PMIC Driver

The DA9053 PMIC driver for Linux provides support for controlling the PMIC multi-function device. This device drivers contain a core MFD (multi-function device) protocol driver and a set of sub device drivers.

5.1 Hardware information

The DA9053 PMIC provides SPI/I2C bus and a dedicated IRQ line to communicate with the host CPU. The main features including:

- Switched DC/USB Charger with power path management
- 4 Buck Converters (3 have DVS)
- 10 Programmable LDO
- Low power Backup Charger
- 32 kHz RTC Oscillator
- 10 channel General Purpose ADC with touch screen interface
- High voltage white LED driver
- 16 bit GPIO bus
- Dual serial control interfaces
- Unique USB supply detection and charge current selection

See DA9053 specs for more details.

5.2 Software Drivers

The PMIC driver implements a MFD class device driver for register access and event notifications. Each sub module is registered as a sub-device of the MFD core device and implemented under different driver model classes.

The DA9053 driver is intergrated from the Dialog-LKML-Source-Code.tar.gz release from Dialog. Inc.

- Porting and intergration are done for different MX53 board powered by DA9053.

Two suspend solutions are provided which are dependent on HW signal connections:

- A software suspend solution can be deployed for DA9053 suspend operation. It is implemented via a standalone polling-mode i2c interface to preset the voltage of DA9053 deep sleep mode. It also issues the DEEP_SLEEP command to DA9053. See the implementation “da9053_suspend_cmd_sw” under arch/arm/mach-mx5/pm_da9053.c. With this solution, only power key which is connected to NONKEY_KEEP_ACT signal can wakeup the system. The detailed flow for DA9053 hardware suspend solutin is like:
  - Enable DA9053 IRQ as the unique wakeup source.
  - In pm_da9053_preset_voltage: Set R46~R59 Registers bit7 to enable power and configure the following LDOs when suspend:

  - Set R46 as 0.85V buckcore for VDDGP
  - Set R47 as 0.95V buckpro for VCC
  - Set R55 as 1.2V LDO6
  - Set R59 as 1.2V LDO10
  - Set BUCKPERI 2.5V for VUSB
- Set power sequencer: Clear R29 bit[0:1] to disable reset mode and default supply for OTP. Add power down delay by set R42 MAX_COUNT to max value.
- Set R15 bit6 to enter DEEPSLEEP mode.
- Enter Suspend by calling suspend_in_iram
- Press power key to resume the system
- Set R35 and R60 to restore VUSB 2.5V

- A hardware suspend solution can be deployed for DA9053 suspend operation. See the function “da9053_suspend_cmd_hw” under arch/arm/mach-mx5/pm_da9053.c for the details. For HW solution, please ensure the right DA9053 chip is used. With this solution, all CPU interrupts can be used as wakeup resources.The detailed flow for DA9053 hardware suspend solutin is like:
  - In pm_da9053_preset_voltage, Set R46~R59 Registers bit7 to enable power and configure the following LDOs when suspend:
    - Set R46 as 0.85V buckcore for VDDGP
    - Set R47 as 0.95V buckpro for VCC
    - Set R55 as 1.2V LDO6
    - Set R59 as 1.2V LDO10
    - Set BUCKPERI 2.5V for VUSB
  - Set R25 to configure GPIO08 as SYS_EN, GPIO9 as GPI, and set R13 to mask GPI9_IRQ
  - Set R36 buckcore_step as 1 and R43 seq_time as 0 to prepare power sequencer
  - Enter Suspend by calling suspend_in_iram
  - Enable any wakeup IRQ to resume the system
  - Set R35 and R60 to restore VUSB 2.5V

5.3 Source code structure

Table 5-1 lists the source files for DA9053 PMIC driver:

Table 5-1. DA9053 PMIC Driver Source Files

Directory	File	Description
include/linux/mfd/da9052/	*.h	header files for mfd sub-devices
drivers/gpio/	da9052-gpio.c	driver source for DA9053 gpio
drivers/hwmon/	da9052-adc.c	driver source for DA9053 adc
drivers/input/misc/	da9052_onkey.c	driver source for DA9053 power key

Table 5-1. DA9053 PMIC Driver Source Files

Directory	File	Description
drivers/input/touchscreen/	da9052_tsi.c	driver source for DA9053 touch screen
drivers/leds/	leds-da9052.c	driver source for DA9053 led
drivers/mfd/	da9052-core.c da9052-i2c.c da9052-spi.c	driver source for DA9053 core
drivers/power/	da9052-battery.c	driver source for DA9053 battery charger
drivers/regulator/	da9052-regulator.c	driver source for DA9053 regulator
drivers/rtc/	rtc-da9052.c	driver source for DA9053 RTC
drivers/video/backlight/	da9052_bl.c	driver source for DA9053 backlight
drivers/watchdog/	da9052_wdt.c	driver source for DA9053 watchdog
arch/arm/mach-mx5/	pm_da9053.c	suspend routine for DA9053

Note: The source get from Dialog is upgraded from the DA9052 driver code. So the device naming is remained as DA9052.

5.4 Menu Configuration Options

To get to the PMIC device driver, use the command `./ltib -c` when located in the `<ltib dir>`. In the screen displayed, select **Configure Kernel** and exit. When the next screen appears, select the following options to enable the PMIC device driver.

To enable: Dialog DA9052 with SPI/I2C

select: PMIC_DA9052

Depends on: MFD_SUPPORT [=y] && SPI_MASTER [=y] && I2C [=y]=y [=y]

Location:

-> Device Drivers

-> Multifunction device drivers (MFD_SUPPORT [=y])

Selects: MFD_CORE [=y]

To enable: Dialog DA9052 GPIO

Depends on: GPIOLIB [=y] && PMIC_DA9052 [=y]

Location:

-> Device Drivers

-> GPIO Support (GPIOLIB [=y])

select: DA9052_GPIO_ENABLE

To enable: Dialog DA9052 WLED

select: BACKLIGHT_DA9052

Depends on: HAS_IOMEM [=y] && BACKLIGHT_LCD_SUPPORT [=y] && BACKLIGHT_CLASS_DEVICE [=y] && PMIC_DA9052 [=y]

Location:

-> Device Drivers

-> Graphics support

-> Backlight & LCD device support (BACKLIGHT_LCD_SUPPORT [=y])

-> Lowlevel Backlight controls (BACKLIGHT_CLASS_DEVICE [=y])

To enable: Dialog DA9052 TSI

select: TOUCHSCREEN_DA9052

Depends on: !S390 [=S390] && INPUT [=y] && INPUT_TOUCHSCREEN [=y] && PMIC_DA9052 [=y]

Location:

-> Device Drivers

-> Input device support

-> Generic input layer (needed for keyboard, mouse, ...) (INPUT [=y])

-> Touchscreens (INPUT_TOUCHSCREEN [=y])

To enable: Dialog DA9052 Battery

select: BATTERY_DA9052

Depends on: POWER_SUPPLY [=y] && PMIC_DA9052 [=y]

Location:

-> Device Drivers

-> Power supply class support (POWER_SUPPLY [=y])

To enable: Dialog DA9052 HWMon

select: SENSORS_DA9052

Depends on: HWMON [=y] && PMIC_DA9052 [=y]

Location:

-> Device Drivers

-> Hardware Monitoring support (HWMON [=y])

To enable: Dialog DA9052 regulators

select: REGULATOR_DA9052

Depends on: REGULATOR [=y] && PMIC_DA9052 [=y]

Location:

-> Device Drivers

-> Voltage and Current Regulator Support (REGULATOR [=y])

To enable: Dialog DA9052 RTC

select: RTC_DRV_DA9052

Depends on: RTC_CLASS [=y] && PMIC_DA9052 [=y]

Location:

-> Device Drivers

-> Real Time Clock (RTC_CLASS [=y])

To enable: Dialog DA9052 Onkey

select: INPUT_DA9052_ONKEY

Depends on: INPUT [=y] && INPUT_MISC [=y] && PMIC_DA9052 [=y]

Location:

-> Device Drivers

-> Input device support

-> Generic input layer (needed for keyboard, mouse, ...) (INPUT [=y])

-> Miscellaneous devices (INPUT_MISC [=y])

To enable: Dialog DA9052 LEDS

select: LEDS_DA9052

Depends on: NEW_LEDS [=y] && LEDS_CLASS [=y] && PMIC_DA9052 [=y]

Location:

-> Device Drivers

-> LED Support (NEW_LEDS [=y])

-> LED Class Support (LEDS_CLASS [=y])

To enable: Dialog DA9052 Watchdog

select: DA9052_WATCHDOG

Depends on: WATCHDOG [=y] && PMIC_DA9052 [=y]

Location:

-> Device Drivers

-> Watchdog Timer Support (WATCHDOG [=y])

.

Chapter 6
MC34708 Digitizer Driver

This chapter describes the Linux PMIC Digitizer Driver that provides low-level access to the PMIC analog-to-digital converters (ADC). This capability includes taking measurements of the X-Y coordinates and contact pressure from an attached touch panel. This device driver uses the PMIC protocol driver to access the PMIC hardware control registers that are associated with the ADC.

The PMIC digitizer driver is used to provide access to and control of the analog-to-digital converter (ADC) that is available with the PMIC. Multiple input channels are available for the ADC, and some of these channels have dedicated functions for various system operations. For example:

- Sampling the voltages on the touch panel interfaces to obtain the (X,Y) position and pressure measurements
- Battery voltage level and current monitoring

The PMIC ADC has a 10-bit resolution and supports either a single channel conversion or automatic conversion of all input channels in succession. The conversion can be triggered by issuing a command.

A hardware interrupt can be generated following the completion of an ADC conversion. Some PMIC chips also provide a pulse generator that is synchronized with the ADC conversion. The pulse generator can enable or drive external circuits in support of the ADC conversion process.

The PMIC ADC components are subject to arbitration rules as documented in the documentation for each PMIC. These arbitration rules determine how requests from both primary and secondary SPI interfaces are handled. SPI bus arbitration configuration and control is not part of this driver because the platform has configured arbitration settings as part of the normal system boot procedure. There is no need to dynamically reconfigure the arbitration settings after the system has been booted.

6.1 Driver Features

The PMIC Digitizer Driveris is a client of the PMIC protocol driver. The PMIC protocol driver provides hardware control register reads and writes through the SPI bus interface and also register/deregister event notification callback functions. The PMIC protocol driver requires access to ADC-specific event notifications.

The PMIC Digitizer Driver supports the following features for supporting a touch panel device:

- Selects either a single ADC input channel or an entire group of input channels to be converted
- Starts an ADC conversion by issuing the appropriate start conversion command
- Enable/disables hardware interrupts for all ADC-related event notifications
- Provides an interrupt handler routine that receives and properly handles all ADC end-of-conversion

- Other device drivers register/deregister additional callback functions to provide custom handling of all ADC-related event notifications
- Provides a read-only device interface for passing touchpanel (X,Y) coordinates and pressure measurements to applications
- Provides the ability to read out one or more ADC conversion results
- Implements the appropriate input scaling equations so that the ADC results are correct
- Specifies the delay between successive ADC conversion operations, if supported by the PMIC. For PMIC chips that do not support this feature, the device driver returns a NOT_SUPPORTED status
- Provides support for a pulse generator that is synchronized with the ADC conversion. For PMIC chips that do not support this feature, returns a NOT_SUPPORTED status
- Provides a complete IOCTL interface to initiate an ADC conversion operation and to return the conversion results
- Provides support for a polling method to detect when the ADC conversion has been completed

This digitizer driver is not responsible for any additional ADC-related activities such as battery level or current. Such functions are handled by other PMIC-related device drivers. Also, this device driver is not responsible for SPI bus arbitration configuration. The appropriate arbitration settings that are required in order for this device driver to work properly are expected to have been set during the system boot process.

6.2 Software Operation

Most of the required operations for this device driver simply involve writing the correct configuration settings to the appropriate PMIC control registers. This can be done by using the APIs that are provided with the PMIC protocol driver.

Once an ADC conversion has been started, suspend the calling thread until the conversion has been completed. Avoid using a busy loop since this negatively impacts processor and overall system performance. Instead, the use of a wait queue offers a much better solution. Therefore, any potentially time-consuming operations results in the calling thread being placed into a wait queue until the operation is completed.

The PMIC ADC conversion can take a significant amount of time. The delay between a start of conversion request and a conversion completed event may even be open ended, if the conversion is not started until the appropriate external trigger signal is received. Therefore, all ADC conversion requests must be placed in a wait queue until the conversion is complete. Once the ADC conversion has completed, the calling thread can be removed from the wait queue and reawakened.

Avoid the use of any polling loops or other thread delay tactics that would negatively impact processor performance. Also, avoid doing anything that prevents hardware interrupts from being handled, because the ADC end-of-conversion event is typically signalled by a hardware interrupt.

6.3 Source Code Structure

Table 6-1 lists the source files for the MC34708-specific version of this driver. These are contained in the following directories:

```
<ltib_dir>/rpm/BUILD/linux/drivers/mxc/pmic/mc34708/mc34708_adc.c
```

<ltib_dir>/rpm/BUILD/linux/include/linux/mc34708_adc.h

<ltib_dir>/rpm/BUILD/linux/drivers/input/touchscreen/mxc_ts.c

Table 6-1. MC34708 Digitizer Driver Files

File	Description
mc34708_adc.c	Implementation of the MC34708 ADC client driver
mc34708_adc.h	Define names of IOCTL user space interface
mxc_ts.c	Common interface to the input driver system

6.4 Menu Configuration Options

The following Linux kernel configurations are provided. To get to the configurations, use the command ./ltib -c when located in the <ltib dir>. In the screen select **Configure Kernel**, exit, and a new screen appears.

- Choose the MC34708 (MC34708) specific digitizer driver for the PMIC ADC. In menuconfig, this option is available under:

  Device Drivers > MXC Support Drivers > MXC PMIC Support > MC34708 ADC support
- Driver for the MXC touch screen. In menuconfig, this option is available under:

  Device Drivers > Input device support > Touchscreens > MXC touchscreen input driver

Chapter 7
MC34708 Regulator Driver

The MC34708 regulator driver provides the low-level control of the power supply regulators, selection of voltage levels, and enabling/disabling of regulators. This device driver makes use of the PMIC protocol driver to access the PMIC hardware control registers.

7.1 Hardware Operation

The MC34708 provides reference and supply voltages for the application processor as well as peripheral devices.The buck converters provide the power supply to processor cores and to other low voltage circuits such as I/O and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and/or other circuitry. Two DVS control pins are provided for pin controlled DVS on the buck switchers targeted for processor core supplies.

Linear regulators are directly supplied from the battery or from the switchers and include supplies for I/O and peripherals, audio, camera, BT, WLAN, and so on. Naming conventions are suggestive of typical or possible use case applications, but the switchers and regulators may be utilized for other system power requirements within the guidelines of specified capabilities.

7.2 Driver Features

The MC34708 PMIC regulator driver is based on the PMIC protocol driver and regulator core driver. It provides the following services for regulator control of the PMIC component:

- Switch ON/OFF all voltage regulators
- Switch ON/OFF all BUCK switchers
- Set the value for all voltage regulators
- Get the current value for all voltage regulators

7.3 Software Operation

The PMIC power management driver and the MC34708 PMIC regulator client driver perform operations by reconfiguring the PMIC hardware control registers. This is done by calling protocol driver APIs with the required register settings.

Some of the PMIC power management operations depend on the system design and configuration. For example, if the system is powered by a power source other than the PMIC, then turning off or adjusting the PMIC voltage regulators has no effect. Conversely, if the system is powered by the PMIC, then any changes that use the power management driver and the regulator client driver can affect the operation or stability of the entire system.

7.4 Regulator APIs

The regulator power architecture is designed to provide a generic interface to voltage and current regulators within the Linux 2.6 kernel. It is intended to provide voltage and current control to client or consumer drivers and also provide status information to user space applications through a sysfs interface. The intention is to allow systems to dynamically control regulator output to save power and prolong battery life. This applies to both voltage regulators (where voltage output is controllable) and current sinks (where current output is controllable).

For more details visit http://opensource.wolfsonmicro.com/node/15

Under this framework, most power operations can be done by the following unified API calls:

- regulator_get—lookup and obtain a reference to a regulator
  ```
  struct regulator *regulator_get(struct device *dev, const char *id);
  ```
- regulator_put—free the regulator source
  ```
  void regulator_put(struct regulator *regulator, struct device *dev);
  ```
- regulator_enable—enable regulator output
  ```
  int regulator_enable(struct regulator *regulator);
  ```
- regulator_disable—disable regulator output
  ```
  int regulator_disable(struct regulator *regulator);
  ```
- regulator_is_enabled—is the regulator output enabled
  ```
  int regulator_is_enabled(struct regulator *regulator);
  ```
- regulator_set_voltage—set regulator output voltage
  ```
  int regulator_set_voltage(struct regulator *regulator, int uV);
  ```
- regulator_get_voltage—get regulator output voltage
  ```
  int regulator_get_voltage(struct regulator *regulator);
  ```

Find more APIs and details in the regulator core source code inside the Linux kernel at:
`<ltib_dir>/rpm/BUILD/linux/drivers/regulator/core.c`.

7.5 Driver Architecture

Figure 7-1 shows the basic architecture of the MC34708 regulator driver.

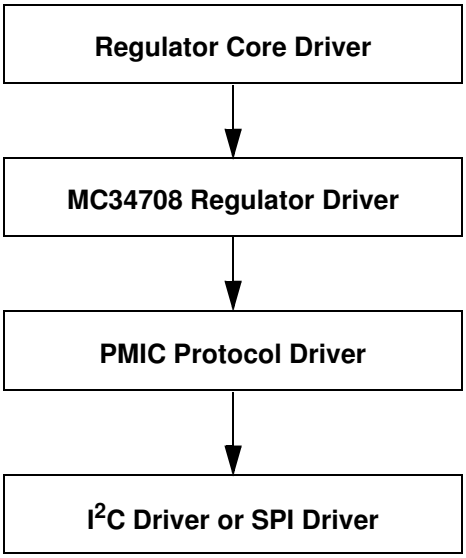


Figure 7-1. MC34708 Regulator Driver Architecture

7.6 Driver Interface Details

Access to the MC34708 regulator is provided through the API of the regulator core driver. The MC34708 regulator driver provides the following regulator controls:

- Buck switch supplies
  - Five buck switch regulators on normal mode: SWx, where x = 1–5
  - Five buck switch regulators on standby mode: SWx_ST, where x = 1–5
  - Five buck switch regulators on DVFS mode: SWx_ST, where x = 1–5
- Linear Regulators
  VGEN1, VPLL, VDAC, VGEN2, VUSB and VUSB2

All of the regulator functions are handled by setting the appropriate PMIC hardware register values. This is done by calling the PMIC protocol driver APIs to access the PMIC hardware registers.

7.7 Source Code Structure

The MC34708 regulator driver is located in the regulator device driver directory:

`<ltib_dir>/rpm/BUILD/linux/drivers/regulator`.

Table 7-1. MC34708 Power Management Driver Files

File	Description
core.c	Linux kernel interface for regulators.
reg-mc34708.c	Implementation of the MC34708 regulator client driver

The MC13892 regulators for MX53 EVK board are registered under
`<ltib_dir>/rpm/BUILD/linux/arch/arm/mach-mx5/mx53_evk_pmic_mc13892.c`.

7.8 Menu Configuration Options

The following Linux kernel configurations are provided for the MC34708 Regulator driver. To get to the PMIC power configuration, use the command `./ltib -c` when located in the `<ltib dir>`. On the configuration screen select **Configure Kernel**, exit, and when the next screen appears, choose.

- Device Drivers > Voltage and Current regulator support > MC34708 Regulator Support.

Chapter 8
MC34708 RTC Driver

The Linux MC34708 RTC driver provides access to the MC34708 RTC control circuits. This device driver makes use of the MC34708 protocol driver to access the MC34708 hardware control registers. The MC34708 device is used for real-time clock control and wait alarm events.

8.1 Driver Features

The MC34708 RTC driver is a client of the MC34708 protocol driver. It provides the services for real time clock control of MC34708 components. The driver is implemented under the standard RTC class framework.

8.2 Software Operation

The MC34708 RTC driver performs operations by reconfiguring the MC34708 hardware control registers. This is done by calling protocol driver APIs with the required register settings.

8.3 Driver Implementation Details

Configuring the MC34708 RTC driver includes the following parameters:

- Set time of day and day value
- Get time of day and day value
- Set time of day alarm and day alarm value
- Get time of day alarm and day alarm value
- Report alarm event to the client

8.3.1 Driver Access and Control

To access this driver, open the `/dev/rtcN` device to allow application-level access to the device driver using the IOCTL interface, where the `N` is the RTC number. /sys/class/rtc/rtcN sysfs attributes support read only access to some RTC attributes.

8.4 Source Code Structure

Table 8-1 lists the source files for MC34708 RTC driver that are available in the `<ltib_dir>/rpm/BUILD/linux/drivers/rtc` directory.

Table 8-1. MC9S08DZ60 RTC Driver Files

File	Description
rtc-mc13892.c	Implementation of the RTC driver, shares wtih the mc13892

8.5 Menu Configuration Options

The following Linux kernel configurations are provided for this module. To get to the MC34708 RTC configuration, use the command ./ltib -c when located in the `<ltib dir>`. In the screen, select **Configure Kernel**, exit, and a new screen appears.

- Device Drivers > Realtime Clock > Freescale MC34708 Real Time Clock.

Chapter 9
ARC USB Driver

The universal serial bus (USB) driver implements a standard Linux driver interface to the ARC USB-HS OTG controller. The USB provides a universal link that can be used across a wide range of PC-to-peripheral interconnects. It supports plug-and-play, port expansion, and any new USB peripheral that uses the same type of port.

The ARC USB controller is enhanced host controller interface (EHCI) compliant. This USB driver has the following features:

- High Speed/Full Speed Host Only core (HOST1)
- High speed and Full Speed OTG core
- Host mode—Supports HID (Human Interface Devices), MSC (Mass Storage Class), and PTP (Still Image) drivers
- Peripheral mode—Supports MSC, and CDC (Communication Devices Class) drivers
- Embedded DMA controller

9.1 Architectural Overview

A USB host system is composed of a number of hardware and software layers. Figure 9-1 shows a conceptual block diagram of the building block layers in a host system that support USB 2.0.

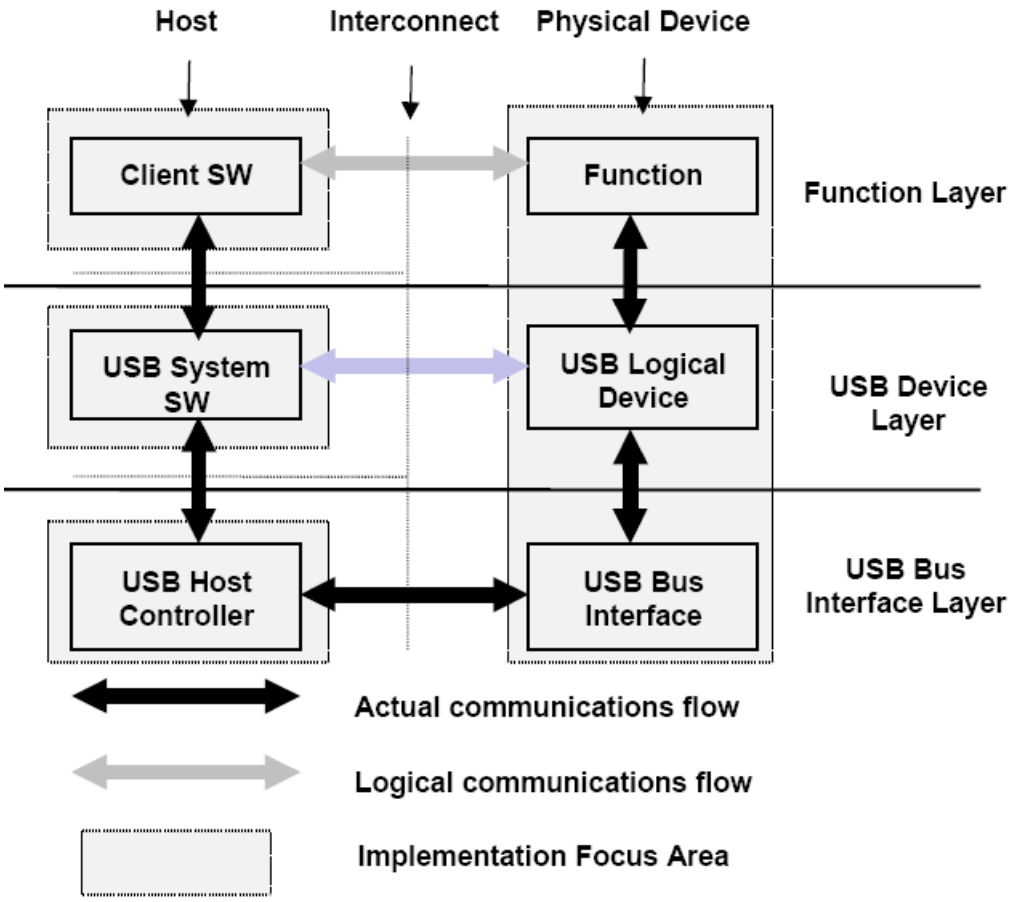


Figure 9-1. USB Block Diagram

9.2 Hardware Operation

For information on hardware operations, refer to the EHCI spec.ehci-r10.pdf available at http://www.usb.org/developers/docs/.

9.3 Software Operation

The Linux OS contains a USB driver, which implements the USB protocols. For the USB host, it only implements the hardware specified initialization functions. For the USB peripheral, it implements the gadget framework.

```
static struct usb_ep_ops fsl_ep_ops = {
        .enable = fsl_ep_enable,
        .disable = fsl_ep_disable,
        .alloc_request = fsl_alloc_request,
        .free_request = fsl_free_request,
```

```
        .queue = fsl_ep_queue,
        .dequeue = fsl_ep_dequeue,
        .set_halt = fsl_ep_set_halt,
        .fifo_status = arcotg_fifo_status,
        .fifo_flush = fsl_ep_fifo_flush,            /* flush fifo */
        };
static struct usb_gadget_ops fsl_gadget_ops = {
        .get_frame = fsl_get_frame,
        .wakeup = fsl_wakeup,
/*      .set_selfpowered = fsl_set_selfpowered, */   /* Always selfpowered */
        .vbus_session = fsl_vbus_session,
        .vbus_draw = fsl_vbus_draw,
        .pullup = fsl_pullup,
        };
```

- `fsl_ep_enable`—configures an endpoint making it usable
- `fsl_ep_disable`—specifies an endpoint is no longer usable
- `fsl_alloc_request`—allocates a request object to use with this endpoint
- `fsl_free_request`—frees a request object
- `arcotg_ep_queue`—queues (submits) an I/O request to an endpoint
- `arcotg_ep_dequeue`—dequeues (cancels, unlinks) an I/O request from an endpoint
- `arcotg_ep_set_halt`—sets the endpoint halt feature
- `arcotg_fifo_status`—get the total number of bytes to be moved with this transfer descriptor

For OTG, an OTG finish state machine (FSM) is implemented.

9.4 Driver Features

The USB stack supports the following features:

- USB device mode
- Mass storage device profile—subclass 8-1 (RBC set)
- USB host mode
- HID host profile—subclasses 3-1-1 and 3-1-2. (USB mouse and keyboard)
- Mass storage host profile—subclass 8-1
- Ethernet USB profile—subclass 2
- DC PTP transfer

9.5 Source Code Structure

Table 9-1 shows the source files available in the source directory, `<ltib_dir>/rpm/BUILD/linux/drivers/usb`.

Table 9-1. USB Driver Files

File	Description
host/ehci-hcd.c	Host driver source file
host/ehci-arc.c	Host driver source file
host/ehci-mem-iram.c	Host driver source file for IRAM support
host/ehci-hub.c	Hub driver source file
host/ehci-mem.c	Memory management for host driver data structures
host/ehci-q.c	EHCI host queue manipulation
host/ehci-q-iram.c	Host driver source file for IRAM support
gadget/arcotg_udc.c	Peripheral driver source file
gadget/arcotg_udc.h	USB peripheral/endpoint management registers
otg/fsl_otg.c	OTG driver source file
otg/fsl_otg.h	OTG driver header file
otg/otg_fsm.c	OTG FSM implement source file
otg/otg_fsm.h	OTG FSM header file
gadget/fsl_updater.c	FSL manufacture tool usb char driver source file
gadget/fsl_updater.h	FSL manufacture tool usb char driver header file

Table 9-2 shows the platform related source files.

Table 9-2. USB Platform Source Files

File	Description
arch/arm/plat-mxc/include/mach/arc_otg.h	USB register define
include/linux/fsl_devices.h	FSL USB specific structures and enums

Table 9-3 shows the platform-related source files in the directory: `<ltib_dir>/rpm/BUILD/linux/arch/arm/mach-mx5/`

Table 9-3. USB Platform Header Files

File	Description
usb_dr.c	Platform-related initialization
usb_h1.c	Platform-related initialization

Table 9-4 shows the common platform source files in the directory:

`<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc`.

Table 9-4. USB Common Platform Files

File	Description
utmixc.c	Internal UTMI transceiver driver
usb_common.c	Common platform related part of USB driver
usb_wakeup.c	Handle usb wakeup events

9.6 Menu Configuration Options

The following Linux kernel configuration options are provided for this module. To get to these options, use the `./ltib -c` command when located in the `<ltib dir>`. On the screen displayed, select **Configure the Kernel** and exit. When the next screen appears, select the following options to enable this module:

- CONFIG_USB—Build support for USB
- CONFIG_USB_EHCI_HCD—Build support for USB host driver. In menuconfig, this option is available under Device drivers > USB support > EHCI HCD (USB 2.0) support.

  By default, this option is Y.
- CONFIG_USB_EHCI_ARC—Build support for selecting the ARC EHCI host. In menuconfig, this option is available under Device drivers > USB support > Support for Freescale controller.
- By default, this option is Y.
- CONFIG_USB_EHCI_ARC_OTG—Build support for selecting the ARC EHCI OTG host. In menuconfig, this option is available under

  Device drivers > USB support > EHCI HCD (USB 2.0) support > Support for DR host port on Freescale controller.

  By default, this option is Y.
- CONFIG_USB_STATIC_IRAM—Build support for selecting the IRAM usage for host. In menuconfig, this option is available under

  Device drivers > USB support > Use IRAM for USB.

  By default, this option is N.
- CONFIG_USB_EHCI_ROOT_HUB_TT—Some EHCI chips have vendor-specific extensions to integrate transaction translators, so that no OHCI or UHCI companion controller is needed. In menuconfig, this option is available under

  Device drivers > USB support > Root Hub Transaction Translators.

  By default, this option is Y selected by USB_EHCI_ARC && USB_EHCI_HCD.
- CONFIG_USB_STORAGE—Build support for USB mass storage devices. In menuconfig, this option is available under

  Device drivers > USB support > USB Mass Storage support.

  By default, this option is Y.

- CONFIG_USB_HID—Build support for all USB HID devices. In menuconfig, this option is available under

  Device drivers > HID Devices > USB Human Interface Device (full HID) support.

  By default, this option is Y.
- CONFIG_USB_GADGET—Build support for USB gadget. In menuconfig, this option is available under

  Device drivers > USB support > USB Gadget Support.

  By default, this option is M.
- CONFIG_USB_GADGET_ARC—Build support for ARC USB gadget. In menuconfig, this option is available under

  Device drivers > USB support > USB Gadget Support > USB Peripheral Controller (Freescale USB Device Controller).

  By default, this option is Y.
- CONFIG_USB_OTG—OTG Support, support dual role with ID pin detection.

  By default, this option is Y.
- CONFIG_USB_ETH—Build support for Ethernet gadget. In menuconfig, this option is available under

  Device drivers > USB support > USB Gadget Support > Ethernet Gadget (with CDC Ethernet Support).

  By default, this option is M.
- CONFIG_USB_ETH_RNDIS—Build support for Ethernet RNDIS protocol. In menuconfig, this option is available under

  Device drivers > USB support > USB Gadget Support > Ethernet Gadget (with CDC Ethernet Support) > RNDIS support.

  By default, this option is Y.
- CONFIG_USB_FILE_STORAGE—Build support for Mass Storage gadget. In menuconfig, this option is available under

  Device drivers > USB support > USB Gadget Support > File-backed Storage Gadget.

  By default, this option is M.
- CONFIG_USB_G_SERIAL—Build support for ACM gadget. In menuconfig, this option is available under

  Device drivers > USB support > USB Gadget Support > Serial Gadget (with CDC ACM support).

  By default, this option is M.

9.7 Programming Interface

This driver implements all the functions that are required by the USB bus protocol to interface with the i.MX USB ports. See the *BSP API* document, for more information.

9.8 Default USB Settings

Table 9-5 shows the default USB settings.

Table 9-5. Default USB Settings

Platform	OTG HS	OTG FS	Host1	Host2(HS)	Host2(FS)
i.MX53 START	Yes	No	Yes	No	No

By default, both usb device and host function are build-in kernel, otg port is used for device mode, and host 1 is used for host mode.

9.9 USB Wakeup usage

9.9.1 How to enable usb wakeup system ability

For otg port:

```
echo enabled > /sys/devices/platform/fsl-usb2-otg/power/wakeup
```

For device-only port:

```
echo enabled > /sys/devices/platform/fsl-usb2-udc/power/wakeup
```

For host-only port:

```
echo enabled > /sys/devices/platform/fsl-ehci.x/power/wakeup
(x is the port num)
```

For usb child device

```
echo enabled > /sys/bus/usb/devices/1-1/power/wakeup
```

9.9.2 What kinds of wakeup event usb support

Take USBOTG port as the example.

Device mode wakeup:

- connect wakeup: when usb line connects to usb port, the other port is connected to PC (Wakeup signal: vbus change)

```
echo enabled > /sys/devices/platform/fsl-usb2-otg/power/wakeup
```

Host mode wakeup:

- connect wakeup: when usb device connects to host port (Wakeup signal: ID/(dm/dp) change)

```
echo enabled > /sys/devices/platform/fsl-usb2-otg/power/wakeup
```

- disconnect wakeup: when usb device disconnects to host port (Wakeup signal: ID/(dm/dp) change)

```
echo enabled > /sys/devices/platform/fsl-usb2-otg/power/wakeup
```

- remote wakeup: press usb device (such as press usb key at usb keyboard) when usb device connects to host port (Wakeup signal: ID/(dm/dp) change):

```
echo enabled > /sys/devices/platform/fsl-usb2-otg/power/wakeup
echo enabled > /sys/bus/usb/devices/1-1/power/wakeup
```

NOTE: For the hub on board, it needs to enable hub's wakeup first. for remote wakeup, it needs to do below three steps:

```
echo enabled > /sys/devices/platform/fsl-usb2-otg/power/wakeup (enable the roothub's
wakeup)
echo enabled > /sys/bus/usb/devices/1-1/power/wakeup (enable the second level hub's
wakeup)
(1-1 is the hub name)

echo enabled > /sys/bus/usb/devices/1-1.1/power/wakeup (enable the usb device's wakeup,
that device connects at second level hub)
(1-1.1 is the usb device name)
```

9.9.3 How to close the usb child device power

```
echo auto > /sys/bus/usb/devices/1-1/power/control
echo auto > /sys/bus/usb/devices/1-1.1/power/control (If there is a hub at usb device)
```

Chapter 10
Image Processing Unit (IPU) Drivers

The image processing unit (IPU) is designed to support video and graphics processing functions and to interface with video and still image sensors and displays. The IPU driver provides a kernel-level API to manipulate logical channels. A logical channel represents a complete IPU processing flow. For example, a complete IPU processing flow (logical channel) might consist of reading a YUV buffer from memory, performing post-processing, and writing an RGB buffer to memory. A logical channel maps one to three IDMA channels and maps to either zero or one IC tasks. A logical channel can have one input, one output, and one secondary input IDMA channel. The IPU API consists of a set of common functions for all channels. Its functions are to initialize channels, set up buffers, enable and disable channels, link channels for auto frame synchronization, and set up interrupts.

Typical logical channels include:

- CSI direct to memory
- CSI to viewfinder pre-processing to memory
- Memory to viewfinder pre-processing to memory
- Memory to viewfinder rotation to memory
- Previous field channel of memory to video deinterlacing and viewfinder pre-processing to memory
- Current field channel of memory to video deinterlacing and viewfinder pre-processing to memory
- Next field channel of memory to video deinterlacing and viewfinder pre-processing to memory
- CSI to encoder pre-processing to memory
- Memory to encoder pre-processing to memory
- Memory to encoder rotation to memory
- Memory to post-processing to memory
- Memory to post-processing rotation to memory
- Memory to synchronous frame buffer background
- Memory to synchronous frame buffer foreground
- Memory to synchronous frame buffer DC
- Memory to synchronous frame buffer mask

The IPU API has some additional functions that are not common across all channels, and are specific to an IPU sub-module. The types of functions for the IPU sub-modules are as follows:

- Synchronous frame buffer functions
  - — Panel interface initialization
  - — Set foreground positions
  - — Set local/global alpha and color key
  - — Set gamma
- CSI functions
  - — Sensor interface initialization

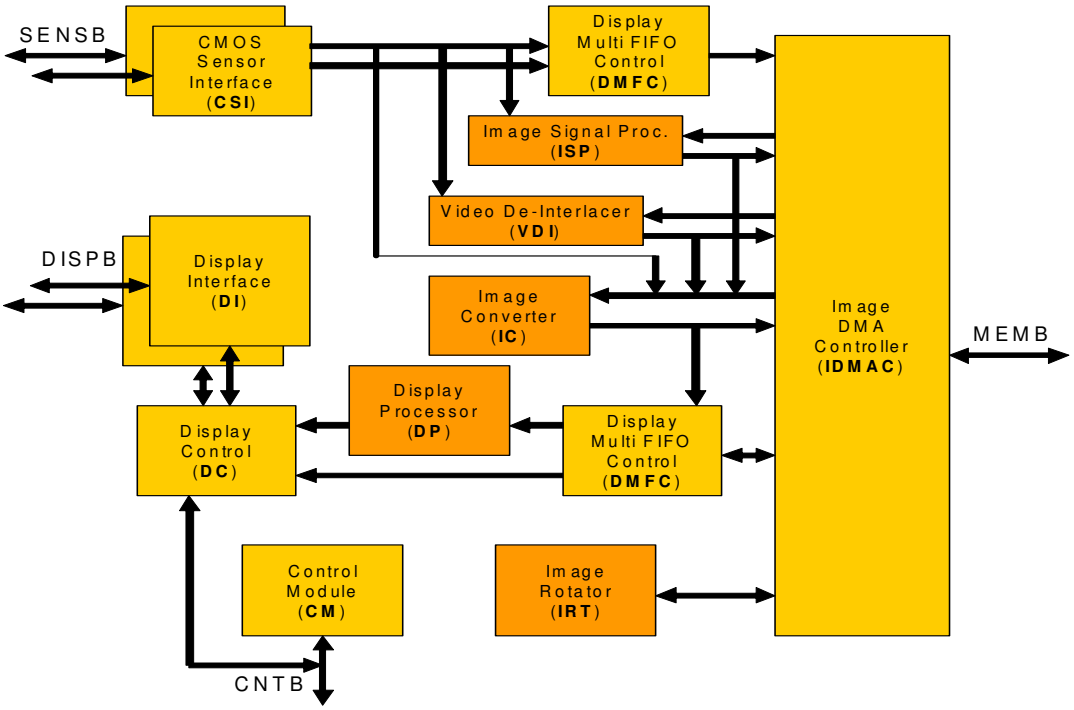
— Set sensor clock
— Set capture size

The higher level drivers are responsible for memory allocation, chaining of channels, and providing user-level API.

10.1 Hardware Operation

The detailed hardware operation of the IPU is discussed in the *MCIMX53 Multimedia Applications Processor Reference Manual (MCIMX53RM)*. Figure 7-3 shows the IPU hardware modules.

Figure 10-1. IPU Module Overview



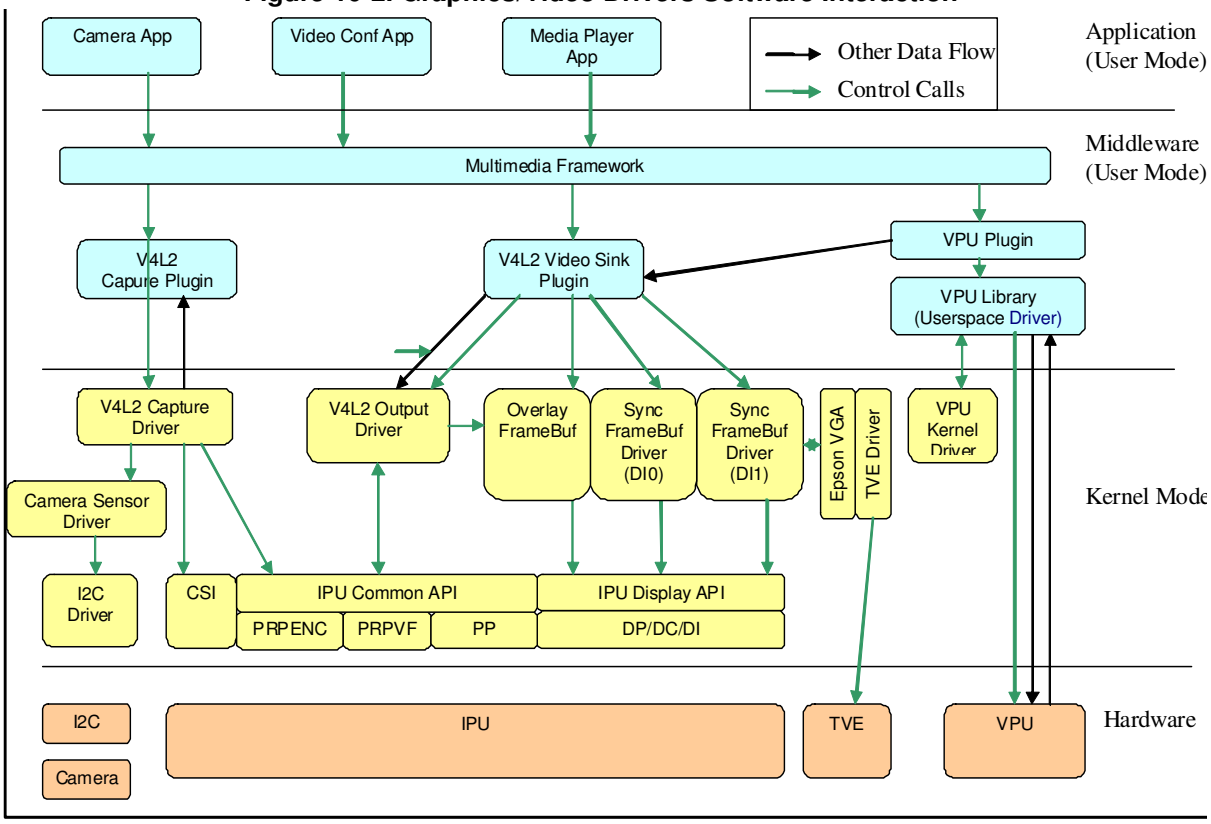
10.2 Software Operation

The IPU driver is a self-contained driver module in the Linux kernel. It consists of a custom kernel-level API for the following blocks:

- Synchronous frame buffer driver
- Display Interface (DI)
- Display Processor (DP)
- Image DMA Controller (IDMAC)
- CMOS Sensor Interface (CSI)
- Image Converter (IC)

Figure 10-2 shows the interaction between the different graphics/video drivers and the IPU.

Figure 10-2. Graphics/Video Drivers Software Interaction



The IPU drivers are sub-divided as follows:

- Device drivers—include the frame buffer driver for the synchronous frame buffer, the frame buffer driver for the displays, V4L2 capture drivers for IPU pre-processing, and the V4L2 output driver for IPU post-processing. The frame buffer device drivers are available in the

  `<ltib_dir>/rpm/BUILD/linux/drivers/video/mxc`

  directory of the Linux kernel. The V4L2 device drivers are available in the

  `<ltib_dir>/rpm/BUILD/linux/drivers/media/video`

  directory of the Linux kernel.
- Low-level library routines—interface to the IPU hardware registers. They take input from the high-level device drivers and communicate with the IPU hardware. The low-level libraries are available in the

  `<ltib_dir>/rpm/BUILD/linux/drivers/mxc/ipu3` directory of the Linux kernel.

10.2.1 IPU Frame Buffer Drivers Overview

The frame buffer device provides an abstraction for the graphics hardware. It represents the frame buffer video hardware, and allows application software to access the graphics hardware through a well-defined interface, so that the software is not required to know anything about the low-level hardware registers.

The driver is enabled by selecting the frame buffer option under the graphics parameters in the kernel configuration. To supplement the frame buffer driver, the kernel builder may also include support for fonts and a startup logo. This device depends on the virtual terminal (VT) console to switch from serial to graphics mode. The device is accessed through special device nodes, located in the `/dev` directory, as `/dev/fb*`. `fb0` is generally the primary frame buffer.

Other than the physical memory allocation and LCD panel configuration, the common kernel video API is utilized for setting colors, palette registration, image blitting, and memory mapping. The IPU reads the raw pixel data from the frame buffer memory and sends it to the panel for display.

10.2.1.1 IPU Frame Buffer Hardware Operation

The frame buffer interacts with the IPU hardware driver module.

10.2.1.2 IPU Frame Buffer Software Operation

A frame buffer device is a memory device, such as `/dev/mem`, and it has features similar to a memory device. Users can read it, write to it, seek to some location in it, and `mmap()` it (the main use). The difference is that the memory that appears in the special file is not the whole memory, but the frame buffer of some video hardware.

`/dev/fb*` also interacts with several IOCTLs, which allows users to query and set information about the hardware. The color map is also handled through IOCTLs. For more information on what IOCTLs exist and which data structures they use, see `<ltib_dir>/rpm/BUILD/linux/include/linux/fb.h`. The following are a few of the IOCTLs functions:

- Request general information about the hardware, such as name, organization of the screen memory (planes, packed pixels, and so on), and address and length of the screen memory.
- Request and change variable information about the hardware, such as visible and virtual geometry, depth, color map format, timing, and so on. The driver suggests values to meet the hardware capabilities (the hardware returns EINVAL if that is not possible) if this information is changed.
- Get and set parts of the color map. Communication is 16 bits-per-pixel (values for red, green, blue, transparency) to support all existing hardware. The driver does all the calculations required to apply the options to the hardware (round to fewer bits, possibly discard transparency value).

The hardware abstraction makes the implementation of application programs easier and more portable. The only thing that must be built into the application programs is the screen organization (bitplanes or chunky pixels, and so on), because it works on the frame buffer image data directly.

The MXC frame buffer driver (`<ltib_dir>/rpm/BUILD/linux/drivers/video/mxc/mxc_ipuv3_fb.c`) interacts closely with the generic Linux frame buffer driver (`<ltib_dir>/rpm/BUILD/linux/drivers/video/fbmem.c`).

10.2.1.3 Synchronous Frame Buffer Driver

The synchronous frame buffer screen driver implements a Linux standard frame buffer driver API for synchronous LCD panels or those without memory. The synchronous frame buffer screen driver is the top level kernel video driver that interacts with kernel and user level applications. This is enabled by selecting

the Synchronous Panel Frame buffer option under the graphics support device drivers in the kernel configuration. To supplement the frame buffer driver, the kernel builder may also include support for fonts and a startup logo. This depends on the VT console for switching from serial to graphics mode.

Except for physical memory allocation and LCD panel configuration, the common kernel video API is utilized for setting colors, palette registration, image blitting and memory mapping. The IPU reads the raw pixel data from the frame buffer memory and sends it to the panel for display.

The frame buffer driver supports different panels as a kernel configuration option. Support for new panels can be added by defining new values for a structure of panel settings.

The frame buffer interacts with the IPU driver using custom APIs that allow:

- Initialization of panel interface settings
- Initialization of IPU channel settings for LCD refresh
- Changing the frame buffer address for double buffering support

The following features are supported:

- Configurable screen resolution
- Configurable RGB 16, 24 or 32 bits per pixel frame buffer
- Configurable panel interface signal timings and polarities
- Palette/color conversion management
- Power management
- LCD power off/on

User applications utilize the generic video API (the standard Linux frame buffer driver API) to perform functions with the frame buffer. These include the following:

- Obtaining screen information, such as the resolution or scan length
- Allocating user space memory using `mmap` for performing direct blitting operations

A second frame buffer driver supports a second video/graphics plane.

10.3 Source Code Structure

Table 10-1 lists the source files associated with the IPU, Sensor, V4L2, and Panel drivers. These files are available in the following directories:

```
<ltib_dir>/rpm/BUILD/linux/drivers/mxc/ipu3
<ltib_dir>/rpm/BUILD/linux/drivers/video/mxc
<ltib_dir>/rpm/BUILD/linux/drivers/media/video/mxc
<ltib_dir>/rpm/BUILD/linux/drivers/video/backlight
```

Table 10-1. IPU Driver Files

File	Description
ipu_capture.c	Asynchronous frame buffer configuration driver
ipu_common.c	Configuration functions for asynchronous and synchronous frame buffers
ipu_device.c	IPU driver device interface and fops functions
ipu_disp.c	IPU display functions
ipu_ic.c	IPU library functions
ipu_calc_stripes_sizes.c	Multi-stripes method functions for ipu_ic.c
mxc_ipuv3_fb.c	Driver for synchronous frame buffer
mxcfb_epson_vga.c	Driver for synchronous framebuffer for VGA
mxcfb_claa_wvga.c	Driver for synchronous frame buffer for WVGA
mxcfb_modedb.c	Parameter settings for Framebuffer devices
ldb.c	Driver for synchronous frame buffer for on chip LVDS
tve.c	Driver for synchronous frame buffer for on chip TVE
mxcfb_sii9022.c	Driver for synchronous frame buffer for HDMI chip sii9022
mxcfb_seiko_wvga.c	Driver for synchronous frame buffer for Seiko WVGA
mxc_edid.c	Driver for EDID

Table 10-2 lists the global header files associated with the IPU and Panel drivers. These files are available in the following directories:

```
<ltib_dir>/rpm/BUILD/linux/drivers/mxc/ipu3/
<ltib_dir>/rpm/BUILD/linux/include/linux/
<ltib_dir>/rpm/BUILD/linux/drivers/media/video/mxc/
```

Table 10-2. IPU Global Header Files

File	Description
ipu_param_mem.h	Helper functions for IPU parameter memory access
ipu_prv.h	Header file for Pre-processing drivers
ipu_regs.h	IPU register definitions
mxcfb.h	Header file for the synchronous framebuffer driver
ipu.h	Header file for ipu basic driver

10.4 Menu Configuration Options

The following Linux kernel configuration options are provided for the IPU module. To get to these options use the command `./ltib -c` when located in the `<ltib dir>`. On the screen displayed, select **Configure the kernel** and exit. When the next screen appears select the options to configure.

- CONFIG_MXC_IPU—Includes support for the Image Processing Unit. In menuconfig, this option is available under:

  Device Drivers > MXC support drivers > Image Processing Unit Driver

  By default, this option is Y for all architectures.

  If ARCH_MX37 or ARCH_MX5 is true, CONFIG_MXC_IPU_V3 will be set, otherwise, CONFIG_MXC_IPU_V1 will be set.
- CONFIG_MXC_CAMERA_MICRON_111—Option for both the Micron mt9v111 sensor driver and the use case driver. This option is dependent on the MXC_IPU option. In menuconfig, this option is available under:

  Device Drivers > Multimedia devices > Video capture adapters > MXC Video For Linux Camera > MXC Camera/V4L2 PRP Features support > Micron mt9v111 Camera support

  Only one sensor should be installed at a time.
- CONFIG_MXC_CAMERA_OV2640—Option for both the OV2640 sensor driver and the use case driver. This option is dependent on the MXC_IPU option. In menuconfig, this option is available under:

  Device Drivers > Multimedia devices > Video capture adapters > MXC Video For Linux Camera > MXC Camera/V4L2 PRP Features support > OmniVision ov2640 camera support

  Only one sensor should be installed at a time.
- CONFIG_MXC_CAMERA_OV3640—Option for both the OV3640 sensor driver and the use case driver. This option is dependent on the MXC_IPU option. In menuconfig, this option is available under:

  Device Drivers > Multimedia devices > Video capture adapters > MXC Video For Linux Camera > MXC Camera/V4L2 PRP Features support > OmniVision ov3640 camera support

  Only one sensor should be installed at a time.
- CONFIG_MXC_IPU_PRP_VF_SDC—Option for the IPU (here the > symbols illustrates data flow direction between HW blocks):

  CSI > IC > MEM MEM > IC (PRP VF) > MEM

  Use case driver for dumb sensor or

  CSI > IC(PRP VF) > MEM

  for smart sensors. In menuconfig, this option is available under:

  Multimedia devices > Video capture adapters > MXC Video For Linux Camera > MXC Camera/V4L2 PRP Features support > Pre-Processor VF SDC library

  By default, this option is M for all.
- CONFIG_MXC_IPU_PRP_ENC—Option for the IPU:

  Use case driver for dumb sensors

CSI > IC > MEM MEM > IC (PRP ENC) > MEM

or for smart sensors

CSI > IC(PRP ENC) > MEM.

In menuconfig, this option is available under:

Device Drivers > Multimedia Devices > Video capture adapters > MXC Video For Linux Camera > MXC Camera/V4L2 PRP Features support > Pre-processor Encoder library

By default, this option is set to M for all.

- CONFIG_VIDEO_MXC_CAMERA—This is configuration option for V4L2 capture Driver. This option is dependent on the following expression:

  VIDEO_DEV && MXC_IPU && MXC_IPU_PRP_VF_SDC && MXC_IPU_PRP_ENC

  In menuconfig, this option is available under:

  Device Drivers > Multimedia devices > Video capture adapters > MXC Video For Linux Camera

  By default, this option is M for all.
- CONFIG_VIDEO_MXC_OUTPUT—This is configuration option for V4L2 output Driver. This option is dependent on VIDEO_DEV && MXC_IPU option. In menuconfig, this option is available under:

  Device Drivers > Multimedia devices > Video capture adapters > MXC Video for Linux Video Output

  By default, this option is Y for all.
- CONFIG_FB—This is the configuration option to include frame buffer support in the Linux kernel. In menuconfig, this option is available under:

  Device Drivers > Graphics support > Support for frame buffer devices

  By default, this option is Y for all architectures.
- CONFIG_FB_MXC—This is the configuration option for the MXC Frame buffer driver. This option is dependent on the CONFIG_FB option. In menuconfig, this option is available under:

  Device Drivers > Graphics support > MXC Framebuffer support

  By default, this option is Y for all architectures.
- CONFIG_FB_MXC_SYNC_PANEL—This is the configuration option that chooses the synchronous panel framebuffer. This option is dependent on the CONFIG_FB_MXC option. In menuconfig, this option is available under:

  Device Drivers > Graphics support > MXC Framebuffer support > Synchronous Panel Framebuffer

  By default this option is Y for all architectures.
- CONFIG_FB_MXC_EPSON_VGA_SYNC_PANEL—This is the configuration option that chooses the Epson VGA panel. This option is dependent on CONFIG_FB_MXC_SYNC_PANEL option. In menuconfig, this option is available under:

  Device Drivers > Graphics support > MXC Framebuffer support > Synchronous Panel Framebuffer > Epson VGA Panel
- CONFIG_FB_MXC_TVOUT_TVE —This configuration option selects the TVOUT encoder on MX5x chip. This option is dependent on CONFIG_FB_MXC_SYNC_PANEL and CONFIG_MXC_IPU_V3 option. In menuconfig, this option is available under:

Device Drivers > Graphics support > MXC Framebuffer support > Synchronous Panel Framebuffer > MXC TVE TV Out Encoder

- CONFIG_FB_MXC_LDB —This configuration option selects the LVDS module on iMX53 chip. This option is dependent on CONFIG_FB_MXC_SYNC_PANEL and CONFIG_MXC_IPU_V3 option. In menuconfig, this option is available under:

  Device Drivers > Graphics support > MXC Framebuffer support > Synchronous Panel Framebuffer > MXC LDB
- CONFIG_FB_MXC_CLAA_WVGA_SYNC_PANEL —This is the configuration option that chooses the CLAA WVGA panel. This option is dependent on CONFIG_FB_MXC_SYNC_PANEL option. In menuconfig, this option is available under:

  Device Drivers > Graphics support > MXC Framebuffer support > Synchronous Panel Framebuffer > CLAA WVGA Panel.
- CONFIG_FB_MXC_SEIKO_WVGA_SYNC_PANEL —This is the configuration option that chooses the SEIKO WVGA panel. This option is dependent on CONFIG_FB_MXC_SYNC_PANEL option. In menuconfig, this option is available under:

  Device Drivers > Graphics support > MXC Framebuffer support > Synchronous Panel Framebuffer > SEIKO WVGA Panel.
- CONFIG_FB_MXC_SII9022 —This configuration option selects the SII9022 HDMI chip. This option is dependent on CONFIG_FB_MXC_SYNC_PANEL option. In menuconfig, this option is available under:

  Device Drivers > Graphics support > MXC Framebuffer support > Synchronous Panel Framebuffer > Si Image SII9022 DVI/HDMI Interface Chip
- CONFIG_FB_MXC_CH7026 —This configuration option selects the CH7026 VGA interface chip. This option is dependent on the CONFIG_FB_MXC_SYNC_PANEL option. In menuconfig, this option is available under:

  Device Drivers > Graphics support > MXC Framebuffer support > Synchronous Panel Framebuffer > Chrontel CH7026 VGA Interface Chip
- CONFIG_FB_MXC_TVOUT_CH7024 —This configuration option selects the CH7024 TVOUT encoder. This option is dependent on the CONFIG_FB_MXC_SYNC_PANEL option. In menuconfig, this option is available under:

  Device Drivers > Graphics support > MXC Framebuffer support > Synchronous Panel Framebuffer > CH7024 TV Out Encoder

10.5 Programming Interface

For more information, see the *API Documents* for the programming interface.

Chapter 11
TV encoder (TVE) Driver

The TVE is one SoC IP supported in i.MX5x (version 2), it provides direct connection between an Application Processor and a TV set via analog interfaces, the features it support includes:

- Up to 10 TV out mode standards including SD and HD mode (3 for version 1)
- Programmable output formats support like CVBS, S-Video, YPrPb, and RGB component through 3 channels
- Cable detection
- CGMS (not support in driver)

Please refer to SoC's RM for detail information.

11.1 Hardware Operation

The TVE block connects with IPUv3 DI1 port through internal signals, a tve_clk must be provided to enable TVE module, and a display clock is fed back to DI1 which drivers IPUv3 display signals to TVE.

The feedback clock to DI1 must be setup before DI1 setup.

There is an interrupt line which will triger an interrupt when a cable plugs in.

3x75 Ohm pull down resistors should be added to 3 output channel lines to make cable detection work.

11.2 Software Operation

TVE driver is implemented based on a fb clienct driver, it mainly contains:

- A fb event notifier callback
- A delay workqueue based on interrupt serves for cable detection

In fb event notifier callback:

- An event as FB_EVENT_MODE_CHANGE or FB_EVENT_BLANK could setup TVE clock and modes according to fbi infomation
- An event as FB_EVENT_SUSPEND or FB_EVENT_RESUME will be resiponsible for system suspend/resume operation

For cable detection:

- An irq handler -- tve_detect_handler() is registered
- Interrupt will be enabled during tve enable
- A delay workqueue will be scheduled when interrupt occurs

- Workqueue callback function -- cd_work_func() will check cable status register to setup output format
- A sysfs node -- /sys/devices/platform/tve.0/headphone is provided to show cable state

11.3 Source Code Structure

Table 11-1 lists the TVE driver source files available in the `<ltib_dir>/rpm/BUILD/linux/drivers/video/mxc` directory.

Table 11-1. Camera File List

File	Description
tve.c	TVE driver implementation

11.4 Linux Menu Configuration Options

The Linux kernel configuration option, CONFIG_FB_MXC_TVOUT_TVE, is provided for the module. This is the configuration option for the TVE driver. In `menuconfig`, this option is available under

Device Drivers > Graphics support > MXC TVE TV Out Encoder

This option is dependent on the support Synchronous Panel Framebuffer and IPUv3 option. By default, this option is Y.

Chapter 12
TVE-VGA Driver

The VGA is supported through TVE (version 2) module in i.MX53, it only use TVE's TVDAC module.

12.1 Hardware Operation

It's almost same as TVE tvout, it works on:

- Test mode 1
- RGB output format
- Under HD tv out mode
- A delayed vsync/hsync output pin

12.2 Software Operation

VGA driver is one part of TVE driver, it does not support cable detection, and a delayed vsync/hsync output pin must be set through IPUv3.

12.3 Source Code Structure

Table 12-1 lists the TVE driver source files available in the `<ltib_dir>/rpm/BUILD/linux/drivers/video/mxc` directory.

Table 12-1. Camera File List

File	Description
tve.c	TVE driver implementation

12.4 Linux Menu Configuration Options

The Linux kernel configuration option, CONFIG_FB_MXC_TVOUT_TVE, is provided for the module. This is the configuration option for the TVE driver. In `menuconfig`, this option is available under

Device Drivers > Graphics support > MXC TVE TV Out Encoder

This option is dependent on the support Synchronous Panel Framebuffer and IPUv3 option. By default, this option is Y.

Chapter 13
HDMI Driver

The HDMI module is supported by a SII902x chip on board or a daughter card, it supports:

- HDMI video output
- Display device EDID fetching
- HDMI audio output

Refer to SII902x's datasheet for detail information.

13.1 Hardware Operation

Normally, the SII902x chip connects with

- IPUv3 DI port for display support
- SoC SPDIF port for audio support
- I2C bus for setup operation and EDID fetching
- A cable detection interrupt line

13.2 Software Operation

The HDMI driver is implemented based on a fb clienct driver, it mainly contains:

- A fb event notifier callback
- A delay workqueue based on interrupt serves for cable detection and EDID fetching

In fb event notifier callback:

- An event as FB_EVENT_MODE_CHANGE will setup SII902x video and audio parameters
- An event as FB_EVENT_BLANK will be resiponsible for SII902x power on/off

For cable detection and EDID fetching:

- An irq handler -- sii902x_detect_handler() is registered
- A delay workqueue will be scheduled when interrupt occurs
- Workqueue callback function -- det_worker() will triger EDID fetching
- A sysfs node -- /sys/devices/platform/sii9022.0/cable_state is provided to show cable state
- An uevent with EVENT=plugin or EVENT=plugout will send out after hdmi cable plugin/out

13.3 Source Code Structure

Table 13-1 lists the TVE driver source files available in the `<ltib_dir>/rpm/BUILD/linux/drivers/video/mxc` directory.

Table 13-1. Camera File List

File	Description
mxcfb_sii902x.c	HDMI Sii902x driver implementation

13.4 Linux Menu Configuration Options

The Linux kernel configuration option, CONFIG_FB_MXC_SII902X, is provided for the module. This is the configuration option for the HDMI SII902x driver. In `menuconfig`, this option is available under

Device Drivers > Graphics support > Si Image SII9022 DVI/HDMI Interface Chip

This option is dependent on the support Synchronous Panel Framebuffer and IPUv3 option. By default, this option is Y.

Chapter 14
i.MX5 Dual Display

This section describes how to setup dual-display on i.MX53 STARTplatform.

14.1 Hardware Operation

i.MX53 multimedia application processes incorporate the Image Processing Unit (IPUv3) hardware image processing accelerator. There are two Display Interfaces (DI) within IPUv3, which provide connection to external display devices and related devices. The external display devices can be a LCD display panel, which connects with DI directly. The related devices may be embedded in chip or integrated on EVK boards. TV Encoder (TVE) is the only embedded device which connects with DI1 in i.MX53 chips. i.MX53 chips embed the LVDS Display Birdge (LDB) module so that external display devices with LVDS interfaces can be connected with the chips directly. TVE is only supported in i.MX53 TO2 chips. There is a connector on i.MX53 START platform which leads the legacy parallel signals of DI0 out so that a LCD display panel can be connected to it directly or a connected DVI convertor can provide an interface for a DVI monitor. One HDMI daughter card can be connected with the DI0 connector on i.MX53 START platform. There is a VGA connector on i.MX53 START platform which is driven by TVE module embedded.

As there are two DIs within IPUv3, we can support dual-display feature, that is, each of the two DIs can support an externel display device simultanously. As long as the hardware bandwidth is not exceeded, i.MX53START platform can drive every possible dual-display feature provided by the board design.

Table 14-1 shows all the external display devices that can be connected with i.MX53 START platform.

Table 14-1. External Display Devices for i.MX53 START Platform

EVK Platform	DI Number	External Display Device
i.MX53 START	0	1) DVI daughter card 2) CLAA-WVGA display panel 3) SEIKO-WVGA display panel (need to populate D4 on the LCD panel) 4) HDMI daughter card
	1	1) VGA (driven by TVE module embedded)

For the detailed information about the external display devices, see the relevant board schematics.

14.2 Software Operation

The user should setup a correct bootup command line if he or she wants to enable dual-display feature. The user may follow these steps to set the bootup command line for display related options:

1. Add ‘`tve`’, ‘vga’, ‘`ldb`’ or ‘hdmi’ to bootup command line if the use case involves TVE, VGA, LDB or HDMI, otherwise, the options should not be added.

2. Add '`di1_primary`' to bootup command line if the device connected with DI1 is the primary device, that is, `/dev/fb0` will be mapped to this device after the system boots up. If the device connected with DI0 is the primary device, no specific option is needed.
3. Add '`di0_primary`' to bootup command line if the device connected with DI0 is the primary device, that is, `/dev/fb0` will be mapped to this device after the system boots up. If the device connected with DI0 is the primary device, no specific option is needed
4. For each of the devices connected with DI, provide a specific video mode in bootup command line in this format: video=mxcdi*x*fb:*DI_pixel_format*, *video_mode*,bpp=*bits_per_pixel_of_frame_buffer*.

The 'x' stands for DI number.

The 'DI_pixel_format' stands for the output pixel format of the related DI. Usually, 'RGB565' is used for CLAA WVGA LCD display panel, 'BGR24' is used for VGA, 'RGB24' is used for DVI monitor/SEIKO WVGA LCD.

The '`bits_per_pixel_of_frame_buffer`' stands for the pixel format of the related framebuffer.

The 'video_mode' can be found here:

1. DVI connector: The video mode is in this format:

   `<xres>x<yres>[M][-<bpp>][@<refresh>`

   with <xres>, <yres>, <bpp> and <refresh> decimal numbers and <name> a string. If 'M' is present after yres (and before refresh/bpp if present), the framebuffer driver will compute the timings using VESA(tm) Coordinated Video Timings (CVT).

Note, if the dislplay resolution is 720P, then '720P60' should be used as 'video_mode', and if the display resolution is UXGA, then 'UXGA' should be used as 'video_mode'.

2. LVDS display panel: Use 'XGA' for XGA LVDS display panel and use '1080P60' for 1080P LVDS display panel.
3. CLAA WVGA LCD display panel: Use 'CLAA-WVGA'.
4. SEIKO WVGA LCD display panel: Use 'SEIKO-WVGA'
5. TV: Use 'TV-1080P60' for 1080P60 TVout, use 'TV-1080P30' for 1080P30 TVout, use 'TV-1080P25' for 1080P25 TVout, use 'TV-1080P24' for 1080P24 TVout, use 'TV-1080I60' for 1080I60 TVout, use 'TV-1080I50' for 1080I50 TVout, use 'TV-720P60' for 720P60 TVout, use 'TV-720P30' for 720P30 TVout, use 'TV-PAL' for PAL TVout and use 'TV-NTSC' for NTSC TVout.
6. VGA: Use 'VGA-XGA' or 'VGA-SXGA'.

As the primary display device will be unblanked automatically after the system boots up but the secondary is still blank, the user needs to unblank the secondary by himself or herself either with framebuffer ioctrls or command line. Here is the command line the user may use on PDK to unblank the secondary display device in an ordinary case:

```
echo 0 > /sys/class/graphics/fb1/blank
```

The user may also swith the primary display device and secondary display device by command lines on PDK. For example, fb0 is the primary device's framebuffer and fb1 is the secondary device's framebuffer. To switch the primary display device and secondary display device, the user may use these command lines:

```
1. echo 1 > /sys/class/graphics/fb0/blank
2. echo 1 > /sys/class/graphics/fb1/blank
3. echo 1 > /sys/class/graphics/fb2/blank
4. echo 1-layer-fb > /sys/class/graphics/fb0/fsl_disp_property
5. echo 0 > /sys/class/graphics/fb0/blank
6. echo 0 > /sys/class/graphics/fb1/blank
```

To switch them back, ther user may use these command lines:

```
1. echo 1 > /sys/class/graphics/fb0/blank
2. echo 1 > /sys/class/graphics/fb1/blank
3. echo 1 > /sys/class/graphics/fb2/blank
4. echo 1-layer-fb > /sys/class/graphics/fb1/fsl_disp_property
5. echo 0 > /sys/class/graphics/fb0/blank
6. echo 0 > /sys/class/graphics/fb1/blank
```

14.3 Examples

Examples for i.MX53 START platform:

1. DI0:CLAA-WVGA LCD display panel, DI1:VGA monitor

   ```
   video=mxcdi0fb:RGB565,CLAA-WVGA video=mxcdi1fb:BGR24,VGA-XGA vga
   ```

Chapter 15
Video for Linux Two (V4L2) Driver

The Video for Linux Two (V4L2) drivers are plug-ins to the V4L2 framework that enable support for camera and preprocessing functions, as well as video and post-processing functions. The V4L2 camera driver implements support for all camera related functions. The V4l2 capture device takes incoming video images, either from a camera or a stream, and manipulates them. The output device takes video and manipulates it, then sends it to a display or similar device. The V4L2 Linux standard API specification is available at http://v4l2spec.bytesex.org/spec/.

The features supported by the V4L2 driver are as follows:

- Direct preview and output to SDC foreground overlay plane (with no processor intervention and synchronized to LCD refresh)
- Direct preview to graphics frame buffer (with no processor intervention, but not synchronized to LCD refresh)
- Color keying or alpha blending of frame buffer and overlay planes
- Simultaneous preview and capture
- Streaming (queued) capture from IPU encoding channel
- Direct (raw Bayer) still capture (sensor dependent)
- Programmable pixel format, size, frame rate for preview and capture
- Programmable rotation and flipping using custom API
- RGB 16-bit, 24-bit, and 32-bit preview formats
- Raw Bayer (still only, sensor dependent), RGB 16, 24, and 32-bit, YUV 4:2:0 and 4:2:2 planar, YUV 4:2:2 interleaved, and JPEG formats for capture
- Control of sensor properties including exposure, white-balance, brightness, contrast, and so on
- Plug-in of different sensor drivers
- Linking post-processing resize and CSC, rotation, and display IPU channels with no ARM processing of intermediate steps
- Streaming (queued) input buffer
- Double buffering of overlay and intermediate (rotation) buffers
- Configurable 3+ buffering of input buffers
- Programmable input and output pixel format and size
- Programmable scaling and frame rate
- RGB 16, 24, and 32-bit, YUV 4:2:0 and 4:2:2 planar, and YUV 4:2:2 interleaved input formats
- TV output

The driver implements the standard V4L2 API for capture, output, and overlay devices. The command `modprobe mxc_v4l2_capture` must be run before using these functions.

15.1 V4L2 Capture Device

MX53 START board doesn't support V4L capture devices. The user can ignore V4L capture sections for MX53 START.

The V4L2 capture device includes two interfaces:

- Capture interface—uses IPU pre-processing ENC channels to record the YCrCb video stream
- Overlay interface—uses the IPU pre-processing VF channels to display the preview video to the SDC foreground panel without ARM processor interaction.

V4L2 capture support can be selected during kernel configuration. The driver includes two layers. The top layer is the common Video for Linux driver, which contains chain buffer management, stream API and other `ioctl` interfaces. The files for this device are located in
`<ltib_dir>/rpm/BUILD/linux/drivers/media/video/mxc/capture/.`

The V4L2 capture device driver is in the `mxc_v4l2_capture.c` file. The lowest layer is in the `ipu_prp_enc.c` file.

This code (`ipu_prp_enc.c`) interfaces with the IPU ENC hardware, `ipu_prp_vf_sdc_bg.c` interfaces with the IPU VF hardware, and `ipu_still.c` interfaces with the IPU CSI hardware. Sensor frame rate control is handled by VIDIOC_S_PARM `ioctl`. Before the frame rate is set, the sensor turns on the AE and AWB turn on. The frame rate may change depending on light sensor samples.

Drivers for specific cameras can be found in
`<ltib_dir>/rpm/BUILD/linux/drivers/media/video/mxc/capture/`

15.1.1 V4L2 Capture IOCTLs

Currently, the memory map stream API is supported. Supported V4L2 IOCTLs include the following:

- VIDIOC_QUERYCAP
- VIDIOC_G_FMT
- VIDIOC_S_FMT
- VIDIOC_REQBUFS
- VIDIOC_QUERYBUF
- VIDIOC_QBUF
- VIDIOC_DQBUF
- VIDIOC_STREAMON
- VIDIOC_STREAMOFF
- VIDIOC_OVERLAY
- VIDIOC_G_FBUF
- VIDIOC_S_FBUF
- VIDIOC_G_CTRL
- VIDIOC_S_CTRL
- VIDIOC_CROPCAP

- VIDIOC_G_CROP
- VIDIOC_S_CROP
- VIDIOC_S_PARM
- VIDIOC_G_PARM
- VIDIOC_ENUMSTD
- VIDIOC_G_STD
- VIDIOC_S_STD
- VIDIOC_ENUMOUTPUT
- VIDIOC_G_OUTPUT
- VIDIOC_S_OUTPUT

V4L2 control code has been extended to provide support for rotation. The ID is V4L2_CID_PRIVATE_BASE. Supported values include:

- 0—Normal operation
- 1—Vertical flip
- 2—Horizontal flip
- 3—180° rotation
- 4—90° rotation clockwise
- 5—90° rotation clockwise and vertical flip
- 6—90° rotation clockwise and horizontal flip
- 7—90° rotation counter-clockwise

Figure 15-1 shows a block diagram of V4L2 Capture API interaction.

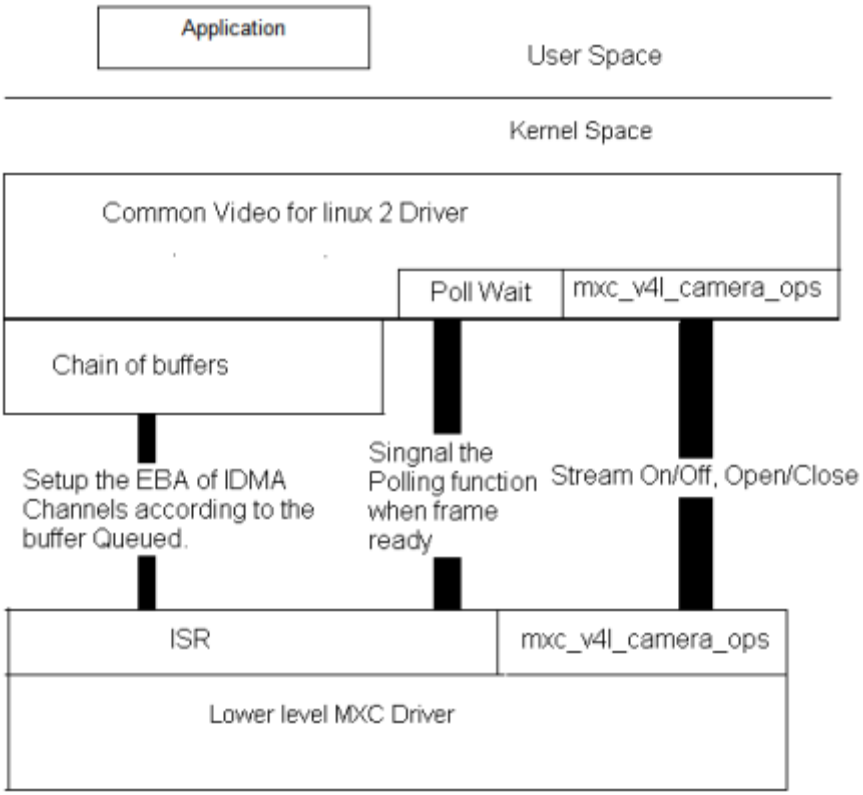


Figure 15-1. Video4Linux2 Capture API Interaction

15.1.2 Use of the V4L2 Capture APIs

This section describes a sample V4L2 capture process. The application completes the following steps:

1. Sets the capture pixel format and size by IOCTL VIDIOC_S_FMT.
2. Sets the control information by IOCTL VIDIOC_S_CTRL for rotation usage.
3. Requests a buffer using IOCTL VIDIOC_REQBUFS. The common V4L2 driver creates a chain of buffers (currently the maximum number of frames is 3).
4. Memory maps the buffer to its user space.
5. Queues buffers using the IOCTL command VIDIOC_QBUF.
6. Starts the stream using the IOCTL VIDIOC_STREAMON. This IOCTL enables the IPU tasks and the IDMA channels. When the processing is completed for a frame, the driver switches to the buffer that is queued for the next frame. The driver also signals the semaphore to indicate that a buffer is ready.
7. Takes the buffer from the queue using the IOCTL VIDIOC_DQBUF. This IOCTL blocks until it has been signaled by the ISR driver.
8. Stores the buffer to a YCrCb file.
9. Replaces the buffer in the queue of the V4L2 driver by executing VIDIOC_QBUF again.

For the V4L2 still image capture process, the application completes the following steps:

1. Sets the capture pixel format and size by executing the IOCTL VIDIOC_S_FMT.
2. Reads one frame still image with YUV422.

FOr the V4L2 overlay support use case, the application completes the following steps:

1. Sets the overlay window by IOCTL VIDIOC_S_FMT.
2. Turns on overlay task by IOCTL VIDIOC_OVERLAY.
3. Turns off overlay task by IOCTL VIDIOC_OVERLAY.

15.2 V4L2 Output Device

The V4L2 output driver uses the IPU post-processing functions for video output. The driver implements the standard V4L2 API for output devices. V4L2 output device support can be selected during kernel configuration. The driver is available at
`<ltib_dir>/rpm/BUILD/linux/drivers/media/video/mxc/output/mxc_v4l2_output.c`.

15.2.1 V4L2 Output IOCTLs

Currently, the memory map stream API is supported. Supported V4L2 IOCTLs include the following:

- VIDIOC_QUERYCAP
- VIDIOC_REQBUFS
- VIDIOC_G_FMT
- VIDIOC_S_FMT
- VIDIOC_QUERYBUF
- VIDIOC_QBUF
- VIDIOC_DQBUF
- VIDIOC_STREAMON
- VIDIOC_STREAMOFF
- VIDIOC_G_CTRL
- VIDIOC_S_CTRL
- VIDIOC_CROPCAP
- VIDIOC_G_CROP
- VIDIOC_S_CROP
- VIDIOC_S_PARM
- VIDIOC_G_PARM

The V4L2 control code has been extended to provide support for rotation. For this use, the ID is V4L2_CID_PRIVATE_BASE. Supported values include the following:

- 0—Normal operation
- 1—Vertical flip
- 2—Horizontal flip

- 3—Horizontal and vertical flip
- 4—90° rotation
- 5—90° rotation and vertical flip
- 6—90° rotation and horizontal flip
- 7—90° rotation with horizontal and vertical flip

15.2.2 Use of the V4L2 Output APIs

This section describes a sample V4L2 capture process that uses the V4L2 output APIs. The application completes the following steps:

1. Sets the capture pixel format and size using IOCTL VIDIOC_S_FMT.
2. Sets the control information using IOCTL VIDIOC_S_CTRL, for rotation.
3. Requests a buffer using IOCTL VIDIOC_REQBUFS. The common V4L2 driver creates a chain of buffers (currently the maximum number of frames is 3).
4. Memory maps the buffer to its user space.
5. Executes the IOCTL VIDIOC_DQBUF.
6. Passes the data that requires post-processing to the buffer.
7. Queues the buffer using the IOCTL command VIDIOC_QBUF.
8. Starts the stream by executing IOCTL VIDIOC_STREAMON.
9. VIDIOC_STREAMON and VIDIOC_OVERLAY cannot be enabled simultaneously.

15.3 Source Code Structure

Table 15-1 lists the source and header files associated with the V4L2 drivers. These files are available in the following directory:

```
<ltib_dir>/rpm/BUILD/linux/drivers/media/video/mxc
```

Table 15-1. V2L2 Driver Files

File	Description
capture/mxc_v4l2_capture.c	V4L2 capture device driver
output/mxc_v4l2_output.c	V4L2 output device driver
capture/mxc_v4l2_capture.h	Header file for V4L2 capture device driver
output/mxc_v4l2_output.h	Header file for V4L2 output device driver
capture/ipu_prp_enc.c	Pre-processing encoder driver
capture/ipu_prp_vf_adc.c	Pre-processing view finder (asynchronous) driver
capture/ipu_prp_vf_sdc.c	Pre-processing view finder (synchronous foreground) driver
capture/ipu_prp_vf_sdc_bg.c	Pre-processing view finder (synchronous background) driver
capture/ipu_still.c	Pre-processing still image capture driver

Drivers for specific cameras can be found in
`<ltib_dir>/rpm/BUILD/linux/drivers/media/video/mxc/capture/`

15.4 Menu Configuration Options

The Linux kernel configuration options are provided in the chapter on the IPU module. See Section 10.4, “Menu Configuration Options.”

15.5 V4L2 Programming Interface

For more information, see the *V4L2 Specification* and the *API Documents* for the programming interface. The API Specification is available at http://v4l2spec.bytesex.org/spec/.

Chapter 16
Graphics Processing Unit (GPU)

The Graphics Processing Unit (GPU) is a graphics accelerator targeting embedded 2D/3D graphics applications. The GPU3D (3D graphics processing unit) is based on the AMD Z430 core, which is an embedded engine that accelerates user level graphics APIs (Application Programming Interface) such as OpenGL ES 1.1 and 2.0. The GPU2D (2D graphics processing unit) is based on the AMD Z160 core, which is an embedded 2D and vector graphics accelerator targeting the OpenVG 1.1 graphics API and feature set. The GPU driver kernel module source is in kernel source tree, but the libs are delivered as binary only.

16.1 Driver Features

The GPU driver enables this board to provide the following software and hardware support:

- EGL (EGL™ is an interface between Khronos rendering APIs such as OpenGL ES or OpenVG and the underlying native platform window system) 1.3 API defined by Khronos Group
- OpenGL ES (OpenGL® ES is a royalty-free, cross-platform API for full-function 2D and 3D graphics on embedded systems) 1.1 API defined by Khronos Group
- OpenGL ES 2.0 API defined by Khronos Group
- OpenVG (OpenVG™ is a royalty-free, cross-platform API that provides a low-level hardware acceleration interface for vector graphics libraries such as Flash and SVG) 1.1 API defined by Khronos Group

16.2 Hardware Operation

Refer to the GPU chapter in the *SOC Reference Manual* for detailed hardware operation and programming information.

16.3 Software Operation

The GPU driver is divided into two layers. The first layer is running in kernel mode and acts as the base driver for the whole stack . This layer provides the essential hardware access, device management, memory management, command stream management, context management and power management. The second layer is running in user mode, implementing the stack logic and providing the following APIs to the upper layer applications:

- OpenGL ES 1.1 and 2.0 API
- EGL 1.3 API
- OpenVG 1.1 API

16.4 Source Code Structure

Table 16-1 lists GPU driver kernel module source structure:

```
<ltib_dir>/rpm/BUILD/linux/drivers/mxc/amd-gpu
```

Table 16-1. GPU Driver Files

File	Description
Kconfig Makefile	kernel configure file and makefile
include	header files
common	common and core code
os	os specific code
platform	platform specific code

16.5 API References

Refer to the following web sites for detailed specifications:

- OpenGL ES 1.1 and 2.0 API: http://www.khronos.org/opengles/
- EGL 1.3 API: http://www.khronos.org/egl/
- OpenVG 1.1 API: http://www.khronos.org/openvg/

16.6 Menu Configuration Options

The following Linux kernel configurations are provided for GPU driver:

- CONFIG_MXC_AMD_GPU —Configuration option for GPU driver. In the menuconfig this option is available under Device Drivers > MXC support drivers > MXC GPU support > MXC GPU support.

To get to the GPU library package in LTIB, use the command `./ltib -c` when located in the <`ltib dir`>. On the screen displayed, select **Configure the kernel** and select “Device Drivers” > “MXC support drivers” > “MXC GPU support” > “MXC GPU support”and exit. When the next screen appears select the following options to enable the GPU driver:

- Package list > amd-gpu-bin-mx51

  This package provides proprietary binary kernel modules, libraries, and test code built from the GPU for framebuffer
- Package list > amd-gpu-x11-bin-mx51

  This package provides proprietary binary kernel modules, libraries, and test code built from the GPU for X-Window

16.7 One tip for GPU pan-swap solution

The default virtual y size of framebuffer is 3 times of the actual framebuffer size. It provides the chance for GPU to use pan-swapping solution in most of cases. But the padding is needed for some framebuffer configurations such as 800x480@16bpp. So the first alignment address of each framebuffer can fall on a page boundary required by GPU.

The user can modify the default virtual y size to match the algorithm used for the GPU pan swapping. See the code below:

```
#define PAGESIZE xxxx
static void calc_height(int *vheight, int width, int height, int bpp)
{
  int height_round_up=0;
  int bytes_per_pixel = bpp/8;
  int bytes=0;

  do{
    bytes += width*bytes_per_pixel;
    ++height_round_up;
  }while( (bytes % PAGESIZE) || (height_round_up<height) );

  if(confVerbose)
    printf("Rounded up Height for one framebuffer: %d\n", height_round_up);

  *vheight = 2*height_round_up + height;
}
```

Chapter 17
X Windows Acceleration

X Windows is a portable, client-server based, graphics display system. X Windows can run with a default frame buffer driver which handles all drawing operations to the main display. Since there is a 2D GPU (graphics processing unit) available, then some of the drawing operations can be accelerated. High level X Windows operations may get decomposed into many low level drawing operations where these low level operations are accelerated for X Windows.

17.1 Hardware Operation

X Windows acceleration utilizes the 2D GPU which is discussed in the Chapter 16, "Graphics Processing Unit (GPU)". Acceleration is also dependent on the frame buffer memory.

17.2 Software Operation

X Windows acceleration is supported for X.org X Server version 1.7.6 and some later versions supporting the EXA interface version 2.5.

The following list summarizes the types of operations that are accelerated for X Windows. All operations involve frame buffer memory which may be onscreen or offscreen:

- Solid fill of a rectangle
- Copy of a rectangle with same pixel format with possible source-target rectangle overlap
- Copy of a rectangle supporting most XRender compositing operations with these options:
  - Pixel format conversion
  - Repeating pattern source
  - Porter-Duff blending of source with target
  - Source alpha masking

The following list includes additional features supported as part of the X Windows acceleration:

- Allocation of X pixmaps directly in frame buffer memory
- EGL swap buffers where the EGL window surface is an X window
- X window can be composited into an X pixmap which can be used directly as any EGL surface

17.2.1 X Windows Acceleration Architecture

The following block diagram shows the components that are involved in the acceleration of X Windows:

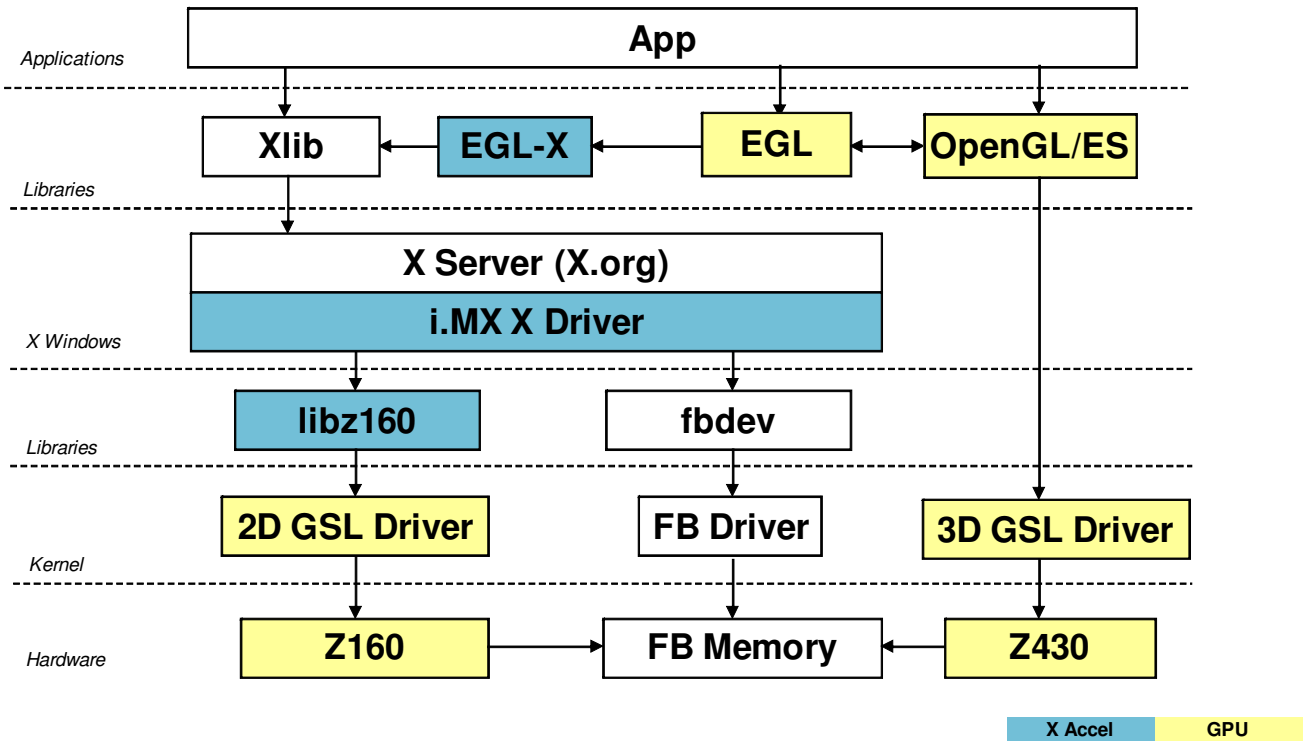


Figure 17-1. X Window Acceleration Block Diagram

The components shown in yellow are those provided as part of the 2D/3D GPU driver support which includes OpenGL/ES and EGL. The components shown in white are the standard components in the X Windows system without acceleration. The components shown in blue are those added to support X Windows acceleration and briefly described here.

The **i.MX X Driver** library module (`imx-drv.so`) is loaded by the X server and contains the high level implementation of the X Windows acceleration interface for i.MX platforms containing the Z160 2D GPU core. The entire linearly contiguous frame buffer memory in `/dev/fb0` is used for allocating pixmaps for X both onscreen and offscreen. The driver supports a custom X extension which allows X clients to query the GPU address of any X pixmap stored in frame buffer memory.

The **libz160** library module (`libz160.so`) contains the register level programming interface to the Z160 GPU module. This includes the storing of register programming commands into packets which can be streamed to the device. The functions in the libz160 library are called by the i.MX X Driver code.

The **EGL-X** library module (`libEGL.so`) contains the X Windows implementation of the low level EGL platform-specific support functions. This allows X window and X pixmap objects to be used as EGL window and pixmap surfaces. The EGL-X library uses Xlib function calls in its implementation along with the i.MX X Driver module's X extension for querying the GPU address of X pixmaps stored in frame buffer memory.

17.2.2 i.MX X Driver Details

The i.MX X Driver, referred to as imx-drv, implements the EXA interface of the X server in providing acceleration. The following list describes details particular to this implementation:

- The implementation builds upon the source from the fbdev frame buffer driver for X so that it can be the fallback when the acceleration is disabled.
- The implementation is based on X server EXA version 2.5.0.
- The EXA solid fill operation is accelerated, except for source/target drawables containing less than 150 pixels in which case fallback is to software rendering.
- The EXA copy operation is accelerated, except for source/target drawables containing less than 150 pixels in which case fallback is to software rendering.
- For EXA solid fill and copy operations, only solid plane masks and only `GXcopy` raster-op operations are accelerated.
- EXA composite allows for many options and combinations of source/mask/target for rendering. Most of the (commonly used) EXA composite operations are accelerated.

  The following types of EXA composite operations are accelerated;

  — Simple source composite with target
  — Simple source-in-mask composite with target
  — Constant source (with or without alpha mask) composite with target
  — Repeating pattern source (with or without alpha mask) composite with target
  — Operations for source/target drawables containing at least 150 pixels
  — Only these blending functions: SOURCE, OVER, IN, IN-REVERSE, OUT-REVERSE, and ADD (some of these are needed to support component-alpha blending which is accelerate)

  In general, the following types of (less commonly used) EXA composite operations are **not** accelerated:

  — Transformed (that is, scaled, rotated) sources and masks
  — Gradient sources
  — Alpha masks with repeating patterns
- The implementation handles all pixmap allocation for X through the EXA callback interface. A first attempt is made to allocate the memory where it can be accessed by a physical GPU address. This attempt can fail if there is insufficient GPU accessible memory remaining, but it can also fail when the bits per pixel being requested for the pixmap is less than 8. If the attempt to allocate from the GPU accessible memory fails, then the memory is allocated from the system. If the pixmap memory is allocated from the system, then this pixmap cannot be involved in a GPU accelerated option. The number of pitch bytes used to access the pixmap memory may be different depending on whether it was allocated from GPU accessible memory or from the system.
- Once the memory for an X pixmap has been allocated, whether it is from GPU accessible memory or from the system, the pixmap is locked and can never migrate to the other type of memory. Pixmap migration from GPU accessible memory to system memory is not necessary since a system virtual address is always available for GPU accessible memory. Pixmap migration from system memory to GPU accessible memory is not currently implemented, but would only help in

situations where there was insufficient GPU accessible memory at initial allocation but more memory becomes available (through de-allocation) at a later time.

- The GPU accessible memory pitch (horizontal) alignment for the Z430 is 32 pixels while the buffer pitch alignment for the Z160 is 4 bytes. Because the memory for X pixmaps can be allocated from GPU accessible memory and these X pixmaps could be used in EGL for OpenGL/ES drawing operations (using the Z430), the pitch alignment requirement is set conservatively for the Z430. There is also a 32-pixel vertical alignment requirement (for the Z430) and a 4096-byte address offset alignment requirement (for the Z160) also for GPU accessible memory.
- All of the memory allocated for `/dev/fb0` is made available to an internal linear offscreen memory manager based on the one used in EXA. The portion of this memory beyond the screen memory is available for allocation of X pixmap where this memory area is GPU accessible. The amount of memory allocated to `/dev/fb0` needs to be several MB more than the amount needed for the screen. The actual amount needed depends on the number of X windows and pixmaps used, possible usage of X pixmaps as texture, and whether X windows are using the XComposite extension.
- An X extension is provided so that X clients can query the physical GPU address associated with an X pixmap, if that X pixmap was allocated in the GPU accessible memory.

17.2.3 libz160 Details

The libz160 library module provides an API for user space programs to perform 2D accelerated graphics operations using the Z160. The following list describes details particular to this implementation:

- The API was originally developed to provide the separation of functionality needed by the EXA implementation in the i.MX X Driver.
- The packet streaming is provided by the 2D GPU driver support command stream interface (CSI) library (`libcsi.a`) which is statically linked into this libz160 library module.
- The kernel support for the 2D GPU driver is provided by the `gsl_kmod` kernel device module

17.2.4 EGL-X Details

The EGL-X library implements the low level EGL interface when used in the X Windows system. The following list describes details particular to this implementation:

- The `eglDisplay` native display type is "`Display*`" in X Windows.
- The `eglWindowSurface` native window surface type is "`Window`" in X Windows.
- The `eglPixmapSurface` native pixmap surface type is "`Pixmap`" in X Windows.
- When an `eglWindowSurface` is created, the back buffers used for double-buffering can have different representations from the window surface (based on the selected `eglConfig`). An attempt is made to create each back buffer using the representation which provides the most efficient blit of the back buffer contents to the window surface when `eglSwapBuffers` is called. Each back buffer is allocated separately using the following approach:
  - Create an X pixmap of the necessary size. Use the X extension for the i.MX X Driver module to query the physical frame buffer address for this X pixmap if it was allocated in the offscreen frame buffer memory.

— If the X pixmap is in the offscreen frame buffer memory then consider the following.
  – If the pixel format of the back buffer matches that of the window, then the `XCopyArea` function is used to blit the back buffer to the window.
  – If the pixel format of the back buffer does **not** match that of the window, then the `XRenderComposite` function is used to convert and blit the back buffer to the window.
— If the X pixmap is **not** in the offscreen frame buffer memory, then a back buffer is allocated from the GSL memory pool and mapped to an `XImage`.
  – If the pixel format of the back buffer matches that of the window, then the `XPutImage` function is used to blit the back buffer to the window.
  – If the pixel format of the back buffer does **not** match that of the window, then the `XPutImage` function is used to first blit the back buffer to the X pixmap (to get image transferred to X server without format conversion) and then the `XRenderComposite` function is used to convert and blit the X pixmap to the window.

17.2.5 The xorg.conf File for i.MX X Driver

The `/etc/X11/xorg.conf` file must be properly configured to use the i.MX X Driver. This configuration appears in a `"Device"` section of the file which contains some required entries and some entries that are optional. The following example shows a preferred configuration for using the i.MX X Driver:

```
Section "Device"
   Identifier      "i.MX Accelerated Framebuffer Device"
   Driver          "imx"
   Option          "fbdev" "/dev/fb0"
   Option          "NoAccel" "false"
   Option          "AccelMethod" "EXA"
   Option          "EXANoComposite" "false"
   Option          "EXANoUploadToScreen" "false"
   Option          "EXANoDownloadFromToScreen" "false"
EndSection
```

Each entry recognized by the i.MX X Driver is described as follows.

`Identifier "i.MX Accelerated Framebuffer Device"`

This mandatory entry specifies the unique name to associate with this graphics device. This is what ties a specific graphics card to a screen. This string must match the `Device` identifier string in a `Screen` section of the `xorg.conf` file. For example:

```
Section "Screen"
   Identifier “Default Screen"
   Device “i.MX Accelerated Framebuffer Device"
   <other entries>
EndSection
```

`Driver "imx"`

This mandatory entry specifies the name of this loadable i.MX X driver.

`Option "fbdev" "string"`
This mandatory entry specifies the path for the frame buffer device to use.

`Option “NoAccel” boolean`
Disables GPU acceleration of all rendering operations. Default: off.

`Option “AccelMethod boolean`
Method of X server interface to use for acceleration. Only supported value is `“EXA”` so any other value specified disables acceleration. Default: `“EXA”`.

`Option “EXANoComposite” boolean`
Disables acceleration of the EXA Composite operation which is the basic interface in EXA to support the X Render extension. This is not related to the X Composite extension. Default: off.

`Option “EXANoUploadToScreen” boolean`
Disables acceleration of uploading pixmap data to the frame buffer. Default: off.

`Option “EXANoDownloadFromScreen” boolean`
Disables acceleration of downloading of pixmap data from the frame buffer. Default: off.

17.2.6 Setup X Windows Acceleration

- Verify that the following packages are available and installed:
  `libz160-bin_<bsp-version>_armel.deb`
  This package contains the `libz160.so` library module and installs it in the `/usr/lib` folder.
  `amd-gpu-x11-bin-mx51_<bsp-version>_armel.deb`
  This package contains the `libEGL.so` library module and installs it in the `/usr/lib` folder.
  `xserver-xorg-video-imx_<bsp-version>_armel.deb`
  This package contains the `imx-dev.so` driver module for X acceleration and installs it in the folder with all the other X.org driver modules.
- Verify that the device file `/dev/gsl_kmod` is present.
- Verify that the file `/etc/X11/xorg.conf` contains the correct entries as described in the previous section.

There are a few ways to verify that X Windows acceleration is indeed operating given that the above steps have been performed.

1. Verify that the device file `/dev/gsl_kmod` is present.
2. Examine the file `/var/log/Xorg.0.log` and confirm that the following lines are present:
   ```
   (II) EXA(0): Using custom EXA
   (II) IMX(0): IMX EXA acceleration setup successful
   ```
3. In the same `/var/log/Xorg.0.log` file, search for a line similar to the following:
   ```
   (II) IMX(0): Offscreen pixmap area of 15062K bytes
   ```
   This indicates the number of bytes available for X pixmaps that can be allocated in the off-screen frame buffer memory. The size indicated here is about 15MB of available memory, but this is just an example.

Chapter 18
Video Processing Unit (VPU) Driver

18.1 Hardware Operation

The VPU hardware performs all of the codec computation and most of the bitstream parsing/packeting. Therefore, the software takes advantage of less control and effort to implement a complex and efficient multimedia codec system.

The VPU hardware data flow is shown in the MPEG4 decoder example in Figure 18-1.

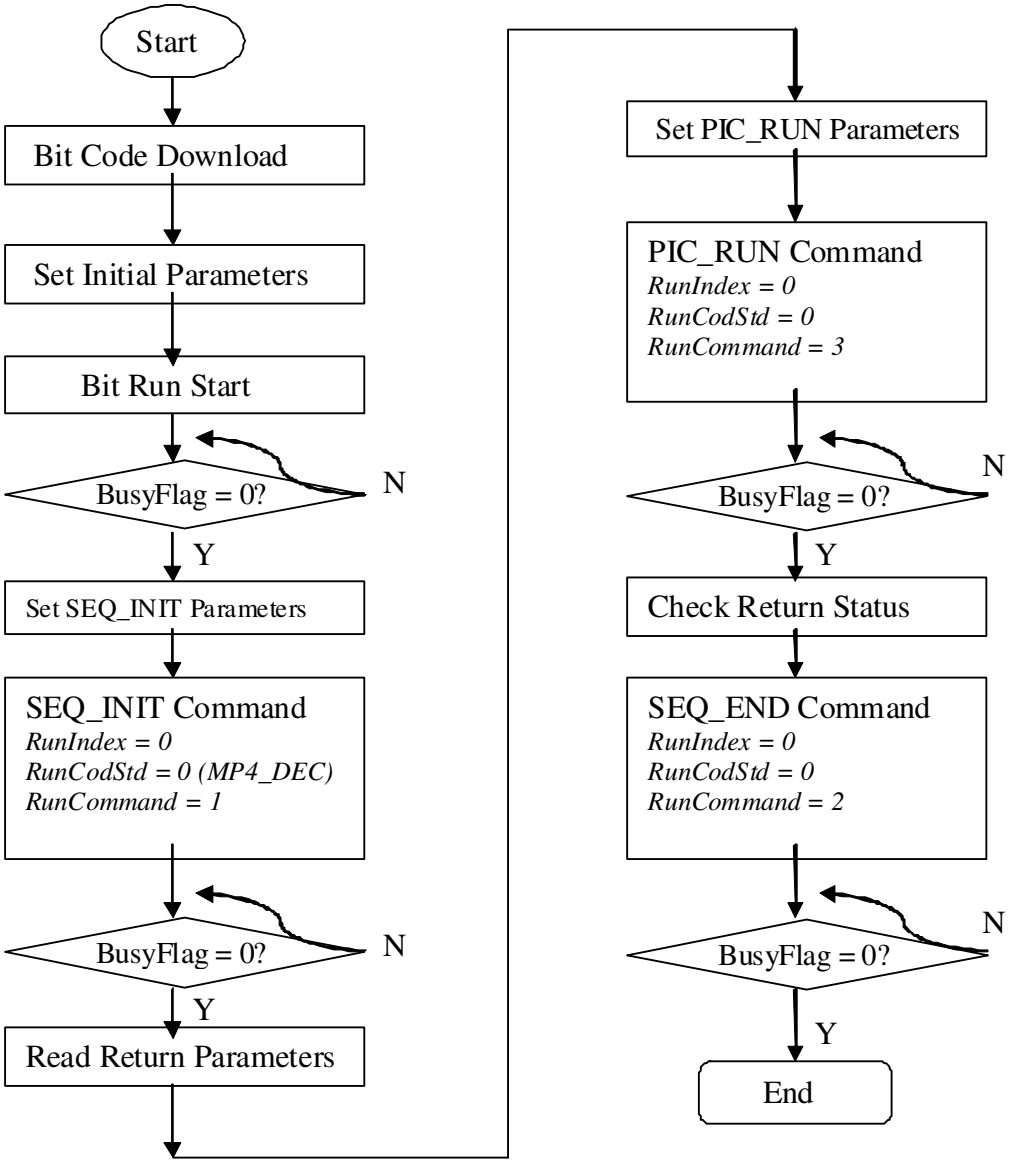


Figure 18-1. VPU Hardware Data Flow

18.2 Software Operation

The VPU software can be divided into two parts: the kernel driver and the user-space library as well as the application in user space. The kernel driver takes responsibility for system control and reserving resources (memory/IRQ). It provides an IOCTL interface for the application layer in user-space as a path to access system resources. The application in user-space calls related IOCTLs and codec library functions to implement a complex codec system.

The VPU kernel driver include the following functions:

- Module initialization—Initializes the module with the device specific structure
- Device initialization—Initializes the VPU clock and hardware, and request the IRQ
- Interrupt servicing routine—Supports events that one frame has been finished
- File operation routines— Provides the following interfaces to user space
  - File open
  - File release
  - File synchronization
  - File IOCTL to provide interface for memory allocating and releasing
  - Memory map for register and memory accessing in user space
- Device Shutdown—Shutdowns the VPU clock and hardware, and release the IRQ

The VPU user space driver has the following functions:

- Codec lib
  - Downloads executable bitcode for hardware
  - Initializes codec system
  - Sets codec system configuration
  - Controls codec system by command
  - Reports codec status and result
- System I/O operation
  - Requests and frees memory
  - Maps and unmaps memory/register to user space
  - Device management

18.3 Source Code Structure

Table 18-1 lists the kernel space source files available in the following directories:

```
<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/include/mach/
<ltib_dir>/rpm/BUILD/linux/drivers/mxc/vpu/
```

Table 18-1. VPU Driver Files

File	Description
mxc_vpu.h	Header file defining IOCTLs and memory structures
mxc_vpu.c	Device management and file operation interface implementation

Table 18-2 lists the user-space library source files available in the `<ltib_dir>/rpm/BUILD/imx-lib-11.09.01/vpu` directory:

Table 18-2. VPU Library Files

File	Description
vpu_io.c	Interfaces with the kernel driver for opening the VPU device and allocating memory
vpu_io.h	Header file for IOCTLs
vpu_lib.c	Core codec implementation in user space
vpu_lib.h	Header file of the codec
vpu_reg.h	Register definition of VPU
vpu_util.c	File implementing common utilities used by the codec
vpu_util.h	Header file

Table 18-3 lists the firmware files available in the following directories:

`<ltib_dir>/rpm/BUILD/firmware-imx-11.09.01/lib/firmware/vpu/` directory

Table 18-3. VPU firmware Files

File	Description
vpu_fw_xxx.bin	VPU firmware

NOTE

To get the to files in Table 18-2, run the command: `./ltib -m prep -p imx-lib` in the console

18.4 Menu Configuration Options

To get to the VPU driver, use the command `./ltib -c` when located in the <`ltib dir`>. On the screen displayed, select **Configure the kernel** and exit. When the next screen appears select the following options to enable the VPU driver:

- CONFIG_MXC_VPU—Provided for the VPU driver. In menuconfig, this option is available under

  Device Drivers > MXC support drivers > MXC VPU (Video Processing Unit) support

18.5 Programming Interface

There is only a user-space programming interface for the VPU module. A user in the application layer cannot access the kernel driver interface directly. The VPU library access the kernel driver interface for users.

The codec library APIs are listed below:

```
RetCode vpu_EncOpen(EncHandle* pHandle, EncOpenParam* pop);
RetCode vpu_EncClose(EncHandle encHandle);
RetCode vpu_EncGetInitialInfo(EncHandle encHandle, EncInitialInfo* initialInfo);
RetCode vpu_EncRegisterFrameBuffer(EncHandle encHandle, FrameBuffer* pBuffer, int num,
```

```
                                    int stride);
RetCode vpu_EncGetBitstreamBuffer(EncHandle handle, PhysicalAddress* prdPrt,
                                    PhysicalAddress* pwrPtr, Uint32* size);
RetCode vpu_EncUpdateBitstreamBuffer(EncHandle handle, Uint32 size);
RetCode vpu_EncStartOneFrame(EncHandle encHandle, EncParam* pParam);
RetCode vpu_EncGetOutputInfo(EncHandle encHandle, EncOutputInfo* info);
RetCode vpu_EncGiveCommand (EncHandle pHandle, CodecCommand cmd, void* pParam);
RetCode vpu_DecOpen(DecHandle* pHandle, DecOpenParam* pop);
RetCode vpu_DecClose(DecHandle decHandle);
RetCode vpu_DecGetBitstreamBuffer(DecHandle pHandle, PhysicalAddress* pRdptr,
                                    PhysicalAddress* pWrptr, Uint32* size);
RetCode vpu_DecUpdateBitstreamBuffer(DecHandle decHandle, Uint32 size);
RetCode vpu_DecSetEscSeqInit(DecHandle pHandle, int escape);
RetCode vpu_DecGetInitialInfo(DecHandle decHandle, DecInitialInfo* info);
RetCode vpu_DecRegisterFrameBuffer(DecHandle decHandle, FrameBuffer* pBuffer, int num,
                                    int stride, DecBufInfo* pBufInfo);
RetCode vpu_DecStartOneFrame(DecHandle handle, DecParam* param);
RetCode vpu_DecGetOutputInfo(DecHandle decHandle, DecOutputInfo* info);
RetCode vpu_DecBitBufferFlush(DecHandle handle);
RetCode vpu_DecClrDispFlag(DecHandle handle, int index);
RetCode vpu_DecGiveCommand(DecHandle pHandle, CodecCommand cmd, void* pParam);
int vpu_WaitForInt(int timeout_in_ms);
RetCode vpu_SWReset(DecHandle handle, int index);
```

System I/O operations are listed below:

```
int IOSystemInit(void);
int IOSystemShutdown(void);
int IOGetPhyMem(vpu_mem_desc* buff);
int IOFreePhyMem(vpu_mem_desc* buff);
int IOGetVirtMem (vpu_mem_desc* buff);
int IOFreeVirtMem(vpu_mem_desc* buff);
```

18.6 Defining an Application

The most important definition for an application is the codec memory descriptor. It is used for `request`, `free`, `mmap and munmap` memory as follows:

```
typedef struct vpu_mem_desc
{
        int size;                   /*request memory size*/
        unsigned long phy_addr;     /*physical memory get from system*/
        unsigned long cpu_addr;     /*address for system usage while freeing, user doesn't need
                                            to handle or use it*/
        unsigned long virt_uaddr; /*virtual user space address*/
} vpu_mem_desc;
```

Chapter 19
Low-level Power Management (PM) Driver

This section describes the low-level Power Management (PM) driver which controls the low-power modes.

19.1 Hardware Operation

The i.MX5 supports four low power modes: RUN, WAIT, STOP, and LPSR (low power screen).

Table 19-1 lists the detailed clock information for the different low power modes.

Table 19-1. Low Power Modes

Mode	Core	Modules	PLL	CKIH/FPM	CKIL
RUN	Active	Active, Idle or Disable	On	On	On
WAIT	Disable	Active, Idle or Disable	On	On	On
STOP	Disable	Disable	Off	Off	On
LPSR	Disable	Disable	Off	On	On

For the detailed information about lower power modes, see the MX53 IC spec.

19.2 Software Operation

The i.MX5 PM driver maps the low-power modes to the kernel power management states as listed below:

- Standby—maps to WAIT mode which offers minimal power saving, while providing a very low-latency transition back to a working system
- Mem (suspend to RAM)—maps to STOP mode which offers significant power saving as all blocks in the system are put into a low-power state, except for memory, which is placed in self-refresh mode to retain its contents
- System idle—maps to WAIT mode

The i.MX5 PM driver performs the following steps to enter and exit low power mode:

1. Enable the gpc_dvfs_clk
2. Allow the Coretex-A8 platform to issue a deep sleep mode request
3. If STOP mode:
   a) Program CCM CLPCR register to set low power control register.
   b) Request switching off ARM/NENO power when pdn_req is asserted.
   c) Request switching off embedded memory peripheral power when pdn_req is asserted.
   d) Program TZIC wakeup register to set wakeup interrupts
4. Call `cpu_do_idle` to execute WFI pending instructions for wait mode

5. If STOP mode, execute `cpu_do_suspend_workaround` in RAM. Change the drive strength of DDR SDCLK as “low” to minum the power leakage in SDCLK. Execute WFI pending instructions for stop mode
6. Generate a wakeup interrupt and exit low power mode. If STOP mode, restore DDR drive strength.
7. Disable gpc_dvfs_clk

19.3 Source Code Structure

Table 19-2 shows the PM driver source files. These files are available in

`<ltib_dir>/rpm/BUILD/linux/arch/arm/mach-mx5/`

Table 19-2. PM Driver Files

File	Description
pm.c	Supports suspend operation
system.c	Supports low-power modes
wfi.S	Assemble file for `cpu_cortexa8_do_idle`
suspend.S	Assemble file for `cpu_do_suspend_workaround`

19.4 Menu Configuration Options

The following Linux kernel configuration options are provided for this module. To get to these options, use the `./ltib -c` command when located in the `<ltib dir>`. On the screen displayed, select **Configure the Kernel** and exit. When the next screen appears, select the following options to enable this module:

- CONFIG_PM—Build support for power management. In menuconfig, this option is available under

  Power management options > Power Management support

  By default, this option is Y.
- CONFIG_SUSPEND—Build support for suspend. In menuconfig, this option is available under

  Power management options > Suspend to RAM and standby

19.5 Programming Interface

The `mxc_cpu_ip_set` API in the `system.c` function is provided for low-power modes. This implements all the steps required to put the system into WAIT and STOP modes.

Chapter 20
Dynamic Voltage Frequency Scaling (DVFS) Driver

The Dynamic Voltage Frequency Scaling (DVFS) device driver allows simple dynamic voltage frequency scaling. The frequency of the core (CPU) clock domain and the voltage of the core power domain can be changed on the fly with all modules continuing their normal operations. The voltage of the core power domain can be changed through the PMIC. The frequency of the core clock domain can be changed by switching temporarily to an alternate PLL clock, and then returning to the updated PLL, already locked at a specific frequency, or by merely changing the post dividers division factors.

20.1 Hardware Operation

The DVFS core module is a power management module. The purpose of the DVFS module is to detect the appropriate operation frequency for the IC. DVFS core is operated under control of the GPC (General Power Controller) block. The hardware DVFS core interrupt is served by GPC IRQ. The DVFS core domain performance update procedure includes both voltage and frequency changes in appropriate order by the GPC controller (hardware). For more information on the HW DVFS Core block refer to the DVFS chapter in the *Multimedia Applications Processor* documentation.

20.2 Software Operation

The DVFS device driver allows the frequency of the core clock domain and the voltage of the core power domain to be changed on the fly. The frequency of the core clock domain and the voltage of the core power domain are changed by switching between defined freq-voltage operating points. The frequencies are manipulated using the clock framework API, while the voltage is set using the regulators API.

To Enable the DVFS core use this command:

```
echo 1 > /sys/devices/platform/mxc_dvfs_core.0/enable
```

To Disable The DVFS core use this command:

```
echo 0 > /sys/devices/platform/mxc_dvfs_core.0/enable
```

20.3 Source Code Structure

Table 20-1 lists the source files and headers available in the following directory:

```
<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/
```

Table 20-1. DVFS Driver Files

File	Description
dvfs_core.c	Linux DVFS functions

In addition, the partial of DVFS core parameters are located into arch/arm/mach-mx5/bus_freq.c.

For DVFS CPU working point settings, see arch/arm/mach-mx5/mx53_wp.c.

20.4 Menu Configuration Options

There are no menu configuration options for this driver. The DVFS core is included by default.

20.4.1 Board Configuration Options

There are no board configuration options for the Linux DVFS core device driver.

Chapter 21
CPU Frequency Scaling (CPUFREQ) Driver

The CPU frequency scaling device driver allows the clock speed of the CPU to be changed on the fly. Once the CPU frequency is changed, the voltage VDDGP is changed to the voltage value defined in mx53_wp.c. This method can reduce power consumption (thus saving battery power), because the CPU uses less power as the clock speed is reduced.

21.1 Software Operation

The CPUFREQ device driver is designed to change the CPU frequency and voltage on the fly. If the frequency is not defined inmx53_wp.c , the CPUFREQ driver changes the CPU frequency to the nearest frequency in the array. The frequencies are manipulated using the clock framework API, while the voltage is set using the regulators API. The CPU frequencies in the array are based on the boot CPU frequency which can be changed by using the clock command in U-Boot. Refer to the API document for more information on the functions implemented in the driver (in the doxygen folder of the documentation package).

To view what values the CPU frequency can be changed to in KHz (The values in the first column are the frequency values) use this command:

```
cat /sys/devices/system/cpu/cpu0/cpufreq/stats/time_in_state
```

To change the CPU frequency to a value that is given by using the command above (for example, to 800 MHz) use this command:

```
echo 800000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
```

The frequency `800000` is in KHz, which is `800` MHz.

The maximum frequency can be checked using this command:

```
cat /sys/devices/system/cpu/cpu0/cpufreq/scaling_max_freq
```

Use the following command to view the current CPU frequency in KHz:

```
cat /sys/devices/system/cpu/cpu0/cpufreq/cpuinfo_cur_freq
```

Use the following command to view available governors:

cat /sys/devices/system/cpu/cpu0/cpufreq/scaling_available_governors

Use the following command to set governors:

echo conservative > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor

21.2 Source Code Structure

Table 21-1 shows the source files and headers available in the following directory:

```
<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/
```

Table 21-1. CPUFREQ Driver Files

File	Description
cpufreq.c	CPUFREQ functions

For CPU frequency working point settings, see arch/arm/mach-mx5/mx53_wp.c.

21.3 Menu Configuration Options

The following Linux kernel configuration is provided for this module:

- CONFIG_CPU__FREQ—In menuconfig, this option is located under
  CPU Power Management > CPU Frequency scaling
  The following options can be selected:
  - CPU Frequency scaling
  - CPU frequency translation statistics
  - Default CPU frequency governor (userspace)
  - Performance governor
  - Powersave governor
  - Userspace governor for userspace frequency scaling
  - Conservative CPU frequency governor
  - CPU frequency driver for i.MX CPUs

21.3.1 Board Configuration Options

There are no board configuration options for the CPUFREQ device driver.

Chapter 22
Software Based Peripheral Domain Frequency Scaling

The frequency of the clocks in the peripheral domain can be changed using the software based Bus Frequency Scaling driver. Enabling this driver can significantly lower the power numbers in the LP domain. Depending on the platform, the voltage of the peripheral domain can also be dropped using the on board PMIC.

22.1 Software based Bus Frequency Scaling

The SW will automatically lower the frequency of the various clocks in the peripheral domain based on which drivers are active (it is assumed that the drivers will use the clock API to enable/disable their clocks). Two setpoints are defined for the peripheral bus clock:

AHB_HIGH_SET_POINT - The module requires the AHB clock to be at the highest frequency (133MHz).

AHB_MED_SET_POINT - The module requires the AHB clock be above 66.5MHz.

The Bus Frequency Scaling driver will take into account the above two associations for the various clocks in the system before changing the peripheral clock.

To enable the SW based Bus Frequency Scaling **(*not needed to enter LPAPM mode*)** use this command:

echo 1 > /sys/devices/platform/busfreq.0/enable

To disable the SW based Bus Frequency Scaling use this command:

echo 0 > /sys/devices/platform/busfreq.0/enable

Based on which clocks are active, the system can be in any of the three modes specified below:

22.1.1 Low Power Audio Playback Mode (LPAPM)

When all the clocks that need either of the above two mentioned setpoints are disabled, the system can enter an ultra low power mode where the AHB clock and other main clocks in the LP domain are dropped down to 24MHz (For MX53, AHB clock, AXI-B clocks are dropped to 400/8=50MHZ). On certain platforms and depending on the type of memory used, the DDR frequency is also dropped down to 24MHz. This mode is most commonly entered when the system is idle and the display is turned off. The implementation automatically detects when this mode can be entered and calls into the Bus Frequency driver to change the clocks (and voltages if it can be done) appropriately. On certain platforms, the entire SoC is clocked off the 24MHz oscillator and all PLLs are turned off to save more power.

If any driver that needs the higher AHB clock enables its clock, LPAPM mode will be exited. **Entry and exit from the LPAPM mode does not require the Bus Frequency Scaling driver to be enabled.**

22.1.2 Medium Frequency Setpoint

In this mode the AHB and some of the LP domain clocks are divided down such that the AHB clock is above 66.5MHz. In this mode all drivers that require AHB_HIGH_SET_POINT are disabled. Depending on the platform, the voltage can also be dropped.

22.1.3 High Frequency Setpoint

In this mode none of the frequencies on the peripheral domain are scaled since drivers that need the AHB_HIGH_SETPOINT are active.

22.2 Source Code Structure

Table 22-1 lists the source files and headers

Table 22-1. Bus Frequency Scaling Driver Files

File	directory	Description
bus_freq.c	arch/arm/mach-mx5	SW bus frequency driver functions

22.3 Menu Configuration Options

There is no option for the SW based Bus Frequency Scaling driver, it included by default.

22.3.1 Board Configuration Options

There are no board configuration options for the Linux Bus Frequency Scaling device driver.

Chapter 23
Advanced Linux Sound Architecture (ALSA) System on a Chip (ASoC) Sound Driver

This section describes the ASoC driver architecture and implementation. ASoC aims to improve code reuse by dividing the ALSA kernel driver into machine layer, platform (CPU) layer, and audio codec components. Any modifications to one component do not impact another components. The machine layer registers the platform layer and the audio codec, and sets up the connection between them, using the DAI link interface. More detailed information about ASoC can be found in the Linux kernel documentation in the linux source tree at linux/Documentation/sound/alsa/soc and at http://www.alsa-project.org/main/index.php/ASoC.

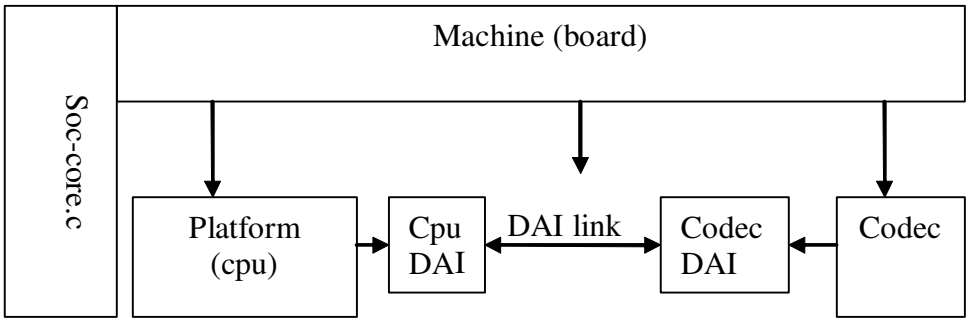


Figure 23-1. ALSA SoC Software Architecture

The ALSA SoC driver has the following components as shown in Figure 23-1:

- Machine driver—handles any machine specific controls and audio events, such as turning on an external amp at the beginning of playback.
- Platform driver—contains the audio DMA engine and audio interface drivers (for example, I^2S, AC97, PCM) for that platform.
- Codec driver—platform independent and contains audio controls, audio interface capabilities, the codec DAPM definition, and codec I/O functions.

23.1 SoC Sound Card

Currently, the stereo codec (`sgtl5000`), 5.1 codec (`wm8580`), 4-channel ADC codec (ak5702), 7.1 codec(cs42888), built-in ADC/DAC codec, and Bluetooth codec drivers are implemented using SoC architecture. The five sound card drivers are built in independently. The stereo sound card supports stereo playback and mono capture. The 5.1 sound card supports up to six channels of audio playback. The 4-channel sound card supports up to four channels of audio record. The Bluetooth sound card supports Bluetooth PCM playback and record with Bluetooth devices. The built-in ADC/DAC codec supports stereo playback and record.

NOTE

Only the Stereo Codec is supported on the i.MX53 START platform.

23.1.1 Stereo Codec Features

The stereo codec supports the following features:

- Sample rates for playback and capture are 32 KHz, 44.1 KHz, 48 KHz, and 96 KHz
- Channels:
  - Playback: supports two channels. (stereo)
  - Capture: supports two channels. (Only one channel has valid voice data due to hardware connection)
- Audio formats:
  - Playback:
    - SNDRV_PCM_FMTBIT_S16_LE
    - SNDRV_PCM_FMTBIT_S20_3LE
    - SNDRV_PCM_FMTBIT_S24_LE
  - Capture:
    - SNDRV_PCM_FMTBIT_S16_LE
    - SNDRV_PCM_FMTBIT_S20_3LE
    - SNDRV_PCM_FMTBIT_S24_LE

23.1.2 Sound Card Information

The registered sound card information can be listed as follows using the commands `aplay -l` and `arecord -l`.

```
root@freescale /$ aplay -l
**** List of PLAYBACK Hardware Devices ****
      card 0: imx3stack [imx-3stack], device 0: SGTL5000 SGTL5000-PCM-0 []
       Subdevices: 1/1
       Subdevice #0: subdevice #0
root@freescale /$ arecord -l
**** List of CAPTURE Hardware Devices ****
      card 0: imx3stack [imx-3stack], device 0: SGTL5000 SGTL5000-PCM-0 []
       Subdevices: 1/1
      Subdevice #0: subdevice #0
```

23.2 ASoC Driver Source Architecture

As shown in Figure 23-1, `imx-pcm.c` is shared by the stereo ALSA SoC driver, the 5.1 ALSA SoC driver and the Bluetooth codec driver. This file is responsible for preallocating DMA buffers and managing DMA channels.

The stereo codec is connected to the CPU through the SSI interface. `imx-ssi.c` registers the CPU DAI driver for the stereo ALSA SoC and configures the on-chip SSI interface. `sgtl5000.c` registers the stereo codec and hifi DAI drivers. The direct hardware operations on the stereo codec are in `sgtl5000.c`. `imx-3stack-sgtl5000.c` is the machine layer code which creates the driver device and registers the stereo sound card.

Figure 23-2 shows the ALSA SoC source file relationship.

Figure 23-2. ALSA Soc Source FIle Relationship

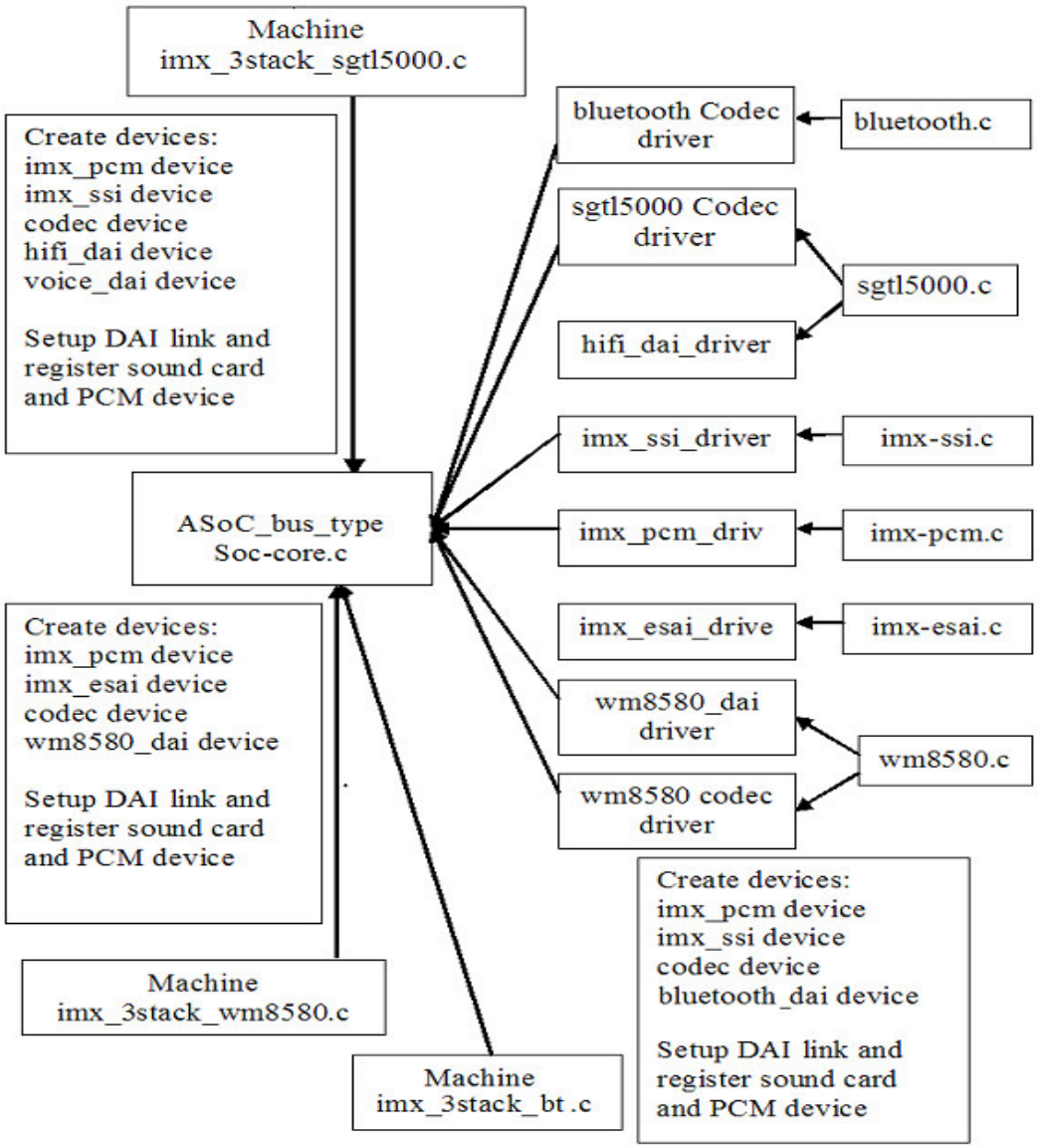


Table 23-1 shows the stereo codec SoC driver source files. These files are under the `<ltib_dir>/rpm/BUILD/linux/sound/soc` directory.

Table 23-1. Stereo Codec SoC Driver Files

File	Description
imx/imx-3stack-sgtl5000.c	Machine layer for stereo codec ALSA SoC
imx/imx-pcm.c	Platform layer for stereo codec ALSA SoC
imx/imx-pcm.h	Header file for PCM driver and AUDMUX register definitions

Table 23-1. Stereo Codec SoC Driver Files (continued)

File	Description
imx/imx-ssi.c	Platform DAI link for stereo codec ALSA SoC
imx/imx-ssi.h	Header file for platform DAI link and SSI register definitions
imx/imx-ac97.c	AC97 driver for i.MX chips
codecs/sgtl5000.c	Codec layer for stereo codec ALSA SoC
codecs/sgtl5000.h	Header file for stereo codec driver

23.3 Menu Configuration Options

The following Linux kernel configuration options are provided for this module. To get to these options, use the `./ltib -c` command when located in the `<ltib dir>`. Select **Configure the Kernel** on the screen displayed and exit. When the next screen appears, select the following options to enable this module:

- SoC Audio support for i.MX SGTL5000. In menuconfig, this option is available under

  Device drivers > Sound card support > Advanced Linux Sound Architecture > ALSA for SoC audio support > SoC Audio for the Freescale i.MX CPU
- CONFIG_SND_MXC_SOC_IRAM: This config is used to allow audio DMA playback buffers in IRAM. In menuconfig, this option is available under

  Device drivers > Sound card support > Advanced Linux Sound Architecture > ALSA for SoC audio support > Locate Audio DMA playback buffers in IRAM
- CONFIG_MXC_SSI_DUAL_FIFO: This config is used to enable 2 SSI FIFO for audio transfer. In menuconfig, this option is available under

  Device drivers > Sound card support > Advanced Linux Sound Architecture > ALSA for SoC audio support > MXC SSI enable dual fifo

23.4 Hardware Operation

The following sections describe the hardware operation of the ASoC driver.

23.4.1 Stereo Audio Codec

The stereo audio codec is controlled by the I^2C interface. The audio data is transferred from the user data buffer to/from the SSI FIFO through the DMA channel. The DMA channel is selected according to the audio sample bits. AUDMUX is used to set up the path between the SSI port and the output port which connects with the codec. The codec works in master mode and provides the BCLK and LRCLK. The BCLK and LRCLK can be configured according to the audio sample rate.

The SGTL5000 ASoC codec driver exports the audio record/playback/mixer APIs according to the ASoC architecture. The ALSA related audio function and the FM loopback function cannot be performed simultaneously.

The codec driver is generic and hardware independent code that configures the codec to provide audio capture and playback. It does not contains code that is specific to the target platform or machine. The codec driver handles:

- Codec DAI and PCM configuration
- Codec control I/O—using I^2C
- Mixers and audio controls
- Codec audio operations
- DAC Digital mute control

The SGTL5000 codec is registered as an I^2C client when the module initializes. The APIs are exported to the upper layer by the structure `snd_soc_dai_ops`. The `io_probe` routine initializes the codec hardware to the desired state.

Headphone insertion/removal can be detected through a MCU interrupt signal. The driver reports the event to user space through sysfs.

23.5 Software Operation

The following sections describe the hardware operation of the ASoC driver.

23.5.1 Sound Card Registration

The codecs have the same registration sequence:

1. The codec driver registers the codec driver, DAI driver, and their operation functions
2. The platform driver registers the PCM driver, CPU DAI driver and their operation functions, preallocates buffers for PCM components and sets playback and capture operations as applicable
3. The machine layer creates the DAI link between codec and CPU registers the sound card and PCM devices

23.5.2 Device Open

The ALSA driver:

- Allocates a free substream for the operation to be performed
- Opens the low level hardware device
- Assigns the hardware capabilities to ALSA runtime information. (the runtime structure contains all the hardware, DMA, and software capabilities of an opened substream)
- Configures DMA read or write channel for operation
- Configures CPU DAI and codec DAI interface.
- Configures codec hardware

- Triggers the transfer

After triggering for the first time, the subsequent DMA read/write operations are configured by the DMA callback.

23.6 Platform Data

struct mxc_audio_platform_data defined in include/linux/fsl_devices.h is used to pass the platform data of audio codec. Its value needs to be updated according to Hardware design.

- ssi_num: indicate which SSI channel is used.
- src_port: indicate which AUDMUX port is connected with SSI
- ext_port: indicate which AUDMUX port is connected with external audio codec.
- hp_irq: the irq number of headphone detect
- hp_status: the callback function to detect headphone status: inserted or removal
- init: the callback function to initialize audio codec. For example, configure the clock of audio codec
- See header file for the details of more variables.

Chapter 24
The Sony/Philips Digital Interface (S/PDIF) Driver

The Sony/Philips Digital Interface (S/PDIF) audio module is a stereo transceiver that allows the processor to receive and transmit digital audio. The S/PDIF transceiver allows the handling of both S/PDIF channel status (CS) and User (U) data and includes a frequency measurement block that allows the precise measurement of an incoming sampling frequency.

24.1 S/PDIF Overview

Figure 24-1 shows the block diagram of the S/PDIF interface.

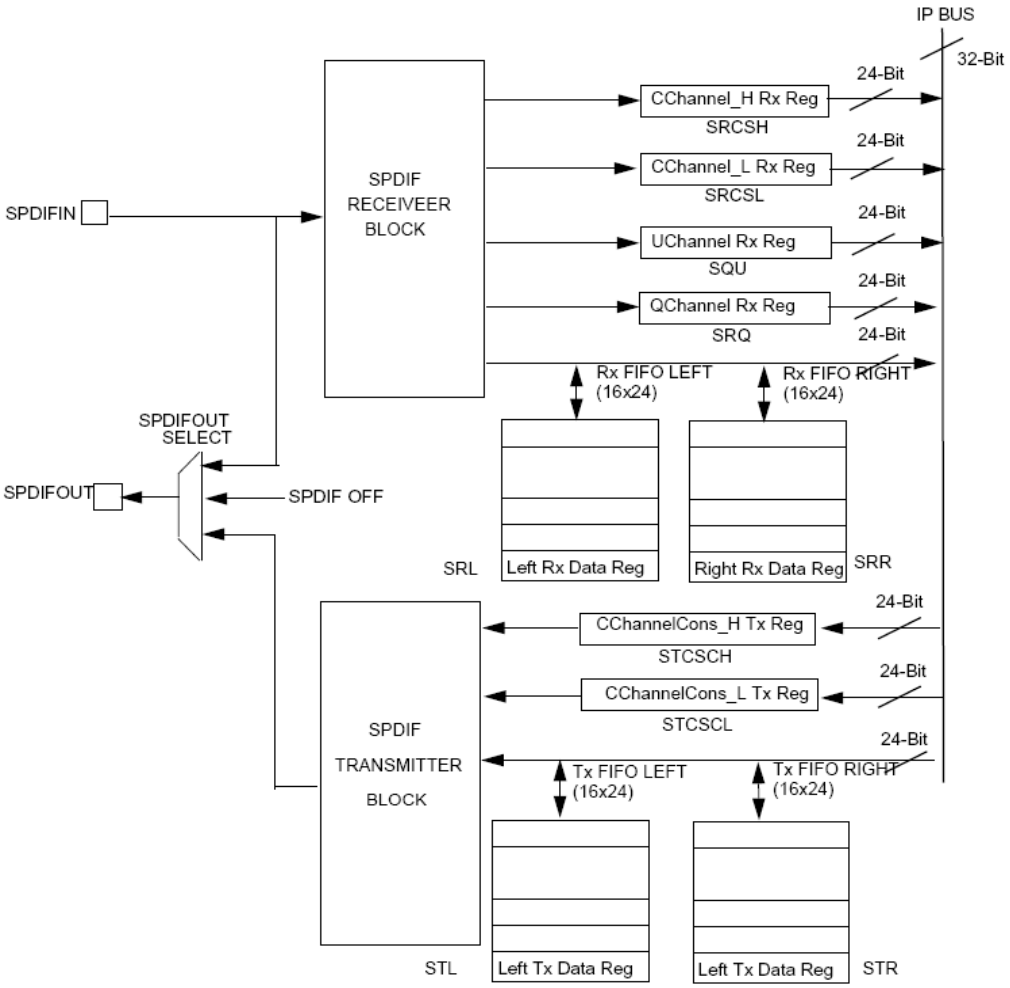


Figure 24-1. S/PDIF Transceiver Data Interface Block Diagram

24.1.1 Hardware Overview

The S/PDIF is composed of two parts:

- The S/PDIF receiver extracts the audio data from each S/PDIF frame and places the data in the S/PDIF Rx left and right FIFOs. The Channel Status and User Bits are also extracted from each frame and placed in the corresponding registers. The S/PDIF receiver provides a bypass option for direct transfer of the S/PDIF input signal to the S/PDIF transmitter.
- For the S/PDIF transmitter, the audio data is provided by the processor through the SPDIFTxLeft and SPDIFTxRight registers. The Channel Status bits are provided through the corresponding registers. The S/PDIF transmitter generates a S/PDIF output bitstream in the biphase mark format (IEC958), which consists of audio data, channel status and user bits.

In the S/PDIF transmitter, the IEC958 biphase bit stream is generated on both edges of the S/PDIF Transmit clock. The S/PDIF Transmit clock is generated by the S/PDIF internal clock dividers and the sources are from outside of the S/PDIF block. The S/PDIF receiver can recover the S/PDIF Rx clock from the S/PDIF stream. Figure 24-1 shows the clock structure of the S/PDIF transceiver. MX53 supports S/PDIF Rx and Tx. But some MX53 boards can only support S/PDIF Tx or Rx.

24.1.2 Software Overview

The S/PDIF driver is designed under ALSA System on Chip (ASoC) layer. The ASoC driver for S/PDIF provides one playback device for Tx and one capture device for Rx. The playback output audio format can be linear PCM data or compressed data with 16-bit default, up to 24-bit expandable support and the allowed sampling bit rates are 44.1, 48 or 32 KHz. The capture input audio format can be linear PCM data or compressed 24-bit data and the allowed sampling bit rates are from 16 to 96 KHz. The driver provides the same interface for PCM and compressed data transmission.

24.1.3 The ASoC layer

The point of the ASoC layer is to divide audio drivers for embedded platforms into separate layers that can be reused. ASoC divides an audio driver into a codec driver, a machine layer, a DAI (digital audio interface) layer, and a platform layer. The Linux kernel documentation has some concise description of these layers in linux/Documentation/sound/alsa/soc. In the case of the S/PDIF driver, we are able to reuse the platform layer (imx-pcm.c) that is used by the ssi stereo codec driver.

24.2 S/PDIF Tx Driver

The S/PDIF Tx driver supports the following features:

- 32, 44.1 and 48 KHz sample rates. MX53 START board only support in-accurate 48KHz sample rate.
- Signed 16 and 24-bit little Endian sample format. Due to S/PDIF SDMA feature, the 24-bit output sample file must have 32-bits in one channel per frame, and only the 24 LSBs are valid

  In the ALSA subsystem, the supported format is defined as S16_LE and S24_LE.
- Two channels
- Driver installation and information query

  If the driver is built as a kernel module, run modprobe to install it:

  ```
  #modprobe snd-spdif
  ```

— The device ID can be determined by using the ‘aplay -l’ or ‘arecord -l’ utility to list out the playback and record audio devices

For example:

```
root@freescale ~$ aplay -l
**** List of PLAYBACK Hardware Devices ****
card 0: imx3stack [imx-3stack], device 0: SGTL5000 SGTL5000-0 []
  Subdevices: 1/1
  Subdevice #0: subdevice #0
card 1: imx3stackspdif [imx-3stack-spdif], device 0: IMX SPDIF mxc spdif-0 []
  Subdevices: 1/1
  Subdevice #0: subdevice #0
```

— Also, the S/PDIF ALSA driver information is exported to user by /sys and /proc file system.

For example:

```
#cat /proc/asound/cards
0 [imx3stack      ]: SGTL5000 - imx-3stack
                     imx-3stack (SGTL5000)
1 [imx3stackspdif ]: mxc spdif - imx-3stack-spdif
                     imx-3stack-spdif (mxc spdif)
```

The number at the beginning of the MXC_SPDIF line is the card ID. The string in the square brackets is the card name

— Get Playback PCM device info

```
#cat /proc/asound/TXRX/pcm[card id]p/info
```

- Software operation

The ALSA utility provides a common method for user spaces to operate and use ALSA drivers

```
#aplay -D "hw:2,0" -t wav audio.wav
```

NOTE

The -D parameter of `aplay` indicates the PCM device with card ID and PCM device ID: `hw:[card id],[pcm device id]`

The “iecset” utility provides a common method to set or dump the IEC958 status bits.

```
#iecset -c 1
```

24.2.1 Driver Design

Before S/PDIF playback, the configuration, interrupt, clock and channel registers are initialized. During S/PDIF playback, the channel status bits are fixed. The DMA and interrupts are enabled. S/PDIF has 16 TX sample FIFOs on Left and Right channel respectively. When both FIFOs are empty, an empty interrupt is generated if the empty interrupt is enabled. If no data are refilled in the 20.8 μs (1/48000), an underrun interrupt is generated. Overrun is avoided if only 16 sample FIFOs are filled for each channel every time. If auto re-synchronization is enabled, the hardware checks if the left and right FIFO are in sync, and if not, it sets the filling pointer of the right FIFO to be equal to the filling pointer of the left FIFO and an interrupt is generated.

24.2.2 Provided User Interface

The S/PDIF transmitter driver provides one ALSA mixer sound control interface to the user besides the common PCM operations interface. It provides the interface for the user to write S/PDIF channel status codes into the driver so they can be sent in the S/PDIF stream. The input parameter of this interface is the IEC958 digital audio structure shown below, and only status member is used:

```
struct snd_aes_iec958 {
        unsigned char status[24];       /* AES/IEC958 channel status bits */
        unsigned char subcode[147];     /* AES/IEC958 subcode bits */
        unsigned char pad;              /* nothing */
        unsigned char dig_subframe[4];  /* AES/IEC958 subframe bits */
};
```

24.3 Interrupts and Exceptions

S/PDIF Tx/Rx hardware block has many interrupts to indicate the success, exception and event. The driver handles the following interrupts:

- DPLL Lock and Loss Lock—Saves the DPLL lock status; this is used when getting the Rx sample rate
- U/Q Channel Full and overrun/underrun—Puts the U/Q channel register data into queue buffer, and update the queue buffer write pointer
- U/Q Channel Sync—Saves the ID of the buffer whose U/Q data is ready for read out
- U/Q Channel Error—Resets the U/Q queue buffer

24.4 Source Code Structure

Table 24-1 lists the source files for the driver. These files are under the `<ltib_dir>/rpm/BUILD/linux/` directory.

Table 24-1. S/PDIF Driver Files

File	Description
sound/soc/codecs/mxc_spdif.c	S/PDIF ALSA SOC codec driver
sound/soc/codecs/mxc_spdif.h	S/PDIF ALSA SOC codec driver header
sound/soc/imx/imx-spdif.c	S/PDIF ALSA SOC machine layer
sound/soc/imx/imx-spdif.h	S/PDIF ALSA SOC machine layer header
sound/soc/imx/imx-spdif-dai.c	S/PDIF ALSA SOC DAI layer
sound/soc/imx/imx-pcm-dai.h	S/PDIF ALSA SOC DAI layer header
sound/soc/imx/imx-pcm.c	ALSA SOC platform layer
sound/soc/imx/imx-pcm.h	ALSA SOC platform layer header

24.5 Menu Configuration Options

The following Linux kernel configurations are provided for this module:

- CONFIG_SND—Configuration option for the Advanced Linux Sound Architecture (ALSA) subsystem. This option is dependent on CONFIG_SOUND option. In the menuconfig this option is available under

  Device Drivers > Sound card support > Advanced Linux Sound Architecture

  By default, this option is Y.
- CONFIG_SND_MXC_SPDIF—Configuration option for the S/PDIF driver. This option is dependent on CONFIG_SND option. In the menuconfig this option is available under

  Device Drivers > Sound card support > Advanced Linux Sound Architecture > ALSA for SoC audio support > SoC Audio support for IMX - S/PDIF. By default, this option is Y.
- SND_MXC_SOC_SPDIF_DAI and SND_SOC_MXC_SPDIF - automagically configured by CONFIG_SND_MXC_SPDIF. By default, these options are Y.

24.6 Platform Data

struct mxc_spdif_platform_data defined in include/linux/fsl_devices.h is used to pass SPDIF platform data according to the detailed Hardware design:

- spdif_tx: indicate whether TX is supported. 1 - support TX. 0- Don’t support TX
- spdif_rx: indicate whether RX is supported. 1 - support RX. 0- Don’t support RX
- spdif_clk_44100: indicate the clock source (in S/PDIF register STC) of 44.1KHz sample rate. -1 - Don’t support this sample rate.
- spdif_clk_48000: indicate the clock source (in S/PDIF register STC) of 48KHz sample rate. -1 - Don’t support this sample rate.
- spdif_core_clk: indicate SPDIF core clocks.
- See header file for the details about more variables.

Chapter 25
Asynchronous Sample Rate Converter (ASRC) Driver

The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs simultaneously.

25.1 Hardware Operation

ASRC includes the following features:

- Supports ratio (Fsin/Fsout) range between 1/24 to 8.
- Designed for rate conversion between 44.1 KHz, 32 KHz, 48 KHz, and 96 KHz.
- Other input sampling rates in the range of 8 KHz to 100 KHz are also supported, but with less performance (see IC spec for more details).
- Other output sampling rates in the range of 30 KHz to 100 KHz are also supported, but with less performance.
- Automatic accommodation to slow variations in the incoming and outgoing sampling rates.
- Tolerant to sample clock jitter.
- Designed mainly for real-time streaming audio usage. Can be used for non-realtime streaming audio usage when the input sampling clocks are not available.
- In any usage case, the output sampling clocks must be activated.
- In case of real-time streaming audio, both input and output clocks need to be available and activated.
- In case of non-realtime streaming audio, the input sampling rate clocks can be avoided by setting ideal-ratio values into ASRC interface registers.

The ASRC supports polling, interrupt and DMA modes, but only DMA mode is used in the platform for better performance. The ASRC supports following DMA channels:

- Peripheral to peripheral, for example: ASRC to SPDIF
- Memory to peripheral, for example: memory to ASRC
- Peripheral to memory, for example: ASRC to memory

For more information, see the chapter on ASRC in the *Multimedia Applications Processor* documentation.

25.2 Software Operation

As an assistant component in the audio system, the ASRC driver implementation depends on the use cases in the platform. Currently ASRC is used in following two scenarios.

- Memory > ASRC > Memory, ASRC is controlled by user application or ALSA plug-in.
- Memory > ASRC > peripheral, ASRC is controlled directly by other ALSA driver.

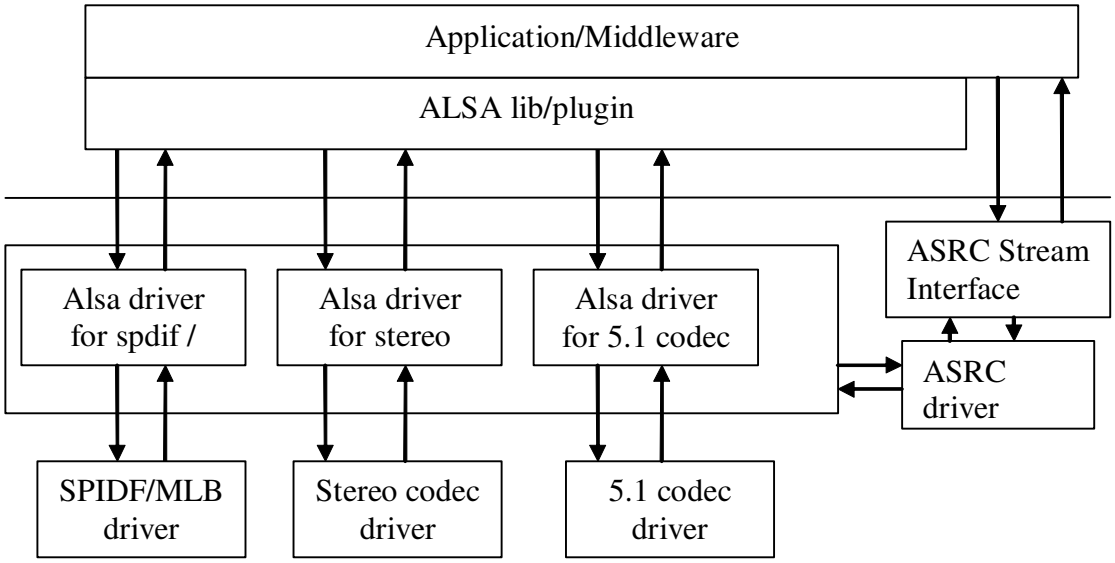


Figure 25-1. Audio Driver Interactions

As illustrated in Figure 25-1, the ASRC stream interface provides the interface for the user space. The ASRC registers itself under `/dev/mxc_asrc` and creates proc file `/proc/driver/asrc` when the module is inserted. proc is used to track the channel number for each pair. If all the pairs are not used, users can adjust the channel number through the proc file. The total channels number should equal five, or else the adjusted value cannot be saved properly. The minimum unit here is one (two channels), for example three represents six channels (three pairs).

25.2.1 Sequence for Memory to ASRC to Memory

- Open `/dev/mxc_asrc` device
- Request ASRC pair - ASRC_REQ_PAIR
- Configure ASRC pair - ASRC_CONIFG_PAIR
- Query DMA buffer info - ASRC_QUERYBUF
- Write the raw audio data (to be converted) into the DMA input buffer. Then, put the DMA input buffer in the input buffer queue (ASRC_Q_INBUF) and put the DMA output buffer in the output buffer queue (ASRC_Q_OUTBUF), so that the ASRC driver can get the buffers. To avoid an underrun, it would be better to queue in three buffers to both input and output.
- Start ASRC - ASRC_START_CONV
- Dequeue ASRC output and input buffer, copy the converted audio data for further process from output buffer and write new audio data to input buffer.
- Repeat enqueue and dequeue steps until conversion is complete
- Stop ASRC conversion - ASRC_STOP_CONV
- Release ASRC pair - ASRC_RELEASE_PAIR
- Close `/dev/mxc_asrc` device

25.2.2 Sequence for Memory to ASRC to Peripheral

- The sound card has been registered and start to enable the DMA channel in ALSA driver
- Request ASRC pair - asrc_req_pair
- Configure ASRC pair - asrc_config_pair
- Enable the DMA channel from Memory to ASRC and from ASRC to Memory
- Start DMA channel and start ASRC conversion - asrc_start_conv
- When audio data playback complete, stop DMA channel and ASRC - asrc_stop_conv
- Release ASRC pair - asrc_release_pair

25.3 Source Code Structure

Table 25-1 lists the source files available in the devices directory:

```
<ltib_dir>/rpm/BUILD/linux/drivers/mxc/asrc
<ltib_dir>/rpm/BUILD/linux/include/linux/
```

Table 25-1. ASRC Source File List

File	Description
mxc_asrc.h	ASRC register definitions and export function declarations
mxc_asrc.c	ASRC driver implementation codes including stream interface

25.3.1 Linux Menu Configuration Options

Device drivers > MXC support drivers > MXC Asynchronous Sample Rate Converter support > ASRC support

25.4 Platform Data

struct mxc_asrc_platform_data defined in include/linux/fsl_devices.h is used to pass the platform information of ASRC according to different SOC:

- channel_bits: indicates the channel bit information.
- clk_map_ver: the mapping relationship in different SOC is different. This version number can be used to indicate clock map information.
- asrc_core_clk: asrc core clock information which is used as ASRC register access.
- asrc_audio_clk: asrc process clock.

25.5 Programming Interface (Exported API and IOCTLs)

The ASRC Exported API allows the ALSA driver to use ASRC services. The ASRC IOCTLs in Table 25-2 are used for user space applications.

Table 25-2. ASRC Exported Functions

Function/ioctl	Description
`int asrc_req_pair(int chn_num, enum asrc_pair_index *index)`	Request the ASRC pair
`void asrc_release_pair (enum asrc_pair_index index)`	Release ASRC pair
`int asrc_config_pair (struct asrc_config *config)`	Configure the ASRC hardware
`void asrc_start_conv (enum asrc_pair_index index)`	Start ASRC conversion for specific pair
`void asrc_stop_conv (enum asrc_pair_index index)`	Stop ASRC conversion
`ASRC_REQ_PAIR`	Request ASRC pair
`ASRC_CONIFG_PAIR`	Configure ASRC pair and allocate DMA buffer
`ASRC_RELEASE_PAIR`	Release ASRC pair and release DMA buffer
`ASRC_QUERYBUF`	Query buffer information
`ASRC_Q_INBUF`	Queue ASRC input buffer (audio data to be converted)
`ASRC_DQ_INBUF`	Dequeue ASRC input buffer (audio processed)
`ASRC_Q_OUTBUF`	Queue ASRC output buffer (empty buffer to hold the converted buffer)
`ASRC_DQ_OUTBUF`	Dequeue ASRC output buffer (buffer hold converted audio data)
`ASRC_START_CONV`	Start ASRC conversion
`ASRC_STOP_CONV`	Stop ASRC conversion

-
  - 0 -- INCLK_NONE
  - 1 -- INCLK_ESAI_RX
  - 2 -- INCLK_SSI1_RX
  - 3 -- INCLK_SSI2_RX
  - 4 -- INCLK_SPDIF_RX
  - 5 -- INCLK_MLB_CLK
  - 6 -- INCLK_ESAI_TX
  - 7 -- INCLK_SSI1_TX
  - 8 -- INCLK_SSI2_TX
  - 9 -- INCLK_SPDIF_TX
  - 10 -- INCLK_ASRCK1_CLK
  - default option for input clock source is 0, using the INCLK_NONE option.
  - 0 -- OUTCLK_NONE
  - 1 -- OUTCLK_ESAI_TX

— 2 -- OUTCLK_SSI1_TX
— 3 -- OUTCLK_SSI2_TX
— 4 -- OUTCLK_SPDIF_TX
— 5 -- OUTCLK_MLB_CLK
— 6 -- OUTCLK_ESAI_RX
— 7 -- OUTCLK_SSI1_RX
— 8 -- OUTCLK_SSI2_RX
— 9 -- OUTCLK_SPDIF_RX
— 10 -- OUTCLK_ASRCK1_CLK
— default option for output clock source is 10, using the OUTCLK_ASRCK1_CLK option.

Chapter 26
SATA Driver

26.1 Hardware Operation

The detailed hardware operation of SATA is detailed in the Synopsys DesignWare Cores SATA AHCI documentation, named SATA_Data_Book.pdf.

26.2 Software Operation

The details about the libata APIs, see the libATA Developer's Guide named libata.pdf pulished by Jeff Gazik.

The SATA AHCI driver is based on the LIBATA layer of the block device infrastructure of the Linux kernel . FSL integrated AHCI linux driver combined the standard AHCI drivers handle the details of the integrated freescale's SATA AHCI controller, while the LIBATA layer understands and executes the SATA protocols. The SATAdevice, such as a hard disk, is exposed to the application in user space by the /dev/sda* interface. Filesystems are built upon the block device. The AHCI specified integrated DMA engine, which assists the SATA controller hardware in the DMA transfer modes.

26.3 Source Code Structure Configuration

The source codes of freescale's AHCI sata driver is integrated into the plat-mxc relative files.
`<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/ahci_sata.c.`

The standard AHCI and AHCI platform drivers are used to do the actual sata operations.

The source codes of the standard AHCI and AHCI platform drivers are located in `drivers/ata/` folder, named as ahci.c and ahci-platform.c.

26.4 Linux Menu Configuration Options

The following Linux kernel configurations are provided for SATA driver:

- CONFIG_SATA_AHCI_PLATFORM: Configure options for SATA driver. In the menuconfig this option is available under "Device Drivers --->Serial ATA (prod) and Parallel ATA (experimental) drivers -> Platform AHCI SATA support".
- CONFIG_SATA_AHCI_FSL_NO_HOTPLUG_MODE: Configure options to disable SATA HOTPLUG mode which is used to close SATA internal clock if SATA device is not found. In the menuconfig this option is available under "Device Drivers --->Serial ATA (prod) and Parallel ATA (experimental) drivers -> Freescale i.MX SATA AHCI NO HOTPLUG mode"

In busybox, enable "fdisk" under "Linux System Utilities".

26.5 Board Configuration Options

With the power off, install the SATA cable and hard drive.

26.6 Programming Interface

The application interface to the SATA driver is the standard POSIX device interface (for example: open, close, read, write, and ioctl) on `/dev/sda*`.

26.7 Usage Example

NOTE

There would be a known error message when the SATA disk is initialized, such as:

ata1.00: serial number mismatch '090311PB0300QKG3TB1A' != ''

ata1.00: revalidation failed (errno=-19)

pls ignore that.

1. After building the kernel and the SATA AHCI driver and deploying, boot the target, and log in as root.
2. Make sure that the AHCI and AHCI paltform drivers are built in kernel or loaded into kernel. Use the following commands to load the drivers into kernel.

```
# insmod libata.ko
# insmod libahci.ko
# insmod ahci-platform.ko
```

You should see messages similar to the following:

```
ahci: SSS flag set, parallel bus scan disabled
ahci ahci.0: AHCI 0001.0100 32 slots 1 ports 3 Gbps 0x1 impl platform mode
ahci ahci.0: flags: ncq sntf stag pm led clo only pmp pio slum part ccc
scsi0 : ahci
ata1: SATA max UDMA/133 irq_stat 0x00000040, connection status changed irq 28
ata1: SATA link up 1.5 Gbps (SStatus 113 SControl 300)
ata1.00: ATA-8: Hitachi HTS545032B9A300, PB3OC60G, max UDMA/133
ata1.00: 625142448 sectors, multi 0: LBA48 NCQ (depth 31/32)
ata1.00: serial number mismatch '090311PB0300QKG3TB1A' != ''
ata1.00: revalidation failed (errno=-19)
ata1: limiting SATA link speed to 1.5 Gbps
ata1.00: limiting speed to UDMA/133:PIO3
ata1: SATA link up 1.5 Gbps (SStatus 113 SControl 310)
ata1.00: configured for UDMA/133
scsi 0:0:0:0: Direct-Access     ATA      Hitachi HTS54503 PB3O PQ: 0 ANSI: 5
sd 0:0:0:0: [sda] 625142448 512-byte logical blocks: (320 GB/298 GiB)
sd 0:0:0:0: [sda] Write Protect is off
sd 0:0:0:0: [sda] Write cache: enabled, read cache: enabled, doesn't support DPO or
FUA
 sda: sda1 sda2 sda3
sd 0:0:0:0: [sda] Attached SCSI disk
```

You may use standard Linux utilities to partition and create a file system on the drive (for example: fdisk and mke2fs) to be mounted and used by applications.

The device nodes for the drive and its partitions appears under `/dev/sda*`. For example, to check basic kernel settings for the drive, execute `hdparm /dev/sda`.

26.8 Usage Example

Create Partitons

The following command can be used to find out the capacities of the hard disk. If the hard disk is pre-formatted, this command shows the size of the hard disk, partitions, and filesystem type:

```
$fdisk –l /dev/sda
```

If the hard disk is not formatted, create the partitions on the hard disk using the following command:

```
$fdisk /dev/sda
```

After the partition, the created files resemble `/dev/sda[1-4]`.

Block Read/Write Test:

The command, `dd`, is used for for reading/writing blocks. Note this command can corrupt the partitions and filesystem on Hard disk.

To clear the first 5 KB of the card, do the following:

```
$dd if=/dev/zero of=/dev/sda1 bs=1024 count=5
```

The response should be as follows:

5+0 records in

5+0 records out

To write a file content to the card enter the following text, substituting the name of the file to be written for `file_name`, do the following:

```
$dd if=file_name of=/dev/sda1
```

To read 1KB of data from the card enter the following text, substituting the name of the file to be written for `output_file`, do the following:

```
$dd if=/dev/sda1 of=output_file bs=1024 count=1
```

Files System Tests

Format the hard disk partitons using mkfs.vfat or mkfs.ext2, depending on the filesystem:

```
$mkfs.ext2 /dev/sda1
$mkfs.vfat /dev/sda1
```

Mount the file system as follows:

```
$mkdir /mnt/sda1
$mount –t ext2 /dev/sda1 /mnt/sda1
```

After mounting, file/directory, operations can be performed in `/mnt/sda1`.

Unmount the filesystem as follows:

```
$umount /mnt/sda1
```

26.9 SATA temperature monitor

The SATA temperature sensor driver is conformed to hardware monitor framework. The following command can be used to get temperature:

```
cat /sys/class/hwmon/hwmon1/device/temp1_input
```

Or run the following command to get temperature if lm-sensors package is installed:

```
$ sensors
imx-ahci-hwmon-isa-0000
Adapter: ISA adapter
temp1:        +58.0 C
```

Chapter 27
MMC/SD/SDIO Host Driver

The MultiMediaCard (MMC)/ Secure Digital (SD)/ Secure Digital Input Output (SDIO) Host driver implements a standard Linux driver interface to the enhanced MMC/SD host controller (eSDHC). The host driver is part of the Linux kernel MMC framework.

The MMC driver has the following features:

- 1-bit or 4-bit operation for SD and SDIO cards
- Supports card insertion and removal detections
- Supports the standard MMC commands
- PIO and DMA data transfers
- Power management
- Supports 1/4/8-bit operations for MMC cards
- Support eMMC4.4 SDR and DDR mode

27.1 Hardware Operation

The MMC communication is based on an advanced 11-pin serial bus designed to operate in a low voltage range. The eSDHC module support MMC along with SD memory and I/O functions. The eSDHC controls the MMC, SD memory, and I/O cards by sending commands to cards and performing data accesses to and from the cards. The SD memory card system defines two alternative communication protocols: SD and SPI. The eSDHConly support the SD bus protocol.

The eSDHC command transfer type and eSDHC command argument registers allow a command to be issued to the card. The eSDHC command, system control and protocol control registers allow the users to specify the format of the data and response and to control the read wait cycle.

The block length register defines the number of bytes in a block (block size). As the Stream mode of MMC is not supported, the block length must be set for every transfer.

There are four 32-bit registers used to store the response from the card in the eSDHC. The eSDHC reads these four registers to get the command response directly. The eSDHC uses a fully configurable 128×32-bit FIFO for read and write. The buffer is used as temporary storage for data being transferred between the host system and the card, and vice versa. The eSDHC data buffer access register bits hold 32-bit data upon a read or write transfer.

For receiving data, the steps are as follows:

1. The eSDHC controller generates a DMA request when there are more words received in the buffer than the amount set in the RD_WML register
2. Upon receiving this request, DMA engine starts transferring data from the eSDHC FIFO to system memory by reading the data buffer access register

To transmitting data, the steps are as follows:

1. The eSDHC controller generates a DMA request whenever the amount of the buffer space exceeds the value set in the WR_WML register
2. Upon receiving this request, the DMA engine starts moving data from the system memory to the eSDHC FIFO by writing to the Data Buffer Access Register for a number of pre-defined bytes

The read-only eSDHC Present State and Interrupt Status Registers provide eSDHC operations status, application FIFO status, error conditions, and interrupt status.

When certain events occur, the module has the ability to generate interrupts as well as set the corresponding Status Register bits. The eSDHC interrupt status enable and signal enable registers allow the user to control if these interrupts occur.

27.2 Software Operation

The Linux OS contains an MMC bus driver which implements the MMC bus protocols. The MMC block driver handles the file system read/write calls and uses the low level MMC host controller interface driver to send the commands to the eSDHC.

The MMC driver is responsible for implementing standard entry points for init, exit, request, and set_ios. The driver implements the following functions:

- The init function `sdhci_drv_init()`—Registers the device_driver structure.
- The probe function `sdhci_probe and sdhci_probe_slot()`—Performs initialization and registration of the MMC device specific structure with MMC bus protocol driver. The driver probes for memory and IRQ resources. Configures the IOMUX to enable eSDHC I/O pins and resets the hardware.
- `sdhci_set_ios()`—Sets bus width, voltage level, and clock rate according to core driver requirements.
- `sdhci_request()`—Handles both read and write operations. Sets up the number of blocks and block length. Configures an DMA channel, allocates safe DMA buffer and starts the DMA channel. Configures the eSDHC transfer type register eSDHC command argument register to issue a command to the card. This function starts the SDMA and starts the clock.
- MMC driver ISR `sdhci_cd_irq()`—Called when the MMC/SD card is detected or removed.
- MMC driver ISR `sdhci_irq()`—Interrupt from eSDHC called when command is done or errors like CRC or buffer underrun or overflow occurs.
- DMA completion routine `sdhci_dma_irq()`—Called after completion of a DMA transfer. Informs the MMC core driver of a request completion by calling `mmc_request_done()` API.

Figure shows how the MMC-related drivers are layered.

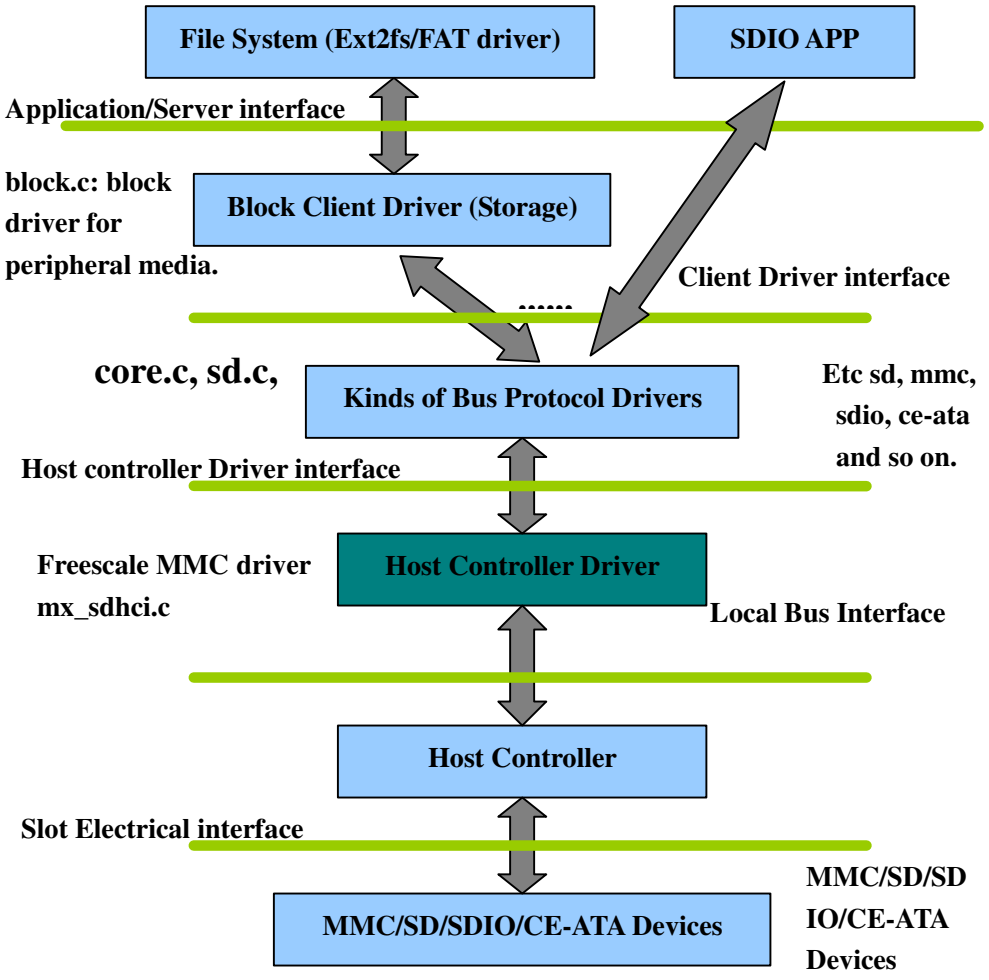


Figure 27-1. MMC Drivers Layering

27.3 Driver Features

The MMC driver supports the following features:

- Supports multiple eSDHC modules
- Provides all the entry points to interface with the Linux MMC core driver
- MMC and SD cards
- Recognizes data transfer errors such as command time outs and CRC errors
- Power management

27.4 Source Code Structure

Table 27-1 shows the eSDHC source files available in the source directory:
`<ltib_dir>/rpm/BUILD/linux/drivers/mmc/host/.`

Table 27-1. eSDHC Driver Files MMC/SD Driver Files

File	Description
mx_sdhci.h	Header file defining registers
mx_sdhci.c	eSDHC driver

27.5 Menu Configuration Options

The following Linux kernel configuration options are provided for this module. To get to these options, use the `./ltib -c` command when located in the `<ltib dir>`. On the screen displayed, select Configure the Kernel and exit. When the next screen appears, select the following options to enable this module:

- CONFIG_MMC—Build support for the MMC bus protocol. In menuconfig, this option is available under

  Device Drivers > MMC/SD/SDIO Card support

  By default, this option is Y.
- CONFIG_MMC_BLOCK—Build support for MMC block device driver, which can be used to mount the file system. In `menuconfig`, this option is available under

  Device Drivers > MMC/SD Card Support > MMC block device driver

  By default, this option is Y.
- CONFIG_MMC_IMX_ESDHCI—Driver used for the i.MX eSDHC ports. In menuconfig, this option is found under

  Device Drivers > MMC/SD Card Support > Freescale i.MX Secure Digital Host Controller Interface support
- CONFIG_MMC_IMX_ESDHCI_PIO_MODE—Sets i.MX Multimedia card Interface to PIO mode. In menuconfig, this option is found under

  Device Drivers > MMC/SD Card support > Freescale i.MX Secure Digital Host Controller Interface PIO mode

  This option is dependent on CONFIG_MMC_IMX_ESDHCI. By default, this option is not set and DMA mode is used.
- CONFIG_MMC_UNSAFE_RESUME—Used for embedded systems which use a MMC/SD/SDIO card for rootfs. In menuconfig, this option is found under

  Device drivers > MMC/SD/SDIO Card Support > Allow unsafe resume.

27.6 Platform Data

struct mxc_mmc_platform_data defined in arch/arm/plat-mxc/include/mach/mmc.h is used to pass platform informaton:

- .caps: set the capability of the slot. 1bit, 4bit or 8bit mode. SDR mode or DDR mode

- .min_clk: the minimal clock value
- .max_clk: the maxium clock value
- .card_inserted_state: indicated the card status. If no CD pin was connected, the value can be set as 1.
- .status: the callback function to get card status: inserted or removed.
- .wp_status: the callback function to check write protection status
- .clock_mmc: the clock name of SDHC.
- See the header file for more variables. The user should pass the right platform to enable MMC/SD according to HW information.

27.7 How to add a SDHC slot support

To add a SDHC slot support, PIN, clock, platform data need to be taken into consideration. Take SDHC3 slot in MX53 START as the example, the following changes need to be done:

- Modify arch/arm/mach-mx5/mx53_loco.c to add PIN supports. In mx53_loco_pads, add for example MX53_PAD_ATA_DATA8__SD3_DAT0. In mx53_loco_io_init, do gpio configurations for CD and WP pins.
- In arch/arm/mach-mx5/devices.c, ensure mxcsdhc3_device and mxcsdhc3_resources are configured.
- Check arch/arm/mach-mx5/clock.c and ensure esdhc3_clk is configured well.
- Modify arch/arm/mach-mx5/mx53_loco.c to register sdhc3 device. Add platform data “mmc3_data” and call “mxc_register_device(&mxcsdhc3_device, &mmc3_data);”

27.8 Programming Interface

This driver implements the functions required by the MMC bus protocol to interface with the i.MX eSDHCmodule. See the *BSP API* document (in the doxygen folder of the documentation package), for additional information.

Chapter 28
Symmetric/Asymmetric Hashing and Random Accelerator (Sahara) Drivers

28.1 Overview

The Symmetric/Asymmetric Hashing and Random Accelerator (Sahara) implements block encryption algorithms, hashing algorithms, a stream cipher algorithm, public key algorithms, and pseudo-random number generation. It has a slave IP bus interface for the host to write configuration and command information, and to read status information. It also has a DMA controller, with an AHB bus interface, to reduce the burden on the host to move the required data to and from memory.

28.2 Software Operation

28.2.1 API Notes

Kernel users should not use blocking mode unless the code is operating on behalf of the kernel process which needs to sleep because blocking mode attempts to put the current process to sleep. Therefore blocking mode cannot be used from bottom half code or from interrupt code.

Kernel users must provide a `kmalloc`-ed buffer address for all data types (key structures, context structures, input/output buffers, and so on)

User-mode users should beware of (or even avoid) using the stack for I/O, as cache line boundaries can cause problems. This can even be true for such simple things as having a context object on the stack, or retrieving a random number into a `uint32_t` stack variable. This applies to key structures, context structures, and input/output buffers.

28.2.2 Architecture

The conceptual model is shown in Figure 28-1. All of the processes in Figure 28-1 are implemented as common code, except for the following platform-centric processes:

- UM Extension
- Init/Cleanup
- Translator
- Completion Notification

The driver operates in poll or interrupt mode, based on how the code is built (compile time option). The modes are mutually exclusive.

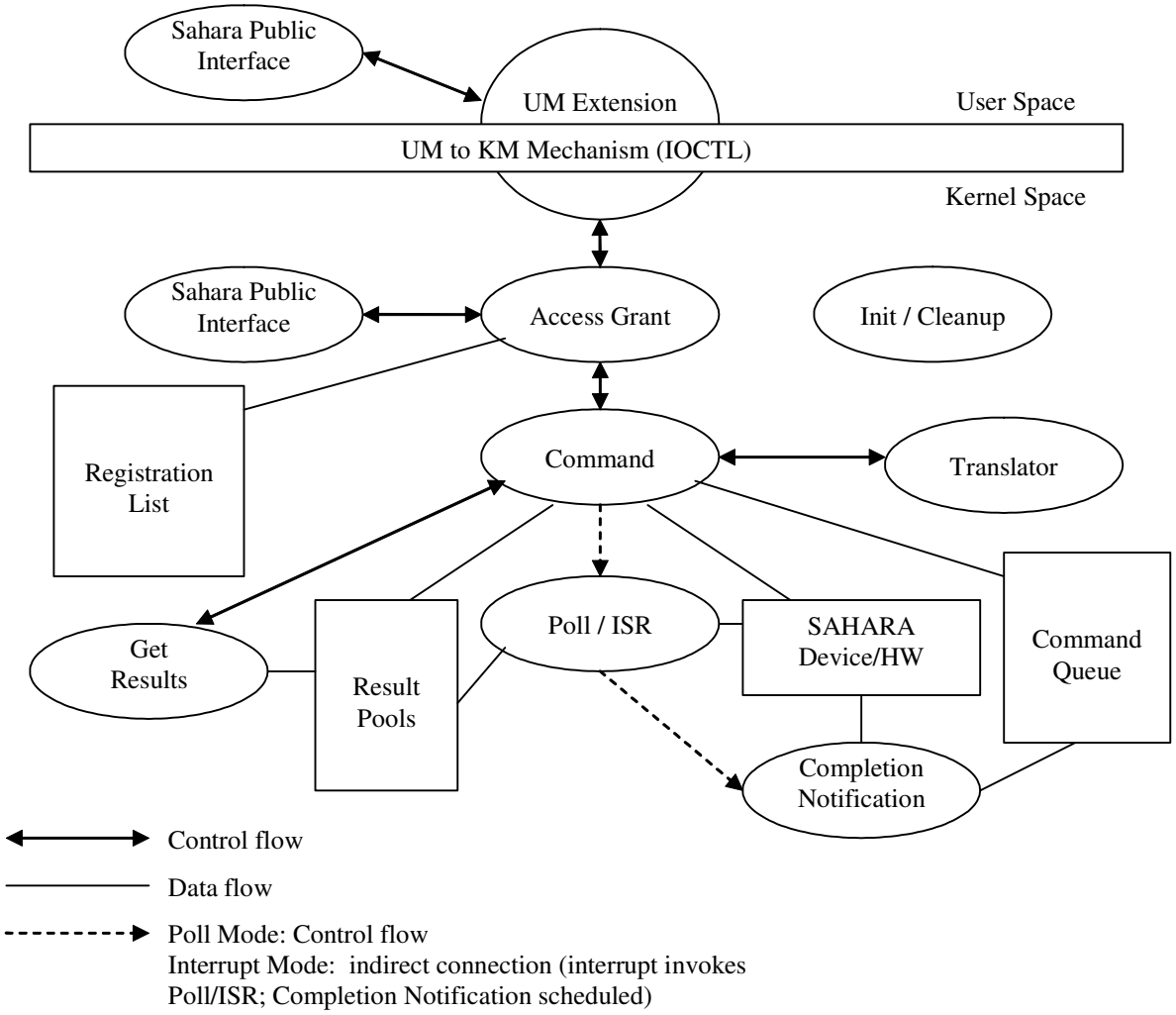


Figure 28-1. Sahara Architecture Overview

28.2.2.1 Registration List

The registration list maintains a list of the tasks that are registered with the driver.

28.2.2.2 Command Queue

The command queue maintains a list of commands (pointers to descriptor chains and their associated user) destined for the Sahara hardware. A pointer is maintained to the current (active) command as well as where the next command is to be entered into the queue.

28.2.2.3 Result Pools

The results pool maintains a list of completed commands. After the Sahara hardware completes, the status, along with its user association is placed in this pool.

28.2.2.4 Sahara Hardware

28.2.2.5 Initialize and Cleanup

This process is invoked by the OS to do the following tasks:

- Initialize the driver when the OS wishes to start the driver
- Cleanup the driver when the OS wishes to shut down the driver

The following stops are used to initialize the driver:

1. Map Sahara registers into kernel space
2. Check that the Sahara version number is
3. Attach handler to Sahara interrupt line (top half) if in interrupt mode
4. Initialize Sahara interrupt
5. Seed the random number generator. The RNG Auto Reseed in the control register cannot be set at startup (Hardware Erratum for RNG reseed). The available choices are:
   — Set this bit after the first random number is obtained
   — Never set this bit but rather detect when the `RNG Reseed Req` bit is set in the Status register and put the RNG in Seed Generation Mode. This is used for this architecture
   — Check for the reseed and set auto reseed when it becomes true
6. Install the tasklet (bottom half), if in interrupt mode (that is, install Complete Notification process)
7. Set up pointers to the command queue, the result pool, and the registration list
8. Populate the Capability Object (most of this can be done at compile time) as follows:
   — Command queue size
   — Result pool size
   — Registration list size
   — Driver version number
   — Algorithms and modes
9. Zero/initialize registration list, command queue, and result pool
10. Register as a device (to IOCTL)
11. If a failure is encountered anywhere within the Init subprocess, it is terminated, the Cleanup subprocess is initiated and an error is returned to the OS

The following steps are used to clean up a process:

1. Unregister as a device (to IOCTL)
2. Uninstall interrupt handler (top half) if in interrupt mode
3. Uninstall tasklet (bottom half) if in interrupt mode

4. Reset Sahara (leave Sahara interrupt disabled)
5. Null pointers to command queue, result pool, and registration list

28.2.2.6 Sahara Public Interface

This is the only access users are permitted to the Sahara functionality (Refer to the API document included in doxygen format). The interface is the same in both User and Kernel Space.

- Converts service requests into descriptor chains, for those requests that required descriptors
  - For final block of data, ensure that it is consumed correctly (Hardware Erratum for buffer length issue)
  - Descriptor pointers are created based on information in the SKO, HCO, and/or SCCO
  - Descriptor pointers reference input and output data buffers, fields in the SKO, HCO, and/or SCCO
- Returns error if input parameters are inconsistent or otherwise in error
- Passes pointers to a descriptor chain and a UCO to the next process
- Receives status information from the rest of the driver to return through the API return value
- Passes raw descriptor chains through (must be registered, that is, have a UCO). It is necessary to determine if the hardware erratum for buffer length issue applies to this descriptor chain and, if so, modify the chain appropriately
- Passes information into, and receives from, the Access Grant or UM Extension process, as appropriate

28.2.2.7 UM Extension

When the Sahara public interface is built for user space, the user mode extension is included in the build to provide a way for the user space sahara public interface to communicate into kernel mode.

- Transports information passed from Sahara Public Interface from User to Kernel space and back
- Passes information into, and receives from, the Access Grant process
- Passes information into, and receives from, the Sahara Public Interface in User Space
- When signaled by the Completion Notification process, invokes the User callback routine (the callback was acquired during registration)

28.2.2.8 Access Grant

All tasks must be registered with the driver before being able to request services.

- If this is a registration request, do the following:
  - Enter user information in Registration List, such as: ID, maximum number of outstanding commands possible (Result Pool size requested)
  - Populate its User Context Object
  - Return `success` or `failure` as appropriate
- If this is a deregistration request and the user is not registered, return `never registered`

- If this is a deregistration request and the user is registered
  - Remove user information in Registration List
  - Depopulate its User Context Object
  - Return `success` or `failure` as appropriate
- If this is not a registration or deregistration request (that is, any other User request), access the Registration List to see if the requestor is registered with the driver
  - If User is registered, pass the request to the Command process
  - If the User is not registered, return `unregistered` error to the requesting process

28.2.2.9 Command

The Command determines what service was requested and directs the driver to fulfill that service. The system determines whether it is a service that the driver can fulfill without the use of the Sahara HW or not

For requests that involve Sahara hardware, the system does the following:

1. Checks that there is room in the Command Queue. If there is not, returns a `queue full` status and terminates
2. Checks that there is room in the Result Pool. If there is not, returns a `pool full` status and terminates
3. Checks that this user has not reached its maximum number of outstanding requests. If it has, return `request limit reached`
4. Invokes the Translator process to convert received memory addresses
5. If Command Queue is empty, enters descriptor chain pointer into the Sahara Descriptor Address Register (DAR). This starts the processing of descriptors which continues until the Command Queue is empty
6. Enters the UCO and descriptor pointer in Command Queue, and whatever additional information may be needed, to await execution
7. Checks if the `RNG Reseed Req` bit is set in the Status register and, if so, puts an RNG Reseed descriptor into the command queue to reseed the RNG

User Blocking/Non-blocking requests are handled as listed Table 28-1.

Table 28-1. Blocking/Non-Blocking Definitions

Feature	Driver Poll Mode	Driver Interrupt Mode
User Blocking	User waits for request completion. Driver never gives up processor.	User waits for request completion. Driver queues request, suspends calling task, and releases processor (on completion the Driver un-suspends task / returns)
User Non-blocking with callback	Driver never gives up processor, therefore User is blocked until request completion (the callback is invoked prior to request completion)	Driver queues request and returns. Upon request completion, the callback is invoked
User Non-blocking without callback	Driver never gives up processor, therefore User is blocked until request completion	Driver queues request and returns. (User is not given any indication of completion. It enters a User Poll mode and polls for the results)

8. If in poll mode, transfer control to Poll/ISR process (if in interrupt mode, the Poll/ISR process is invoked through the interrupt mechanism)

Requests that do not involve Sahara hardware, are processed and immediately returned to the user. For example, if a `get results` request is received, the list is populated with the user results and the driver returns to the user.

28.2.2.10 Translator

The translator has the following features:

- Translates pointer addresses from virtual addresses to physical addresses
- Ensures that blocks of data that have become fragmented due to page discontinuity are handled with links in the descriptor chain
- Locks pages so addresses remain stable
- Clears processor cache

28.2.2.11 Polling and Interrupts

Polling has the following features:

1. Continuously checks if operation is done (poll the State field in the Status Register) to determine when the Sahara hardware has completed
2. Moves the content of the in-progress element from the Command Queue to the Result Pool
3. Copies Sahara Status and Error Status registers into the result pool
4. Writes `Clr_Error` in Command register and flag as FAILED if State field in Status register is 010 or 110 (otherwise set to PASSED)
5. Loads the next command into Sahara, if one exists (to keep Sahara loaded with two commands at a time if possible)
6. If in Interrupt mode, schedule tasklet (bottom half) process Completion Notification (that is, place it in the ready queue)
7. If polling, transfer control to process Completion Notification

28.2.2.12 Completion Notification

Using compiler switches, this runs as a tasklet or is invoked as a function as follows:

1. Invoke callback function, available in UCO, if in interrupt mode and callbacks are not suppressed by user
   - If the User is in Kernel Space, invoke callback
   - If the User is in User Space, signal UM Extension to invoke callback
2. Clean up memory, flags, and so on as needed
3. Unlock pages

28.2.2.13 Get Results

When a Get Results request is received (a request that does not involve Sahara hardware), the following are performed and the result is immediately returned to the user:

1. If no results are found for this user, return `no results found` status
2. If at least one result is found for the user, populate the user supplied result list in whatever order the results are found in the Result Pool (return the lesser of the max number of requests or number of results in pool)
3. If the status is PASSED (set by Poll/ISR process), check and return the following:
   - Failed if State field in Status register is 011. Also sends notification to Sahara Public Interface to reject all future calls to Sahara driver
   - Failed if SCC Fail bit in Status register is set
   - Specific descriptor error from Error Source field in the Error Status register, if the Error bit in the Status register is set
   - Failed if Error bit in Status register is set and the Error Source field in the Error Status register shows No Error
   - Passed otherwise
4. Clear result pool entry
5. Adjust number of outstanding requests

28.3 Driver Features

The SAHARA driver supports the following features:

- Hashing with MD5, SHA-1, SHA-224 and SHA-256 algorithms
- HMAC with the same algorithms as for hashing
- Symmetric cryptography support for AES, DES, and triple DES, in ECB, CBC, and CTR modes (though only AES is supported in CTR mode); ARC4 support is also provided
- CCM for AES
- Wrapped keys (hiding keys in the SCC), using the SCC key to encrypt or decrypt, HMAC functions, or CCM
- Generation of an arbitrary number of bytes of random data
- User mode and kernel mode; callbacks and non-callback non-blocking

28.4 Source Code Structure

Table 28-2 lists the source files associated with the SAHARA driver that are available in the directory `<ltib_dir>/rpm/BUILD/linux/drivers/mxc/security/sahara2`.

Table 28-2. Sahara Source Files

File	Description
sah_driver_interface.c	Sahara low level driver
sah_hardware_interface.c	Provides an interface to the SAHARA hardware registers
sah_interrupt_handler.c	Sahara Interrupt Handler
sah_memory_mapper.c	Re-creates SAHARA Data structures in kernel memory such that they are suitable for DMA
sah_queue.c	Provides FIFO Queue implementation
sah_queue_manager.c	This file provides a Queue Manager implementation. The Queue Manager manages additions and removal from the queue and updates the status of queue entries. Also calls `sah_HW_*` functions to interact with the hardware.
sah_status_manager.c	Contains functions which processes the SAHARA status registers
sf_util.c	Security Functions component API - Utility functions
fsl_shw_auth.c	Contains the routines which do the combined encryption and authentication
fsl_shw_hash.c	Implements Cryptographic Hashing functions of the API
fsl_shw_hmac.c	Provides HMAC functions of the API
fsl_shw_rand.c	Generates random numbers
fsl_shw_sym.c	Provides Symmetric-Key encryption support for block cipher algorithms
fsl_shw_user.c	Implements user and platform capabilities functions
fsl_shw_wrap.c	Implements Key-Wrap (Black Key) functions
km_adaptor.c	Adaptor provides interface to driver for kernel user

Table 28-3 lists the header files associated with the SAHARA driver are found in the directory `<ltib_dir>/rpm/BUILD/linux/drivers/mxc/security/sahara2/include`.

Table 28-3. Sahara Header Files

File	Description
fsl_shw.h	Sahara Definition of the Freescale Security Hardware API
fsl_platform.h	File to isolate code which might be platform-dependent
sahara.h	All of the defines used throughout user and kernel space
sah_driver_common.h	Provides types and defined values for use in the Driver Interface
sah_hardware_interface.h	Provides an interface to the SAHARA hardware registers
sah_interrupt_handler.h	Provides a hardware interrupt handling mechanism for device driver
sah_kernel.h	Provides definitions for items that user-space and kernel-space share
sah_memory_mapper.h	Re-creates SAHARA Data structures in kernel memory such that they are suitable for DMA
sah_queue_manager.h	This file provides a Queue Manager implementation.The Queue Manager manages additions and removal from the queue and updates the status of queue entries. It also calls `sah_HW_*` functions to interact with the hardware.
sah_status_manager.h	SAHARA Status Manager Types and Function Prototypes

Table 28-3. Sahara Header Files (continued)

File	Description
sf_util.h	Security Function Utility Functions
diagnostic.h	Macros for outputting kernel and user space diagnostics
adaptor.h	The Adaptor component provides an interface to the device driver

28.5 Menu Configuration Options

The following Linux kernel configurations are provided for this module:

- CONFIG_MXC_SAHARA —Configuration option for Sahara Hardware support. In the menuconfig this option is found under

  MXC support drivers > MXC Security Drivers > SAHARA2 Security Hardware Support
- CONFIG_MXC_SAHARA_USER_MODE—The driver can be configured to provide an interface to user space (used by the library). This configuration switch is currently ignored, and the user space interface is currently always provided. In the menuconfig this option is found under

  MXC support drivers > MXC Security Drivers > SAHARA2 Security Hardware Support
- CONFIG_MXC_SAHARA_POLL_MODE—The driver can be configured to poll the Sahara2 hardware device for end-of-operation status, or it can (by default) process an interrupt for end-of-operation. In the menuconfig this option is found under

  MXC support drivers > MXC Security Drivers > SAHARA2 Security Hardware Support
- CONFIG_MXC_SAHARA_POLL_MODE_TIMEOUT—To avoid infinite polling, a time-out is provided. Should the time-out be reached, a fault is reported causing the Sahara to be reset. This time-out period is configurable. When poll mode is selected, the value for CONFIG_MXC_SAHARA_POLL_MODE_TIMEOUT can be modified. Poll mode works nearly the same as interrupt mode, that is, blocking mode returns the result of the descriptor chain (succeeded, erred, and so on); non-blocking mode queues results in a results pool and `fsl_shw_get_results()` retrieves them; callback mode (non-blocking mode only) the callback is made just before control is returned from the API call (in interrupt mode it is some time after).

28.6 Programming Interface

This driver implements all the methods that are required by the Linux serial API to interface with the Sahara driver. It implements and provides a set of control methods to the core Sahara driver present in Linux. Refer to the API document (included doxygen document) for more information on the methods implemented in the driver.

28.7 Interrupt Requirements

There is no interrupt requirement in this module.

Chapter 29
Security Drivers

The security drivers provide several APIs that facilitate access to various security features in the processor. The secure controller (SCC) consists of two modules, a secure RAM module and a secure monitor module. The SCC key encryption module (KEM) has a security feature for storing encrypted data in the on-chip RAM (Red data = unencrypted data, Black data = encrypted data), with a total size of 2 Kbytes. This module is needed in cases where data must be stored securely in external memory in encrypted form. This module can clear the secure RAM during intrusion.

The security design covers the following modules:

- Boot Security
- SCC (Secure RAM, Secure Monitor)
- Algorithm Integrity Checker
- Security Timer
- Key Encryption Module (KEM), Zeroization module

29.1 Hardware Overview

The platform has several different security blocks. The details of the individual blocks are described in the following sections.

29.1.1 Boot Security

During boot, the boot pins must be set to enable the processor to boot. The SCC module must be enabled by blowing specific fuses. By booting in this manner, the integrity of the data in the Flash (kernel image) can be assured. Any violation in the data integrity raises an alarm.

29.1.2 Secure RAM

Figure 29-1 shows the SCC-Secure RAM and its modules. Individual modules are described in the following sections.

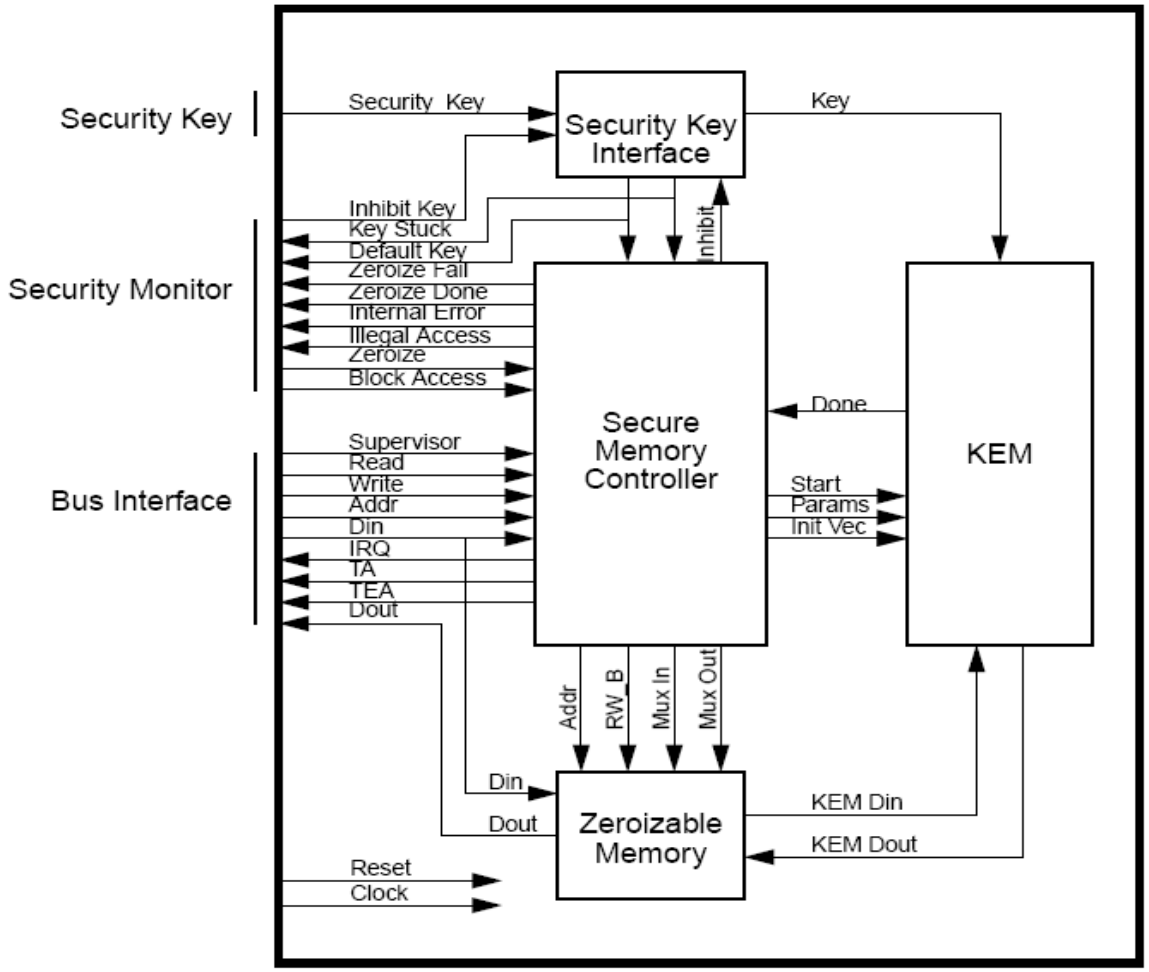


Figure 29-1. Secure RAM Block Diagram

29.1.3 KEM

The KEM uses the algorithm and a -bit key for encryption of data. The key is programmed during manufacture and is accessible only to the encryption module. It is not accessible on any bus external to the secure memory module. The data in the external RAM is stored in an encrypted format. The data is encrypted using algorithm so that it can be decoded only using the SCC module.

29.1.4 Zeroizable Memory

The memory module can be multiplexed in and out of the RAM to allow the memory controller to switch paths according to the Secure RAM state and the host read and write accesses. When zeroing sections of memory, only the memory controller has access. When encrypting or decrypting, only the KEM module

has access. When the Secure RAM is in the Idle state, the host can access the memory. The Zeroize Done signal is used to reset the encryption module and the memory controller. While the Zeroize Done signal is low, any attempted access by the host is ignored. When the Zeroize signal is asserted, or when the Zeroize Memory bit in the Interrupt Control register is set, not only is the Red and Black memory initialized, but most of the registers are also reset. The Red Start, Black Start, Length, Control, Error Status, Init Vector 0, and Init Vector 1 registers are cleared. The encryption engine is also reset. The Zeroization takes place whenever there is a security violation like external bus intrusion. The Red and Black memory area is usually cleared during system boot-up.

29.1.5 Security Key Interface Module

The Security Key Interface module uses a -bit encryption key. The physical structures for the encryption key resides elsewhere. The Secret Key Interface contains a key mux to select between the encryption key and the default key and test the logic to determine the validity of the encryption key. In the Secure state the encryption key is used. In the Non-Secure state, the default key prevents unauthorized access to SCC-encrypted data and is useful for test purposes.

29.1.6 Secure Memory Controller

The Secure Memory controller implements an internal data handler that moves data in and out of the KEM, a memory clear function, and all of the supervisor-accessible Control and Status registers.

29.1.7 Security Monitor

The Security Monitor (SMN) is a critical component of security assurance for the platform. It determines when and how Secure RAM resources are available to the system, and it also provides mechanisms for verifying software algorithm integrity. This block ensures that the system is running in such a manner as to provide protection for the sensitive data that is resident in the SCC. The Security Monitor consists of five main sub-blocks:

- Secure State Controller
- Security Policy
- Algorithm Integrity Checker (AIC)
- Security Timer
- Debug Detector

Figure 29-2 shows a block diagram of the SMN.

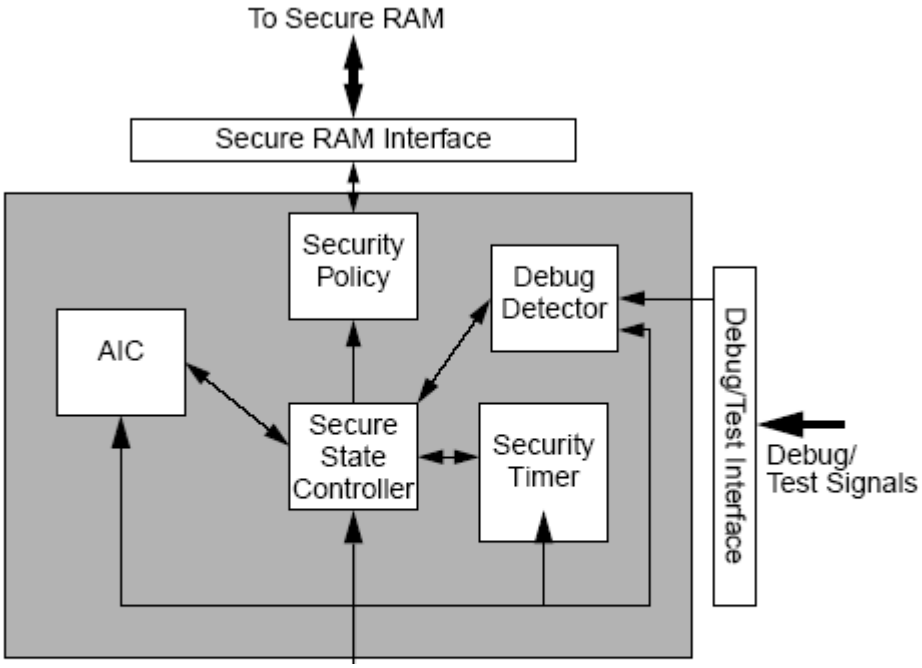


Figure 29-2. Security Monitor Block Diagram

29.1.8 Secure State Controller

The Secure State Controller, shown in Figure 29-3, is a state machine that controls the security states of the chip.

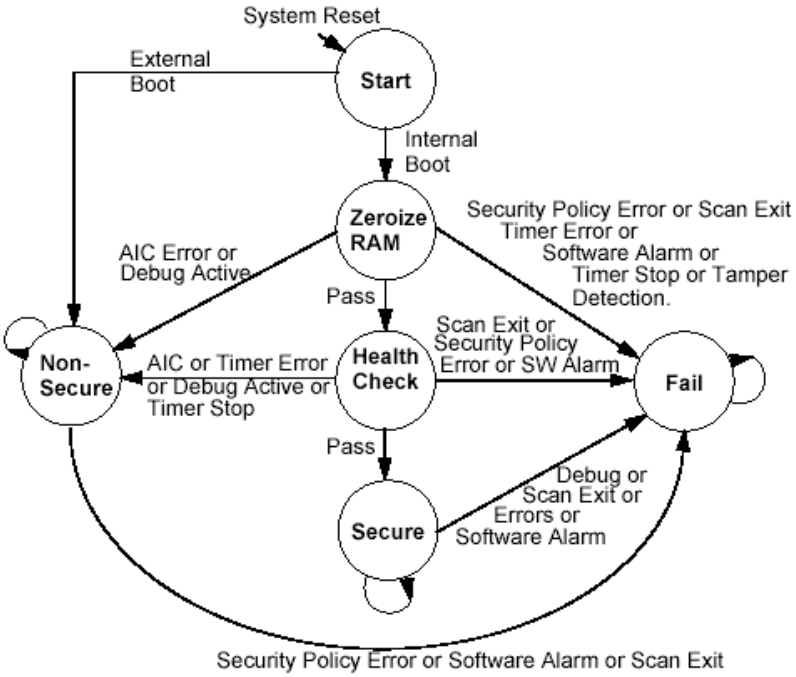


Figure 29-3. Secure State Controller State Diagram

29.1.9 Security Policy

The Security Policy block uses state information from the Secure State Controller along with inputs from the Secure RAM to determine what access to the Secure RAM is allowed based on the policy table. The policy table is available in the L3 specification document of the corresponding platform.

29.1.10 Algorithm Integrity Checker (AIC)

The Algorithm Integrity Checker (AIC) is used in conjunction with software to provide assurance that critical software (such as a software encryption algorithm) operates correctly. It is also an integral part of the power-up procedure as it must be used to achieve a secure state.

29.1.11 Secure Timer

The Secure Timer is a 32-bit programmable timer. It is used in conjunction with the Secure State Controller during power-up to ensure that the transition to the Secure state happens in the appropriate amount of time. After power-up, the timer can be used as a watchdog timer for any time-critical routines or algorithms. If the timer is allowed to expire, it generates an error.

29.1.12 Debug Detector

The debug detector monitors the various debug and test signals and informs the secure state controller of the status. The secure state controller receives an alert when debug modes, such as JTAG and scan are active. The debug detector status register can be read by the host processor to determine which debug signals are currently active. Refer to the SCC section in L3 specification document of the corresponding platform for more information on the SCC-Debug Detector.

29.2 Software Operation

Besides the hardware security modules, there is optional, specialized software that helps to deliver security.

29.2.1 SCC Common Software Operations

The SCC driver is only available to other kernel modules. That is, there is no node file in `/dev`. Thus, it is not possible for a user-mode program to access the driver, and it is not possible for a user program to access the device directly.

The driver does not allow storage of data in either the Red or Black memories. Any decrypted information is returned to the user. If the user wants to use the information at a later point, the encrypted form must again be passed to the driver, and it must be decrypted again.

The SCC encrypts and decrypts using with an internally stored key. When the SCC is in Secure mode, it uses its secret, unique-per-chip key. When it is in Non-Secure mode, it uses a default key. This ensures that secrets stay secret if the SCC is not in Secure mode.

Not all functions are implemented, such as interfaces to the ASC/AIC components and the timer functions. These and other features must be accessed through `scc_read_register()` and `scc_write_register()`, using the `#define` values provided.

29.3 Driver Features

The SCC driver supports the following features:

- Checks whether the SCC fuse is blown or not (SCC Disabled/Enabled)
- Configures the Red and Black memory area addresses and number of blocks to be encrypted/decrypted
- Loads the data to be encrypted
- Loads the data to be decrypted
- Starts the Ciphering mechanism
- Reports back the status of the KEM module
- Zeros blocks in the Red/Black memory area
- Checks for the boot type: internal or external
- Raises a software alarm
- Reports back the status of the Zeroize module
- Configures the AIC start and end algorithm sequence number
- Checks the sequence of the algorithm
- Finds the next sequence number given the current sequence number
- Configures the Security Timer
- Reports back the status of the Security Timer module

29.4 Source Code Structure

This section contains the various files that implement the Security modules. Table 29-1 lists the headers and source files associated with the security driver.

- The C source files are available in the directory, `<ltib_dir>/rpm/BUILD/linux/drivers/mxc/security` directory.
- Header files are available in the directory, `<ltib_dir>/rpm/BUILD/linux/include/linux`.

Table 29-1. SCCDriver Files

File	Description
Makefile	Used to compile, link and generate the final binary image

29.5 Menu Configuration Options

The following Linux kernel configurations are provided for this module. In order to get to the security configuration, use the command `./ltib -c` when located in the <ltib dir>. In the screen select **Configure kernel**, exit and a new screen appears.

Chapter 30
Fast Ethernet Controller (FEC) Driver

The Fast Ethernet Controller (FEC) driver performs the full set of IEEE 802.3/Ethernet CSMA/CD media access control and channel interface functions. The FEC requires an external interface adapter and transceiver function to complete the interface to the Ethernet media. It supports half or full-duplex operation on 10 Mbps or 100 Mbps related Ethernet networks.

The FEC driver supports the following features:

- Full/Half duplex operation
- Link status change detect
- Auto-negotiation (determines the network speed and full or half-duplex operation)
- Transmit features such as automatic retransmission on collision and CRC generation
- Obtaining statistics from the device such as transmit collisions

The network adapter can be accessed through the `ifconfig` command with interface name `ethx`. The driver auto-probes the external adaptor (PHY device).

30.1 Hardware Operation

The FEC is an Ethernet controller that interfaces the system to the LAN network. The FEC supports different standard MAC-PHY (physical) interfaces for connection to an external Ethernet transceiver. The FEC supports the 10/100 Mbps MII and the 10 Mbps-only 7-wire serial network interface (SNI), which uses a subset of the MII pins.

A brief overview of the device functionality is provided here. For details see the FEC chapter of the *i.MX53 Multimedia Applications Processor Reference Manual*.

In MII mode, there are 18 signals defined by the IEEE 802.3 standard and supported by the EMAC. SNI mode uses a subset of the 18 signals. These signals are listed in Table 30-1.

Table 30-1. Pin Usage in MII and SNI Modes

Direction	EMAC Pin Name	MII Usage	SNI Usage	RMII Usage
In/Out	FEC_MDIO	Management Data Input/Output	General I/O	Management Data Input/Output
Out	FEC_MDC	Management Data Clock	General output	Management Data Clock
Out	FEC_TXD[0]	Data out, bit 0	Data out	Data out, bit 0
Out	FEC_TXD[1]	Data out, bit 1	General output	Data out, bit 1
Out	FEC_TXD[2]	Data out, bit 2	General output	Not Used
Out	FEC_TXD[3]	Data out, bit 3	General output	Not Used
Out	FEC_TX_EN	Transmit Enable	Transmit Enable	Transmit Enable
Out	FEC_TX_ER	Transmit Error	General output	Not Used
In	FEC_CRS	Carrier Sense	Not Used	Not Used

Table 30-1. Pin Usage in MII and SNI Modes (continued)

Direction	EMAC Pin Name	MII Usage	SNI Usage	RMII Usage
In	FEC_COL	Collision	Collision	Not Used
In	FEC_TX_CLK	Transmit Clock	Transmit Clock	Synchronous clock reference (REF_CLK)
In	FEC_RX_ER	Receive Error	General input	Receive Error
In	FEC_RX_CLK	Receive Clock	Receive Clock	Not Used
In	FEC_RX_DV	Receive Data Valid	Receive Data Valid	Not Used
In	FEC_RXD[0]	Data in, bit 0	Data in	Data in, bit 0
In	FEC_RXD[1]	Data in, bit 1	General input	Data in, bit 1
In	FEC_RXD[2]	Data in, bit 2	General input	Not Used
In	FEC_RXD[3]	Data in, bit 3	General input	Not Used

The MII management interface consists of two pins, FEC_MDIO and FEC_MDC. The FEC hardware operation can be divided in the following parts. For detailed information consult the *i.MX53Multimedia Applications Processor Reference Manual*.

- Transmission—The Ethernet transmitter is designed to work with almost no intervention from software. Once ECR[ETHER_EN] is asserted and data appears in the transmit FIFO, the Ethernet MAC is able to transmit onto the network. When the transmit FIFO fills to the watermark (defined by the TFWR), the MAC transmit logic asserts FEC_TX_EN and starts transmitting the preamble (PA) sequence, the start frame delimiter (SFD), and then the frame information from the FIFO. However, the controller defers the transmission if the network is busy (FEC_CRS asserts).

  Before transmitting, the controller waits for carrier sense to become inactive, then determines if carrier sense stays inactive for 60 bit times. If the transmission begins after waiting an additional 36 bit times (96 bit times after carrier sense originally became inactive). Both buffer (TXB) and frame (TXF) interrupts may be generated as determined by the settings in the EIMR.
- Reception—The FEC receiver is designed to work with almost no intervention from the host and can perform address recognition, CRC checking, short frame checking, and maximum frame length checking. When the driver enables the FEC receiver by asserting ECR[ETHER_EN], it immediately starts processing receive frames. When FEC_RX_DV asserts, the receiver checks for a valid PA/SFD header. If the PA/SFD is valid, it is stripped and the frame is processed by the receiver. If a valid PA/SFD is not found, the frame is ignored. In MII mode, the receiver checks for at least one byte matching the SFD. Zero or more PA bytes may occur, but if a 00 bit sequence is detected prior to the SFD byte, the frame is ignored.

  After the first six bytes of the frame have been received, the FEC performs address recognition on the frame. During reception, the Ethernet controller checks for various error conditions and once the entire frame is written into the FIFO, a 32-bit frame status word is written into the FIFO. This status word contains the M, BC, MC, LG, NO, CR, OV, and TR status bits, and the frame length. Receive Buffer (RXB) and Frame Interrupts (RXF) may be generated if enabled by the EIMR register. When the receive frame is complete, the FEC sets the L bit in the RxBD, writes the other frame status bits into the RxBD, and clears the E bit. The Ethernet controller next generates a

maskable interrupt (RXF bit in EIR, maskable by RXF bit in EIMR), indicating that a frame has been received and is in memory. The Ethernet controller then waits for a new frame.

- Interrupt management—When an event occurs that sets a bit in the EIR, an interrupt is generated if the corresponding bit in the interrupt mask register (EIMR) is also set. The bit in the EIR is cleared if a one is written to that bit position; writing zero has no effect. This register is cleared upon hardware reset. These interrupts can be divided into operational interrupts, transceiver/network error interrupts, and internal error interrupts. Interrupts which may occur in normal operation are GRA, TXF, TXB, RXF, RXB. Interrupts resulting from errors/problems detected in the network or transceiver are HBERR, BABR, BABT, LC, and RL. Interrupts resulting from internal errors are HBERR and UN. Some of the error interrupts are independently counted in the MIB block counters. Software may choose to mask off these interrupts as these errors are visible to network management through the MIB counters.
- PHY management—phylib was used to manage all the FEC phy related operation such as phy discovery, link status, and state machine.MDIO bus will be created in FEC driver and registered into the system.You can refer to Documentation/networking/phy.txt under linux source directory for more information.

30.2 Software Operation

The FEC driver supports the following functions:

- Module initialization—Initializes the module with the device specific structure
- Rx/Tx transmition
- Interrupt servicing routine
- PHY management
- FEC management such init/start/stop

30.3 Source Code Structure

Table 30-2 shows the source files available in the `<ltib_dir>/rpm/BUILD/linux/drivers/net` directory.

Table 30-2. FEC Driver Files

File	Description
fec.h	Header file defining registers
fec.c	Linux driver for Ethernet LAN controller

For more information about the generic Linux driver, see the `<ltib_dir>/rpm/BUILD/linux/drivers/net/fec.c` source file.

30.4 Menu Configuration Options

The following Linux kernel configuration option is provided for this module. To get to this option, use the `./ltib -c` command when located in the `<ltib dir>`. On the screen displayed, select **Configure the Kernel** and exit. When the next screen appears, select the following option to enable this module:

- CONFIG_FEC—Provided for this module. This option is available under Device Drivers > Network device support > Ethernet (10 or 100Mbit) > FEC Ethernet controller.

To mount NFS-rootfs through FEC, disable the other Network config in the menuconfig if need.

30.5 Programming Interface

Table 30-2 lists the source files for the FEC driver. The following section shows the modifications that were required to the original Ethernet driver source for porting it to the i.MX device.

30.5.1 Device-Specific Defines

Device-specific defines are added to the header file (`fec.h`) and they provide common board configuration options.

`fec.h` defines the struct for the register access and the struct for the buffer descriptor. For example,

```
/*
 *      Define the buffer descriptor structure.
 */
struct bufdesc {
         unsigned short    cbd_datlen;               /* Data length */
         unsigned short    cbd_sc;                   /* Control and status info */
         unsigned long     cbd_bufaddr;              /* Buffer address */
};
/*
 *      Define the register access structure.
 */
#define FEC_IEVENT              0x004 /* Interrupt event reg */
#define FEC_IMASK               0x008 /* Interrupt mask reg */
#define FEC_R_DES_ACTIVE        0x010 /* Receive descriptor reg */
#define FEC_X_DES_ACTIVE        0x014 /* Transmit descriptor reg */
#define FEC_ECNTRL              0x024 /* Ethernet control reg */
#define FEC_MII_DATA            0x040 /* MII manage frame reg */
#define FEC_MII_SPEED           0x044 /* MII speed control reg */
#define FEC_MIB_CTRLSTAT        0x064 /* MIB control/status reg */
#define FEC_R_CNTRL             0x084 /* Receive control reg */
#define FEC_X_CNTRL             0x0c4 /* Transmit Control reg */
#define FEC_ADDR_LOW            0x0e4 /* Low 32bits MAC address */
#define FEC_ADDR_HIGH           0x0e8 /* High 16bits MAC address */
#define FEC_OPD                 0x0ec /* Opcode + Pause duration */
#define FEC_HASH_TABLE_HIGH     0x118 /* High 32bits hash table */
#define FEC_HASH_TABLE_LOW      0x11c /* Low 32bits hash table */
#define FEC_GRP_HASH_TABLE_HIGH 0x120 /* High 32bits hash table */
#define FEC_GRP_HASH_TABLE_LOW  0x124 /* Low 32bits hash table */
#define FEC_X_WMRK              0x144 /* FIFO transmit water mark */
#define FEC_R_BOUND             0x14c /* FIFO receive bound reg */
#define FEC_R_FSTART            0x150 /* FIFO receive start reg */
#define FEC_R_DES_START         0x180 /* Receive descriptor ring */
#define FEC_X_DES_START         0x184 /* Transmit descriptor ring */
#define FEC_R_BUFF_SIZE         0x188 /* Maximum receive buff size */
#define FEC_MIIGSK_CFGR         0x300 /* MIIGSK config register */
#define FEC_MIIGSK_ENR          0x308 /* MIIGSK enable register */
```

30.5.2 Getting a MAC Address

.

The MAC address can be set through bootloader such as u-boot.FEC driver will use it to confiure the MAC address for network devices.

Chapter 31
Inter-IC (I^2C) Driver

I^2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. The I^2C driver for Linux has two parts:

- I^2C bus driver—low level interface that is used to talk to the I^2C bus
- I^2C chip driver—acts as an interface between other device drivers and the I^2C bus driver

31.1 I^2C Bus Driver Overview

The I^2C bus driver is invoked only by the I^2C chip driver and is not exposed to the user space. The standard Linux kernel contains a core I^2C module that is used by the chip driver to access the I^2C bus driver to transfer data over the I^2C bus. The chip driver uses a standard kernel space API that is provided in the Linux kernel to access the core I^2C module. The standard I^2C kernel functions are documented in the files available under `Documentation/i2c` in the kernel source tree. This bus driver supports the following features:

- Compatible with the I^2C bus standard
- Bit rates up to 400 Kbps
- Starts and stops signal generation/detection
- Acknowledge bit generation/detection
- Interrupt-driven, byte-by-byte data transfer
- Standard I^2C master mode

31.2 I^2C Device Driver Overview

The I^2C device driver implements all the Linux I^2C data structures that are required to communicate with the I^2C bus driver. It exposes a custom kernel space API to the other device drivers to transfer data to the device that is connected to the I^2C bus. Internally, these API functions use the standard I^2C kernel space API to call the I^2C core module. The I^2C core module looks up the I^2C bus driver and calls the appropriate function in the I^2C bus driver to transfer data. This driver provides the following functions to other device drivers:

- Read function to read the device registers
- Write function to write to the device registers

The camera driver uses the APIs provided by this driver to interact with the camera.

31.3 Hardware Operation

The I^2C module provides the functionality of a standard I^2C master and slave. It is designed to be compatible with the standard Philips I^2C bus protocol. The module supports up to 64 different clock frequencies that can be programmed by setting a value to the Frequency Divider Register (IFDR). It also generates an interrupt when one of the following occurs:

- One byte transfer is completed

- Address is received that matches its own specific address in slave-receive mode
- Arbitration is lost

31.4 Software Operation

The I^2C driver for Linux has two parts: an I^2C bus driver and an I^2C chip driver.

31.4.1 I^2C Bus Driver Software Operation

The I^2C bus driver is described by a structure called `i2c_adapter`. The most important field in this structure is `struct i2c_algorithm *algo`. This field is a pointer to the `i2c_algorithm` structure that describes how data is transferred over the I^2C bus. The algorithm structure contains a pointer to a function that is called whenever the I^2C chip driver wants to communicate with an I^2C device.

During startup, the I^2C bus adapter is registered with the I^2C core when the driver is loaded. Certain architectures have more than one I^2C module. If so, the driver registers separate `i2c_adapter` structures for each I^2C module with the I^2C core. These adapters are unregistered (removed) when the driver is unloaded.

After transmitting each packet, the I^2C bus driver waits for an interrupt indicating the end of a data transmission before transmitting the next byte. It times out and returns an error if the transfer complete signal is not received. Because the I^2C bus driver uses wait queues for its operation, other device drivers should be careful not to call the I^2C API methods from an interrupt mode.

31.4.2 I^2C Device Driver Software Operation

The I^2C driver controls an individual I^2C device on the I^2C bus. A structure, `i2c_driver`, describes the I^2C chip driver. The fields of interest in this structure are `flags` and `attach_adapter`. The `flags` field is set to a value `I2C_DF_NOTIFY` so that the chip driver can be notified of any new I^2C devices, after the driver is loaded. The `attach_adapter` callback function is called whenever a new I^2C bus driver is loaded in the system. When the I^2C bus driver is loaded, this driver stores the `i2c_adapter` structure associated with this bus driver so that it can use the appropriate methods to transfer data.

31.5 Driver Features

The I^2C driver supports the following features:

- I^2C communication protocol
- I^2C master mode of operation

NOTE

The I^2C driver do not support the I^2C slave mode of operation.

31.6 Source Code Structure

Table 31-1 shows the I^2C bus driver source files available in the directory:

`<ltib_dir>/rpm/BUILD/linux/drivers/i2c/busses`.

Table 31-1. I^2C Bus Driver Files

File	Description
i2c-imx.c	I^2C bus driver source file

31.7 Menu Configuration Options

The following Linux kernel configuration option is provided for this module. To get to this option, use the `./ltib -c` command when located in the `<ltib dir>`. On the screen displayed, select **Configure the Kernel** and exit. When the next screen appears, select the following options to enable this module:

Device Drivers > I2C support > I2C Hardware Bus support > IMX I2C interface.

31.8 Programming Interface

The I^2C device driver can use the standard SMBus interface to read and write the registers of the device connected to the I^2C bus. For more information, see `<ltib_dir>/rpm/BUILD/linux/include/linux/i2c.h`.

31.9 Interrupt Requirements

The I^2C module generates many kinds of interrupts. The highest interrupt rate is associated with the transfer complete interrupt as shown in Table 31-2.

Table 31-2. I^2C Interrupt Requirements

Parameter	Equation	Typical	Best Case
Rate	Transfer Bit Rate/8	25,000/sec	50,000/sec
Latency	8/Transfer Bit Rate	40 µs	20 µs

The typical value of the transfer bit-rate is 200 Kbps. The best case values are based on a baud rate of 400 Kbps (the maximum supported by the I^2C interface).

Chapter 32
Configurable Serial Peripheral Interface (CSPI) Driver

The CSPI driver implements a standard Linux driver interface to the CSPI controllers. It supports the following features:

- Interrupt- and SDMA-driven transmit/receive of bytes
- Multiple master controller interface
- Multiple slaves select
- Multi-client requests

32.1 Hardware Operation

CSPI is used for fast data communication with fewer software interrupts than conventional serial communications. Each CSPI is equipped with a data FIFO and is a master/slave configurable serial peripheral interface module, allowing the processor to interface with external SPI master or slave devices.

The primary features of the CSPI includes:

- Master/slave-configurable
- Two chip selects allowing a maximum of four different slaves each for master mode operation
- Up to 32-bit programmable data transfer
- 8 × 32-bit FIFO for both transmit and receive data
- Configurable polarity and phase of the Chip Select (SS) and SPI Clock (SCLK)

32.2 Software Operation

The following sections describe the CSPI software operation.

32.2.1 SPI Sub-System in Linux

The CSPI driver layer is located between the client layer (PMIC and SPI Flash are examples of clients) and the hardware access layer. Figure 32-1 shows the block diagram for SPI subsystem in Linux.

The SPI requests go into I/O queues. Requests for a given SPI device are executed in FIFO order, and complete asynchronously through completion callbacks. There are also some simple synchronous

wrappers for those calls, including ones for common transaction types like writing a command and then reading its response.

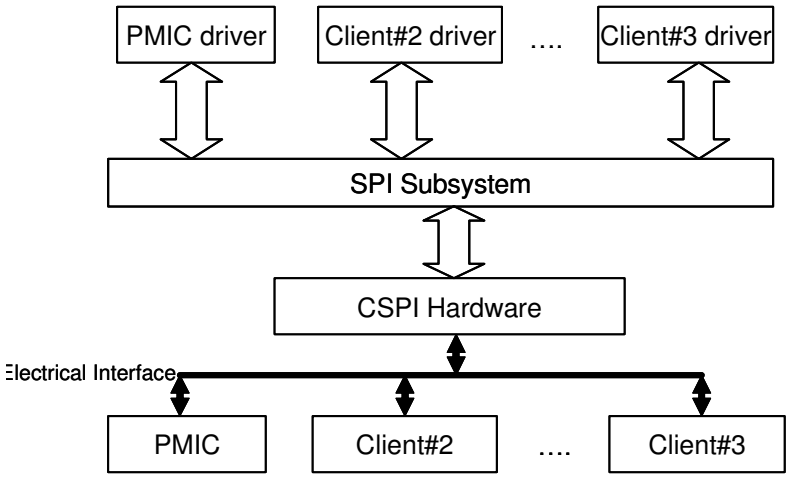


Figure 32-1. SPI Subsystem

All SPI clients must have a protocol driver associated with them and they must all be sharing the same controller driver. Only the controller driver can interact with the underlying SPI hardware module. Figure 32-2 shows how the different SPI drivers are layered in the SPI subsystem.

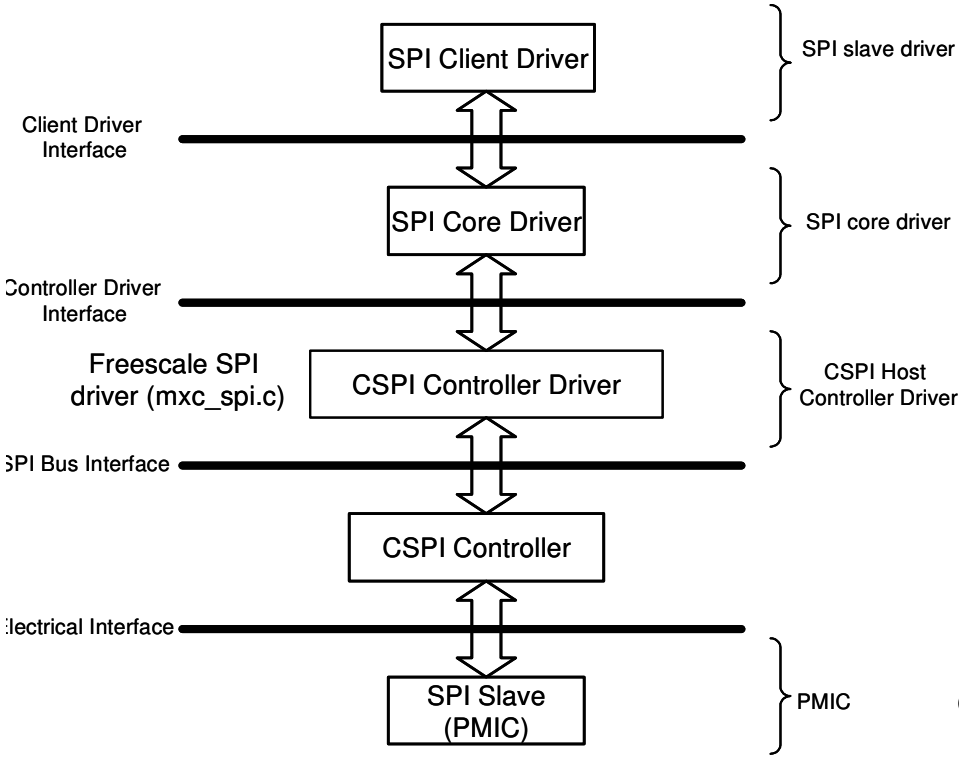


Figure 32-2. Layering of SPI Drivers in SPI Subsystem

32.2.2 Software Limitations

The CSPI driver limitations are as follows:

- Does not currently have SPI slave logic implementation
- Does not support a single client connected to multiple masters
- Does not currently implement the user space interface with the help of the device node entry but supports `sysfs` interface

32.2.3 Standard Operations

The CSPI driver is responsible for implementing standard entry points for init, exit, chip select and transfer. The driver implements the following functions:

- Init function `mxc_spi_init()`—Registers the `device_driver` structure.
- Probe function `mxc_spi_probe()`—Performs initialization and registration of the SPI device specific structure with SPI core driver. The driver probes for memory and IRQ resources. Configures the IOMUX to enable CSPI I/O pins, requests for IRQ and resets the hardware.
- Chip select function `mxc_spi_chipselect()`—Configures the hardware CSPI for the current SPI device. Sets the word size, transfer mode, data rate for this device.
- SPI transfer function `mxc_spi_transfer()`—Handles data transfers operations.
- SPI setup function `mxc_spi_setup()`—Initializes the current SPI device.
- SPI driver ISR `mxc_spi_isr()`—Called when the data transfer operation is completed and an interrupt is generated.

32.2.4 CSPI Synchronous Operation

Figure 32-3 shows how the CSPI provides synchronous read/write operations.

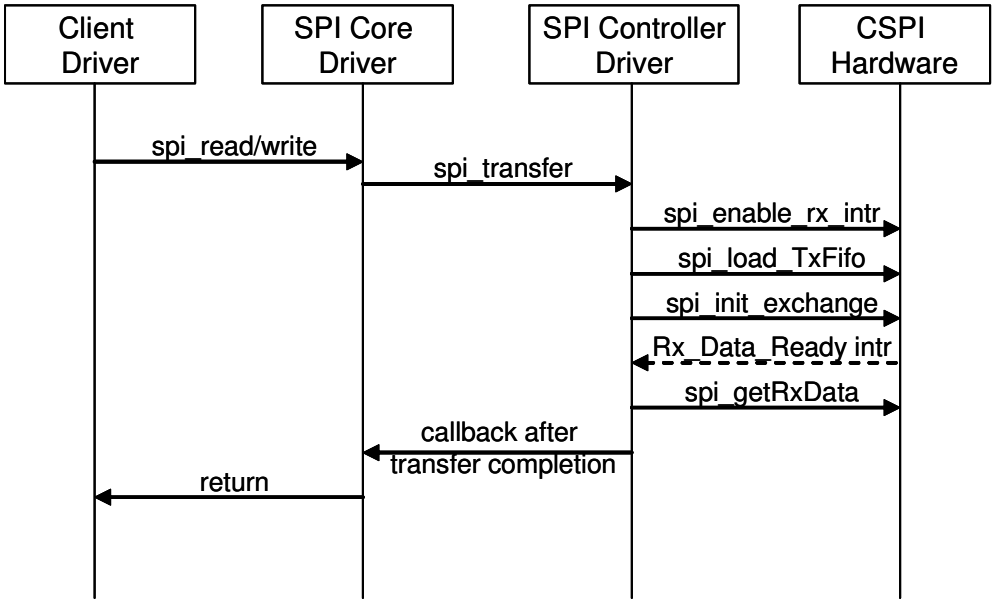


Figure 32-3. CSPI Synchronous Operation

32.3 Driver Features

The CSPI module supports the following features:

- Implements each of the functions required by a CSPI module to interface to Linux
- Multiple SPI master controllers
- Multi-client synchronous requests

32.4 Source Code Structure

Table 32-1 shows the source files available in the devices directory:

`<ltib_dir>/rpm/BUILD/linux/drivers/spi/`

Table 32-1. CSPI Driver Files

File	Description
mxc_spi.c	SPI Master Controller driver

32.5 Menu Configuration Options

The following Linux kernel configuration options are provided for this module. To get to these options, use the `./ltib -c` command when located in the `<ltib dir>`. On the screen displayed, select **Configure the Kernel** and exit. When the next screen appears, select the following options to enable this module:

- CONFIG_SPI—Build support for the SPI core. In menuconfig, this option is available under

Device Drivers > SPI Support.

- CONFIG_BITBANG—Library code that is automatically selected by drivers that need it. SPI_MXC selects it. In menuconfig, this option is available under

  Device Drivers > SPI Support > Utilities for Bitbanging SPI masters.
- CONFIG_SPI_MXC—Implements the SPI master mode for MXC CSPI. In menuconfig, this option is available under

  Device Drivers > SPI Support > MXC CSPI controller as SPI Master.
- CONFIG_SPI_MXC_SELECTn—Selects the CSPI hardware modules into the build (where n = 1 or 2). In menuconfig, this option is available under

  Device Drivers > SPI Support > CSPIn.
- CONFIG_SPI_MXC_TEST_LOOPBACK—To select the enable testing of CSPIs in loop back mode. In menuconfig, this option is available under

  Device Drivers > SPI Support > LOOPBACK Testing of CSPIs.

  By default this is disabled as it is intended to use only for testing purposes.

32.6 Programming Interface

This driver implements all the functions that are required by the SPI core to interface with the CSPI hardware. For more information, see the API document generated by Doxygen (in the doxygen folder of the documentation package).

32.7 Interrupt Requirements

The SPI interface generates interrupts. CSPI interrupt requirements are listed in Table 32-2.

Table 32-2. CSPI Interrupt Requirements

Parameter	Equation	Typical	Worst Case
BaudRate/ Transfer Length	(BaudRate/(TransferLength)) * (1/Rxtl)	31250	1500000

The typical values are based on a baud rate of 1 Mbps with a receiver trigger level (Rxtl) of 1 and a 32-bit transfer length. The worst-case is based on a baud rate of 12 Mbps (max supported by the SPI interface) with a 8-bits transfer length.

Chapter 33
Secure Real Time Clock (SRTC) Driver

The Secure Real Time Clock (SRTC) module is used to keep the time and date. It provides a certifiable time to the user and can raise an alarm if tampering with counters is detected. The SRTC is composed of two sub-modules: Low power domain (LP) and High power domain (HP). The SRTC driver only supports the LP domain with low security mode.

33.1 Hardware Operation

The SRTC is a real time clock with enhanced security capabilities. It provides an accurate, constant time, regardless of the main system power state and without the need to use an external on-board time source, such as an external RTC. The SRTC can wake up the system when a pre-set alarm is reached.

33.2 Software Operation

The following sections describe the software operation of the SRTC driver.

33.2.1 IOCTL

The SRTC driver complies with the Linux RTC driver model. See the Linux documentation in `<ltib_dir>/rpm/BUILD/linux/Documentation/rtc.txt` for information on the RTC API.

Besides the initialization function, the SRTC driver provides IOCTL functions to set up the RTC timers and alarm functions. The following RTC IOCTLs are implemented by the SRTC driver:

- RTC_RD_TIME
- RTC_SET_TIME
- RTC_AIE_ON
- RTC_AIE_OFF
- RTC_ALM_READ
- RTC_ALM_SET

In addition, the following IOCTLS were added to allow user space application such as Digital Rights Management (DRM) to track changes in the time, which is user settable. The DRM application needs a way to track how much the time changed by so that it can manage its own secure clock = SRTC time counter + secureclk_offset. The secureclk_offset should be calculated by the DRM application based on changes to the SRTC time counter.

- RTC_READ_TIME_47BIT: allows a read of the 47-bit LP time counter on SRTC
- RTC_WAIT_TIME_SET: allows user thread to block until 47-bit LP time counter is set. At which point, the user thread is woken up and is provided the SRTC offset (which is the difference between the new and old LP counter)

The DRM process, which is not part of the BSP and is to be implemented by the device manufacturer, must be loaded during bootup before the user has a chance to change the time. This ensures that any time change

by the user is not missed by the DRM process. While the device is powered off, the SRTC time counter will continue to tick, drawing power from the coin cell. At bootup, the DRM process should first read the 47 bit SRTC time counte to account for the time that has elapsed since poweroff. Any detection of clock rollback should invalidate the DRM clock. Given that no rollback is detected, the DRM should proceed to call the RTC_WAIT_TIME_SET ioctl to catch any future changes in time. Any user changes to time before the DRM process calls this ioctl are missed, which compromises the integrity of the DRM secure clock. Therefore, it is essential that the DRM process is able to call this ioctl before the user is able to change the time. The priority of the DRM process should also be set to a highest possible value to ensure that it is awakened upon the time change and gets a chance to process the event. These system integration tasks are left upto to the device manufacturer to implement.

The driver information can be access by the proc file system. For example,

```
root@freescale /unit_tests$ cat /proc/driver/rtc
rtc_time        : 12:48:29
rtc_date        : 2009-08-07
alrm_time       : 14:41:16
alrm_date       : 1970-01-13
alarm_IRQ       : no
alrm_pending    : no
24hr            : yes
```

33.2.2 Keep Alive in the Power Off State

To keep preserve the time when the device is in the power off state, the SRTC clock source should be set to CKIL and the voltage input, NVCC_SRTC_POW, should remain active. Usually these signals are connected to the PMIC and software can configure the PMIC registers to enable the SRTC clock source and power supply. Ordinarily, when the main battery is removed and the device is in power off state, a coin-cell battery is used as a backup power supply. To avoid SRTC time loss, the voltage of the coin-cell battery should be sufficient to power the SRTC. If the coin-cell battery is chargeable, it is recommend to automatically enable the coin-cell charger so that the SRTC is properly powered.

33.3 Driver Features

The SRTC driver includes the following features:

- Implements all the functions required by Linux to provide the real time clock and alarm interrupt
- Reserves time in power off state
- Alarm wakes up the system from low power modes

33.4 Source Code Structure

The RTC module is implemented in the following directory:

```
<ltib_dir>/rpm/BUILD/linux/drivers/rtc
```

Table 33-1 shows the RTC module files.

Table 33-1. RTC Driver Files

File	Description
rtc-mxc_v2.c	SRTC driver implementation file

The source file for the SRTC specifies the SRTC function implementations.

33.5 Menu Configuration Options

To get to the SRTC driver, use the command `./ltib -c` when located in the <`ltib dir`>. On the screen displayed, select **Configure the kernel** and exit. When the next screen appears select the following options to enable the SRTC driver:

- Device Drivers > Real Time Clock > Freescale MXC Secure Real Time Clock

Chapter 34
Watchdog (WDOG) Driver

The Watchdog Timer module protects against system failures by providing an escape from unexpected hang or infinite loop situations or programming errors. Some platforms may have two WDOG modules with one of them having interrupt capability.

34.1 Hardware Operation

Once the WDOG timer is activated, it must be serviced by software on a periodic basis. If servicing does not take place in time, the WDOG times out. Upon a time-out, the WDOG either asserts the `wdog_b` signal or a `wdog_rst_b` system reset signal, depending on software configuration. The watchdog module cannot be deactivated once it is activated.

34.2 Software Operation

The Linux OS has a standard WDOG interface that allows support of a WDOG driver for a specific platform. WDOG can be suspended/resumed in STOP/DOZE and WAIT modes independently. Since some bits of the WGOD registers are only one-time programmable after booting, ensure these registers are written correctly.

34.3 Generic WDOG Driver

The generic WGOD driver is implemented in the `<ltib_dir>/rpm/BUILD/linux/drivers/watchdog/mxc_wdt.c` file. It provides functions for various IOCTLs and read/write calls from the user level program to control the WDOG.

34.3.1 Driver Features

This WDOG implementation includes the following features:

- Generates the reset signal if it is enabled but not serviced within a predefined timeout value (defined in milliseconds in one of the WDOG source files)
- Does not generate the reset signal if it is serviced within a predefined timeout value
- Provides IOCTL/read/write required by the standard WDOG subsystem

34.3.2 Menu Configuration Options

The following Linux kernel configuration option is provided for this module. To get to this option, use the `./ltib -c` command when located in the `<ltib dir>`. On the screen displayed, select **Configure the Kernel** and exit. When the next screen appears, select the following option to enable this module:

- CONFIG_MXC_WATCHDOG—Enables Watchdog timer module. This option is available under Device Drivers > Watchdog Timer Support > MXC watchdog.

34.3.3 Source Code Structure

Table 34-1 shows the source files for WDOG drivers that are in the following directory:

`<ltib_dir>/rpm/BUILD/linux/drivers/watchdog.`

Table 34-1. WDOG Driver Files

File	Description
mxc_wdt.c	WDOG function implementations
mxc_wdt.h	Header file for WDOG implementation

Watchdog system reset function is located under

`<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/system.c`

34.3.4 Programming Interface

The following IOCTLs are supported in the WDOG driver:

- WDIOC_GETSUPPORT
- WDIOC_GETSTATUS
- WDIOC_GETBOOTSTATUS
- WDIOC_KEEPALIVE
- WDIOC_SETTIMEOUT
- WDIOC_GETTIMEOUT

For detailed descriptions about these IOCTLs, see

`<ltib_dir>/rpm/BUILD/linux/Documentation/watchdog.`

Chapter 35
MMA8450Q Accelerometer Driver

The MMA8450Q is a digitcal accelerometer device with a flexible programming interface exposed to the software. It can be used on many applications, such as orientation decection, real-time activity analysis, motion dection, shock and vibration monitor, and so forth.

35.1 MMA8450Q Features

- 1.71 V to 1.89 V supply voltage
- Output Data Rate (ODR) from 400 Hz to 1.563 Hz
- 375 ¶Ãg/°ÃHz noise at normal mode ODR = 400 Hz
- 12-bit digital output
- I2C digital output interface (operates up to 400 kHz Fast Mode)
- Programmable 2 interrupt pins for 8 interrupt sources
- Embedded 4 channels of motion detection
  - Freefall or motion detection: 2 channels
  - Pulse Detection: 1 channel
  - Transient (Jolt) Detection: 1 channel
- Orientation (Portrait/Landscape) detection with hysteresis compensation
- Automatic ODR change for auto-wake and return-to-sleep
- 32 sample FIFO
- Selectable Sensitivity (±2g, ±4g, ±8g)
- Self-Test
- Robust Design, High Shocks Survivability (10,000 g)
- RoHS Compliant

35.2 Driver Requirements

MMA8450Q driver is based on a I^2C driver and makes use of hardware monitor system and input poll device system; therefore, the user must enable this support in the Linux kernel.

35.3 Driver Architecture

Figure 35-1 shows the software architecture. The MMA8450Q uses the I^2C for register access. At driver initial phase, a I^2C client is registered to the I^2C system and is used during the process of MMA8450Q operations. The MMA8450Q registers itself to the hardware monitor system and the input poll device system that provide user access facilities.

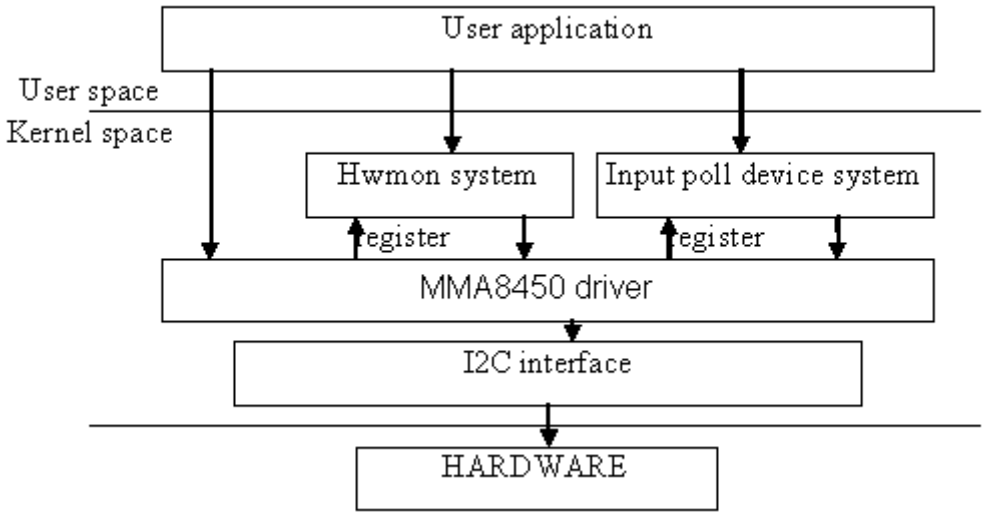


Figure 35-1. Driver Architecture

35.4 Driver Source Code Structure

The driver source code structure contains only one file located in the directory:

`<ltib_dir>/rpm/BUILD/linux/drivers/hwmon/`

Table 35-1. Driver Source Code Structure File

File	Description
mxc_mma8450.c	Implementation of the mma8450 accelerometer driver.

35.5 Driver Configuration

To get to the MMA8450 driver use the command `./ltib -c` when located in the <`ltib dir`>. On the screen displayed, select **Configure the kernel** and exit. When the next screen appears select the following options to enable the MMA8450 driver:

- Device Drivers > Hardware Monitoring support > MMA8450 device driver

Chapter 36
Pulse-Width Modulator (PWM) Driver

The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and generate tones. The PWM has 16-bit resolution and uses a 4×16 data FIFO to generate sound. The software module is composed of a Linux driver that allows privileged users to control the backlight by the appropriate duty cycle of the PWM Output (PWMO) signal.

36.1 Hardware Operation

Figure 36-1 shows the PWM block diagram.

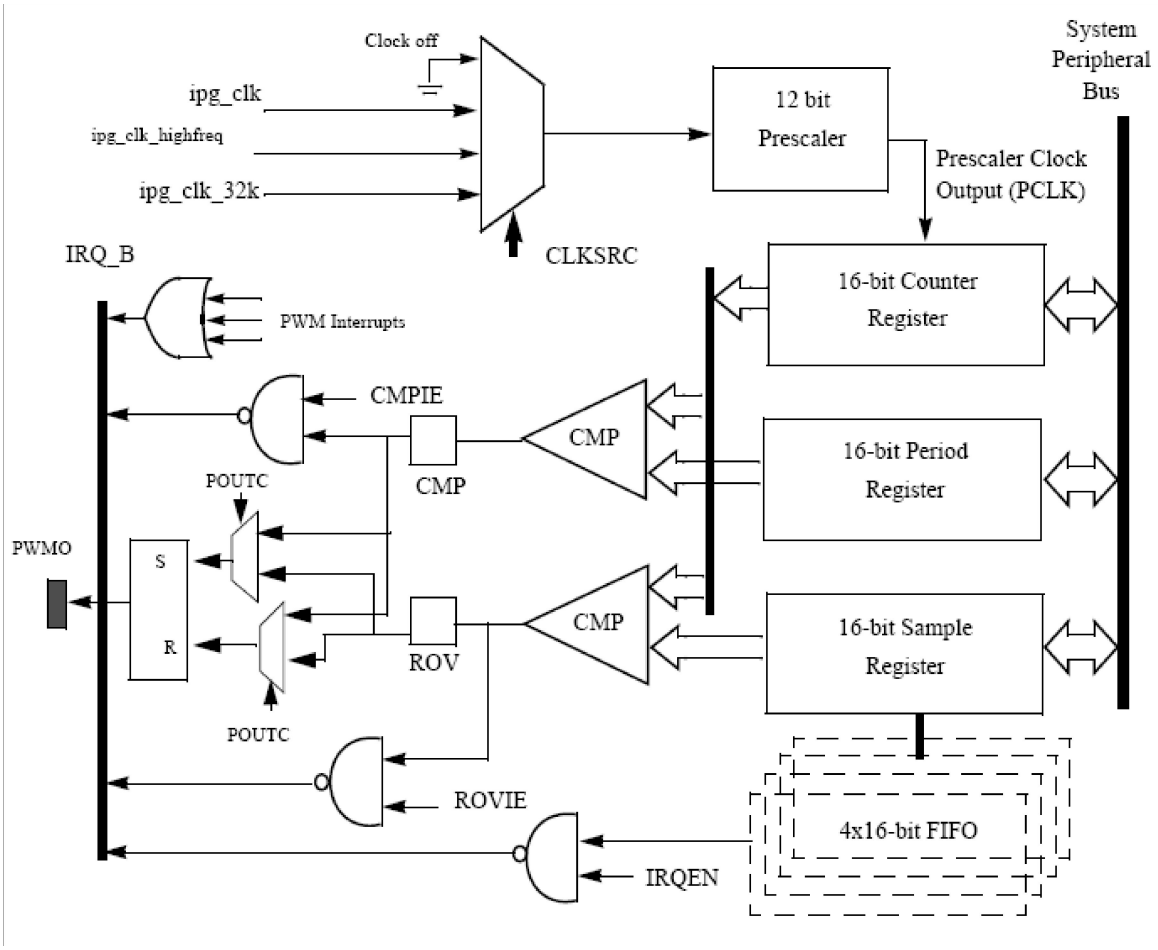


Figure 36-1. PWM Block Diagram

The PWM follows IP Bus protocol for interfacing with the processor core. It does not interface with any other modules inside the device except for the clock and reset inputs from the Clock Control Module (CCM) and interrupt signals to the processor interrupt handler. The PWM includes a single external output signal, PMWO. The PWM includes the following internal signals:

- Three clock inputs

- Four interrupt lines
- One hardware reset line
- Four low power and debug mode signals
- Four scan signals
- Standard IP slave bus signals

36.2 Clocks

The clock that feeds the prescaler can be selected from:

- High frequency clock—provided by the CCM. The PWM can be run from this clock in low power mode.
- Low reference clock—32 KHz low reference clock provided by the CCM. The PWM can be run from this clock in the low power mode.
- Global functional clock—for normal operations. In low power modes this clock can be switched off.

The clock input source is determined by the CLKSRC field of the PWM control register. The CLKSRC value should only be changed when the PWM is disabled.

36.3 Software Operation

The PWM device driver reduces the amount of power sent to a load by varying the width of a series of pulses to the power source. One common and effective use of the PWM is controlling the backlight of a QVGA panel with a variable duty cycle.

Table 36-1 provides a summary of the interface functions in source code.

Table 36-1. PWM Driver Summary

Function	Description
struct pwm_device *pwm_request(int pwm_id, const char *label)	Request a PWM device
void pwm_free(struct pwm_device *pwm)	Free a PWM device
int pwm_config(struct pwm_device *pwm, int duty_ns, int period_ns)	Change a PWM device configuration
int pwm_enable(struct pwm_device *pwm)	Start a PWM output toggling
int pwm_disable(struct pwm_device *pwm)	Stop a PWM output toggling

The function `pwm_config()` includes most of the configuration tasks for the PWM module, including the clock source option, and period and duty cycle of the PWM output signal. It is recommended to select the peripheral clock of the PWM module, rather than the local functional clock, as the local functional clock can change.

36.4 Driver Features

The PWM driver includes the following software and hardware support:

- Duty cycle modulation
- Varying output intervals
- Two power management modes—full on and full of

36.5 Source Code Structure

Table 36-2 lists the source files and headers available in the following directories:

`<ltib_dir>/rpm/BUILD/linux/arch/arm/plat-mxc/pwm.c`

`<ltib_dir>/rpm/BUILD/linux/include/linux/pwm.h`

Table 36-2. PWM Driver Files

File	Description
pwm.h	Functions declaration
pwm.c	Functions definition

36.6 Menu Configuration Options

To get to the PWM driver, use the command `./ltib -c` when located in the `<ltib dir>`. On the screen displayed, select **Configure the kernel** and exit. When the next screen appears select the following option to enable the PWM driver:

- System Type > Enable PWM driver
- Select the following option to enable the Backlight driver:

  Device Drivers > Graphics support > Backlight & LCD device support > Generic PWM based Backlight Driver

Chapter 37
OProfile

OProfile is a system-wide profiler for Linux systems, capable of profiling all running code at low overhead. OProfile is released under the GNU GPL. It consists of a kernel driver, a daemon for collecting sample data, and several post-profiling tools for turning data into information.

37.1 Overview

OProfile leverages the hardware performance counters of the CPU to enable profiling of a wide variety of interesting statistics, which can also be used for basic time-spent profiling. All code is profiled: hardware and software interrupt handlers, kernel modules, the kernel, shared libraries, and applications.

37.2 Features

The features of the OProfile are as follows:

- Unobtrusive—No special recompilations or wrapper libraries are necessary. Even debug symbols (-g option to `gcc`) are not necessary unless users want to produce annotated source. No kernel patch is needed; just insert the module.
- System-wide profiling—All code running on the system is profiled, enabling analysis of system performance.
- Performance counter support—Enables collection of various low-level data and association for particular sections of code.
- Call-graph support—With an 2.6 kernel, OProfile can provide gprof-style call-graph profiling data.
- Low overhead—OProfile has a typical overhead of 1–8% depending on the sampling frequency and workload.
- Post-profile analysis—Profile data can be produced on the function-level or instruction-level detail. Source trees, annotated with profile information, can be created. A hit list of applications and functions that utilize the most CPU time across the whole system can be produced.
- System support—Works with almost any 2.2, 2.4 and 2.6 kernels, and works on based platforms.

37.3 Hardware Operation

OProfile is a statistical continuous profiler. In other words, profiles are generated by regularly sampling the current registers on each CPU (from an interrupt handler, the saved PC value at the time of interrupt is stored), and converting that runtime PC value into something meaningful to the programmer.

OProfile achieves this by taking the stream of sampled PC values, along with the detail of which task was running at the time of the interrupt, and converting the values into a file offset against a particular binary file. Each PC value is thus converted into a tuple (group or set) of binary-image offset. The userspace tools can use this data to reconstruct where the code came from, including the particular assembly instructions, symbol, and source line (through the binary debug information if present).

Regularly sampling the PC value like this approximates what actually was executed and how often and more often than not, this statistical approximation is good enough to reflect reality. In common operation,

the time between each sample interrupt is regulated by a fixed number of clock cycles. This implies that the results reflect where the CPU is spending the most time. This is a very useful information source for performance analysis.

The ARM CPU provides hardware performance counters capable of measuring these events at the hardware level. Typically, these counters increment once per each event and generate an interrupt on reaching some pre-defined number of events. OProfile can use these interrupts to generate samples and the profile results are a statistical approximation of which code caused how many instances of the given event.

37.4 Software Operation

37.4.1 Architecture Specific Components

If OProfile supports the hardware performance counters available on a particular architecture. Code for managing the details of setting up and managing these counters can be located in the kernel source tree in the relevant `<ltib_dir>/rpm/BUILD/linux/arch/arm/oprofile` directory. The architecture-specific implementation operates through filling in the `oprofile_operations` structure at initialization. This provides a set of operations, such as setup(), start(), stop(), and so on, that manage the hardware-specific details the performance counter registers.

The other important facility available to the architecture code is `oprofile_add_sample`(). This is where a particular sample taken at interrupt time is fed into the generic OProfile driver code.

37.4.2 oprofilefs Pseudo Filesystem

OProfile implements a pseudo-filesystem known as oprofilefs, which is mounted from userspace at `/dev/oprofile`. This consists of small files for reporting and receiving configuration from userspace, as well as the actual character device that the OProfile userspace receives samples from. At setup() time, the architecture-specific code may add further configuration files related to the details of the performance counters. The filesystem also contains a `stats` directory with a number of useful counters for various OProfile events.

37.4.3 Generic Kernel Driver

The generic kernel driver resides in `<ltib_dir>/rpm/BUILD/linux/drivers/oprofile/`, and forms the core of how OProfile operates in the kernel. The generic kernel driver takes samples delivered from the architecture-specific code (through `oprofile_add_sample`()), and buffers this data (in a transformed configuration) until releasing the data to the userspace daemon through the `/dev/oprofile/buffer` character device.

37.4.4 OProfile Daemon

The OProfile userspace daemon takes the raw data provided by the kernel and writes it to the disk. It takes the single data stream from the kernel and logs sample data against a number of sample files (available in `/var/lib/oprofile/samples/current/`). For the benefit of the separate functionality, the names and paths

of these sample files are changed to reflect where the samples were from. This can include thread IDs, the binary file path, the event type used, and more.

After this final step from interrupt to disk file, the data is now persistent (that is, changes in the running of the system do not invalidate stored data). This enables the post-profiling tools to run on this data at any time (assuming the original binary files are still available and unchanged).

37.4.5 Post Profiling Tools

The collected data must be presented to the user in a useful form. This is the job of the post-profiling tools. In general, they collate a subset of the available sample files, load and process each one correlated against the relevant binary file, and produce user readable information.

37.5 Requirements

The requirements of OProfile are as follows:

- Add Oprofile support with Cortex-A8 Event Monitor

37.6 Source Code Structure

Oprofile platform-specific source files are available in the directory:

`<ltib_dir>/rpm/BUILD/linux/arch/arm/oprofile/`

Table 37-1. OProfile Source Files

File	Description
op_arm_model.h	Header File with the register and bit definitions
common.c	Source file with the implementation required for all platforms
op_model_v7.c	Source file for ARM V7 (Cortex A8) Event Monitor Driver
op_model_v7.h	Header file for ARM V7 (Cortex A8) Event Monitor Driver

The generic kernel driver for Oprofile is located under `<ltib_dir>/rpm/BUILD/linux/drivers/oprofile/`

37.7 Menu Configuration Options

The following Linux kernel configurations are provided for this module. To get to the Oprofile configuration, use the command `./ltib -c` from the <`ltib dir`>. On the screen, first go to Package list and select oprofile. Then return to the first screen and, select **Configure Kernel**, then exit, and a new screen appears.

- CONFIG_OPROFILE—configuration option for the oprofile driver. In the menuconfig this option is available under

  General Setup > Profiling support (EXPERIMENTAL) > OProfile system profiling (EXPERIMENTAL)

37.8 Programming Interface

This driver implements all the methods required to configure and control PMU and L2 cache EVTMON counters. Refer to the doxygen documentation for more information (in the doxygen folder of the documentation package).

37.9 Interrupt Requirements

The number of interrupts generated with respect to the OProfile driver are numerous. The latency requirements are not needed. The rate at which interrupts are generated depends on the event.

37.10 Example Software Configuration

The following steps show and example of how to configure the OProfile:

1. Use the command `./ltib -c` from the <ltib dir>. On the screen, first go to Package list and select oprofile. The current version in ltib is 0.9.5.
2. Then return to the first screen and select `Configure Kernel`, follow the instruction from Section 37.7, “Menu Configuration Options,” to enable Oprofile in the kernel space.
3. Save the configuration and start to build.
4. Copy Oprofile binaries to target rootfs. Copy vmlinux to `/boot` directory and run Oprofile

```
root@ubuntu:/boot# opcontrol --separate=kernel --vmlinux=/boot/vmlinux
root@ubuntu:/boot# opcontrol --reset
Signalling daemon... done
root@ubuntu:/boot# opcontrol --setup --event=CPU_CYCLES:100000
root@ubuntu:/boot# opcontrol --start
Profiler running.
root@ubuntu:/boot# opcontrol --dump
root@ubuntu:/boot# opreport
Overflow stats not available
CPU: ARM V7 PMNC, speed 0 MHz (estimated)
Counted CPU_CYCLES events (Number of CPU cycles) with a unit mask of 0x00 (No un
it mask) count 100000
CPU_CYCLES:100000|
  samples|      %|
------------------
        4 22.2222 grep
        CPU_CYCLES:100000|
```

```
          samples|      %|
        ------------------
                4 100.000 libc-2.9.so
        2 11.1111 cat
        CPU_CYCLES:100000|
          samples|      %|
        ------------------
                1 50.0000 ld-2.9.so
                1 50.0000 libc-2.9.so
...
root@ubuntu:/boot# opcontrol --stop
Stopping profiling.
```