

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.9.3.1 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 39 provides EIM interface pads allocation in different modes.

Table 39. EIM Internal Module Multiplexing¹

Setup	Non Multiplexed Address/Data Mode							Multiplexed Address/Data mode	
	8 Bit				16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_DATA [09:00]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	—	—	EIM_DATA [07:00]	—	EIM_DATA [07:00]	EIM_AD [07:00]	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	—	—	EIM_DATA [15:08]	—	EIM_DATA [15:08]	EIM_AD [15:08]	EIM_AD [15:08]
EIM_DATA [23:16], EIM_EB2_B	—	—	EIM_DATA [23:16]	—	—	EIM_DATA [23:16]	EIM_DATA [23:16]	—	EIM_DATA [07:00]
EIM_DATA [31:24], EIM_EB3_B	—	—	—	EIM_DATA [31:24]	—	EIM_DATA [31:24]	EIM_DATA [31:24]	—	EIM_DATA [15:08]

¹ For more information on configuration ports mentioned in this table, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 12, Figure 13, and Table 40 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

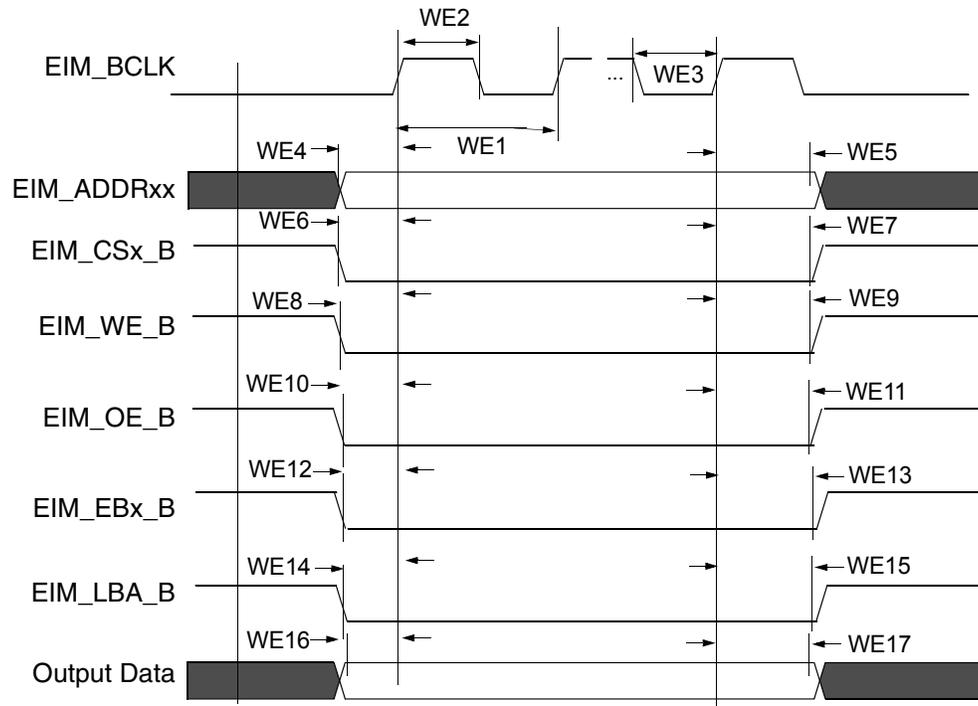


Figure 12. EIM Output Timing Diagram

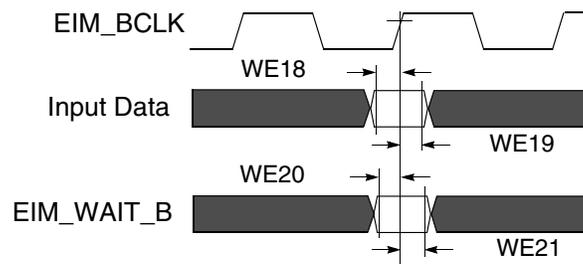


Figure 13. EIM Input Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 40. EIM Bus Timing Parameters

ID	Parameter	Min ¹	Max ¹	Unit
WE1	EIM_BCLK cycle time ²	$t \times (k+1)$	—	ns
WE2	EIM_BCLK high level width	$0.4 \times t \times (k+1)$	—	ns
WE3	EIM_BCLK low level width	$0.4 \times t \times (k+1)$	—	ns

Table 40. EIM Bus Timing Parameters (continued)

ID	Parameter	Min ¹	Max ¹	Unit
WE4	Clock rise to address valid	$-0.5 \times t \times (k+1) - 1.25$	$-0.5 \times t \times (k+1) + 2.25$	ns
WE5	Clock rise to address invalid	$0.5 \times t \times (k+1) - 1.25$	$0.5 \times t \times (k+1) + 2.25$	ns
WE6	Clock rise to EIM_CSx_B valid	$-0.5 \times t \times (k+1) - 1.25$	$-0.5 \times t \times (k+1) + 2.25$	ns
WE7	Clock rise to EIM_CSx_B invalid	$0.5 \times t \times (k+1) - 1.25$	$0.5 \times t \times (k+1) + 2.25$	ns
WE8	Clock rise to EIM_WE_B valid	$-0.5 \times t \times (k+1) - 1.25$	$-0.5 \times t \times (k+1) + 2.25$	ns
WE9	Clock rise to EIM_WE_B invalid	$0.5 \times t \times (k+1) - 1.25$	$0.5 \times t \times (k+1) + 2.25$	ns
WE10	Clock rise to EIM_OE_B valid	$-0.5 \times t \times (k+1) - 1.25$	$-0.5 \times t \times (k+1) + 2.25$	ns
WE11	Clock rise to EIM_OE_B invalid	$0.5 \times t \times (k+1) - 1.25$	$0.5 \times t \times (k+1) + 2.25$	ns
WE12	Clock rise to EIM_EBx_B valid	$-0.5 \times t \times (k+1) - 1.25$	$-0.5 \times t \times (k+1) + 2.25$	ns
WE13	Clock rise to EIM_EBx_B invalid	$0.5 \times t \times (k+1) - 1.25$	$0.5 \times t \times (k+1) + 2.25$	ns
WE14	Clock rise to EIM_LBA_B valid	$-0.5 \times t \times (k+1) - 1.25$	$-0.5 \times t \times (k+1) + 2.25$	ns
WE15	Clock rise to EIM_LBA_B invalid	$0.5 \times t \times (k+1) - 1.25$	$0.5 \times t \times (k+1) + 2.25$	ns
WE16	Clock rise to output data valid	$-0.5 \times t \times (k+1) - 1.25$	$-0.5 \times t \times (k+1) + 2.25$	ns
WE17	Clock rise to output data invalid	$0.5 \times t \times (k+1) - 1.25$	$0.5 \times t \times (k+1) + 2.25$	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from clock rise	2	—	ns

¹ k represents register setting BCD value.

² t is clock period (1/Freq). For 104 MHz, t = 9.165 ns.

Figure 14 to Figure 17 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

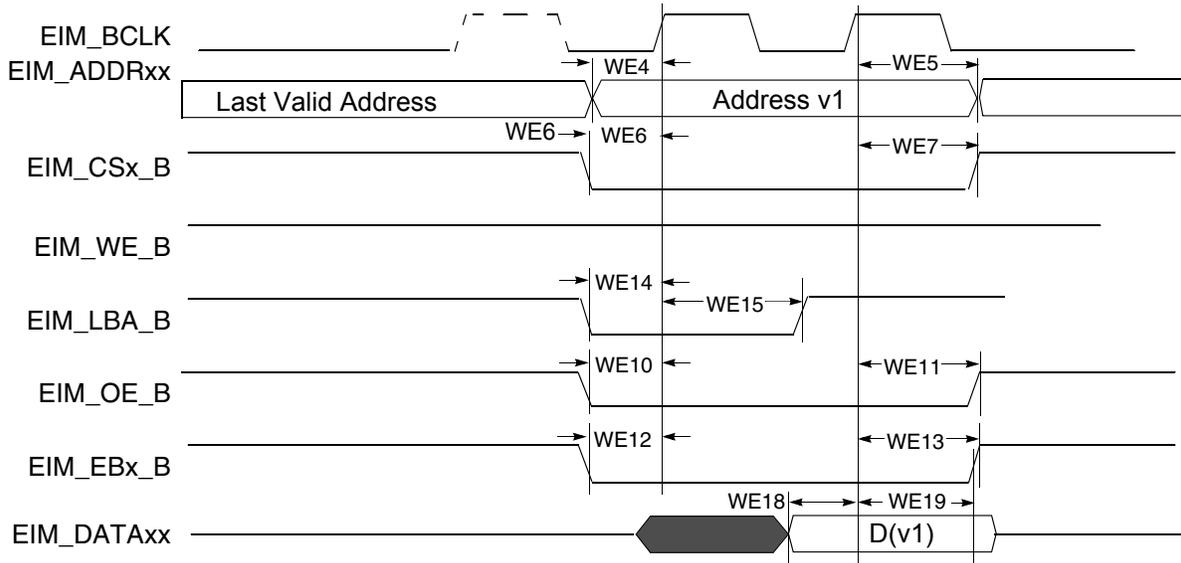


Figure 14. Synchronous Memory Read Access, WSC=1

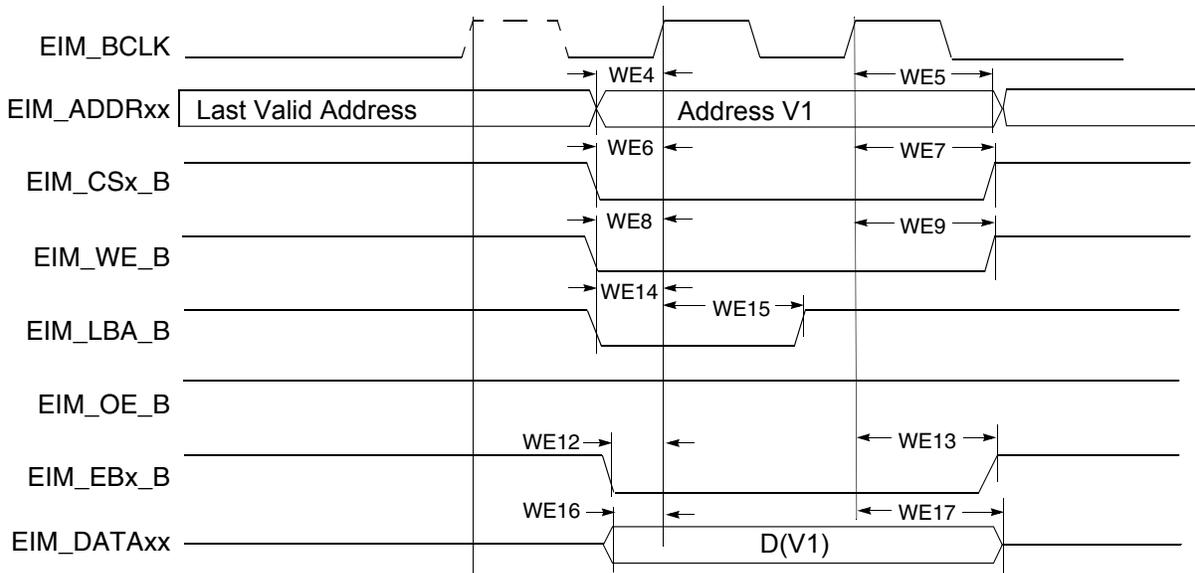


Figure 15. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADV=0

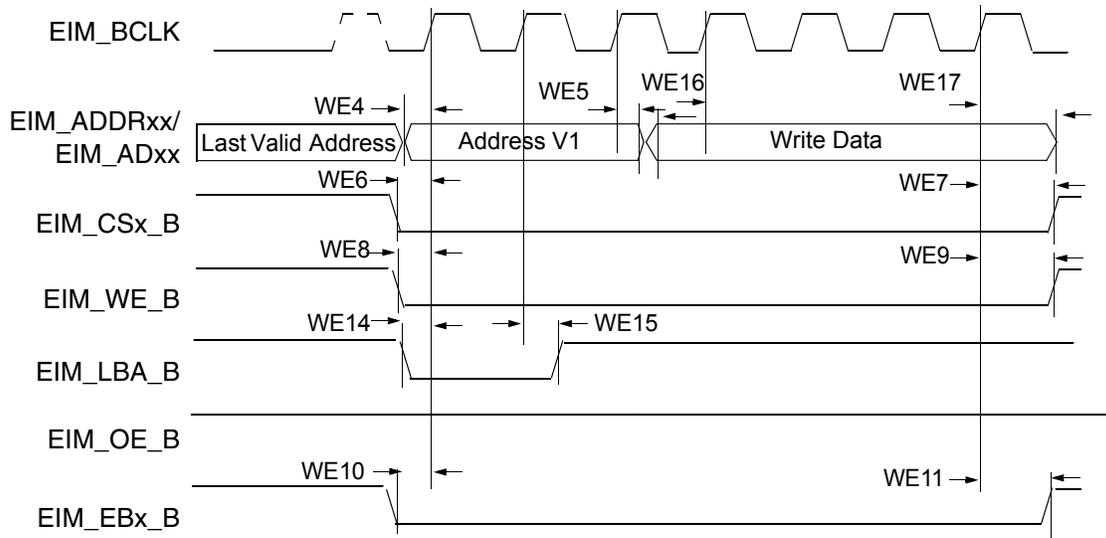


Figure 16. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

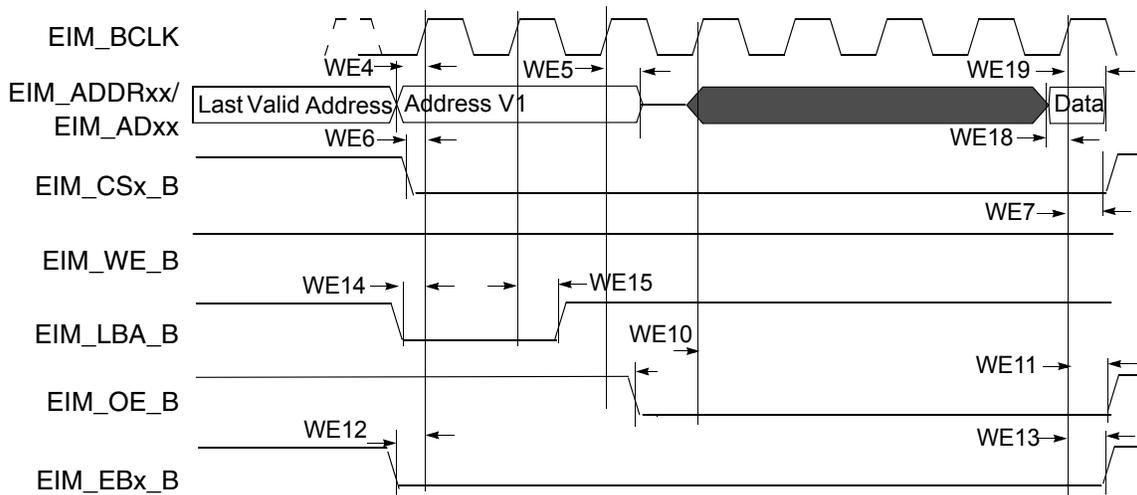


Figure 17. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 18 through Figure 22 and Table 41 provide timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 18 through Figure 21 as RWSC, OEN & CSN is configured differently. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for the EIM programming model.

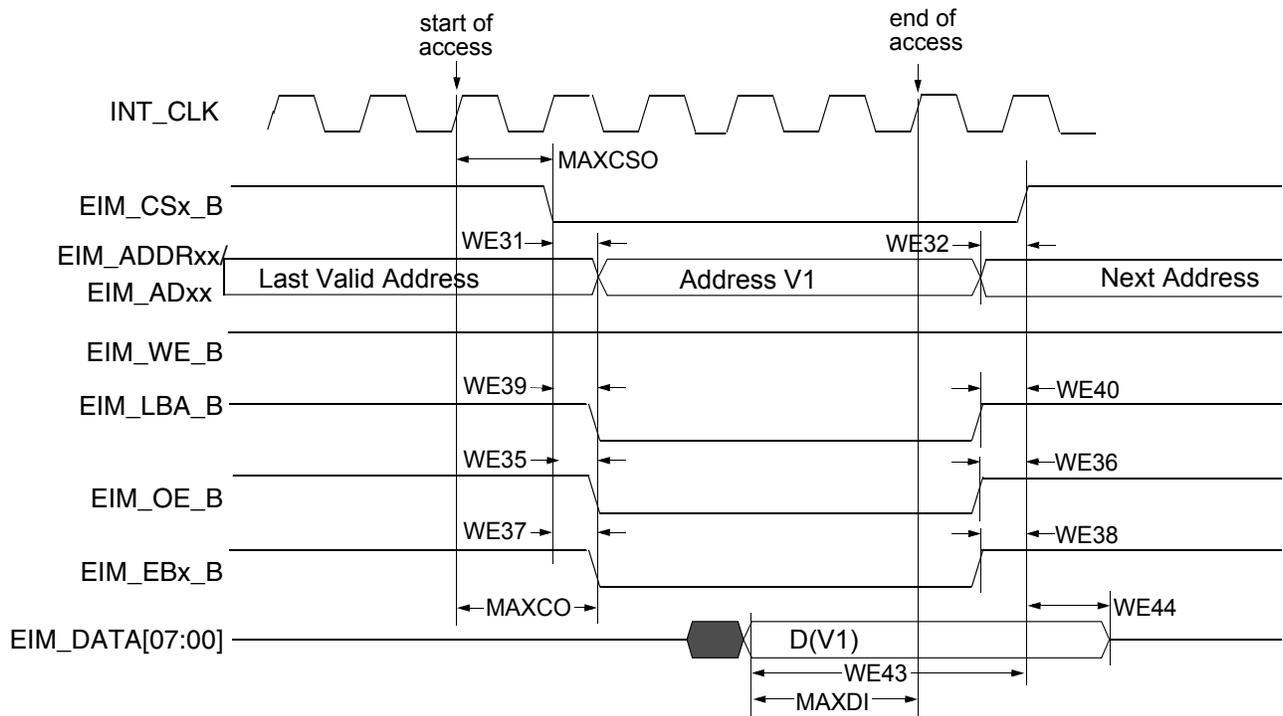


Figure 18. Asynchronous Memory Read Access (RWSC = 5)

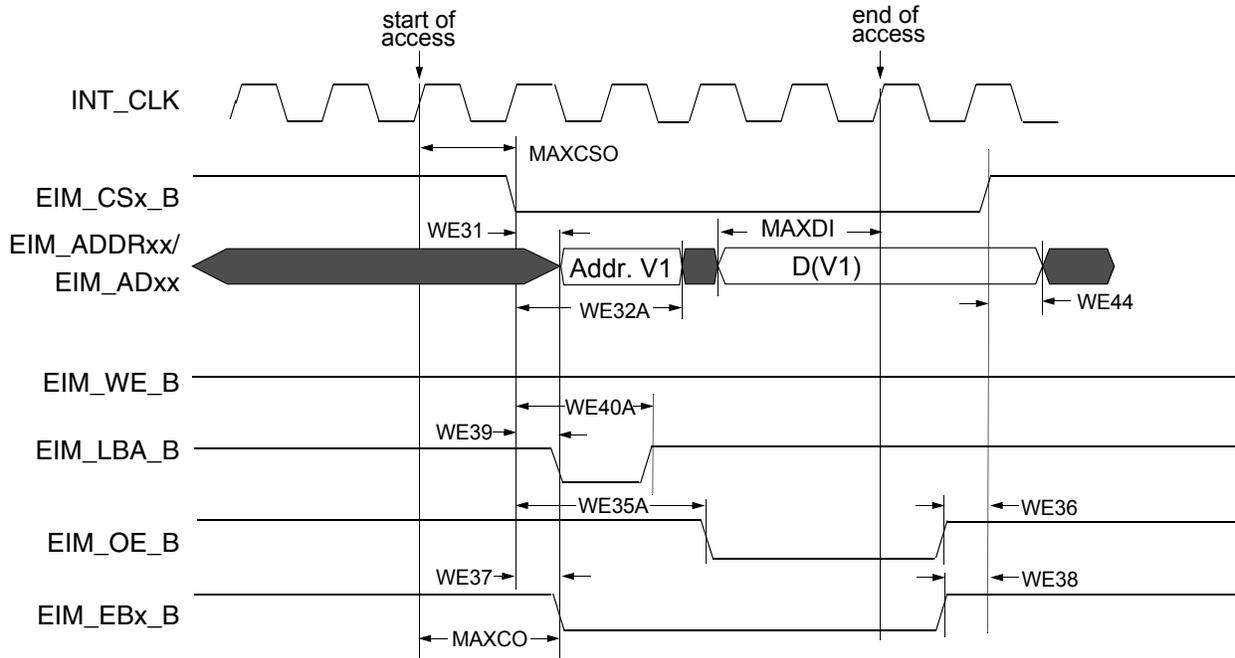


Figure 19. Asynchronous A/D Muxed Read Access (RWSC = 5)

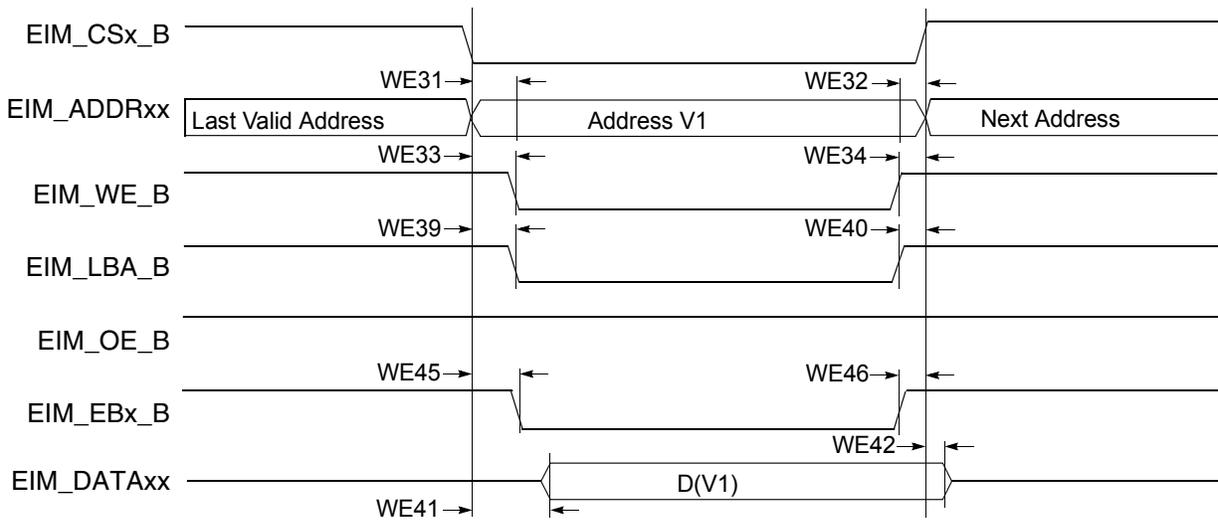


Figure 20. Asynchronous Memory Write Access

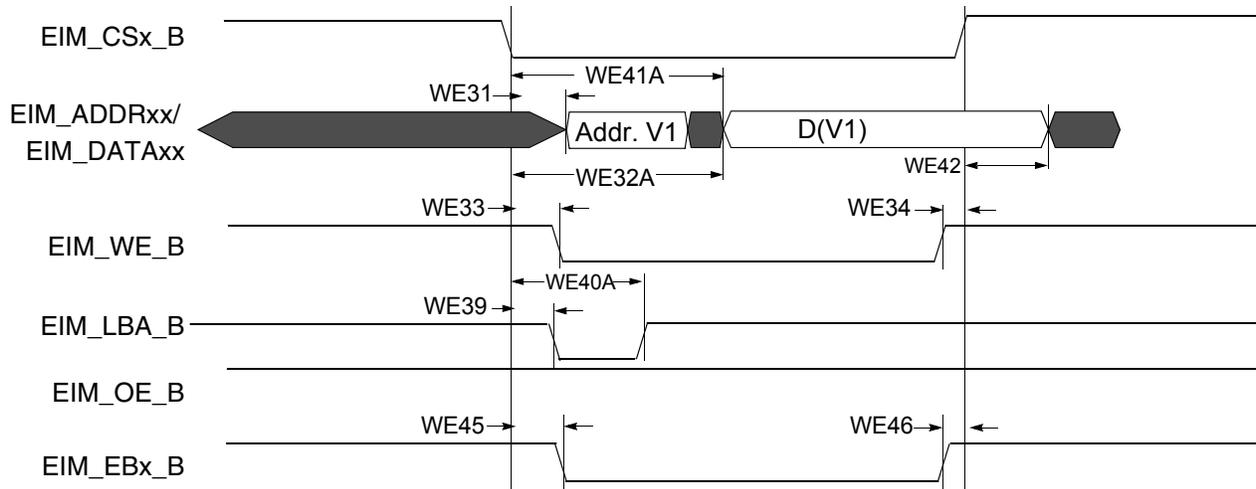


Figure 21. Asynchronous A/D Muxed Write Access

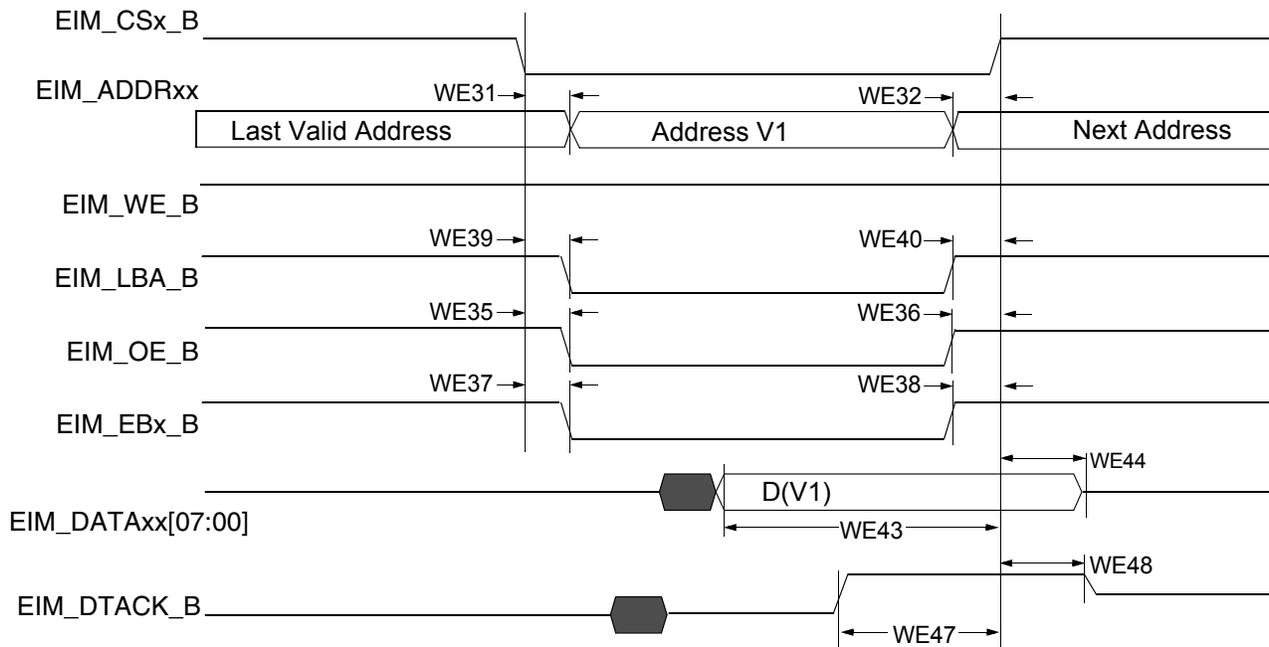


Figure 22. DTACK Mode Read Access (DAP=0)

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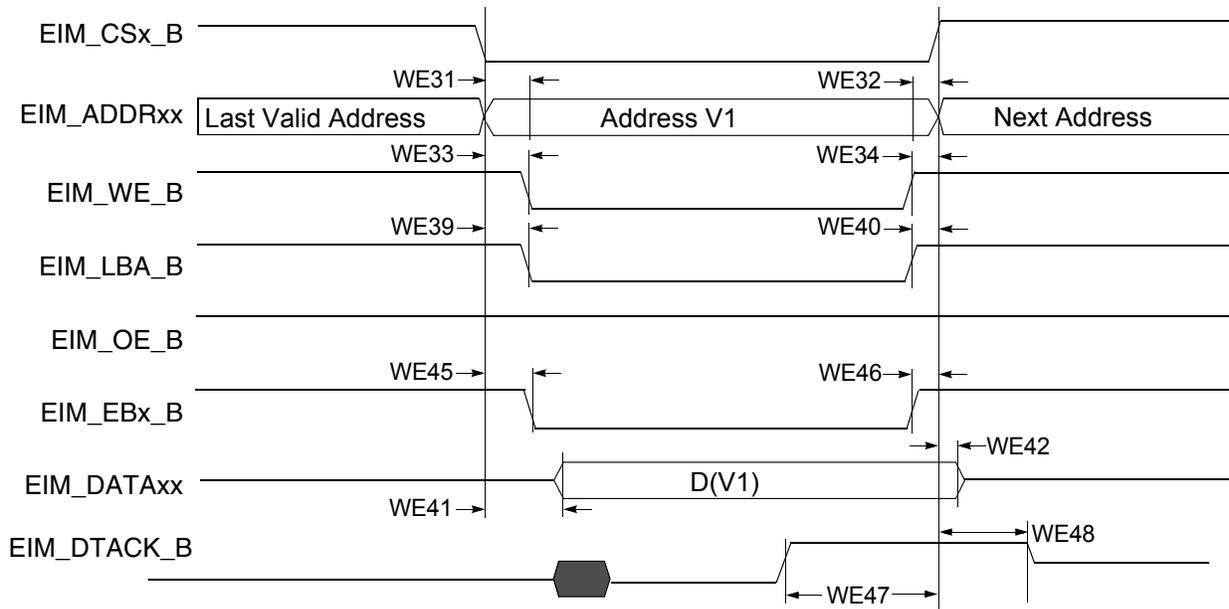


Figure 23. DTACK Mode Write Access (DAP=0)

Table 41. EIM Asynchronous Timing Parameters Relative to Chip Select^{1, 2}

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4-WE6-CSA×t	-3.5-CSA×t	3.5-CSA×t	ns
WE32	Address Invalid to EIM_CSx_B Invalid	WE7-WE5-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
WE32A (muxed A/D)	EIM_CSx_B valid to Address Invalid	t+WE4-WE7+(ADVN+ADVA+1-CSA)×t	t-3.5+(ADVN+ADVA+1-CSA)×t	t+3.5+(ADVN+ADVA+1-CSA)×t	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8-WE6+(WEA-WCSA)×t	-3.5+(WEA-WCSA)×t	3.5+(WEA-WCSA)×t	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7-WE9+(WEN-WCSN)×t	-3.5+(WEN-WCSN)×t	3.5+(WEN-WCSN)×t	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10-WE6+(OEA-RCSA)×t	-3.5+(OEA-RCSA)×t	3.5+(OEA-RCSA)×t	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10-WE6+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	-3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7-WE11+(OEN-RCSN)×t	-3.5+(OEN-RCSN)×t	3.5+(OEN-RCSN)×t	ns
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12-WE6+(RBEA-RCSA)×t	-3.5+(RBEA-RCSA)×t	3.5+(RBEA-RCSA)×t	ns
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7-WE13+(RBEN-RCSN)×t	-3.5+(RBEN-RCSN)×t	3.5+(RBEN-RCSN)×t	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14-WE6+(ADVA-CSA)×t	-3.5+(ADVA-CSA)×t	3.5+(ADVA-CSA)×t	ns

Table 41. EIM Asynchronous Timing Parameters Relative to Chip Select^{1,2} (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7-WE15-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14-WE6+(ADVN+ADVA+1-CSA)×t	-3.5+(ADVN+ADVA+1-CSA)×t	3.5+(ADVN+ADVA+1-CSA)×t	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16-WE6-WCSA×t	-3.5-WCSA×t	3.5-WCSA×t	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16-WE6+(WADV+ADVA+ADH+1-WCSA)×t	-3.5+(WADV+ADVA+ADH+1-WCSA)×t	3.5+(WADV+ADVA+ADH+1-WCSA)×t	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17-WE7-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control flip-flops to chip outputs.	10	—	10	ns
MAXCSO	Output maximum delay from internal chip selects driving flip-flops to EIM_CSx_B out.	10	—	10	ns
MAXDI	EIM_DATAxx MAXIMUM delay from chip input data to its internal flip-flop	5	—	5	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDI	MAXCO-MAXCSO+MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data Invalid	0	0	—	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12-WE6+(WBEA-WCSA)×t	-3.5+(WBEA-WCSA)×t	3.5+(WBEA-WCSA)×t	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7-WE13+(WBEN-WCSN)×t	-3.5+(WBEN-WCSN)×t	3.5+(WBEN-WCSN)×t	ns
MAXDTI	Maximum delay from EIM_DTACK_B input to its internal flip-flop + 2 cycles for synchronization	10	—	10	ns
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDTI	MAXCO-MAXCSO+MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B invalid	0	0	—	ns

¹ For more information on configuration parameters mentioned in this table, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

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² In this table:

- t means clock period from axi_clk frequency.
- CSA means register setting for WCSA when in write operations or RCSA when in read operations.
- CSN means register setting for WCSN when in write operations or RCSN when in read operations.
- ADVN means register setting for WADV when in write operations or RADVN when in read operations.
- ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

4.9.4 DDR SDRAM Specific Parameters (DDR3/DDR3L and LPDDR2)

4.9.4.1 DDR3/DDR3L Parameters

Figure 24 shows the DDR3/DDR3L basic timing diagram. The timing parameters for this diagram appear in Table 42.

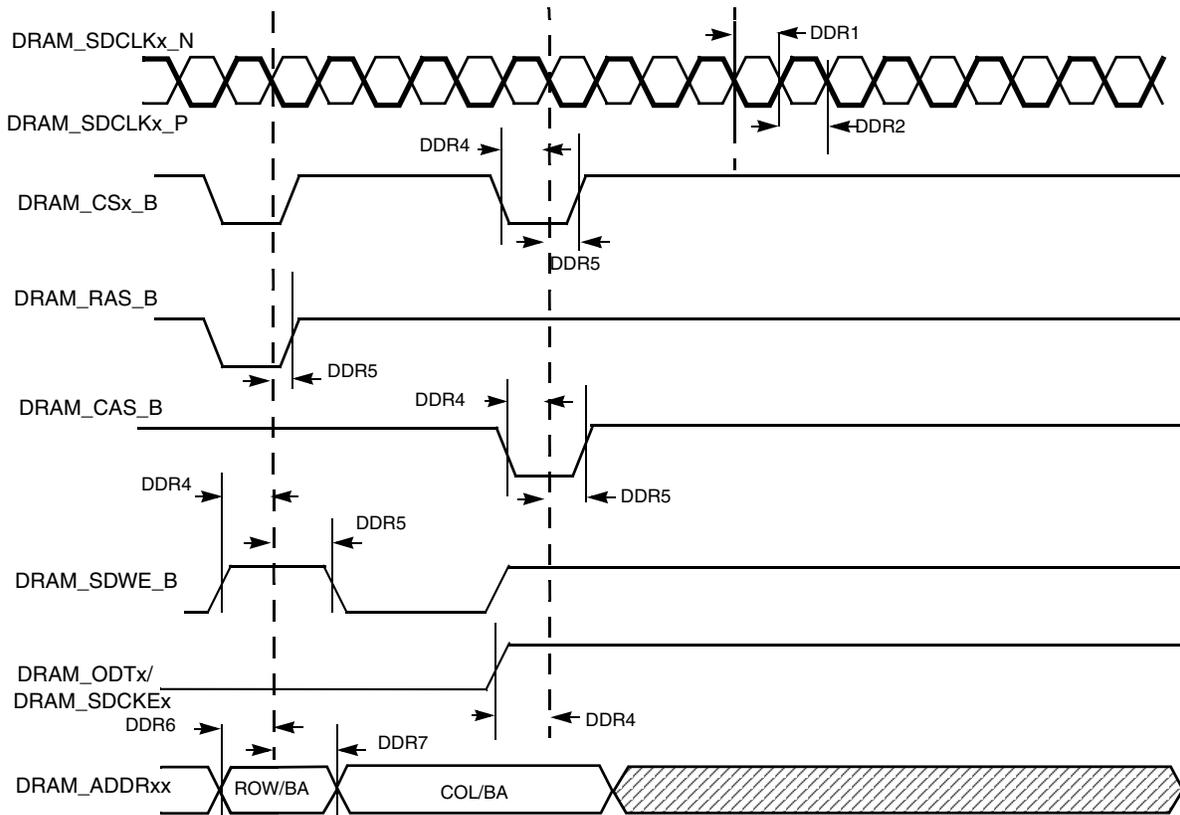


Figure 24. DDR3/DDR3L Command and Address Timing Diagram

Table 42. DDR3/DDR3L Timing Parameter Table

ID	Parameter ^{1,2}	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR1	DRAM_SDCLKx_P clock high-level width	tCH	0.47	0.53	tCK
DDR2	DRAM_SDCLKx_P clock low-level width	tCL	0.47	0.53	tCK