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Revisions

Rev	Description	Date	Approved
A	First version. Based on CPU1 schematics	xx/xx/10	Eyal L.
A	Changed DDR3 memories to LPDDR2 memory. Also replaced power of the LPDDR2.		
A	Changed connectivity of HSIC USB ports to Port5 instead of Port1 to decrease the net length		

i.MX6Quad
LPDDR2 CPU board

Marketing P/N: MX6QCPULPDDR2
Description: I.MX6Q ARIK LPDDR2 CPU Board FIL P/N: 084-00461-1
PCB P/N: 700-27122 rev X {PROTOTYPE}
SCH-27122 {PDF} SPF-27122

freescale semiconductor

Multimedia Application Division, Wireless & Mobile System Group

ICAP Classification: FCP: FIUO: PUBI:

Designer: DESIGNER	Drawing Title: MX6QCPULPDDR2		
Drawn by: DRAWN_BY	Page Title: COVER		
Approved: <Approver>	Size C	Document Number SOURCE:SCH-27016 PDF:SPF-27016	Rev X
	Date: Wednesday, May 25, 2011	Sheet 1 of 23	

GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 1%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

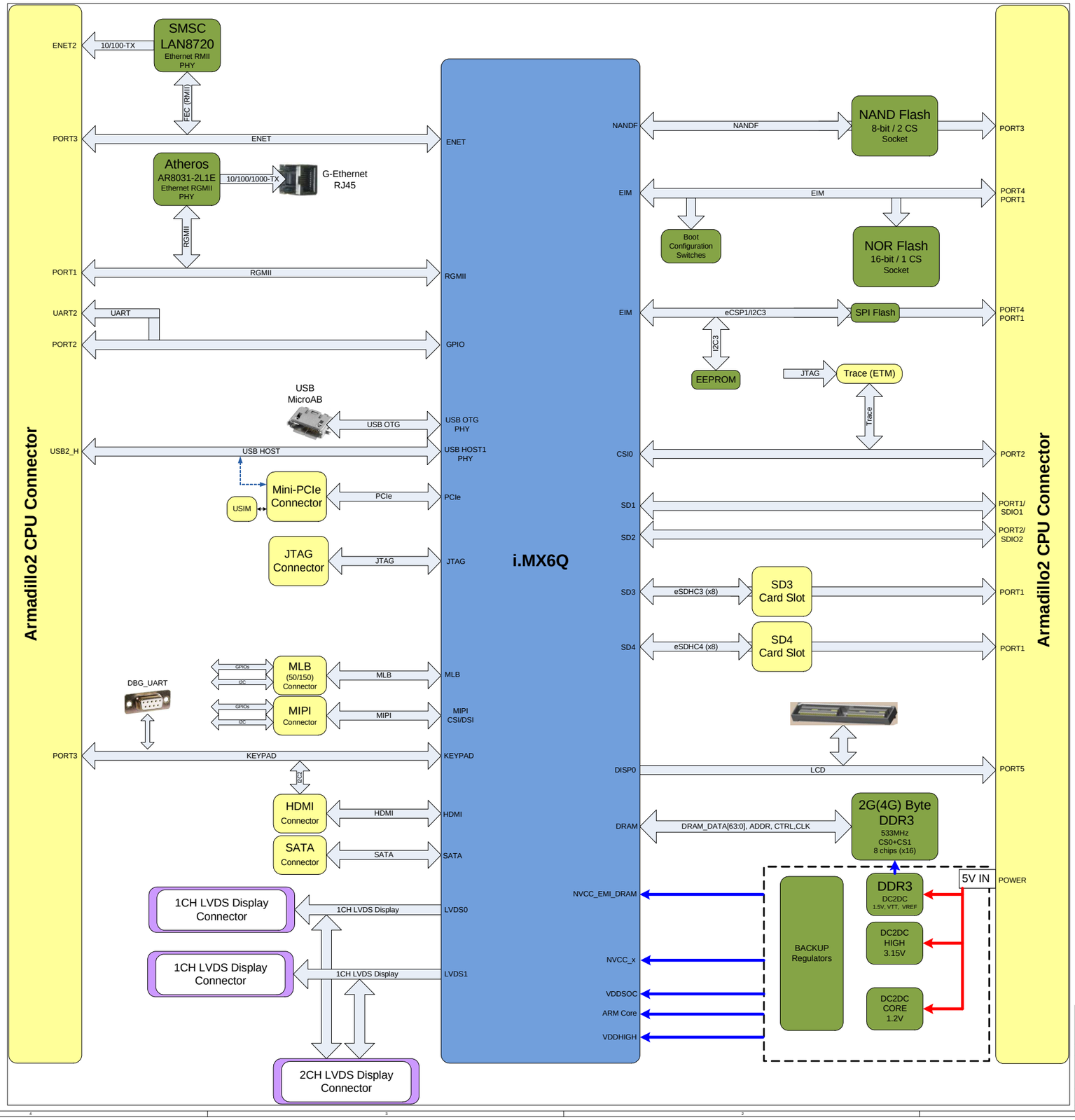
3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC
Current Output: > 3A (depending on application)
Polarity:
Inner Diameter: 2.1mm
Outer Diameter: 5.5mm



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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **MX6QCPULPDDR2**

Page Title: **Block Diagram**

Size	Document Number	Rev
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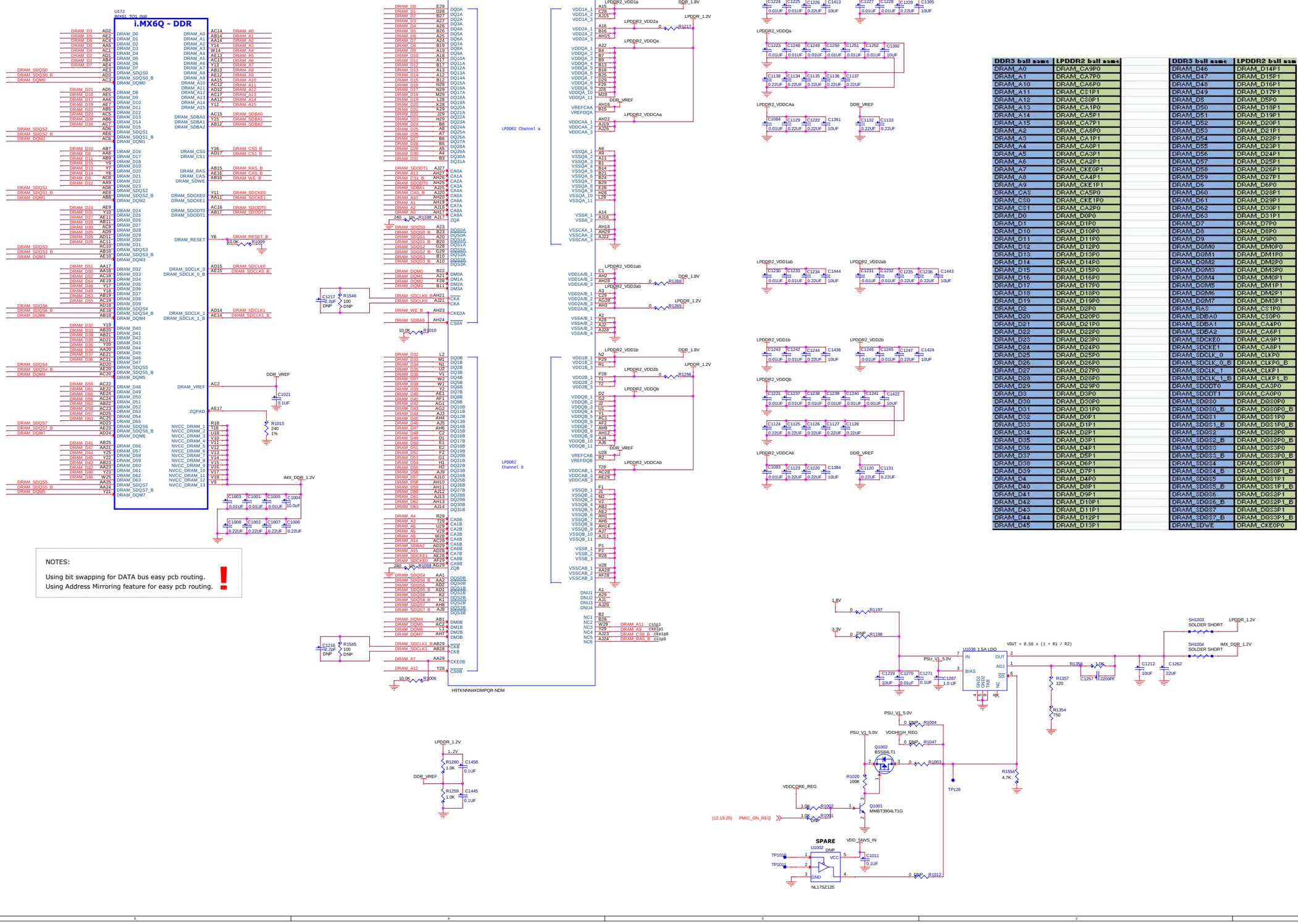

DDR3 ball name	LPDDR2 ball name	DDR3 ball name	LPDDR2 ball name
DRAM_A0	DRAM_CA9P0	DRAM_D46	DRAM_D14P1
DRAM_A1	DRAM_CA7P0	DRAM_D47	DRAM_D15P1
DRAM_A10	DRAM_CA5P0	DRAM_D48	DRAM_D16P1
DRAM_A11	DRAM_CS1P1	DRAM_D49	DRAM_D17P1
DRAM_A12	DRAM_CS0P1	DRAM_D5	DRAM_D5P0
DRAM_A13	DRAM_CA1P0	DRAM_D50	DRAM_D18P1
DRAM_A14	DRAM_CA5P1	DRAM_D51	DRAM_D19P1
DRAM_A15	DRAM_CA7P1	DRAM_D52	DRAM_D20P1
DRAM_A2	DRAM_CA8P0	DRAM_D53	DRAM_D21P1
DRAM_A3	DRAM_CA1P1	DRAM_D54	DRAM_D22P1
DRAM_A4	DRAM_CA0P1	DRAM_D55	DRAM_D23P1
DRAM_A5	DRAM_CA3P1	DRAM_D56	DRAM_D24P1
DRAM_A6	DRAM_CA2P1	DRAM_D57	DRAM_D25P1
DRAM_A7	DRAM_CKE0P1	DRAM_D58	DRAM_D26P1
DRAM_A8	DRAM_CA4P1	DRAM_D59	DRAM_D27P1
DRAM_A9	DRAM_CKE1P1	DRAM_D6	DRAM_D6P0
DRAM_CAS	DRAM_CA5P0	DRAM_D60	DRAM_D28P1
DRAM_CS0	DRAM_CKE1P0	DRAM_D61	DRAM_D29P1
DRAM_CS1	DRAM_CA2P0	DRAM_D62	DRAM_D30P1
DRAM_D0	DRAM_D0P0	DRAM_D63	DRAM_D31P1
DRAM_D1	DRAM_D1P0	DRAM_D7	DRAM_D7P0
DRAM_D10	DRAM_D10P0	DRAM_D8	DRAM_D8P0
DRAM_D11	DRAM_D11P0	DRAM_D9	DRAM_D9P0
DRAM_D12	DRAM_D12P0	DRAM_DQM0	DRAM_DM0P0
DRAM_D13	DRAM_D13P0	DRAM_DQM1	DRAM_DM1P0
DRAM_D14	DRAM_D14P0	DRAM_DQM2	DRAM_DM2P0
DRAM_D15	DRAM_D15P0	DRAM_DQM3	DRAM_DM3P0
DRAM_D16	DRAM_D16P0	DRAM_DQM4	DRAM_DM0P1
DRAM_D17	DRAM_D17P0	DRAM_DQM5	DRAM_DM1P1
DRAM_D18	DRAM_D18P0	DRAM_DQM6	DRAM_DM2P1
DRAM_D19	DRAM_D19P0	DRAM_DQM7	DRAM_DM3P1
DRAM_D2	DRAM_D2P0	DRAM_RAS	DRAM_CS1P0
DRAM_D20	DRAM_D20P0	DRAM_SDBA0	DRAM_CS0P0
DRAM_D21	DRAM_D21P0	DRAM_SDBA1	DRAM_CA4P0
DRAM_D22	DRAM_D22P0	DRAM_SDBA2	DRAM_CA6P1
DRAM_D23	DRAM_D23P0	DRAM_SDCKE0	DRAM_CA9P1
DRAM_D24	DRAM_D24P0	DRAM_SDCKE1	DRAM_CA8P1
DRAM_D25	DRAM_D25P0	DRAM_SDCLK_0	DRAM_CLKP0
DRAM_D26	DRAM_D26P0	DRAM_SDCLK_0_B	DRAM_CLKP0_B
DRAM_D27	DRAM_D27P0	DRAM_SDCLK_1	DRAM_CLKP1
DRAM_D28	DRAM_D28P0	DRAM_SDCLK_1_B	DRAM_CLKP1_B
DRAM_D29	DRAM_D29P0	DRAM_SDODT0	DRAM_CA3P0
DRAM_D3	DRAM_D3P0	DRAM_SDODT1	DRAM_CA0P0
DRAM_D30	DRAM_D30P0	DRAM_SDQS0	DRAM_DQS0P0
DRAM_D31	DRAM_D31P0	DRAM_SDQS0_B	DRAM_DQS0P0_B
DRAM_D32	DRAM_D0P1	DRAM_SDQS1	DRAM_DQS1P0
DRAM_D33	DRAM_D1P1	DRAM_SDQS1_B	DRAM_DQS1P0_B
DRAM_D34	DRAM_D2P1	DRAM_SDQS2	DRAM_DQS2P0
DRAM_D35	DRAM_D3P1	DRAM_SDQS2_B	DRAM_DQS2P0_B
DRAM_D36	DRAM_D4P1	DRAM_SDQS3	DRAM_DQS3P0
DRAM_D37	DRAM_D5P1	DRAM_SDQS3_B	DRAM_DQS3P0_B
DRAM_D38	DRAM_D6P1	DRAM_SDQS4	DRAM_DQS0P1
DRAM_D39	DRAM_D7P1	DRAM_SDQS4_B	DRAM_DQS0P1_B
DRAM_D4	DRAM_D4P0	DRAM_SDQS5	DRAM_DQS1P1
DRAM_D40	DRAM_D8P1	DRAM_SDQS5_B	DRAM_DQS1P1_B
DRAM_D41	DRAM_D9P1	DRAM_SDQS6	DRAM_DQS2P1
DRAM_D42	DRAM_D10P1	DRAM_SDQS6_B	DRAM_DQS2P1_B
DRAM_D43	DRAM_D11P1	DRAM_SDQS7	DRAM_DQS3P1
DRAM_D44	DRAM_D12P1	DRAM_SDQS7_B	DRAM_DQS3P1_B
DRAM_D45	DRAM_D13P1	DRAM_SDWE	DRAM_CKE0P0

U17A
IMX61_TO1_0p8

i.MX6Q - EIM

NVCC_EIM1: EIM_LBA, EIM_OE, EIM_RW, EIM_CS0, EIM_CS1, EIM_A16–EIM_A24, EIM_A25
NVCC_EIM0: EIM_D16–EIM_D31, EIM_EB2, EIM_EB3, EIM_BCLK, EIM_WAIT
NVCC_EIM2: EIM_EB0, EIM_EB1, EIM_DA0–EIM_DA15

K22	EIM_LBA	0	R843	PORT4_P79 {17}	LCD_PWR_EN
J24	EIM_OE	0	R776	PORT4_P37 {17}	LCD_PS
K20	EIM_RW	0	R607	PORT4_P120 {17}	LCD_REV
H24	EIM_CS0	0	R774	PORT4_P118 {17}	LCD_SPL
J23	EIM_CS1	0	R842	PORT4_P53 {13,17}	LCD_CLS
H25	DISP1_CLK	0 R802 EIM_A16	0 R808	PORT4_P43 {17}	DI1_DISP_CLK
G24	EIM_A17			PORT4_P86 {17}	LCD_D12
J22	EIM_A18			PORT4_P88 {17}	LCD_D13
G25	EIM_A19			PORT4_P90 {17}	LCD_D14
H22	EIM_A20			PORT4_P92 {17}	LCD_D15
H23	EIM_A21			PORT4_P94 {17}	LCD_D16
F24	EIM_A22			PORT4_P96 {17}	LCD_D17
J21	EIM_A23			PORT4_P98 {17}	LCD_D18
F25	EIM_A24			PORT4_P100 {17}	LCD_D19
H19	EIM_A25	0	R807	PORT4_P117 {17}	LCD_RD
C25	EIM_D16	0	R775	PORT4_P89 {17}	LCD_SCLK
F21	EIM_D17	0	R781	PORT4_P85 {17}	LCD_DOUT
D24	EIM_D18	0	R782	PORT4_P87 {17}	LCD_DIN
G21	EIM_D19	0	R785	PORT4_P91 {17}	LCD_SER_RS_DEN
G20	EIM_D20			EIM_D20 {9}	
H20	EIM_D21			EIM_D21 {6,9}	
E23	EIM_D22	0	R800	PORT5_P59 {17}	
D25	EIM_D23	0	R799	PORT4_P63 {17}	LCD_PAR_RS2
F22	EIM_D24			PORT2_P38 {9,17}	LCD_PORTS_PWR_EN
G22	EIM_D25			PORT2_P40 {17}	GP_LED
E24	EIM_D26	0	R783	PORT4_P106 {17}	LCD_D22
E25	EIM_D27	0	R786	PORT4_P108 {17}	LCD_D23
G23	EIM_D28	0	R790	PORT5_P119 {17}	
J19	EIM_D29	0	R795	PORT5_P63 {17}	
J20	EIM_D30	0	R797	PORT4_P104 {17}	LCD_D21
H21	EIM_D31	0	R803	PORT4_P102 {17}	LCD_D20
E22	EIM_EB2	0	R338	PORT4_P81 {17}	LCD_CS#
F23	EIM_EB3	0	R741	PORT4_P33 {17}	LCD_LCS1_RST
N22	EIM_BCLK			PORT1_P88 {17}	
M25	EIM_WAIT			PORT1_P86 {9,17}	
K21	EIM_EB0	0	R335	PORT4_P84 {17}	LCD_D11
K23	EIM_EB1	0	R336	PORT4_P82 {17}	LCD_D10
L20	EIM_DA0			PORT4_P80 {17}	LCD_D9
J25	EIM_DA1			PORT4_P78 {17}	LCD_D8
L21	EIM_DA2			PORT4_P76 {17}	LCD_D7
K24	EIM_DA3			PORT4_P74 {17}	LCD_D6
L22	EIM_DA4			PORT4_P72 {17}	LCD_D5
L23	EIM_DA5			PORT4_P70 {17}	LCD_D4
K25	EIM_DA6			PORT4_P68 {17}	LCD_D3
L25	EIM_DA7			PORT4_P66 {17}	LCD_D2
L24	EIM_DA8			PORT4_P64 {17}	LCD_D1
M21	EIM_DA9			PORT4_P62 {17}	LCD_D0
M22	EIM_DA10	0	R609	PORT4_P116 {17}	LCD_DRDY
M20	EIM_DA11	0	R610	PORT4_P114 {17}	LCD_HSYNC
M24	EIM_DA12	0	R612	PORT4_P110 {17}	LCD_VSYNC
M23	EIM_DA13	0	R614	PORT4_P105 {17}	LCD_LCS0
N23	EIM_DA14	0	R616	PORT4_P107 {17}	LCD_CS#
N24	EIM_DA15	0	R618	PORT4_P112 {9,17}	LCD_CONTRAST
		0	R617	PORT4_P59 {17}	LCD_SD_I

SPI: LCD_SCLK, LCD_DOUT, LCD_DIN, LCD_SER_RS_DEN

eCSPI1 (SS0)

EIM_EB2	0 R695	PORT3_P91	{17}
EIM_D16	R696	PORT3_P89	{17}
EIM_D17	R698	PORT3_P85	{17}
EIM_D18	R697	PORT3_P87	{17}

EIM_A25 → EIM_A25 {9,10}

EIM_D16 → EIM_D16 {9}
EIM_D17 → EIM_D17 {9}
EIM_D18 → EIM_D18 {9}
EIM_D19 → EIM_D19 {9}

EIM_D22 → EIM_D22 {6,9}
EIM_D23 → EIM_D23 {9}
EIM_D24 → EIM_D24 {9,17}

EIM_D26	0 R819	PORT4_P109 {17}	LCD_WR
EIM_D27	R817	PORT4_P119 {17}	LCD_PAR_RS1
EIM_D28		EIM_D28 {9,17}	
EIM_D29		EIM_D29 {9,17}	
EIM_D30		EIM_D30 {6,9}	
EIM_D31		EIM_D31 {6,9}	

{17} UART2_RX	UART2_RX	0 R727	EIM_D26
{17} UART2_TX	UART2_TX	0 R726	EIM_D27
{9,17} UART2_RTS			EIM_D29
{9,17} UART2_CTS			EIM_D28
{17} UART2_DTR	0 R531		
{17} UART2_DSR			

NOR Flash Socket (TSOP56)

DNP U60 — SKT TSOP 56 SMT

EIM_DA0	31	43	NRF1 3.3V
EIM_DA1	26	29	NRF2 3.3V
EIM_DA2	25	35	EIM_D16
EIM_DA3	24	37	EIM_D17
EIM_DA4	23	39	EIM_D18
EIM_DA5	22	41	EIM_D19
EIM_DA6	21	44	EIM_D20
EIM_DA7	20	46	EIM_D21
EIM_DA8	10	48	EIM_D22
EIM_DA9	9	50	EIM_D23
EIM_DA10	8	36	EIM_D24
EIM_DA11	7	38	EIM_D25
EIM_DA12	6	40	EIM_D26
EIM_DA13	5	42	EIM_D27
EIM_DA14	4	45	EIM_D28
EIM_DA15	3	47	EIM_D29
EIM_A16	54	49	EIM_D30
EIM_A17	19	51	EIM_D31
EIM_A18	18	14	NOR_RST_N → PORT3_P38 {5,11,12,14,17,20}
EIM_A19	11	27	
EIM_A20	12	28	
EIM_A21	15	30	
EIM_A22	2	55	EIM_A25
EIM_A23	1	17	0 DNP R666 EIM_WAIT
EIM_A24	56		3.3V, 10.0K R662
EIM_OE	34	33	
EIM_RW	13	52	
BYTE_N	53		
NOR_WP_N	16		
EIM_CS0	32		

C479 0.1UF, C480 0.1UF, 3.3V, 0 R787, 0 R772

3.3V — R811 10.0K — DNP R810 0
3.3V — R673 10.0K — DNP R672 0

SPI NOR Flash

3.3V — C493 4.7uF, C494 0.1UF

U78 — M25P32-VMW6TG

EIM_D18	0 R880	SPI_NOR_MOSI	5 D
EIM_D16	0 R881	SPI_NOR_SCK	6 C
EIM_D19	0 R887	SPI_NOR_CS_B	1 S
SPI_NOR_WP_B			3 W/VPP
		SPI_NOR_MISO	2 Q — 0 R886 EIM_D17
		SPI_NOR_RST_B	7 HOLD
			VCC 8, VSS 4

R889 10.0K

{5,11,12,14,17,20} PORT3_P38 — 0 R879

Boot Configuration Select

Switch mapping with the configuration options is described on the Notes page of the schematics.

NVCC_EIM0, NVCC_EIM1, NVCC_EIM2
SW5, SW8, SW2, SW1 — SW DIP-8

RN1 10K, RN2 10K, RN4 10K, RN3 10K

BT_CFG0	4.7K R828	EIM_DA0	
BT_CFG1	4.7K R826	EIM_DA1	
BT_CFG2	4.7K R824	EIM_DA2	
BT_CFG3	4.7K R822	EIM_DA3	
BT_CFG4	4.7K R820	EIM_DA4	
BT_CFG5	4.7K R818	EIM_DA5	
BT_CFG6	4.7K R823	EIM_DA6	
BT_CFG7	4.7K R821	EIM_DA7	
BT_CFG8	4.7K R827	EIM_DA8	
BT_CFG9	4.7K R825	EIM_DA9	
BT_CFG10	4.7K R606	EIM_DA10	
BT_CFG11	4.7K R608	EIM_DA11	
BT_CFG12	4.7K R611	EIM_DA12	
BT_CFG13	4.7K R613	EIM_DA13	
BT_CFG14	4.7K R615	EIM_DA14	
BT_CFG15	4.7K R619	EIM_DA15	
BT_CFG16	4.7K R804	EIM_A16	
BT_CFG17	4.7K R841	EIM_A17	
BT_CFG18	4.7K R839	EIM_A18	
BT_CFG19	4.7K R837	EIM_A19	
BT_CFG20	4.7K R835	EIM_A20	
BT_CFG21	4.7K R833	EIM_A21	
BT_CFG22	4.7K R831	EIM_A22	
BT_CFG23	4.7K R829	EIM_A23	
BT_CFG24	4.7K R830	EIM_A24	
BT_CFG25	4.7K R663	EIM_WAIT	
BT_CFG26	4.7K R840	EIM_LBA	
BT_CFG27	4.7K R838	EIM_EB0	
BT_CFG28	4.7K R836	EIM_EB1	
BT_CFG29	4.7K R605	EIM_RW	
BT_CFG30	4.7K R834	EIM_EB2	
BT_CFG31	4.7K R832	EIM_EB3	

Boot I2C EEPROM (For testing only)

NVCC_EIM0
R597 10.0K, R601 10.0K
EIM_D17 — 0 R598 — I2C3_SCL_BOOT
EIM_D18 — 0 R602 — I2C3_SDA_BOOT
U59 — AT24C512B-TH-B
R595 10.0K
C405 0.1UF

I2C Address: 1010000(R/W)

R675 10.0K, R670 10.0K, R667 10.0K
R674 0 DNP, R671 0 DNP, R669 0 DNP

Debug LED

3.3V — R308 150 — D10 LED_YELLOW
EIM_D25 — 4.7K R816 — Q5 MMBT3904LT1G

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ICAP Classification: FCP:___ FIUO: X PUBI:___
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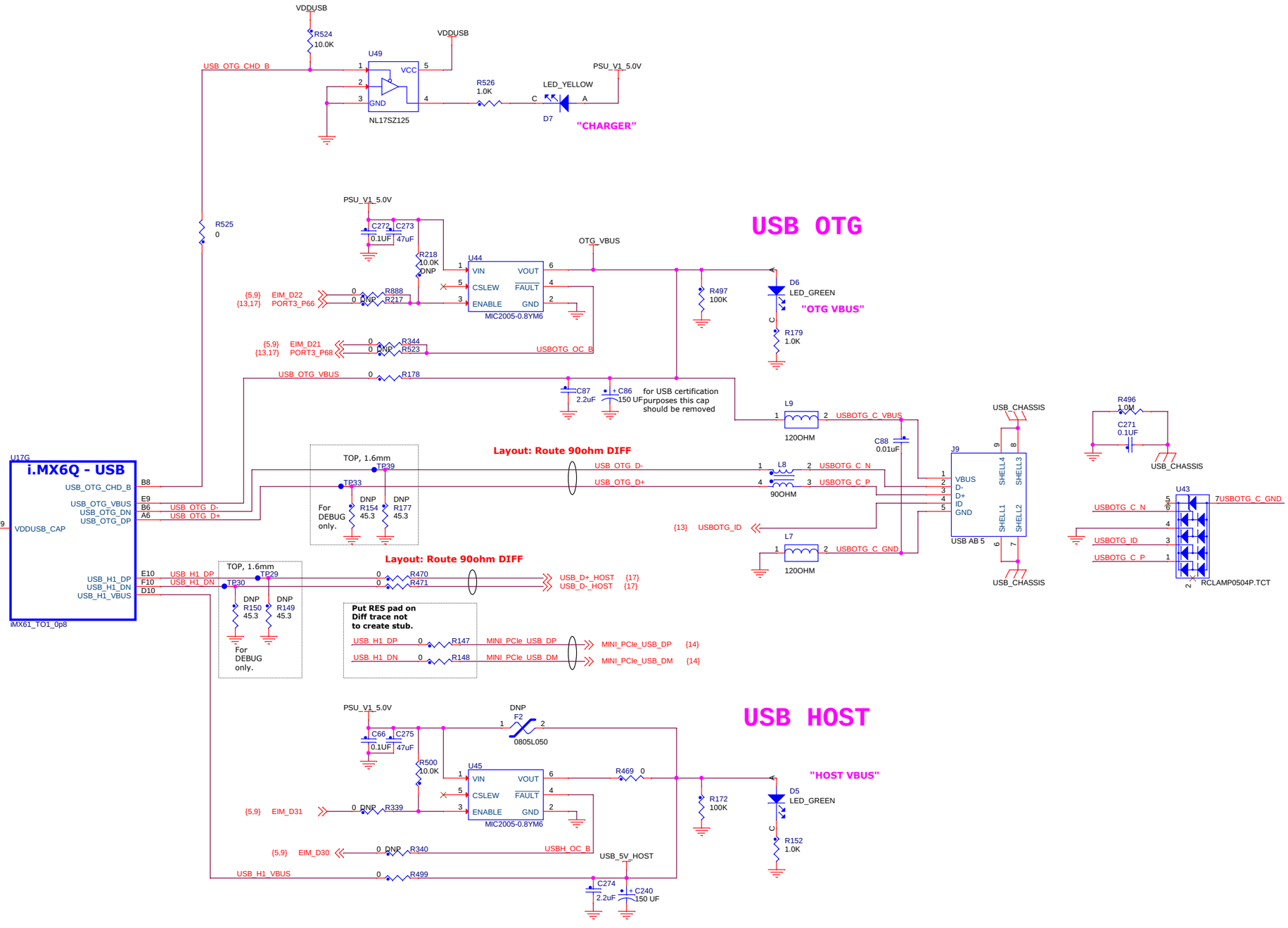
USB OTG



USB HOST

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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **MX6QCPULPDDR2**

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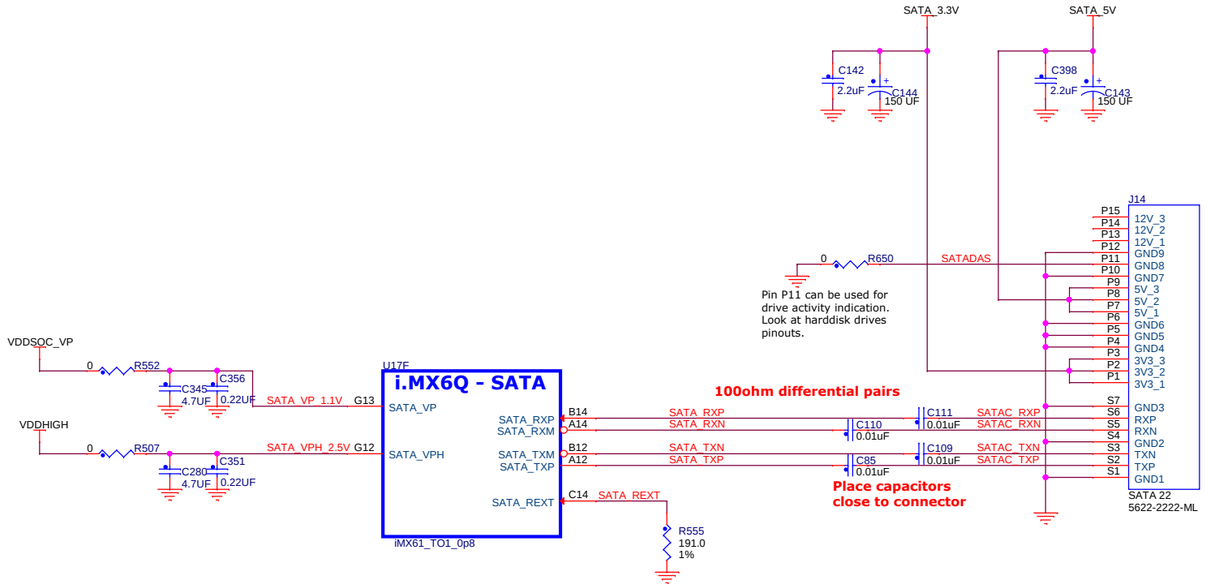

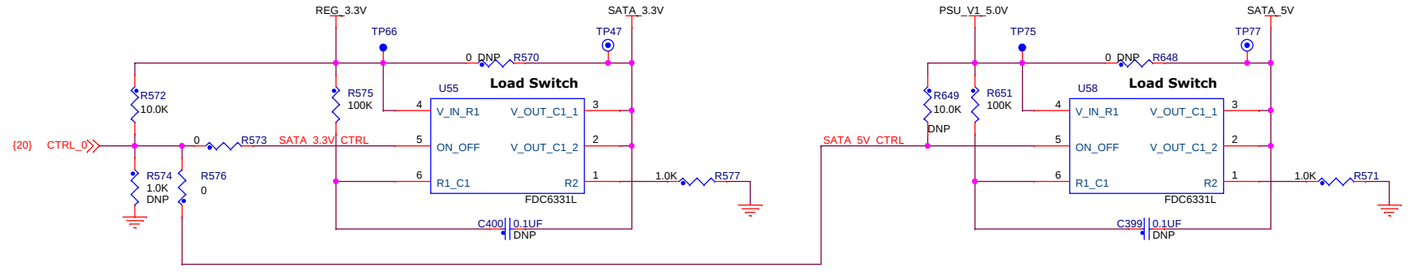

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SATA

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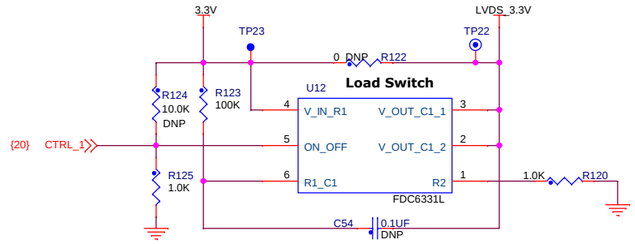
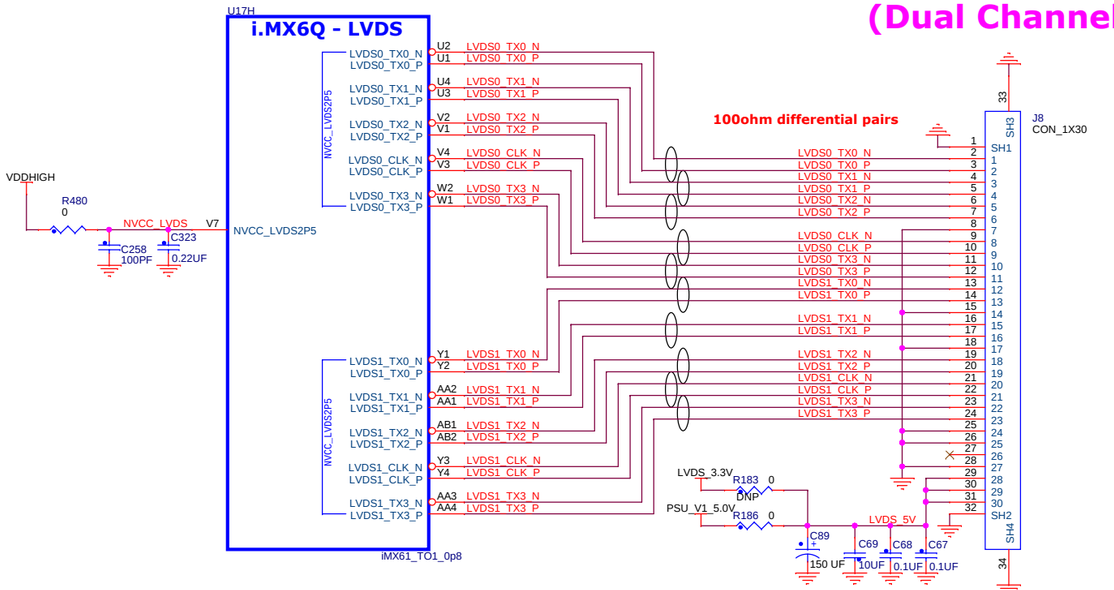
LVDS0 + LVDS1 (Dual Channel)

Load Switch

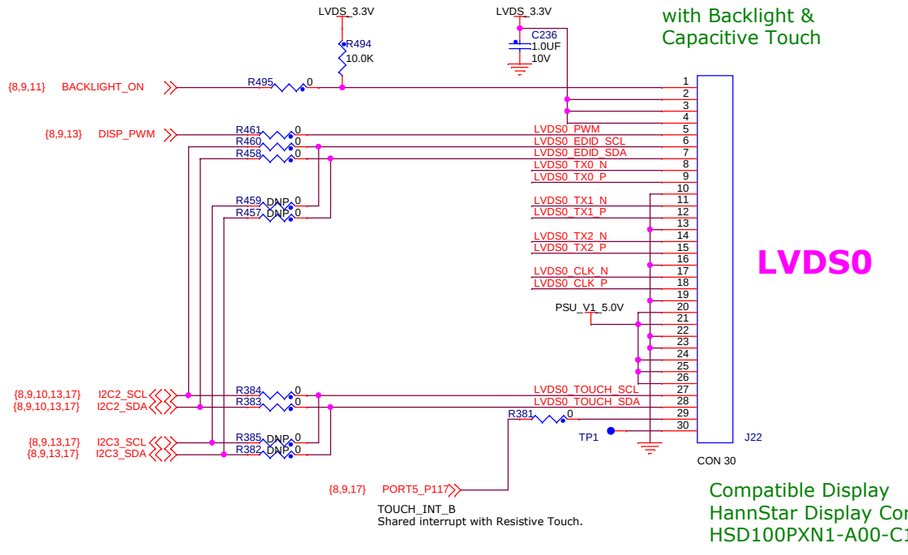


i.MX6Q - LVDS



100ohm differential pairs

LVDS LCD with Backlight & Capacitive Touch

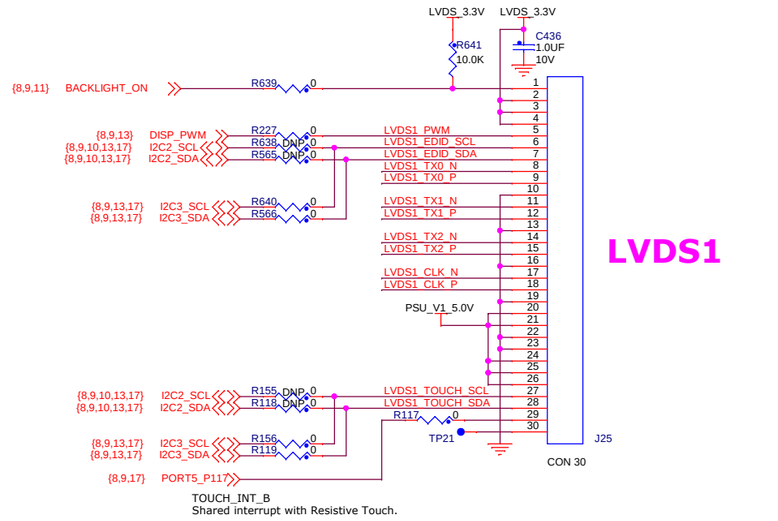


LVDS0

Compatible Display

HannStar Display Corp
HSD100PXN1-A00-C11

FSL Cable #600-76876



LVDS1

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ICAP Classification: FCP:___ FIUO: X PUBI:___

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Page Title: **LVDS**

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i.MX6Q - DISP; CSI

U17D

CSI0_MCLK P4
CSI0_PIXCLK P1
CSI0_VSYNC N2
CSI0_DATA_EN P3
CSI0_DAT4 N1
CSI0_DAT5 P2
CSI0_DAT6 N4
CSI0_DAT7 N3
CSI0_DAT8 N6
CSI0_DAT9 N5
CSI0_DAT10 M1
CSI0_DAT11 M3
CSI0_DAT12 M2
CSI0_DAT13 L1
CSI0_DAT14 M4
CSI0_DAT15 M5
CSI0_DAT16 L4
CSI0_DAT17 L3
CSI0_DAT18 M6
CSI0_DAT19 L6
NVCC_CSI

CSI_CLK0M F4
CSI_CLK0P F3
CSI_D0M E4
CSI_D0P E3
CSI_D1M D1
CSI_D1P D2
CSI_D2M E1
CSI_D2P E2
CSI_D3M F2
CSI_D3P F1
CSI_REXT D4
NVCC_MIPI

DI0_DISP_CLK N19
DI0_PIN2 N25
DI0_PIN3 N20
DI0_PIN4 P25
DI0_PIN15 N21
DISP0_DAT0 P24
DISP0_DAT1 P22
DISP0_DAT2 P23
DISP0_DAT3 P21
DISP0_DAT4 R25
DISP0_DAT5 R23
DISP0_DAT6 R24
DISP0_DAT7 R22
DISP0_DAT8 T25
DISP0_DAT9 R21
DISP0_DAT10 T23
DISP0_DAT11 T24
DISP0_DAT12 R20
DISP0_DAT13 U25
DISP0_DAT14 T22
DISP0_DAT15 T21
DISP0_DAT16 U24
DISP0_DAT17 V25
DISP0_DAT18 U23
DISP0_DAT19 U22
DISP0_DAT20 T20
DISP0_DAT21 V24
DISP0_DAT22 P26
DISP0_DAT23 W24
NVCC_LCD

DSI_CLK0M H3
DSI_CLK0P H4
DSI_D0M G2
DSI_D0P G1
DSI_D1M H2
DSI_D1P H1
DSI_REXT G4
NVCC_MIPI

iMX61_TO1_0p8

R508 6.04K 1%
R475 6.04K 1%

TRACE Connector

CAUTION: When using the ARM TRACE connector, NVCC_CSI should be the same voltage as NVCC_JTAG.

Vsupply should be 2V-5.0V
VTRef should be a power of the IO level

NVCC_JTAG 3.3V NVCC_JTAG
R486 0 DNP
R487 0
R511 100

P1 HDR_2X19_F

(DBGRQ)
(SRST_B)
(TDO)
(RTCK)
(TCK)
(TMS)
(TDI)
(TRST_B)
(TRACED15)
(TRACED14)
(TRACED13)
(TRACED12)
(TRACED11)
(TRACED10)
(TRACED9)
(TRACED8)
(TRACECLK) CSI0_DATA_EN
(DBGACK)
(EXTTRIG)
(VTRef)
(VSupply)
(TRACEDATA7) CSI0_DAT10
(TRACEDATA6) CSI0_DAT9
(TRACEDATA5) CSI0_DAT8
(TRACEDATA4) CSI0_DAT7
(TRACEDATA3) CSI0_DAT6
(TRACEDATA2) CSI0_DAT5
(TRACEDATA1) CSI0_DAT4
(TRACECTL) CSI0_MCLK
(TRACEDATA0) CSI0_VSYNC

{12} TR_JTAG_nSRST
{12} TR_JTAG_TDO
{12} TR_JTAG_TCK
{12} TR_JTAG_TMS
{12} TR_JTAG_TDI
{12} TR_JTAG_nTRST
R512 4.7K
R513 4.7K
R482 4.7K
R510 4.7K

{5} EIM_D16 R777 0 DI0_PIN5 PORT5_P118 {17}
{5} EIM_D17 R779 DI0_PIN6 PORT5_P53 {17}
{5} EIM_D18 R780 DI0_PIN7 PORT5_P37 {17}
{5} EIM_D19 R784 DI0_PIN8 PORT5_P120 {17}
{5} EIM_D20 R788 SER_DISP0_CS PORT5_P81 {17}
{5,6} EIM_D21 R789 DISP0_SER_CLK PORT5_P89 {17}
{5,6} EIM_D22 R801 DI0_PIN1
R805 DISP0_SER_DIN PORT5_P85 {17}
{5} EIM_D23 R794 DI0_D0_CS PORT5_P105 {17}
{5,10} EIM_A25 R809 0 DI0_D1_CS PORT5_P107 {17}
{5,17} EIM_D28 R792 0 DI0_PIN13
R791 DISP0_SER_DIO PORT5_P87 {17}
{5,17} EIM_D29 R793 DI0_PIN14
R796 DISP0_SER_RS PORT5_P91 {17}
{5,6} EIM_D30 R798 DI0_PIN11 PORT5_P109 {17}
{5,6} EIM_D31 R806 DI0_PIN12 PORT5_P117 {8,9,17}

DISP0 Expansion Connector

J19

CPU_AUX1 1.8V
3.3V PSU_V1_5.0V
CPU_AUX0 BKLT_HV_18MA_A {9,17} PORT5_P9
1.8V BKLT_HV_18MA_C {9,17} PORT5_P15
BKLT_5V_60MA_A
BKLT_5V_60MA_C
CPU_AUX2
CPU_AUX3
I2C LCD_I2C_DATA {9,17} PORT5_P29
LCD_I2C_CLOCK {9,17} PORT5_P31
DISP0_RST_B LCD_LCS1_RST
CPU_AUX0 DI0_PIN7 LCD_PS
DI0_DISP_CLK LCD_DOTCLK
3.3V
CPU_AUX1 DI0_PIN6 LCD_CLS
DI0_PIN1 LCD_SD_I
DI0_PIN14
TP80 DISP_BATT
TP83 DISP_5V
DISP0_PWR_EN LCD_PWR_EN
LCD_CS#(SPI_CS) SER_DISP0_CS
SPI LCD_DOUT(SPI_MISO) DISP0_SER_DIN
LCD_DIN(SPI_MOSI) DISP0_SER_DIO
LCD_SCLK DISP0_SER_CLK
LCD_SER_RS_DEN DISP0_SER_RS
TOUCHSCREEN_Y+ {9,17} PORT5_P95
TOUCHSCREEN_Y- {9,17} PORT5_P97
TOUCHSCREEN_X+ {9,17} PORT5_P99
TOUCHSCREEN_X- {9,17} PORT5_P101
LCD_LCS0 DI0_D0_CS
LCD_CS# DI0_D1_CS
LCD_WR DI0_PIN11
PSU_V5_1.5V
LCD_RD DI0_PIN12
LCD_PAR_RS DI0_PIN13

SH1 SH2 SH3 SH4 SH5 SH6 SH7 SH8
QSH-060-01-L-D-A
GND GND

LCD_D0 LCD_D1 LCD_D2 LCD_D3 LCD_D4 LCD_D5 LCD_D6 LCD_D7 LCD_D8 LCD_D9 LCD_D10 LCD_D11 LCD_D12 LCD_D13 LCD_D14 LCD_D15 LCD_D16 LCD_D17 LCD_D18 LCD_D19 LCD_D20 LCD_D21 LCD_D22 LCD_D23
LCD_VSYNC LCD_CONTRAST LCD_HSYNC LCD_EN(DRDY) LCD_SPL LCD_REV

NVCC_EIM0 U77 NL17SZ07DFT2G
{5,17} EIM_D24 DISP0_PWR_EN PORT5_P79 {17}

NVCC_EIM2 U75 NL17SZ07DFT2G
{5,17} PORT1_P86 R876 10.0K DISP0_RST_B PORT5_P33 {17}

LCD Backlight Driver - DI0

PSU_V1_5.0V
R874 0
C491 4.7uF C490 0.1UF
DNP R872 10.0K
R873 10.0K
L29 47UH
U73 IN SW SHDN GND FB CAT4238
D32 MBR140SFT
DI0_LED_P0 R868 PORT5_P9 {9,17}
C489 0.22UF
Up to 38V / 40mA
{8,13} DISP_PWM R875 0
DI0_LED_N0 R869 PORT5_P15 {9,17}
R870 15
20mA

LCD Backlight Driver - DI1

PSU_V1_5.0V
R337 0
C177 4.7uF C176 0.1UF
DNP R332 10.0K
R334 10.0K
R333 0
L18 47UH
U33 IN SW SHDN GND FB CAT4238
D11 MBR140SFT
DI1_LED_P0 R314 PORT4_P9 {17}
C169 0.22UF
Up to 38V / 40mA
DI1_LED_N0 R313 PORT4_P15 {17}
R311 15
ILED = 0.3V/R
20mA

NVCC_LCD
U34 DNP NL17SZ126DF
C178 DNP 0.1UF
PORT4_P112 {5,17} (Contrast)

NVCC_LCD
U74 DNP NL17SZ126DF
C492 DNP 0.1UF
PORT5_P112 (Contrast)

MIPI Connector

PSU_V1_5.0V
1.8V 2.8V
R61 0
R60 DNP 0
L3 120OHM
VDD_ANA
J2 QSH-030-01-L-D-A-K-TR
TP91 TP90 TP89 TP87 TP86
I2C3_SCL R378 DNP 0 DISP_PWM
I2C3_SDA R376 DNP 0 MIPI_I2C_SCL
I2C2_SCL R379 0 MIPI_I2C_SDA
I2C2_SDA R375 0
CAM_LPM R412 0
CAM_RST_B R373 0 BACKLIGHT_ON
R411 0 CPU_PER_RST_B
R409 0 DISP0_RST_B
CSI0_MCLK DISP0_PWR_EN
DSI_D1M DSI_D1P
DSI_CLK0M DSI_CLK0P
DSI_D0M DSI_D0P
CSI_D3P CSI_D3M CSI_D1P CSI_D1M CSI_CLK0P CSI_CLK0M CSI_D0P CSI_D0M CSI_D2P CSI_D2M

Touch Panel decoder, Analog to Digital converter.

NVCC_LCD
L19 120OHM 1.7V to 3.6V
C182 0.1UF C184 0.1UF C183 4.7uF
A2D_TP_VDD
NVCC_EIM0
R866 100K
R863 0
DNP R865 0
DNP R864 0
U35
{8,9,17} PORT5_P117 PENIRQ_B
{9,17} PORT5_P29 SDA
{9,17} PORT5_P31 SCL
A0
A1
TIRQ VDD EP GND AUX
X+ R362 PORT5_P99 {9,17} TOUCHSCREEN_X+
X- R361 PORT5_P101 {9,17} TOUCHSCREEN_X-
Y+ R363 PORT5_P95 {9,17} TOUCHSCREEN_Y+
Y- R360 PORT5_P97 {9,17} TOUCHSCREEN_Y-
TP85
R862 100K R867 100K
MAX11801
I2C Address: 10010xx(R/W)

PSU_V1_5.0V 1.8V 3.3V VDD_ANA
C194 4.7uF C193 0.1UF
C198 4.7uF C195 0.1UF
C196 4.7uF C197 0.1UF
C20 4.7uF C8 0.1UF

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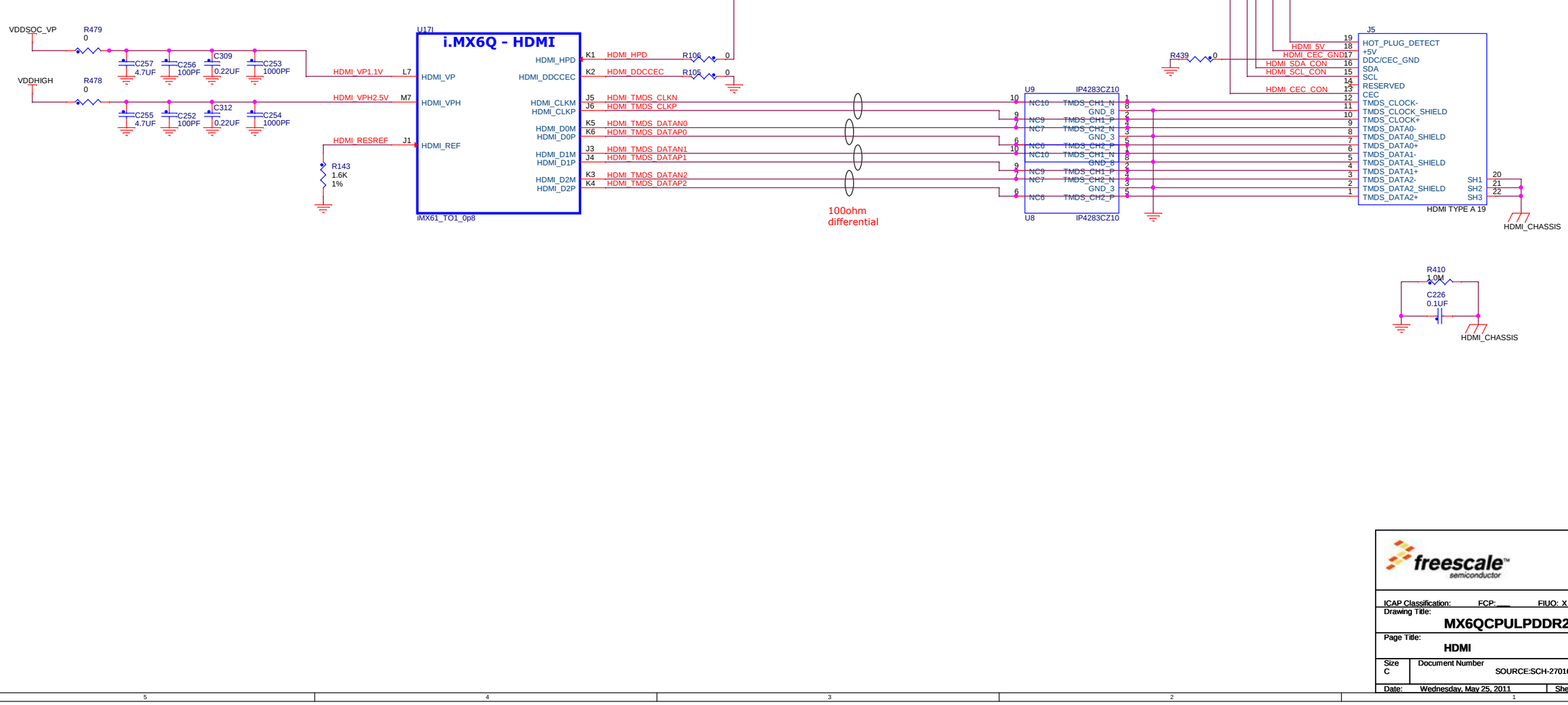
ICAP Classification: FCP: ___ FIUO: X PUBI: ___
Drawing Title: **MX6QCPULPDDR2**
Page Title: **DISPLAY Interface**
Size C | Document Number: SOURCE:SCH-27016 PDF:SPF-27016 | Rev X
Date: Wednesday, May 25, 2011 | Sheet 9 of 23



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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **MX6QCPULPDDR2**

Page Title: **HDMI**

Size	Document Number	Rev
C	SOURCE:SCH-27016 PDF:SPF-27016	X

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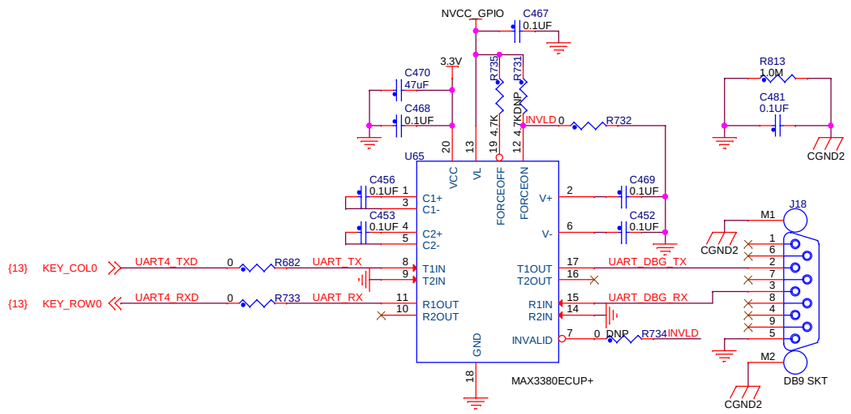

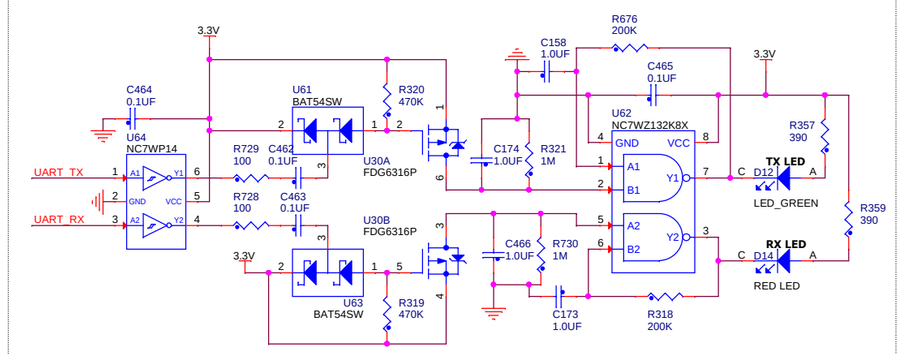

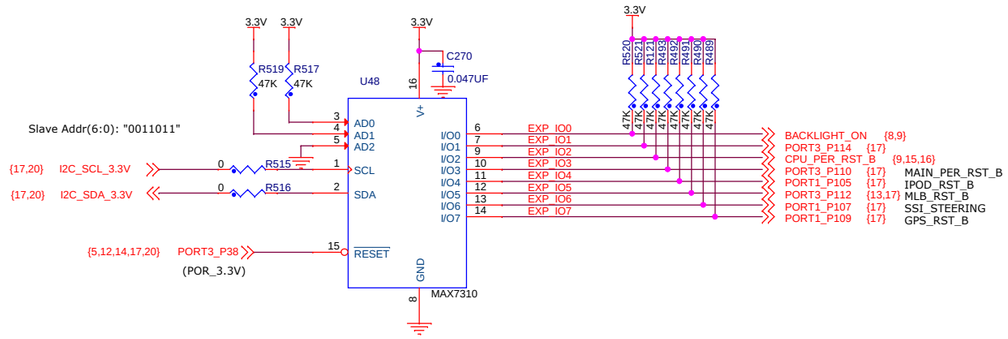

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Drawing Title:
MX6QCPULPDDR2

Page Title:
Debug UART

Size	Document Number	Rev
C	SOURCE:SCH-27016 PDF:SPF-27016	X

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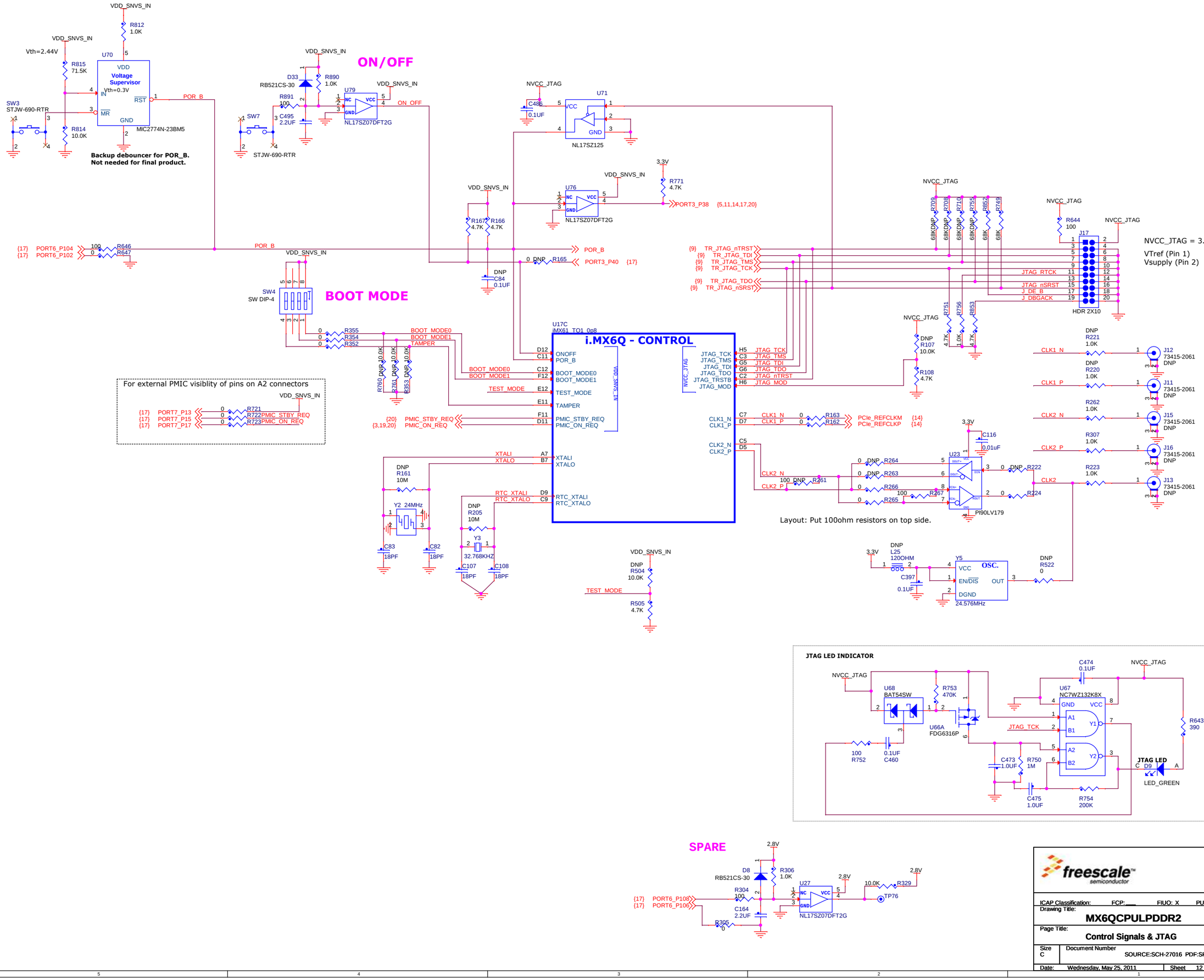

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: MX6QCPULPDDR2

Page Title: Control Signals & JTAG

Size	Document Number	Rev
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U17B
iMX61_TO1_0p8

i.MX6Q

SD1_CMD B21
SD1_CLK D20
SD1_DAT0 A21
SD1_DAT1 C20
SD1_DAT2 E19
SD1_DAT3 F18
NVCC_SD1

SD2_CMD F19
SD2_CLK C21
SD2_DAT0 A22
SD2_DAT1 E20
SD2_DAT2 A23
SD2_DAT3 B22
NVCC_SD2

SD3_CMD B13
SD3_CLK D14
SD3_DAT0 E14
SD3_DAT1 F14
SD3_DAT2 A15
SD3_DAT3 B15
SD3_DAT4 D13
SD3_DAT5 C13
SD3_DAT6 E13
SD3_DAT7 F13
SD3_RST D15
NVCC_SD3

MLB_CP B11
MLB_CN A11
MLB_SP B9
MLB_SN A9
MLB_DP A10
MLB_DN B10

ENET_MDC V20
ENET_MDIO V23
ENET_CRS_DV U21
ENET_REF_CLK V22
ENET_RX_ER W23
ENET_TX_EN V21
NVCC_ENET

ENET_RXD0 W21
ENET_RXD1 W22

ENET_TXD0 U20
ENET_TXD1 W20

KEY_COL0 W5
KEY_ROW0 V6
KEY_COL1 U7
KEY_ROW1 U6
KEY_COL2 W6
KEY_ROW2 W4
KEY_COL3 T7
KEY_ROW3 T6
KEY_COL4 V5
KEY_ROW4
NVCC_GPIO

GPIO_0 T5
GPIO_1 T4
GPIO_2 T1
GPIO_3 R7
GPIO_4 R6
GPIO_5 R4
GPIO_6 T3
GPIO_7 R3
GPIO_8 R5
GPIO_9 T2
GPIO_16 R2
GPIO_17 R1
GPIO_18 P6
GPIO_19 P5

NANDF_CS0 F15
NANDF_CS1 C16
NANDF_CS2 A17
NANDF_CS3 D16
NANDF_ALE A16
NANDF_CLE C15
NANDF_WP_B E15
NANDF_RB0 B16
NANDF_D0 A18
NANDF_D1 C17
NANDF_D2 F16
NANDF_D3 D17
NANDF_D4 A19
NANDF_D5 B18
NANDF_D6 E17
NANDF_D7 C18
NVCC_NANDF

SD4_CLK E16
SD4_CMD B17
SD4_DAT0 B19
SD4_DAT1 F17
SD4_DAT2 A20
SD4_DAT3 E18
SD4_DAT4 C19
SD4_DAT5 B20
SD4_DAT6 D19
SD4_DAT7

MLB_CP MLB_CN MLB_SP MLB_SN MLB_DP MLB_DN
100 R171 R169 R170
100ohm differential pairs

PORT6_P96 PORT6_P92 PORT6_P88 PORT6_P84 PORT6_P80 PORT6_P76 PORT6_P90 PORT6_P78 PORT6_P66 PORT6_P72 PORT6_P68 PORT6_P64 PORT6_P86 PORT6_P74 PORT6_P62
R88 R86 R89 R81 R84 R80 R90 R50 R51
D21 D22 D20 D28 D27 D26 D23 D24 D25
RB521CS-30
0 DNP R87 PORT2_P108 ROW5
RPP (Keypad Port)
columns should be configured as open-drain outputs
rows should be configured as inputs.
0 DNP R48 PORT2_P112 COL5
0 DNP R83 PORT2_P102 ROW6
0 DNP R82 PORT2_P104 COL6
0 DNP R49 PORT2_P118 ROW7
0 DNP R85 PORT2_P120 COL7

R445 R448 R451 R452 R442 R443 R444 R446 R449 R450 R413
R556 R554 R553
R699 R694 R111 R394 R417 R428 R387 R71 R109 R430
R691 R689 R692 R693 R456 R312 R687 R688 R498 R219
R175 R464 R463 R176 R173 R454 R174 R742 R79 R877 R878
R100 R139 R453
R342 R343 R345 R346 R348 R347 R350 R324 R249 R247 R246 R245 R242 R241 R240 R238
R557
R59 R52 R53 R54 R56 R57 R58
R94 R92 R23
R551 R550 R548 R547 R585 R549 R349 R341 R244
R415 R462 R414
R542 R421

PORT3_P80 PORT3_P99 PORT3_P86 PORT3_P82 PORT3_P84 PORT3_P76 PORT3_P90 PORT3_P88 PORT3_P78 PORT3_P74
PORT3_P120 PORT3_P118 PORT3_P119 PORT3_P117 PORT2_P87 PORT3_P64 PORT3_P44 PORT3_P46 PORT3_P68 {6,17} {6,17} PORT3_P66
PORT2_P76 {17}
MLBDAT MLBCLK MLBSIG
PORT2_P91 PORT2_P98 PORT2_P100 PORT2_P105
PORT3_P105 PORT3_P106 PORT3_P70 PORT3_P72 PORT3_P98 PORT3_P102 PORT3_P104 PORT2_P106 PORT2_P110 PORT2_P114 PORT2_P116 PORT3_P95 PORT3_P97 PORT1_P85
PORT1_P87 PORT1_P89 PORT1_P91 PORT1_P94 PORT1_P96 PORT1_P98 PORT1_P100
PORT2_P119 USBOTG_ID SDIO1_CARD_DETECT PORT3_P96 PORT3_P92 PORT2_P117 PORT2_P85 PORT3_P94 PORT3_P62 PORT2_P89 SDIO1_WRITE_PROTECT DISP_PWM
SD3_VSELECT CPU_INT_B
SD2_DAT4 SD2_DAT5 SD2_DAT6 SD2_DAT7

ENET_CRS_DV ENET_REF_CLK ENET_REF_CLK_50M ENET_RX_ER ENET_TX_EN
ENET_RXD0 ENET_RXD1
ENET_TXD0 ENET_TXD1
KEY_COL0 KEY_ROW0
KEY_COL1 KEY_COL2
SD1_VSELECT ENET_MDIO ENET_MDC
SD_CLK_NANDF_WE SD_CMD_NANDF_RE SD_DAT0_NANDF_DQS
NANDF_WE_B SD4_CLK NANDF_RE_B SD4_CMD NANDF_DQS SD4_DAT0
SD4_DAT1 SD4_DAT2 SD4_DAT3 SD4_DAT4 SD4_DAT5 SD4_DAT6 SD4_DAT7
SD_CD SD_WP
SD4_VSELECT

NVCC_SD3
J20
SD3_DAT0 SD3_DAT1 SD3_DAT2 SD3_DAT3 SD3_DAT4 SD3_DAT5 SD3_DAT6 SD3_DAT7 SD3_CLK SD3_CMD
DAT0 DAT1 DAT2 DAT3 DAT4 DAT5 DAT6 DAT7 CLK CMD CD WP VDD VSS1 VSS2 GND1 GND2 GND3 GND4
R99 10.0K
SD3_CD 4.7K R93
SD3_WP 4.7K R91
SD3_RST TP11
CONN CRD 19
1.8V 3.3V
0 DNP R98
0 R97
C38 10UF

NVCC_NANDF
R55 10.0K
J1
SD4_DAT0 SD4_DAT1 SD4_DAT2 SD4_DAT3 SD4_DAT4 SD4_DAT5 SD4_DAT6 SD4_DAT7 SD4_CLK SD4_CMD
DAT0 DAT1 DAT2 DAT3 DAT4 DAT5 DAT6 DAT7 CLK CMD CD WP VDD VSS1 VSS2 GND1 GND2 GND3 GND4
SD4_RST TP2
CONN CRD 19
1.8V 3.3V
0 DNP R95
0 R96
C19 10UF

NVCC_GPIO
R372 R371 4.7K
I2C2_SCL I2C2_SDA
R377 R374 4.7K
I2C3_SCL I2C3_SDA

3.3V
R528 0
VDD_SDIO1
UART_LOGIC_PWR
R168 0
R532 0 UART2_EN {17}

NVCC_SD2
R529 0
VDD_SDIO2

R101 1.0K
GPIO_0
J7 73415-2061 DNP CLKO
R136 1.0K
GPIO_3
J4 73415-2061 DNP CLKO2

J10
QSH-020-01-L-D-DP-A
3.3V (<370mA) R527 0
I2C2_SDA I2C2_SCL
MLB_12V TP50
R216 0 3.3V (<50mA)
KEY_ROW1 MLB_INT_B
MLB_RST_B {11,17} PORT3_P112
MLB_PWDN_B (Input to CPU) PORT4_P53 {5,17}
MLB_CP MLB_CN MLB_DP MLB_DN MLB_SP MLB_SN
R135 0 MLBDAT
R138 0 MLBSIG
MLBCLK
100 R141 DNP
DNP C64 27 PF

NAND Flash Socket (TSOP48)
3.3V
C175 10.0uF C136 0.1UF C179 0.1UF
U31
980020-48-P2
VCC_12 VCC_37
NANDF_D0 NANDF_D1 NANDF_D2 NANDF_D3 NANDF_D4 NANDF_D5 NANDF_D6 NANDF_D7
I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7
NANDF_CLE NANDF_ALE NANDF_CS0 NANDF_RE_B NANDF_WE_B NANDF_WP_B NANDF_RB0
CLE ALE CE1n REn WEn WPn R/B1n
NC1 NC2 NC3 R/B4n R/B3n R/B2n CE2n NC11 CE3n CE4n NC20 NC21 NC22 NC23 NC24 NC25/GND NC26 NC27 NC28 NC33 NC34/VCC NC35/DQS NC38 VSS_13 VSS_36
NC48/GND NC47 NC46 NC45 NC40 NC39/VCC
NANDF_RB0 NANDF_RB3 NANDF_RB2 NANDF_RB1 NANDF_CS1 NANDF_CS2 NANDF_CS3 NANDF_DQS
R325 R322 R326
R323 10.0K NVCC_NANDF
R290 0 NVCC_NANDF
R294 0
R293 0 NVCC_NANDF
R292 0
DNP R291 10.0K

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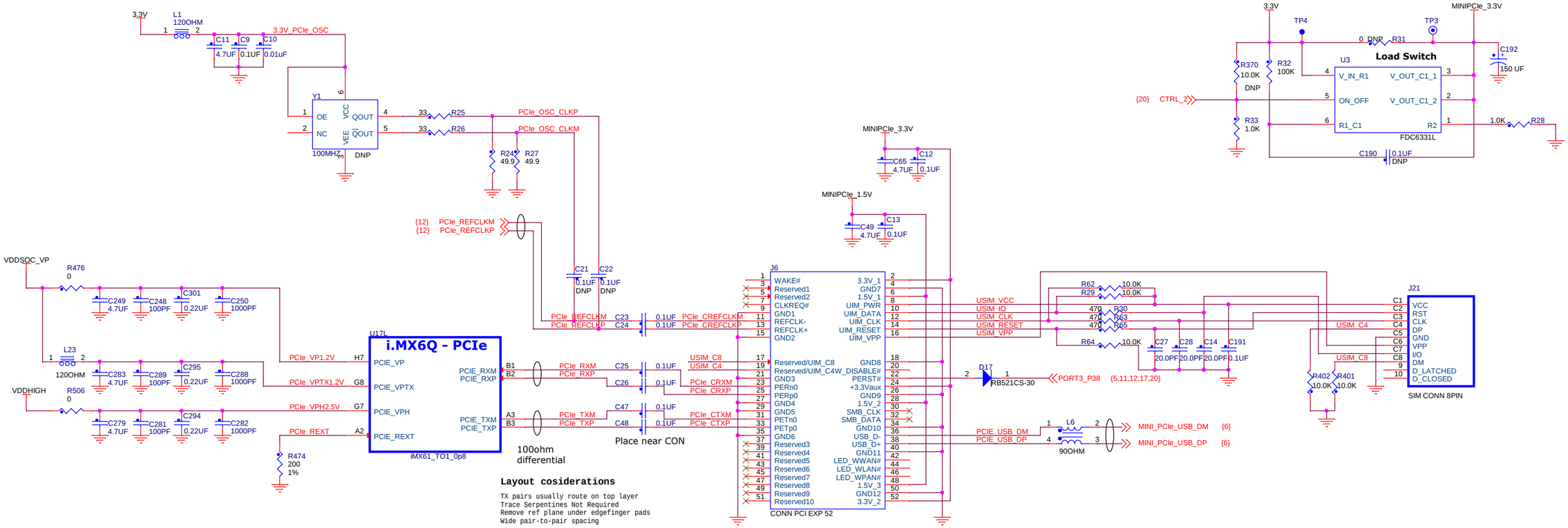
ICAP Classification: FCP:___ FIUO: X PUBI:___
Drawing Title:
MX6QCPULPDDR2
Page Title:
MLB, NAND & SD Interface
Size C | Document Number SOURCE:SCH-27016 PDF:SPF-27016 | Rev X
Date: Wednesday, May 25, 2011 | Sheet 13 of 23



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Drawing Title: **MX6QCPULPDDR2**

Page Title: **PCIe**

Size	Document Number	Rev
C	SOURCE:SCH-27016 PDF:SPF-27016	X

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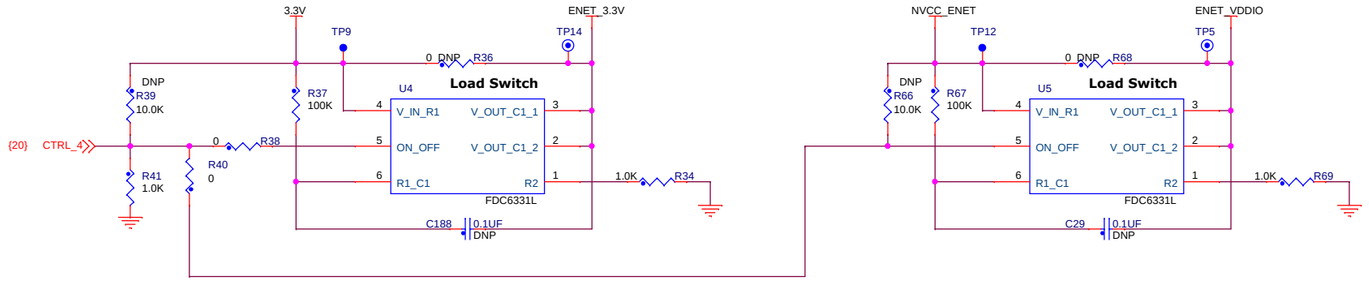

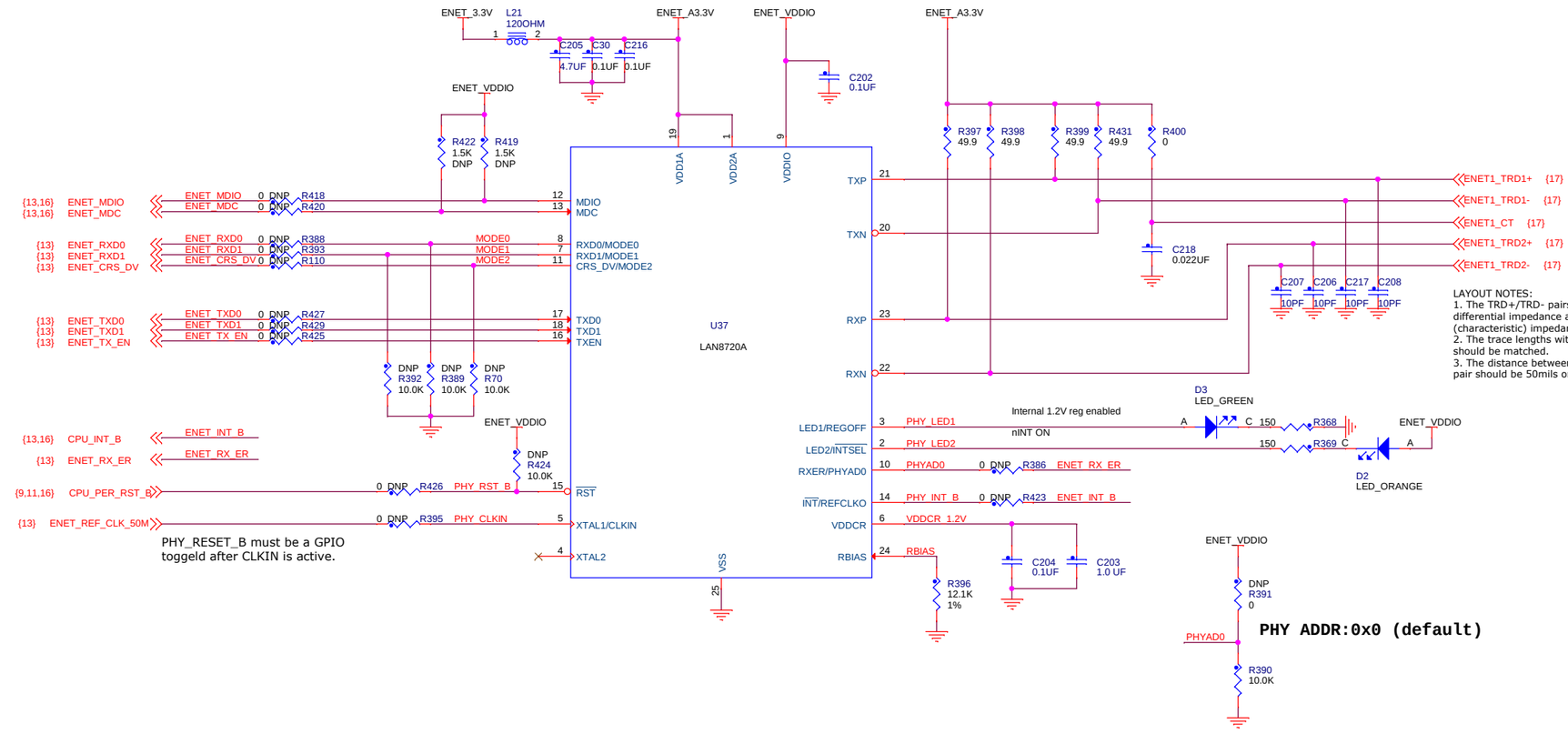

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Drawing Title: **MX6QCPULPDDR2**

Page Title: **RMII Ethernet Phy**

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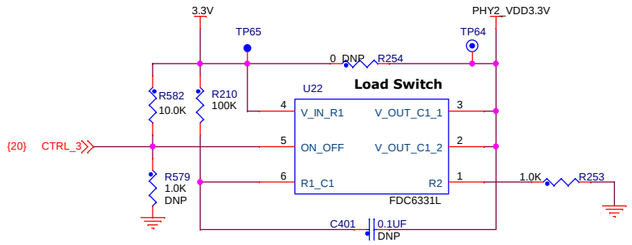
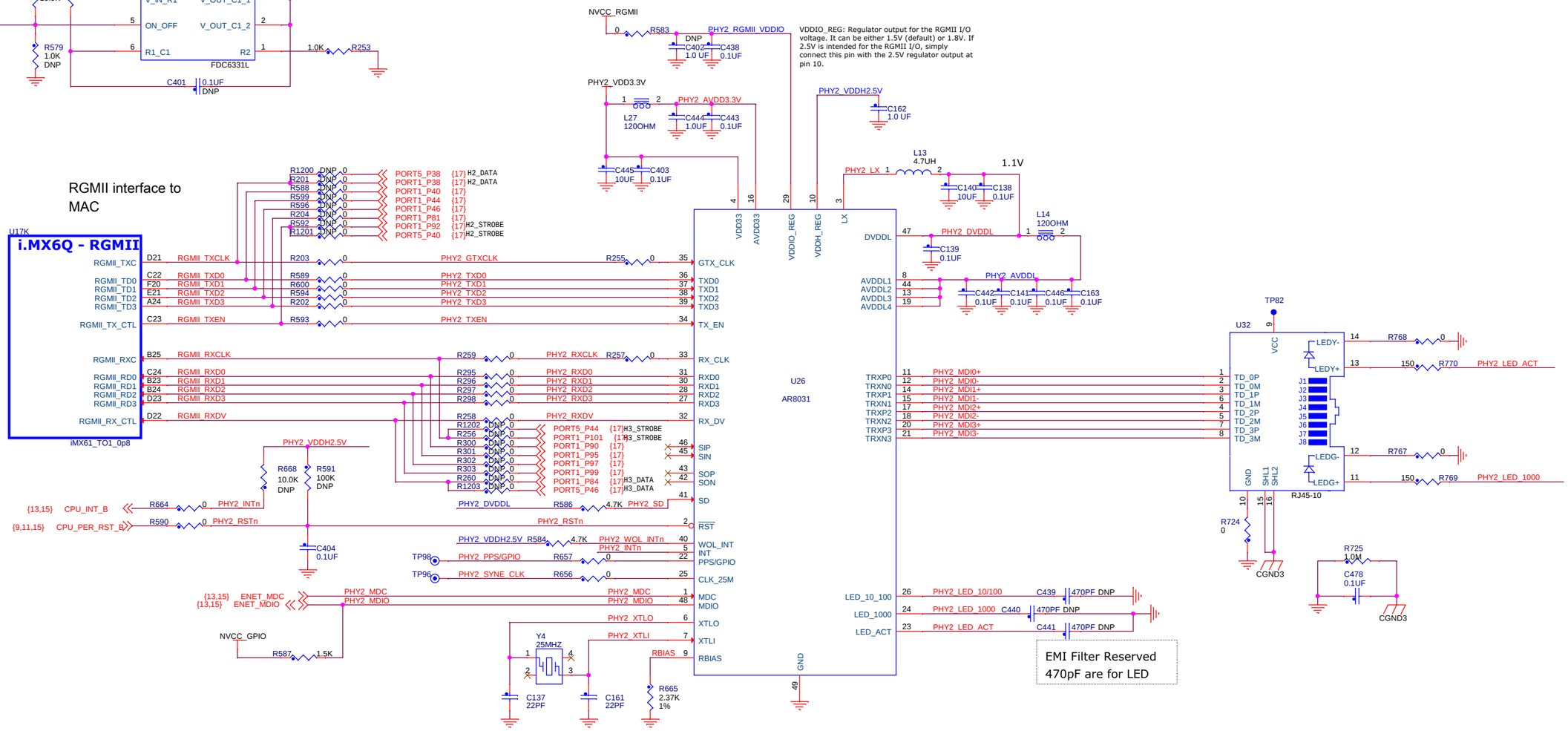
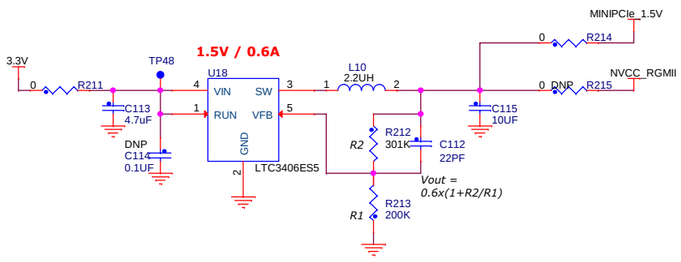
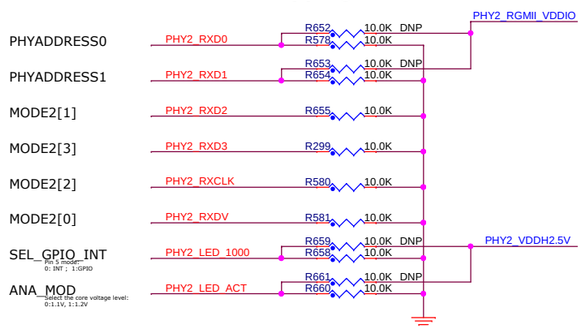






Power-on Strapping Pins



MODE2[3:0]

(Default assemble: 0000)
1100 BaseT, RMII1;
1101 BaseT, RMII2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMII;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RGMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, RGMII, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved

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Drawing Title: **MX6QCPULPDDR2**

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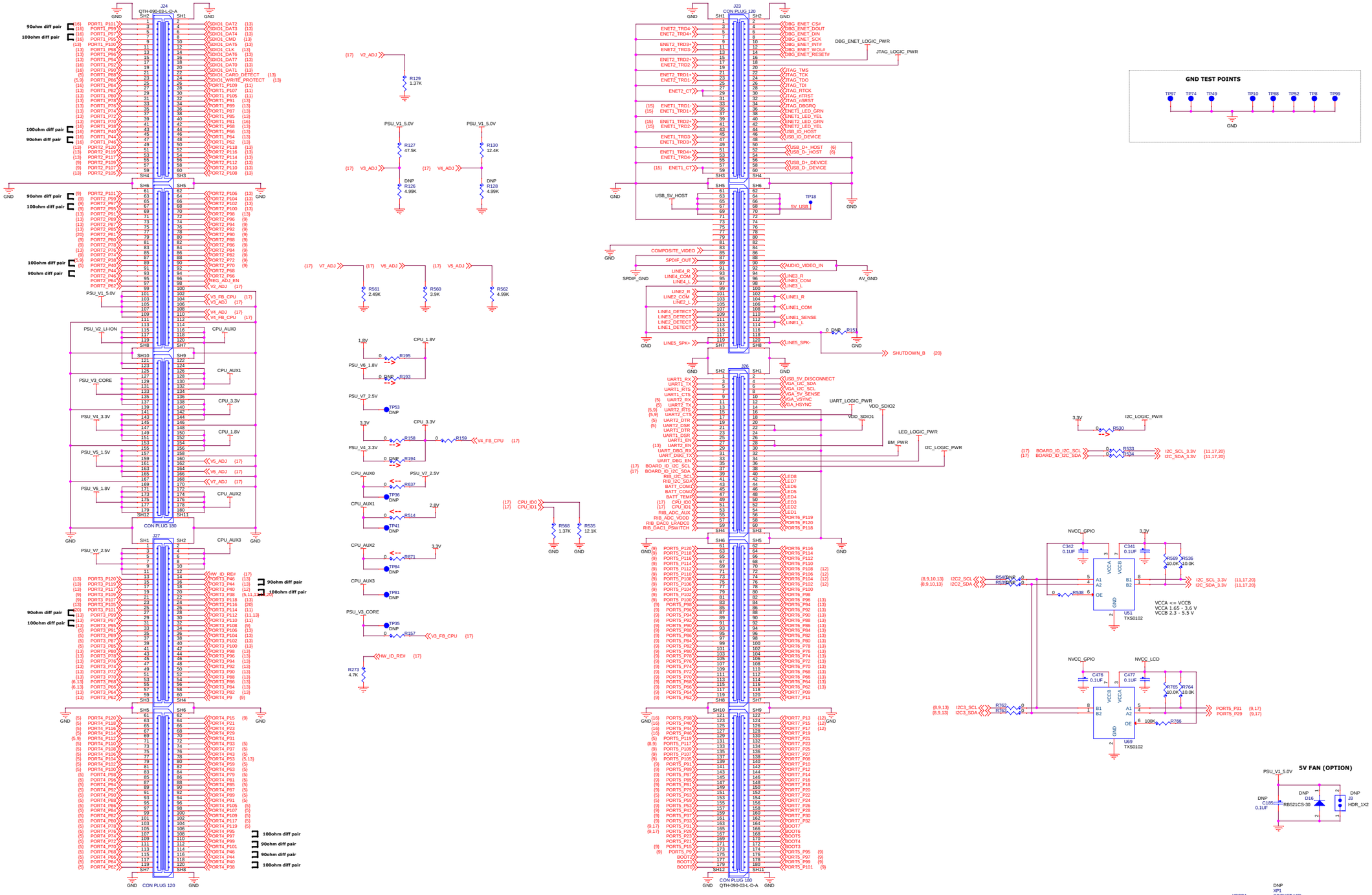

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Designer: <Designer>	Drawing Title: MX6QCPUIPDDR2	
Drawn by: <DrawnBy>	Page Title: CPU CARD & MOUNTING HOLES	
Approved: <Approver>	Size: D	Document Number: SOURCE:SCH-27016 PDF:SPF-27016
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U17E
iMX61_TO1_0p8

i.MX6Q - POWER

VDDARM_IN
VDDARM23_IN
VDDSOC_IN
VDDHIGH_REG
VDD_SNVS_IN
VDDHIGH_IN
VDD_CACHE_CAP
VDDSOC_CAP
VDDPU_CAP
VDDARM_CAP
VDDARM_CAP23

C362 0.22UF, C348 10UF, C350 22UF
JP8
C316 0.22UF, C260 22UF
JP2
0.02 R207
C366 0.22UF, C349 10UF, C346 22UF
SH5 SOLDER SHORT
C305 0.22UF, C225 10UF
D4 NSR0320
R153 3.12K
B1 LICELL
C291 0.1UF

VDDARM_IN_1 … VDDARM_IN_8 (H14, J14, K14, L14, M14, N14, P14, R14)
VDDARM23_IN_1 … VDDARM23_IN_8 (K9, L9, M9, N9, P9, R9, T9, U9)
VDDSOC_IN_1 … VDDSOC_IN_10 (H16, J16, K16, L16, M16, N16, P16, R16, T16, U16)
VDDHIGH_IN_1, VDDHIGH_IN_2 (H9, J9)
VDD_SNVS_IN (G11)

GND_1 … GND_79 (A13, A25, A4, A8, AA10, AA13, AA16, AA19, AA22, AA7, AB24, AB3, AD10, AD13, AD16, AD19, AD22, AD4, AD7, AE1, AE25, B4, C1, C10, C4, C6, D3, D6, D8, E5, E6, E7, F5, F6, F7, F8, G10, G19, G3, H12, H15, H18, H8, J12, J15, J18, J2, J8, K10, K12, K15, K18, K8, L10, L12, L15, L18, L2, L5, L8, M10, M12, M15, M18, M8, N10, N15, N18, N8, P10, P12, P15, P18, P8, R12, R15, R17, R8, T11)

VDDARM_CAP_1 … VDDARM_CAP_8 (H13, J13, K13, L13, M13, N13, P13, R13)
VDD_ARM_CAP
C315 0.01UF, C246 0.01UF
JP7
C371 0.22UF, C303 0.22UF, C320 0.22UF, C306 0.01UF, C358 0.01UF, C298 0.01UF, C245 22UF, C347 22UF
DNP 0.01 R473 <-- VDDARM_IN

VDDARM_CAP23_1 … VDDARM_CAP23_8 (H11, J11, K11, L11, M11, N11, P11, R11)
VDD_ARM_CAP23
C307 0.22UF, C299 0.22UF, C318 0.22UF, C310 0.01UF, C304 0.01UF, C314 0.01UF, C247 22UF, C222 22UF

VDDSOC_CAP_1 … VDDSOC_CAP_7 (R10, T10, T13, T14, U10, U13, U14)
C321 0.22UF, C373 0.22UF, C370 0.22UF, C324 0.22UF, C319 0.01UF, C374 0.01UF, C322 0.01UF, C408 22UF
VDDSOC R604 0.02 DNP VDDSOC_IN

VDDPU_CAP_1 … VDDPU_CAP_7 (H17, J17, K17, L17, M17, N17, P17)
C357 0.22UF, C368 0.22UF, C360 0.22UF, C363 0.22UF, C364 0.01UF, C361 0.01UF, C359 0.01UF, C407 22UF, C406 22UF
VDDPU R250 0.02 DNP
VDD_CACHE
SH7 SOLDER SHORT VDDSOC
C311 0.22UF, C251 10UF

VDDSOC SH6 SOLDER SHORT VDDSOC_VP

VDDHIGH_CAP_1, VDDHIGH_CAP_2 (H10, J10)
2.5V
C300 0.01UF, C287 0.01UF, C286 0.22UF, C284 10UF
VDDHIGH R477 0 DNP VDDHIGH_IN

VDD_SNVS_CAP (G9)
VDD_SNVS
C296 0.22UF, C243 10UF

NVCC_LCD (P19 NVCC_LCD)
NVCC_CSI (N7 NVCC_CSI)
NVCC_MIPI (K7)
NVCC_MIPI
C308 0.22UF
R144 0 <-- VDDHIGH
TP27, TP28

NVCC_EIM0 (K19 NVCC_EIM0)
NVCC_EIM1 (L19 NVCC_EIM1)
NVCC_EIM2 (M19 NVCC_EIM2)
NVCC_ENET (R19 NVCC_ENET)
NVCC_GPIO (P7 NVCC_GPIO)

NVCC_LCD
C369 0.22UF
R243 0 3.3V
TP58, TP56

NVCC_PLL_OUT (E8)
NVCC_PLL
C292 0.22UF, C293 0.01UF, C290 10UF
NVCC_RGMII (G18)
C354 0.22UF

R137 0 DNP 2.8V
NVCC_CSI
C313 0.22UF
R142 0 3.3V
TP26, TP17

NVCC_SD1 (G16 NVCC_SD1)
NVCC_SD2 (G17 NVCC_SD2)
NVCC_SD3 (G14 NVCC_SD3)
NVCC_NANDF (G15 NVCC_NANDF)
NVCC_JTAG (J7 NVCC_JTAG)

NVCC_EIM0
C355 0.22UF
R252 0 3.3V
TP63, TP43

NVCC_EIM1
C367 0.22UF
R248 0 3.3V
TP59, TP60

NVCC_EIM2
C365 0.22UF
R251 0 3.3V
TP62, TP61

NVCC_ENET
C372 0.22UF
R239 0 3.3V
TP55, TP57

GPANAIO (C8 TP94)
FA_ANA (A5 TP92)
VDD_FA (B5 TP93)

GND_80 … GND_107 (T12, T15, T17, T19, T8, U11, U12, U15, U17, U8, U19, V8, V19, W3, W7, W8, W9, W10, W11, W12, W13, W15, W16, W17, W18, W19, Y5, Y24)

DNP R133 0 VDDHIGH
NVCC_GPIO
C317 0.22UF
R134 0 3.3V
TP24, TP25

2.5V (For MLB)

NVCC_SD2
C353 0.22UF
R206 0 3.3V
TP44, TP42

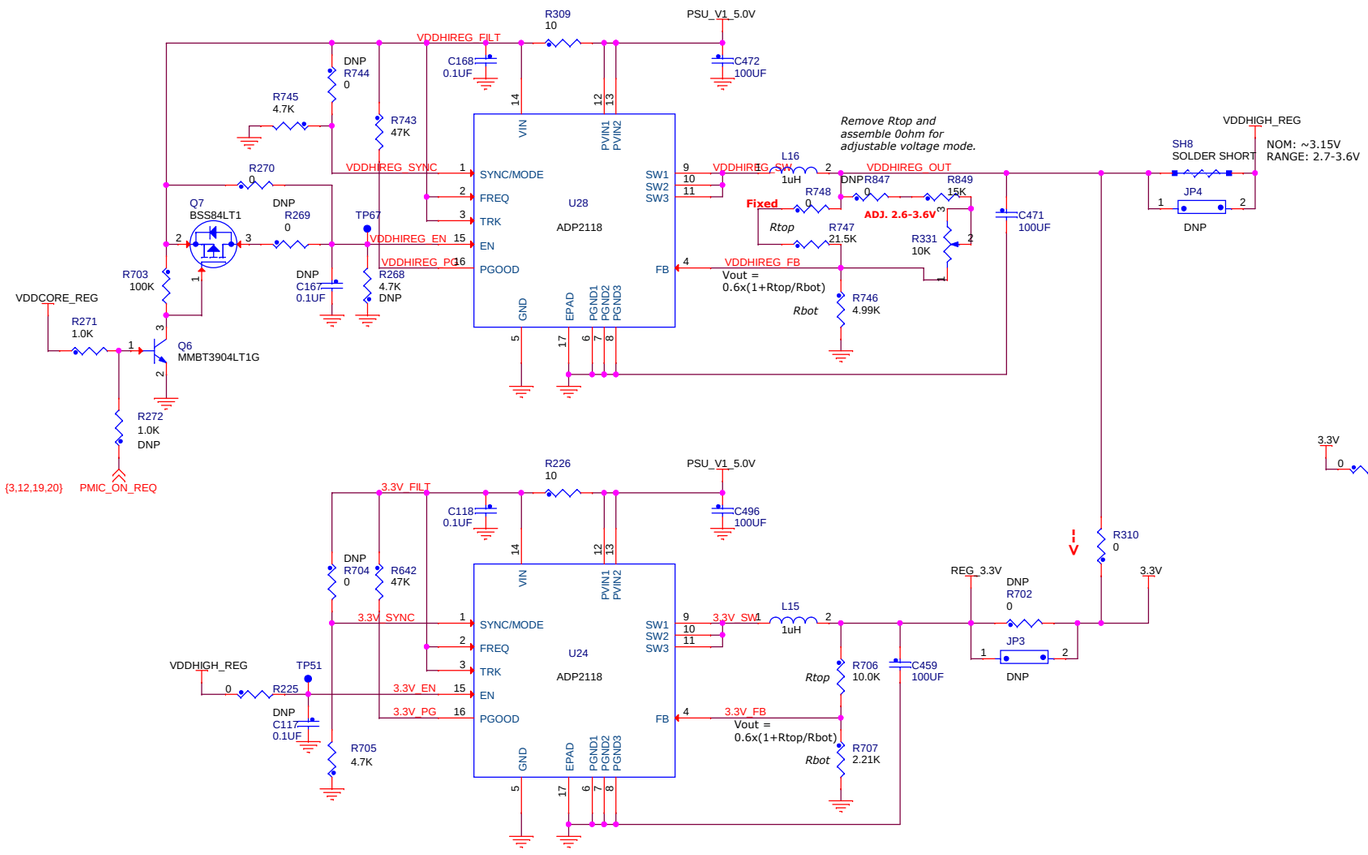
DNP R209 0 1.8V
NVCC_NANDF
C352 0.22UF
R208 0 3.3V
TP46, TP45

NVCC_JTAG
C302 0.22UF
R164 0 3.3V
TP37, TP38

Resistors are for current measurement only.
Not required for final applications. !

3.3V 1.8V
R544 0 DNP, R546 0
NVCC_SD1
C344 0.22UF
C343 0.1UF
U52 ADG849 (VDD, S2, S1, IN, D, GND)
R545 0 DNP
{13} SD1_VSELECT
R543 0
C276 0.1UF 3.3V
U50 NC7WZ132K8X (GND, VCC, A1, B1, Y1, A2, B2, Y2)
Optional backup inversion
DNP

3.3V 1.8V
R502 0, R541 0 DNP
NVCC_SD3
C278 0.22UF
C277 0.1UF
U46 ADG849 (VDD, S2, S1, IN, D, GND)
R503 0 DNP
{13} SD3_VSELECT
R537 0



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MX6QCPULPDDR2

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Power Supplies 1

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P2
CON_1_PWR
R848 0.1
R851 2.7K
R850 10.0K
C485 1.0 UF
D31 MMSZ5231BT1G
5V_DC_JACK
Q8A MBT3906DW1T1
OVERV_PROT
D30 RB521CS-30
MAINBOARD_DETECT_B
{17,20} SHUTDOWN_B
R846 10.0K
R845 10.0K
Q8B MBT3906DW1T1
R844 470K
DNP JP6
Q4 FDMS6681Z
D29 ESD9L5.0ST5G
PSU_V1_5.0V
C484 0.1UF
C483 1.0 UF
C482 100UF
D15 RED LED
R358 1.0K
5V ON

S1
S2
SW6 DPDT Switch
{17,20} SHUTDOWN_B

PSU_V1_5.0V
U1
NL17SZ125
VCC
GND
C3 0.1 UF
R380 1.0K
D1 LED_GREEN
CORE POWER GOOD

VDDCORE_REG_PGOOD
AVP Mode
R10 68K
DNP R18 0
DNP C4 0.1 UF
PSU_V1_5.0V
C200 47UF
C212 22UF
C199 22UF
C214 22UF
C201 22UF
R19 24
C7 1.0UF
SVIN
PVIN1
PVIN2
PVIN3
PVIN4
PGOOD
SW1_1
SW1_2
SW1_3
SW1_4
SW2_1
SW2_2
SW2_3
SW2_4
SW
ITH
U2
LTC3616
L2 0.47UH
NOM: 1.2V
RANGE: 0.9-1.4V
JP1
VDDCORE_REG
VDDARM_IN
R78 0.01
C35 47uF
C213 47uF
C34 10UF
C18 47uF
DNP C17 100UF
R12 39.2K
C6 10PF
C5 220pF
R45 0
DNP R77 0
VDDARM_IN
Option for Feedback from the chip for IR drop comensation
C1 22PF
R5 110K
R2 0
VFB
Vout = 0.6x(1+Rtop/Rbot)
R20 51.1K
R22 100K
DNP R21 0
R8 110K
BSS138LT1G Q1
R3 100K
DNP C2 0.1UF
R1 110K
DNP R6 301K
(BURST MODE EXTERNAL CLAMP)
DNP R7 100K

VDDHIGH_REG
PSU_V1_5.0V
DNP R17 0
R14 0
DNP R16 0
{3,12,19} PMIC_ON_REQ
R15 4.7M
VDDCORE_REG_EN
RUN
R42 4.7M
INT SS
DNP R43 0
SS
TRACK/SS
SS_CAP
EXT SS
R13 0
C16 0.01uF
DNP R47 0
RT
R46 165K
R44 0
RT/SYNC
SRLIM/DDR
MODE
DDR_1
NC1
NC2
PGND_PAD
SGND
R11 0
(PULSE-SKIP MODE)
(BURST MODE)
DNP R9 0
For FORCED CONTINUOUS mode (0.58 x SVIN) change PD to 1.13M (470-31179) and PU to 866K (470-31167).
{12} PMIC_STBY_REQ
R4 0

3.3V
R180 47K
R181 47K
R182 47K
U19
MAX7310
C119 0.047UF
Slave Addr(6:0): "0011111"
{11,17} I2C_SCL_3.3V
{11,17} I2C_SDA_3.3V
R185 0
R184 0
AD0
AD1
AD2
SCL
SDA
RESET
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
CTRL_0 {7}
CTRL_1 {8}
CTRL_2 {14}
CTRL_3 {16}
CTRL_4 {15}
PORT3_P116 {17}
PORT2_P81 {17}
PORT3_P101 {17}
{5,11,12,14,17} PORT3_P38
(POR_3.3V)

2.8V / 0.6A
U54
LTC3406ES5
R636 0
C394 4.7uF
L24 2.2UH
C395 10UF
TP34
TP40
2.8V
R518 0
R563 301K
C396 22PF
R564 82K
R2
R1
Vout = 0.6x(1+R2/R1)

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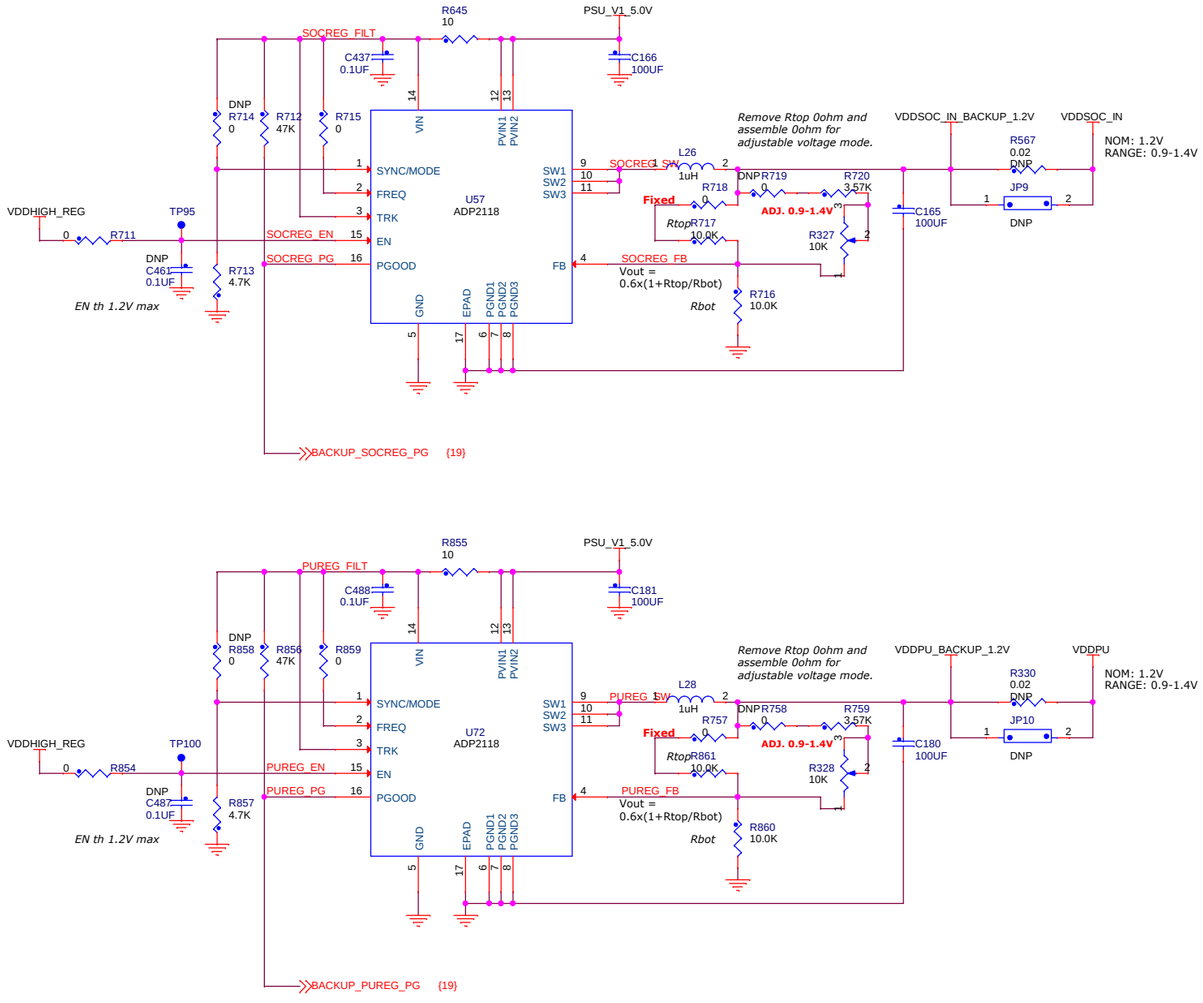

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Drawing Title:

MX6QCPULPDDR2

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Power Supplies 3

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Reserved configuration switch should be set to '0' (OFF)

SW1								
	BOOT_CFG1 [7]	**BOOT_CFG1 [6]**	**BOOT_CFG1 [5]**	**BOOT_CFG1 [4]**	**BOOT_CFG1 [3]**	**BOOT_CFG1 [2]**	**BOOT_CFG1 [1]**	**BOOT_CFG1 [0]**
Reserved-NVM	0	0	0	1	Reserved	Reserved	Reserved	Reserved
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
SATA	0	0	1	0	Reserved	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		Reserved (SDXC power control - XPC) 100mA/150mA TBD	SD Loopback Clock Source Sel '0' - direct '1' - through SD pad
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High! 1- Normal	Reserved	Reserved	MMC Loopback Clock Source Sel '0' - direct '1' - through SD pad
NAND	1	Reserved (Freq select)	BT_TOGGLEMODE	Override Pad Settings (using PAD_SETTINGS value)	Interleave Scheme: (TBD)		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

Reserved configuration switch should be set to '0' (OFF)

SW2								
	BOOT_CFG2 [7]	**BOOT_CFG2 [6]**	**BOOT_CFG2 [5]**	**BOOT_CFG2 [4]**	**BOOT_CFG2 [3]**	**BOOT_CFG2 [2]**	**BOOT_CFG2 [1]**	**BOOT_CFG2 [0]**
Reserved-NVM	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
WEIM	Muxing Scheme: A/D16 (HW Default in external boot) A+DH ,A+DL A/D32		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Reserved	Reserved	Reserved
SATA	Reserved	Reserved	Reserved	Tx Spread Spectrum '0' - Disabled '1' - Enabled	Rx Spread Spectrum '0' - Disabled '1' - Enabled	SATA_SPEED 0 - Gen2 (3.0Gbps) 1 - Gen1 (1.5Gbps)	SATA Type: '00' - i '01' - m '10' - x '11' - Reserved	
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select: 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3 11 - eSDHC4		Reserved (SDXC Current Limit) 200mA/400mA/600mA/800mA (TBD)		Override Pad Settings (using PAD_SETTINGS value)
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3 (eMMC4.4) 11 - eSDHC4		DLL Override: 0 - Boot ROM default. 1 - Apply value per fuse field MMC_DLL_DLY[3:0]	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	Override Pad Settings (using PAD_SETTINGS value)
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Pages In Block: 00 - 128 01 - 64 10 - 32 11 - Reserved		TBD (LBA-Nand) 0 - Non LBA (11ms delay) 1 - LBA (22ms delay)

Reserved configuration switch should be set to '0' (OFF)

SW3								
	BOOT_CFG3 [7]	**BOOT_CFG3 [6]**	**BOOT_CFG3 [5]**	**BOOT_CFG3 [4]**	**BOOT_CFG3 [3]**	**BOOT_CFG3 [2]**	**BOOT_CFG3 [1]**	**BOOT_CFG3 [0]**
	L1 I-Cache DISABLE	BT_MMU_DISABLE	DDR Memory Map default config '00' - Single DDR channel '01' - Fixed 2x32 map '10' - 4KB Interleaving Enabled '11' - Illegal		Reserved (DDR3 SPI config) '1' - DDR3 config. Read via SPI.	Boot Frequencies (ARM/DDR) 0 - 792 / 528 MHz 1 - 528 / 352MHz	Reserved	Reserved

Reserved configuration switch should be set to '0' (OFF)

SW4								
	BOOT_CFG4 [7]	**BOOT_CFG4 [6]**	**BOOT_CFG4 [5]**	**BOOT_CFG4 [4]**	**BOOT_CFG4 [3]**	**BOOT_CFG4 [2]**	**BOOT_CFG3 [1]**	**BOOT_CFG3 [0]**
	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)		Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - eCSPI5 101 - I2C1 110 - I2C2 111 - I2C3	

I2C Port Summary

iMX53 Port	Voltage Rail	Device	Address	Comment
I2C2	3.3V	Board ID	(001)01(00)x	Level Shifted
I2C2	3.3V	RIB		Level Shifted
I2C2	2.775V	MC13892 PMIC	000100(0)x	Level Shifted
I2C2	VCC_KEY_PAD (3.3V)	Audio CODEC	0(0)1 1010	
I2C2	NVCC_LCD (2.775V)	TSC2007	10010(00)x	Touch Screen Controller A2D. Level Shifted
I2C2	NVCC_LCD (2.775V)	PORT5 - Parallel Display Connector		Level Shifted
I2C2	5V	Digital POT.	010110(0)x	CCFL Inverter backlight control. Level Shifted
I2C2	5V	VGA DDC2 VGA DDC/CI	1010000x 0011111x	Level Shifted
I2C3	NVCC_EIM_MAIN (3.3V)	I2C EEPROM	1010(000)x	

NEEDS UPDATE

SW5 - Boot Mode			
BOOT_MODE [1]	**BOOT_MODE [0]**	**Boot Type**	**Boot Details**
0	0	Boot from fuses	Like 10, but boot fuses will be always used, if BT_FUSE_SEL=1
0	1	Serial Download via USB	Load and execute code, via serial device: USB (high-speed, non-stream, bulk mode)
1	0	Normal Boot (Development)	Executing ROM code, which handles booting from following sources NOR Flash (via WEIM, 16-bit, slow asynchronous mode for debugging purpose only) OneNAND SPI (serial flash) / I2C NAND Flash SD/MMC /MoviNAND SATA (Hard disk or SSD) A fallback to ALL above modes, on error exception: USB If BT_FUSE_SEL=0, GPIO boot pins will be sampled.
1	1	FSL Test Mode	Freescale Test Mode, special mode reserved for device testing.

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IOMUX Table

PIN NAME	RESET	ALT0		ALT1		ALT2		ALT3		ALT4		ALT5		ALT6		ALT7	
SD2_DAT1	ALT5	usdhc2	DAT1	ecspi5	SS0	weim	WEIM_CS[2]	audmux	AUD4_TXFS	kpp	COL[7]	gpio1	GPIO[14]	ccm	WAIT	anatop	ANATOP_TESTO[0]
SD2_DAT2	ALT5	usdhc2	DAT2	ecspi5	SS1	weim	WEIM_CS[3]	audmux	AUD4_TXD	kpp	ROW[6]	gpio1	GPIO[13]	ccm	STOP	anatop	ANATOP_TESTO[1]
SD2_DAT0	ALT5	usdhc2	DAT0	ecspi5	MISO			audmux	AUD4_RXD	kpp	ROW[7]	gpio1	GPIO[15]	dcic2	DCIC_OUT	anatop	ANATOP_TESTO[2]
RGMII_TXC	ALT5	usboh3	H2_DATA	enet	RGMII_TXC	spdif	SPDIF_EXTCLK					gpio6	GPIO[19]	mipi_core	DPHY_TEST_IN[0]	anatop	ANATOP_24M_OUT
RGMII_TD0	ALT5	mipi_hsi_ctrl	TX_READY	enet	RGMII_TD0							gpio6	GPIO[20]	mipi_core	DPHY_TEST_IN[1]		
RGMII_TD1	ALT5	mipi_hsi_ctrl	RX_FLAG	enet	RGMII_TD1							gpio6	GPIO[21]	mipi_core	DPHY_TEST_IN[2]	ccm	PLL3_BYP
RGMII_TD2	ALT5	mipi_hsi_ctrl	RX_DATA	enet	RGMII_TD2							gpio6	GPIO[22]	mipi_core	DPHY_TEST_IN[3]	ccm	PLL2_BYP
RGMII_TD3	ALT5	mipi_hsi_ctrl	RX_WAKE	enet	RGMII_TD3							gpio6	GPIO[23]	mipi_core	DPHY_TEST_IN[4]		
RGMII_RX_CTL	ALT5	usboh3	H3_DATA	enet	RGMII_RX_CTL							gpio6	GPIO[24]	mipi_core	DPHY_TEST_IN[5]		
RGMII_RD0	ALT5	mipi_hsi_ctrl	RX_READY	enet	RGMII_RD0							gpio6	GPIO[25]	mipi_core	DPHY_TEST_IN[6]		
RGMII_TX_CTL	ALT5	usboh3	H2_STROBE	enet	RGMII_TX_CTL							gpio6	GPIO[26]	mipi_core	DPHY_TEST_IN[7]	enet	ANATOP_ETHERNET_REF_OUT
RGMII_RD1	ALT5	mipi_hsi_ctrl	TX_FLAG	enet	RGMII_RD1							gpio6	GPIO[27]	mipi_core	DPHY_TEST_IN[8]	sjc	FAIL
RGMII_RD2	ALT5	mipi_hsi_ctrl	TX_DATA	enet	RGMII_RD2							gpio6	GPIO[28]	mipi_core	DPHY_TEST_IN[9]		
RGMII_RD3	ALT5	mipi_hsi_ctrl	TX_WAKE	enet	RGMII_RD3							gpio6	GPIO[29]	mipi_core	DPHY_TEST_IN[10]		
RGMII_RXC	ALT5	usboh3	H3_STROBE	enet	RGMII_RXC							gpio6	GPIO[30]	mipi_core	DPHY_TEST_IN[11]		
EIM_A25	ALT0	weim	WEIM_A[25]	ecspi4	SS1	ecspi2	RDY	ipu1	DI1_PIN12	ipu1	DI0_D1_CS	gpio5	GPIO[2]	hdmi_tx	CEC_LINE	pl301_mx63per1	HBURST[0]
EIM_EB2	ALT5	weim	WEIM_EB[2]	ecspi1	SS0	ccm	DI1_EXT_CLK	ipu2	CSI1_D[19]	hdmi_tx	DDC_SCL	gpio2	GPIO[30]	i2c2	SCL	src	BT_CFG[30]
EIM_D16	ALT5	weim	WEIM_D[16]	ecspi1	SCLK	ipu1	DI0_PIN5	ipu2	CSI1_D[18]	hdmi_tx	DDC_SDA	gpio3	GPIO[16]	i2c2	SDA		
EIM_D17	ALT5	weim	WEIM_D[17]	ecspi1	MISO	ipu1	DI0_PIN6	ipu2	CSI1_PIXCLK	dcic1	DCIC_OUT	gpio3	GPIO[17]	i2c3	SCL	pl301_mx63per1	HBURST[1]
EIM_D18	ALT5	weim	WEIM_D[18]	ecspi1	MOSI	ipu1	DI0_PIN7	ipu2	CSI1_D[17]	ipu1	DI1_D0_CS	gpio3	GPIO[18]	i2c3	SDA	pl301_mx63per1	HBURST[2]
EIM_D19	ALT5	weim	WEIM_D[19]	ecspi1	SS1	ipu1	DI0_PIN8	ipu2	CSI1_D[16]	uart1	CTS	gpio3	GPIO[19]	epit1	EPITO	pl301_mx63per1	HRESP
EIM_D20	ALT5	weim	WEIM_D[20]	ecspi4	SS0	ipu1	DI0_PIN16	ipu2	CSI1_D[15]	uart1	RTS	gpio3	GPIO[20]	epit2	EPITO		
EIM_D21	ALT5	weim	WEIM_D[21]	ecspi4	SCLK	ipu1	DI0_PIN17	ipu2	CSI1_D[11]	usboh3	USBOTG_OC	gpio3	GPIO[21]	i2c1	SCL	spdif	IN1
EIM_D22	ALT5	weim	WEIM_D[22]	ecspi4	MISO	ipu1	DI0_PIN1	ipu2	CSI1_D[10]	usboh3	USBOTG_PWR	gpio3	GPIO[22]	spdif	OUT1	pl301_mx63per1	HWRITE
EIM_D23	ALT5	weim	WEIM_D[23]	ipu1	DI0_D0_CS	uart3	CTS	uart1	DCD	ipu2	CSI1_DATA_EN	gpio3	GPIO[23]	ipu1	DI1_PIN2	ipu1	DI1_PIN14
EIM_EB3	ALT5	weim	WEIM_EB[3]	ecspi4	RDY	uart3	RTS	uart1	RI	ipu2	CSI1_HSYNC	gpio2	GPIO[31]	ipu1	DI1_PIN3	src	BT_CFG[31]
EIM_D24	ALT5	weim	WEIM_D[24]	ecspi4	SS2	uart3	TXD_MUX	ecspi1	SS2	ecspi2	SS2	gpio3	GPIO[24]	audmux	AUD5_RXFS	uart1	DTR
EIM_D25	ALT5	weim	WEIM_D[25]	ecspi4	SS3	uart3	RXD_MUX	ecspi1	SS3	ecspi2	SS3	gpio3	GPIO[25]	audmux	AUD5_RXC	uart1	DSR
EIM_D26	ALT5	weim	WEIM_D[26]	ipu1	DI1_PIN11	ipu1	CSI0_D[1]	ipu2	CSI1_D[14]	uart2	TXD_MUX	gpio3	GPIO[26]	ipu1	SISG[2]	ipu1	DISP1_DAT[22]
EIM_D27	ALT5	weim	WEIM_D[27]	ipu1	DI1_PIN13	ipu1	CSI0_D[0]	ipu2	CSI1_D[13]	uart2	RXD_MUX	gpio3	GPIO[27]	ipu1	SISG[3]	ipu1	DISP1_DAT[23]
EIM_D28	ALT5	weim	WEIM_D[28]	i2c1	SDA	ecspi4	MOSI	ipu2	CSI1_D[12]	uart2	CTS	gpio3	GPIO[28]	ipu1	EXT_TRIG	ipu1	DI0_PIN13
EIM_D29	ALT5	weim	WEIM_D[29]	ipu1	DI1_PIN15	ecspi4	SS0			uart2	RTS	gpio3	GPIO[29]	ipu2	CSI1_VSYNC	ipu1	DI0_PIN14
EIM_D30	ALT5	weim	WEIM_D[30]	ipu1	DISP1_DAT[21]	ipu1	DI0_PIN11	ipu1	CSI0_D[3]	uart3	CTS	gpio3	GPIO[30]	usboh3	USBH1_OC	pl301_mx63per1	HPROT[0]
EIM_D31	ALT5	weim	WEIM_D[31]	ipu1	DISP1_DAT[20]	ipu1	DI0_PIN12	ipu1	CSI0_D[2]	uart3	RTS	gpio3	GPIO[31]	usboh3	USBH1_PWR	pl301_mx63per1	HPROT[1]
EIM_A24	ALT0	weim	WEIM_A[24]	ipu1	DISP1_DAT[19]	ipu2	CSI1_D[19]	ipu2	SISG[2]	ipu1	SISG[2]	gpio5	GPIO[4]	pl301_mx63per1	HPROT[2]	src	BT_CFG[24]
EIM_A23	ALT0	weim	WEIM_A[23]	ipu1	DISP1_DAT[18]	ipu2	CSI1_D[18]	ipu2	SISG[3]	ipu1	SISG[3]	gpio6	GPIO[6]	pl301_mx63per1	HPROT[3]	src	BT_CFG[23]
EIM_A22	ALT0	weim	WEIM_A[22]	ipu1	DISP1_DAT[17]	ipu2	CSI1_D[17]					gpio2	GPIO[16]	tpsmp	HDATA[0]	src	BT_CFG[22]
EIM_A21	ALT0	weim	WEIM_A[21]	ipu1	DISP1_DAT[16]	ipu2	CSI1_D[16]			mipi_core	DPHY_TEST_OUT[18]	gpio2	GPIO[17]	tpsmp	HDATA[1]	src	BT_CFG[21]
EIM_A20	ALT0	weim	WEIM_A[20]	ipu1	DISP1_DAT[15]	ipu2	CSI1_D[15]			mipi_core	DPHY_TEST_OUT[19]	gpio2	GPIO[18]	tpsmp	HDATA[2]	src	BT_CFG[20]
EIM_A19	ALT0	weim	WEIM_A[19]	ipu1	DISP1_DAT[14]	ipu2	CSI1_D[14]			mipi_core	DPHY_TEST_OUT[20]	gpio2	GPIO[19]	tpsmp	HDATA[3]	src	BT_CFG[19]
EIM_A18	ALT0	weim	WEIM_A[18]	ipu1	DISP1_DAT[13]	ipu2	CSI1_D[13]			mipi_core	DPHY_TEST_OUT[21]	gpio2	GPIO[20]	tpsmp	HDATA[4]	src	BT_CFG[18]
EIM_A17	ALT0	weim	WEIM_A[17]	ipu1	DISP1_DAT[12]	ipu2	CSI1_D[12]			mipi_core	DPHY_TEST_OUT[22]	gpio2	GPIO[21]	tpsmp	HDATA[5]	src	BT_CFG[17]
EIM_A16	ALT0	weim	WEIM_A[16]	ipu1	DI1_DISP_CLK	ipu2	CSI1_PIXCLK			mipi_core	DPHY_TEST_OUT[23]	gpio2	GPIO[22]	tpsmp	HDATA[6]	src	BT_CFG[16]
EIM_CS0	ALT0	weim	WEIM_CS[0]	ipu1	DI1_PIN5	ecspi2	SCLK			mipi_core	DPHY_TEST_OUT[24]	gpio2	GPIO[23]	tpsmp	HDATA[7]		
EIM_CS1	ALT0	weim	WEIM_CS[1]	ipu1	DI1_PIN6	ecspi2	MOSI			mipi_core	DPHY_TEST_OUT[25]	gpio2	GPIO[24]	tpsmp	HDATA[8]		
EIM_OE	ALT0	weim	WEIM_OE	ipu1	DI1_PIN7	ecspi2	MISO			mipi_core	DPHY_TEST_OUT[26]	gpio2	GPIO[25]	tpsmp	HDATA[9]		
EIM_RW	ALT0	weim	WEIM_RW	ipu1	DI1_PIN8	ecspi2	SS0			mipi_core	DPHY_TEST_OUT[27]	gpio2	GPIO[26]	tpsmp	HDATA[10]	src	BT_CFG[29]
EIM_LBA	ALT0	weim	WEIM_LBA	ipu1	DI1_PIN17	ecspi2	SS1					gpio2	GPIO[27]	tpsmp	HDATA[11]	src	BT_CFG[26]
EIM_EB0	ALT0	weim	WEIM_EB[0]	ipu1	DISP1_DAT[11]	ipu2	CSI1_D[11]	mipi_core	DPHY_TEST_OUT[0]	ccm	PMIC_RDY	gpio2	GPIO[28]	tpsmp	HDATA[12]	src	BT_CFG[27]
EIM_EB1	ALT0	weim	WEIM_EB[1]	ipu1	DISP1_DAT[10]	ipu2	CSI1_D[10]	mipi_core	DPHY_TEST_OUT[1]			gpio2	GPIO[29]	tpsmp	HDATA[13]	src	BT_CFG[28]
EIM_DA0	ALT0	weim	WEIM_DA_A[0]	ipu1	DISP1_DAT[9]	ipu2	CSI1_D[9]	mipi_core	DPHY_TEST_OUT[2]			gpio3	GPIO[0]	tpsmp	HDATA[14]	src	BT_CFG[0]
EIM_DA1	ALT0	weim	WEIM_DA_A[1]	ipu1	DISP1_DAT[8]	ipu2	CSI1_D[8]	mipi_core	DPHY_TEST_OUT[3]	anatop	USBPHY1_TSTI_TX_LS_MODE	gpio3	GPIO[1]	tpsmp	HDATA[15]	src	BT_CFG[1]
EIM_DA2	ALT0	weim	WEIM_DA_A[2]	ipu1	DISP1_DAT[7]	ipu2	CSI1_D[7]	mipi_core	DPHY_TEST_OUT[4]	anatop	USBPHY1_TSTI_TX_HS_MODE	gpio3	GPIO[2]	tpsmp	HDATA[16]	src	BT_CFG[2]
EIM_DA3	ALT0	weim	WEIM_DA_A[3]	ipu1	DISP1_DAT[6]	ipu2	CSI1_D[6]	mipi_core	DPHY_TEST_OUT[5]	anatop	USBPHY1_TSTI_TX_HIZ	gpio3	GPIO[3]	tpsmp	HDATA[17]	src	BT_CFG[3]
EIM_DA4	ALT0	weim	WEIM_DA_A[4]	ipu1	DISP1_DAT[5]	ipu2	CSI1_D[5]	mipi_core	DPHY_TEST_OUT[6]	anatop	USBPHY1_TSTI_TX_EN	gpio3	GPIO[4]	tpsmp	HDATA[18]	src	BT_CFG[4]
EIM_DA5	ALT0	weim	WEIM_DA_A[5]	ipu1	DISP1_DAT[4]	ipu2	CSI1_D[4]	mipi_core	DPHY_TEST_OUT[7]	anatop	USBPHY1_TSTI_TX_DP	gpio3	GPIO[5]	tpsmp	HDATA[19]	src	BT_CFG[5]
EIM_DA6	ALT0	weim	WEIM_DA_A[6]	ipu1	DISP1_DAT[3]	ipu2	CSI1_D[3]	mipi_core	DPHY_TEST_OUT[8]	anatop	USBPHY1_TSTI_TX_DN	gpio3	GPIO[6]	tpsmp	HDATA[20]	src	BT_CFG[6]
EIM_DA7	ALT0	weim	WEIM_DA_A[7]	ipu1	DISP1_DAT[2]	ipu2	CSI1_D[2]	mipi_core	DPHY_TEST_OUT[9]			gpio3	GPIO[7]	tpsmp	HDATA[21]	src	BT_CFG[7]
EIM_DA8	ALT0	weim	WEIM_DA_A[8]	ipu1	DISP1_DAT[1]	ipu2	CSI1_D[1]	mipi_core	DPHY_TEST_OUT[10]			gpio3	GPIO[8]	tpsmp	HDATA[22]	src	BT_CFG[8]
EIM_DA9	ALT0	weim	WEIM_DA_A[9]	ipu1	DISP1_DAT[0]	ipu2	CSI1_D[0]	mipi_core	DPHY_TEST_OUT[11]			gpio3	GPIO[9]	tpsmp	HDATA[23]	src	BT_CFG[9]
EIM_DA10	ALT0	weim	WEIM_DA_A[10]	ipu1	DI1_PIN15	ipu2	CSI1_DATA_EN	mipi_core	DPHY_TEST_OUT[12]			gpio3	GPIO[10]	tpsmp	HDATA[24]	src	BT_CFG[10]
EIM_DA11	ALT0	weim	WEIM_DA_A[11]	ipu1	DI1_PIN2	ipu2	CSI1_HSYNC	mipi_core	DPHY_TEST_OUT[13]	sdma	DEBUG_EVT_CHN_LINES[6]	gpio3	GPIO[11]	tpsmp	HDATA[25]	src	BT_CFG[11]
EIM_DA12	ALT0	weim	WEIM_DA_A[12]	ipu1	DI1_PIN3	ipu2	CSI1_VSYNC	mipi_core	DPHY_TEST_OUT[14]	sdma	DEBUG_EVT_CHN_LINES[3]	gpio3	GPIO[12]	tpsmp	HDATA[26]	src	BT_CFG[12]
EIM_DA13	ALT0	weim	WEIM_DA_A[13]	ipu1	DI1_D0_CS	ccm	DI1_EXT_CLK	mipi_core	DPHY_TEST_OUT[15]	sdma	DEBUG_EVT_CHN_LINES[4]	gpio3	GPIO[13]	tpsmp	HDATA[27]	src	BT_CFG[13]
EIM_DA14	ALT0	weim	WEIM_DA_A[14]	ipu1	DI1_D1_CS	ccm	DI0_EXT_CLK	mipi_core	DPHY_TEST_OUT[16]	sdma	DEBUG_EVT_CHN_LINES[5]	gpio3	GPIO[14]	tpsmp	HDATA[28]	src	BT_CFG[14]
EIM_DA15	ALT0	weim	WEIM_DA_A[15]	ipu1	DI1_PIN1	ipu1	DI1_PIN4	mipi_core	DPHY_TEST_OUT[17]			gpio3	GPIO[15]	tpsmp	HDATA[29]	src	BT_CFG[15]
EIM_WAIT	ALT0	weim	WEIM_WAIT	weim	WEIM_DTACK_B							gpio5	GPIO[0]	tpsmp	HDATA[30]	src	BT_CFG[25]
EIM_BCLK	ALT0	weim	WEIM_BCLK	ipu1	DI1_PIN16							gpio6	GPIO[31]	tpsmp	HDATA[31]		
DI0_DISP_CLK	ALT5	ipu1	DI0_DISP_CLK	ipu2	DI0_DISP_CLK			mipi_core	DPHY_TEST_OUT[28]	sdma	DEBUG_CORE_STATE[0]	gpio4	GPIO[16]	mmdc	MMDC_DEBUG[0]		
DI0_PIN15	ALT5	ipu1	DI0_PIN15	ipu2	DI0_PIN15	audmux	AUD6_TXC	mipi_core	DPHY_TEST_OUT[29]	sdma	DEBUG_CORE_STATE[1]	gpio4	GPIO[17]	mmdc	MMDC_DEBUG[1]		
DI0_PIN2	ALT5	ipu1	DI0_PIN2	ipu2	DI0_PIN2	audmux	AUD6_TXD	mipi_core	DPHY_TEST_OUT[30]	sdma	DEBUG_CORE_STATE[2]	gpio4	GPIO[18]	mmdc	MMDC_DEBUG[2]	pl301_mx63per1	HADDR[9]
DI0_PIN3	ALT5	ipu1	DI0_PIN3	ipu2	DI0_PIN3	audmux	AUD6_TXFS	mipi_core	DPHY_TEST_OUT[31]	sdma	DEBUG_CORE_STATE[3]	gpio4	GPIO[19]	mmdc	MMDC_DEBUG[3]	pl301_mx63per1	HADDR[10]
DI0_PIN4	ALT5	ipu1	DI0_PIN4	ipu2	DI0_PIN4	audmux	AUD6_RXD	usdhc1	WP	sdma	DEBUG_YIELD	gpio4	GPIO[20]	mmdc	MMDC_DEBUG[4]	pl301_mx63per1	HADDR[11]
DISP0_DAT0	ALT5	ipu1	DISP0_DAT[0]	ipu2	DISP0_DAT[0]	ecspi3	SCLK	usdhc1	USDHC_DEBUG[0]	sdma	DEBUG_CORE_RUN	gpio4	GPIO[21]	mmdc	MMDC_DEBUG[5]		
DISP0_DAT1	ALT5	ipu1	DISP0_DAT[1]	ipu2	DISP0_DAT[1]	ecspi3	MOSI	usdhc1	USDHC_DEBUG[1]	sdma	DEBUG_EVENT_CHANNEL_SEL	gpio4	GPIO[22]	mmdc	MMDC_DEBUG[6]	pl301_mx63per1	HADDR[12]
DISP0_DAT2	ALT5	ipu1	DISP0_DAT[2]	ipu2	DISP0_DAT[2]	ecspi3	MISO	usdhc1	USDHC_DEBUG[2]	sdma	DEBUG_MODE	gpio4	GPIO[23]	mmdc	MMDC_DEBUG[7]	pl301_mx63per1	HADDR[13]
DISP0_DAT3	ALT5	ipu1	DISP0_DAT[3]	ipu2	DISP0_DAT[3]	ecspi3	SS0	usdhc1	USDHC_DEBUG[3]	sdma	DEBUG_BUS_ERROR	gpio4	GPIO[24]	mmdc	MMDC_DEBUG[8]	pl301_mx63per1	HADDR[14]
DISP0_DAT4	ALT5	ipu1	DISP0_DAT[4]	ipu2	DISP0_DAT[4]	ecspi3	SS1	usdhc1	USDHC_DEBUG[4]	sdma	DEBUG_BUS_RWB	gpio4	GPIO[25]	mmdc	MMDC_DEBUG[9]	pl301_mx63per1	HADDR[15]
DISP0_DAT5	ALT5	ipu1	DISP0_DAT[5]	ipu2	DISP0_DAT[5]	ecspi3	SS2	audmux	AUD6_RXFS	sdma	DEBUG_MATCHED_DMBUS	gpio4	GPIO[26]	mmdc	MMDC_DEBUG[10]	pl301_mx63per1	HADDR[16]
DISP0_DAT6	ALT5	ipu1	DISP0_DAT[6]	ipu2	DISP0_DAT[6]	ecspi3	SS3	audmux	AUD6_RXC	sdma	DEBUG_RTBUFFER_WRITE	gpio4	GPIO[27]	mmdc	MMDC_DEBUG[11]	pl301_mx63per1	HADDR[17]
DISP0_DAT7	ALT5	ipu1	DISP0_DAT[7]	ipu2	DISP0_DAT[7]	ecspi3	RDY	usdhc1	USDHC_DEBUG[5]	sdma	DEBUG_EVENT_CHANNEL[0]	gpio4	GPIO[28]	mmdc	MMDC_DEBUG[12]	pl301_mx63per1	HADDR[18]
DISP0_DAT8	ALT5	ipu1	DISP0_DAT[8]	ipu2	DISP0_DAT[8]	pwm1	PWMO	wdog1	WDOG_B	sdma	DEBUG_EVENT_CHANNEL[1]	gpio4	GPIO[29]	mmdc	MMDC_DEBUG[13]	pl301_mx63per1	HADDR[19]
DISP0_DAT9	ALT5	ipu1	DISP0_DAT[9]	ipu2	DISP0_DAT[9]	pwm2	PWMO	wdog2	WDOG_B	sdma	DEBUG_EVENT_CHANNEL[2]	gpio4	GPIO[30]	mmdc	MMDC_DEBUG[14]	pl301_mx63per1	HADDR[20]
DISP0_DAT10	ALT5	ipu1	DISP0_DAT[10]	ipu2	DISP0_DAT[10]			usdhc1	USDHC_DEBUG[6]	sdma	DEBUG_EVENT_CHANNEL[3]	gpio4	GPIO[31]	mmdc	MMDC_DEBUG[15]	pl301_mx63per1	HADDR[21]
DISP0_DAT11	ALT5	ipu1	DISP0_DAT[11]	ipu2	DISP0_DAT[11]			usdhc1	USDHC_DEBUG[7]	sdma	DEBUG_EVENT_CHANNEL[4]	gpio5	GPIO[5]	mmdc	MMDC_DEBUG[16]	pl301_mx63per1	HADDR[22]
DISP0_DAT12	ALT5	ipu1	DISP0_DAT[12]	ipu2	DISP0_DAT[12]					sdma	DEBUG_EVENT_CHANNEL[5]	gpio5	GPIO[6]	mmdc	MMDC_DEBUG[17]	pl301_mx63per1	HADDR[23]
DISP0_DAT13	ALT5	ipu1	DISP0_DAT[13]	ipu2	DISP0_DAT[13]			audmux	AUD5_RXFS	sdma	DEBUG_EVT_CHN_LINES[0]	gpio5	GPIO[7]	mmdc	MMDC_DEBUG[18]	pl301_mx63per1	HADDR[24]
DISP0_DAT14	ALT5	ipu1	DISP0_DAT[14]	ipu2	DISP0_DAT[14]			audmux	AUD5_RXC	sdma	DEBUG_EVT_CHN_LINES[1]	gpio5	GPIO[8]	mmdc	MMDC_DEBUG[19]		
DISP0_DAT15	ALT5	ipu1	DISP0_DAT[15]	ipu2	DISP0_DAT[15]	ecspi1	SS1	ecspi2	SS1	sdma	DEBUG_EVT_CHN_LINES[2]	gpio5	GPIO[9]	mmdc	MMDC_DEBUG[20]	pl301_mx63per1	HADDR[25]
DISP0_DAT16	ALT5	ipu1	DISP0_DAT[16]	ipu2	DISP0_DAT[16]	ecspi2	MOSI	audmux	AUD5_TXC	sdma	SDMA_EXT_EVENT[0]	gpio5	GPIO[10]	mmdc	MMDC_DEBUG[21]	pl301_mx63per1	HADDR[26]
DISP0_DAT17	ALT5	ipu1	DISP0_DAT[17]	ipu2	DISP0_DAT[17]	ecspi2	MISO	audmux	AUD5_TXD	sdma	SDMA_EXT_EVENT[1]	gpio5	GPIO[11]	mmdc	MMDC_DEBUG[22]	pl301_mx63per1	HADDR[27]
DISP0_DAT18	ALT5	ipu1	DISP0_DAT[18]	ipu2	DISP0_DAT[18]	ecspi2	SS0	audmux	AUD5_TXFS	audmux	AUD4_RXFS	gpio5	GPIO[12]	mmdc	MMDC_DEBUG[23]	weim	WEIM_CS[2]
DISP0_DAT19	ALT5	ipu1	DISP0_DAT[19]	ipu2	DISP0_DAT[19]	ecspi2	SCLK	audmux	AUD5_RXD	audmux	AUD4_RXC	gpio5	GPIO[13]	mmdc	MMDC_DEBUG[24]	weim	WEIM_CS[3]
DISP0_DAT20	ALT5	ipu1	DISP0_DAT[20]	ipu2	DISP0_DAT[20]	ecspi1	SCLK	audmux	AUD4_TXC	sdma	DEBUG_EVT_CHN_LINES[7]	gpio5	GPIO[14]	mmdc	MMDC_DEBUG[25]	pl301_mx63per1	HADDR[28]
DISP0_DAT21	ALT5	ipu1	DISP0_DAT[21]	ipu2	DISP0_DAT[21]	ecspi1	MOSI	audmux	AUD4_TXD	sdma	DEBUG_BUS_DEVICE[0]	gpio5	GPIO[15]	mmdc	MMDC_DEBUG[26]	pl301_mx63per1	HADDR[29]
DISP0_DAT22	ALT5	ipu1	DISP0_DAT[22]	ipu2	DISP0_DAT[22]	ecspi1	MISO	audmux	AUD4_TXFS	sdma	DEBUG_BUS_DEVICE[1]	gpio5	GPIO[16]	mmdc	MMDC_DEBUG[27]	pl301_mx63per1	HADDR[30]
DISP0_DAT23	ALT5	ipu1	DISP0_DAT[23]	ipu2	DISP0_DAT[23]	ecspi1	SS0	audmux	AUD4_RXD	sdma	DEBUG_BUS_DEVICE[2]	gpio5	GPIO[17]	mmdc	MMDC_DEBUG[28]	pl301_mx63per1	HADDR[31]
ENET_MDIO	ALT5			enet	MDIO	esai1	SCKR	sdma	DEBUG_BUS_DEVICE[3]	enet	1588_EVENT1_OUT	gpio1	GPIO[22]	spdif	PLOCK		
ENET_REF_CLK	ALT5			enet	TX_CLK	esai1	FSR	sdma	DEBUG_BUS_DEVICE[4]			gpio1	GPIO[23]	spdif	SRCLK	anatop	USBPHY1_TSTO_RX_SQUELCH
ENET_RX_ER	ALT5	usboh3	USBOTG_ID	enet	RX_ER	esai1	HCKR	spdif	IN1	enet	1588_EVENT2_OUT	gpio1	GPIO[24]	phy	TDI	anatop	USBPHY1_TSTO_RX_HS_RXD
ENET_CRS_DV	ALT5			enet	RX_EN	esai1	SCKT	spdif	SPDIF_EXTCLK			gpio1	GPIO[25]	phy	TDO	anatop	USBPHY1_TSTO_RX_FS_RXD
ENET_RXD1	ALT5	mlb	MLBSIG	enet	RDATA[1]	esai1	FST			enet	1588_EVENT3_OUT	gpio1	GPIO[26]	phy	TCK	anatop	USBPHY1_TSTO_RX_DISCON_DET
ENET_RXD0	ALT5	osc32k	32K_OUT	enet	RDATA[0]	esai1	HCKT	spdif	OUT1			gpio1	GPIO[27]	phy	TMS	anatop	USBPHY1_TSTO_PLL_CLK20DIV
ENET_TX_EN	ALT5			enet	TX_EN	esai1	TX3_RX2					gpio1	GPIO[28]	sata_phy	TDI	anatop	USBPHY2_TSTO_RX_SQUELCH
ENET_TXD1	ALT5	mlb	MLBCLK	enet	TDATA[1]	esai1	TX2_RX3			enet	1588_EVENT0_IN	gpio1	GPIO[29]	sata_phy	TDO	anatop	USBPHY2_TSTO_RX_HS_RXD
ENET_TXD0	ALT5			enet	TDATA[0]	esai1	TX4_RX1					gpio1	GPIO[30]	sata_phy	TCK	anatop	USBPHY2_TSTO_RX_FS_RXD
ENET_MDC	ALT5	mlb	MLBDAT	enet	MDC	esai1	TX5_RX0			enet	1588_EVENT1_IN	gpio1	GPIO[31]	sata_phy	TMS	anatop	USBPHY2_TSTO_RX_DISCON_DET
KEY_COL0	ALT5	ecspi1	SCLK	enet	RDATA[3]	audmux	AUD5_TXC	kpp	COL[0]	uart4	TXD_MUX	gpio4	GPIO[6]	dcic1	DCIC_OUT	src	ANY_PU_RST
KEY_ROW0	ALT5	ecspi1	MOSI	enet	TDATA[3]	audmux	AUD5_TXD	kpp	ROW[0]	uart4	RXD_MUX	gpio4	GPIO[7]	dcic2	DCIC_OUT	pl301_mx63per1	HADDR[0]
KEY_COL1	ALT5	ecspi1	MISO	enet	MDIO	audmux	AUD5_TXFS	kpp	COL[1]	uart5	TXD_MUX	gpio4	GPIO[8]	usdhc1	VSELECT	pl301_mx63per1	HADDR[1]
KEY_ROW1	ALT5	ecspi1	SS0	enet	COL	audmux	AUD5_RXD	kpp	ROW[1]	uart5	RXD_MUX	gpio4	GPIO[9]	usdhc2	VSELECT	pl301_mx63per1	HADDR[2]
KEY_COL2	ALT5	ecspi1	SS1	enet	RDATA[2]	can1	TXCAN	kpp	COL[2]	enet	MDC	gpio4	GPIO[10]	usboh3	H1USB_PWRCTL_WAKEUP	pl301_mx63per1	HADDR[3]
KEY_ROW2	ALT5	ecspi1	SS2	enet	TDATA[2]	can1	RXCAN	kpp	ROW[2]	usdhc2	VSELECT	gpio4	GPIO[11]	hdmi_tx	CEC_LINE	pl301_mx63per1	HADDR[4]
KEY_COL3	ALT5	ecspi1	SS3	enet	CRS	hdmi_tx	DDC_SCL	kpp	COL[3]	i2c2	SCL	gpio4	GPIO[12]	spdif	IN1	pl301_mx63per1	HADDR[5]
KEY_ROW3	ALT5	osc32k	32K_OUT	asrc	ASRC_EXT_CLK	hdmi_tx	DDC_SDA	kpp	ROW[3]	i2c2	SDA	gpio4	GPIO[13]	usdhc1	VSELECT	pl301_mx63per1	HADDR[6]
KEY_COL4	ALT5	can2	TXCAN	ipu1	SISG[4]	usboh3	USBOTG_OC	kpp	COL[4]	uart5	RTS	gpio4	GPIO[14]	mmdc	MMDC_DEBUG[49]	pl301_mx63per1	HADDR[7]
KEY_ROW4	ALT5	can2	RXCAN	ipu1	SISG[5]	usboh3	USBOTG_PWR	kpp	ROW[4]	uart5	CTS	gpio4	GPIO[15]	mmdc	MMDC_DEBUG[50]	pl301_mx63per1	HADDR[8]
GPIO_0	ALT5	ccm	CLKO			kpp	COL[5]	asrc	ASRC_EXT_CLK	epit1	EPITO	gpio1	GPIO[0]	usboh3	USBH1_PWR	snvs_hp_wrapper	SNVS_VIO_5
GPIO_1	ALT5	esai1	SCKR	wdog2	WDOG_B	kpp	ROW[5]	usboh3	USBOTG_ID	pwm2	PWMO	gpio1	GPIO[1]	usdhc1	CD	src	TESTER_ACK
GPIO_9	ALT5	esai1	FSR	wdog1	WDOG_B	kpp	COL[6]	ccm	REF_EN_B	pwm1	PWMO	gpio1	GPIO[9]	usdhc1	WP	src	EARLY_RST
GPIO_3	ALT5	esai1	HCKR	observe_mux	OBSRV_INT_OUT0	i2c3	SCL	anatop	ANATOP_24M_OUT	ccm	CLKO2	gpio1	GPIO[3]	usboh3	USBH1_OC	mlb	MLBCLK
GPIO_6	ALT5	esai1	SCKT	observe_mux	OBSRV_INT_OUT1	i2c3	SDA	ccm	CCM_OUT_0	csu	CSU_INT_DEB	gpio1	GPIO[6]	usdhc2	LCTL	mlb	MLBSIG
GPIO_2	ALT5	esai1	FST	observe_mux	OBSRV_INT_OUT2	kpp	ROW[6]	ccm	CCM_OUT_1	csu	CSU_ALARM_AUT[0]	gpio1	GPIO[2]	usdhc2	WP	mlb	MLBDAT
GPIO_4	ALT5	esai1	HCKT	observe_mux	OBSRV_INT_OUT3	kpp	COL[7]	ccm	CCM_OUT_2	csu	CSU_ALARM_AUT[1]	gpio1	GPIO[4]	usdhc2	CD	ocotp_ctrl_wrapper	FUSE_LATCHED
GPIO_5	ALT5	esai1	TX2_RX3	observe_mux	OBSRV_INT_OUT4	kpp	ROW[7]	ccm	CLKO	csu	CSU_ALARM_AUT[2]	gpio1	GPIO[5]	i2c3	SCL	cheetah	EVENTI
GPIO_7	ALT5	esai1	TX4_RX1	ecspi5	RDY	epit1	EPITO	can1	TXCAN	uart2	TXD_MUX	gpio1	GPIO[7]	spdif	PLOCK	usboh3	OTGUSB_HOST_MODE
GPIO_8	ALT5	esai1	TX5_RX0	anatop	ANATOP_32K_OUT	epit2	EPITO	can1	RXCAN	uart2	RXD_MUX	gpio1	GPIO[8]	spdif	SRCLK	usboh3	OTGUSB_PWRCTL_WAKEUP
GPIO_16	ALT5	esai1	TX3_RX2	enet	1588_EVENT2_IN	enet	ANATOP_ETHERNET_REF_OUT	usdhc1	LCTL	spdif	IN1	gpio7	GPIO[11]	i2c3	SDA	sjc	DE_B
GPIO_17	ALT5	esai1	TX0	enet	1588_EVENT3_IN	ccm	PMIC_RDY	sdma	SDMA_EXT_EVENT[0]	spdif	OUT1	gpio7	GPIO[12]			sjc	JTAG_ACT
GPIO_18	ALT5	esai1	TX1	enet	RX_CLK	usdhc3	VSELECT	sdma	SDMA_EXT_EVENT[1]	asrc	ASRC_EXT_CLK	gpio7	GPIO[13]	snvs_hp_wrapper	SNVS_VIO_5_CTL	src	SYSTEM_RST
GPIO_19	ALT5	kpp	COL[5]	enet	1588_EVENT0_OUT	spdif	OUT1	ccm	CLKO	ecspi1	RDY	gpio4	GPIO[5]	enet	TX_ER	src	INT_BOOT
CSI0_PIXCLK	ALT5	ipu1	CSI0_PIXCLK			pcie_ctrl	DIAG_STATUS_BUS_MUX[12]			sdma	DEBUG_PC[0]	gpio5	GPIO[18]	mmdc	MMDC_DEBUG[29]	cheetah	EVENTO
CSI0_MCLK	ALT5	ipu1	CSI0_HSYNC			pcie_ctrl	DIAG_STATUS_BUS_MUX[13]	ccm	CLKO	sdma	DEBUG_PC[1]	gpio5	GPIO[19]	mmdc	MMDC_DEBUG[30]	cheetah	TRCTL
CSI0_DATA_EN	ALT5	ipu1	CSI0_DATA_EN	weim	WEIM_D[0]	pcie_ctrl	DIAG_STATUS_BUS_MUX[14]			sdma	DEBUG_PC[2]	gpio5	GPIO[20]	mmdc	MMDC_DEBUG[31]	cheetah	TRCLK
CSI0_VSYNC	ALT5	ipu1	CSI0_VSYNC	weim	WEIM_D[1]	pcie_ctrl	DIAG_STATUS_BUS_MUX[15]			sdma	DEBUG_PC[3]	gpio5	GPIO[21]	mmdc	MMDC_DEBUG[32]	cheetah	TRACE[0]
CSI0_DAT4	ALT5	ipu1	CSI0_D[4]	weim	WEIM_D[2]	ecspi1	SCLK	kpp	COL[5]	audmux	AUD3_TXC	gpio5	GPIO[22]	mmdc	MMDC_DEBUG[43]	cheetah	TRACE[1]
CSI0_DAT5	ALT5	ipu1	CSI0_D[5]	weim	WEIM_D[3]	ecspi1	MOSI	kpp	ROW[5]	audmux	AUD3_TXD	gpio5	GPIO[23]	mmdc	MMDC_DEBUG[44]	cheetah	TRACE[2]
CSI0_DAT6	ALT5	ipu1	CSI0_D[6]	weim	WEIM_D[4]	ecspi1	MISO	kpp	COL[6]	audmux	AUD3_TXFS	gpio5	GPIO[24]	mmdc	MMDC_DEBUG[45]	cheetah	TRACE[3]
CSI0_DAT7	ALT5	ipu1	CSI0_D[7]	weim	WEIM_D[5]	ecspi1	SS0	kpp	ROW[6]	audmux	AUD3_RXD	gpio5	GPIO[25]	mmdc	MMDC_DEBUG[46]	cheetah	TRACE[4]
CSI0_DAT8	ALT5	ipu1	CSI0_D[8]	weim	WEIM_D[6]	ecspi2	SCLK	kpp	COL[7]	i2c1	SDA	gpio5	GPIO[26]	mmdc	MMDC_DEBUG[47]	cheetah	TRACE[5]
CSI0_DAT9	ALT5	ipu1	CSI0_D[9]	weim	WEIM_D[7]	ecspi2	MOSI	kpp	ROW[7]	i2c1	SCL	gpio5	GPIO[27]	mmdc	MMDC_DEBUG[48]	cheetah	TRACE[6]
CSI0_DAT10	ALT5	ipu1	CSI0_D[10]	audmux	AUD3_RXC	ecspi2	MISO	uart1	TXD_MUX	sdma	DEBUG_PC[4]	gpio5	GPIO[28]	mmdc	MMDC_DEBUG[33]	cheetah	TRACE[7]
CSI0_DAT11	ALT5	ipu1	CSI0_D[11]	audmux	AUD3_RXFS	ecspi2	SS0	uart1	RXD_MUX	sdma	DEBUG_PC[5]	gpio5	GPIO[29]	mmdc	MMDC_DEBUG[34]	cheetah	TRACE[8]
CSI0_DAT12	ALT5	ipu1	CSI0_D[12]	weim	WEIM_D[8]	pcie_ctrl	DIAG_STATUS_BUS_MUX[16]	uart4	TXD_MUX	sdma	DEBUG_PC[6]	gpio5	GPIO[30]	mmdc	MMDC_DEBUG[35]	cheetah	TRACE[9]
CSI0_DAT13	ALT5	ipu1	CSI0_D[13]	weim	WEIM_D[9]	pcie_ctrl	DIAG_STATUS_BUS_MUX[17]	uart4	RXD_MUX	sdma	DEBUG_PC[7]	gpio5	GPIO[31]	mmdc	MMDC_DEBUG[36]	cheetah	TRACE[10]
CSI0_DAT14	ALT5	ipu1	CSI0_D[14]	weim	WEIM_D[10]	pcie_ctrl	DIAG_STATUS_BUS_MUX[18]	uart5	TXD_MUX	sdma	DEBUG_PC[8]	gpio6	GPIO[0]	mmdc	MMDC_DEBUG[37]	cheetah	TRACE[11]
CSI0_DAT15	ALT5	ipu1	CSI0_D[15]	weim	WEIM_D[11]	pcie_ctrl	DIAG_STATUS_BUS_MUX[19]	uart5	RXD_MUX	sdma	DEBUG_PC[9]	gpio6	GPIO[1]	mmdc	MMDC_DEBUG[38]	cheetah	TRACE[12]
CSI0_DAT16	ALT5	ipu1	CSI0_D[16]	weim	WEIM_D[12]	pcie_ctrl	DIAG_STATUS_BUS_MUX[20]	uart4	RTS	sdma	DEBUG_PC[10]	gpio6	GPIO[2]	mmdc	MMDC_DEBUG[39]	cheetah	TRACE[13]
CSI0_DAT17	ALT5	ipu1	CSI0_D[17]	weim	WEIM_D[13]	pcie_ctrl	DIAG_STATUS_BUS_MUX[21]	uart4	CTS	sdma	DEBUG_PC[11]	gpio6	GPIO[3]	mmdc	MMDC_DEBUG[40]	cheetah	TRACE[14]
CSI0_DAT18	ALT5	ipu1	CSI0_D[18]	weim	WEIM_D[14]	pcie_ctrl	DIAG_STATUS_BUS_MUX[22]	uart5	RTS	sdma	DEBUG_PC[12]	gpio6	GPIO[4]	mmdc	MMDC_DEBUG[41]	cheetah	TRACE[15]
CSI0_DAT19	ALT5	ipu1	CSI0_D[19]	weim	WEIM_D[15]	pcie_ctrl	DIAG_STATUS_BUS_MUX[23]	uart5	CTS	sdma	DEBUG_PC[13]	gpio6	GPIO[5]	mmdc	MMDC_DEBUG[42]	anatop	ANATOP_TESTO[9]
TAMPER	ALT0	snvs_lp_wrapper	SNVS_TD1														
PMIC_ON_REQ	ALT0	snvs_lp_wrapper	SNVS_WAKEUP_ALARM														
PMIC_STBY_REQ	ALT0	ccm	PMIC_VSTBY_REQ														
POR_B	ALT0	src	POR_B														
BOOT_MODE1	ALT0	src	BOOT_MODE[1]														
ONOFF		src	RESET_B														
BOOT_MODE0	ALT0	src	BOOT_MODE[0]														
TEST_MODE	ALT0	tcu	TEST_MODE														
SD3_DAT7	ALT5	usdhc3	DAT7	uart1	TXD_MUX	pcie_ctrl	DIAG_STATUS_BUS_MUX[24]	usboh3	UH3_DFD_OUT[0]	usboh3	UH2_DFD_OUT[0]	gpio6	GPIO[17]	mipi_core	DPHY_TEST_IN[12]	anatop	USBPHY2_TSTO_PLL_CLK20DIV
SD3_DAT6	ALT5	usdhc3	DAT6	uart1	RXD_MUX	pcie_ctrl	DIAG_STATUS_BUS_MUX[25]	usboh3	UH3_DFD_OUT[1]	usboh3	UH2_DFD_OUT[1]	gpio6	GPIO[18]	mipi_core	DPHY_TEST_IN[13]	anatop	ANATOP_TESTO[10]
SD3_DAT5	ALT5	usdhc3	DAT5	uart2	TXD_MUX	pcie_ctrl	DIAG_STATUS_BUS_MUX[26]	usboh3	UH3_DFD_OUT[2]	usboh3	UH2_DFD_OUT[2]	gpio7	GPIO[0]	mipi_core	DPHY_TEST_IN[14]	anatop	ANATOP_TESTO[11]
SD3_DAT4	ALT5	usdhc3	DAT4	uart2	RXD_MUX	pcie_ctrl	DIAG_STATUS_BUS_MUX[27]	usboh3	UH3_DFD_OUT[3]	usboh3	UH2_DFD_OUT[3]	gpio7	GPIO[1]	mipi_core	DPHY_TEST_IN[15]	anatop	ANATOP_TESTO[12]
SD3_CMD	ALT5	usdhc3	CMD	uart2	CTS	can1	TXCAN	usboh3	UH3_DFD_OUT[4]	usboh3	UH2_DFD_OUT[4]	gpio7	GPIO[2]	mipi_core	DPHY_TEST_IN[16]	anatop	ANATOP_TESTO[13]
SD3_CLK	ALT5	usdhc3	CLK	uart2	RTS	can1	RXCAN	usboh3	UH3_DFD_OUT[5]	usboh3	UH2_DFD_OUT[5]	gpio7	GPIO[3]	mipi_core	DPHY_TEST_IN[17]	anatop	ANATOP_TESTO[14]
SD3_DAT0	ALT5	usdhc3	DAT0	uart1	CTS	can2	TXCAN	usboh3	UH3_DFD_OUT[6]	usboh3	UH2_DFD_OUT[6]	gpio7	GPIO[4]	mipi_core	DPHY_TEST_IN[18]	anatop	ANATOP_TESTO[15]
SD3_DAT1	ALT5	usdhc3	DAT1	uart1	RTS	can2	RXCAN	usboh3	UH3_DFD_OUT[7]	usboh3	UH2_DFD_OUT[7]	gpio7	GPIO[5]	mipi_core	DPHY_TEST_IN[19]	anatop	ANATOP_TESTI[0]
SD3_DAT2	ALT5	usdhc3	DAT2			pcie_ctrl	DIAG_STATUS_BUS_MUX[28]	usboh3	UH3_DFD_OUT[8]	usboh3	UH2_DFD_OUT[8]	gpio7	GPIO[6]	mipi_core	DPHY_TEST_IN[20]	anatop	ANATOP_TESTI[1]
SD3_DAT3	ALT5	usdhc3	DAT3	uart3	CTS	pcie_ctrl	DIAG_STATUS_BUS_MUX[29]	usboh3	UH3_DFD_OUT[9]	usboh3	UH2_DFD_OUT[9]	gpio7	GPIO[7]	mipi_core	DPHY_TEST_IN[21]	anatop	ANATOP_TESTI[2]
SD3_RST	ALT5	usdhc3	RST	uart3	RTS	pcie_ctrl	DIAG_STATUS_BUS_MUX[30]	usboh3	UH3_DFD_OUT[10]	usboh3	UH2_DFD_OUT[10]	gpio7	GPIO[8]	mipi_core	DPHY_TEST_IN[22]	anatop	ANATOP_TESTI[3]
NANDF_CLE	ALT5	rawnand	CLE	ipu2	SISG[4]	pcie_ctrl	DIAG_STATUS_BUS_MUX[31]	usboh3	UH3_DFD_OUT[11]	usboh3	UH2_DFD_OUT[11]	gpio6	GPIO[7]	mipi_core	DPHY_TEST_IN[23]	tpsmp	HTRANS[0]
NANDF_ALE	ALT5	rawnand	ALE	usdhc4	RST	pcie_ctrl	DIAG_STATUS_BUS_MUX[0]	usboh3	UH3_DFD_OUT[12]	usboh3	UH2_DFD_OUT[12]	gpio6	GPIO[8]	mipi_core	DPHY_TEST_IN[24]	tpsmp	HTRANS[1]
NANDF_WP_B	ALT5	rawnand	RESETN	ipu2	SISG[5]	pcie_ctrl	DIAG_STATUS_BUS_MUX[1]	usboh3	UH3_DFD_OUT[13]	usboh3	UH2_DFD_OUT[13]	gpio6	GPIO[9]	mipi_core	DPHY_TEST_OUT[32]	pl301_mx63per1	HSIZE[0]
NANDF_RB0	ALT5	rawnand	READY0	ipu2	DI0_PIN1	pcie_ctrl	DIAG_STATUS_BUS_MUX[2]	usboh3	UH3_DFD_OUT[14]	usboh3	UH2_DFD_OUT[14]	gpio6	GPIO[10]	mipi_core	DPHY_TEST_OUT[33]	pl301_mx63per1	HSIZE[1]
NANDF_CS0	ALT5	rawnand	CE0N					usboh3	UH3_DFD_OUT[15]	usboh3	UH2_DFD_OUT[15]	gpio6	GPIO[11]			pl301_mx63per1	HSIZE[2]
NANDF_CS1	ALT5	rawnand	CE1N	usdhc4	VSELECT	usdhc3	VSELECT			pcie_ctrl	DIAG_STATUS_BUS_MUX[3]	gpio6	GPIO[14]			pl301_mx63per1	HREADYOUT
NANDF_CS2	ALT5	rawnand	CE2N	ipu1	SISG[0]	esai1	TX0	weim	WEIM_CRE	ccm	CLKO2	gpio6	GPIO[15]	ipu2	SISG[0]		
NANDF_CS3	ALT5	rawnand	CE3N	ipu1	SISG[1]	esai1	TX1	weim	WEIM_A[26]	pcie_ctrl	DIAG_STATUS_BUS_MUX[4]	gpio6	GPIO[16]	ipu2	SISG[1]	tpsmp	CLK
SD4_CMD	ALT5	usdhc4	CMD	rawnand	RDN	uart3	TXD_MUX			pcie_ctrl	DIAG_STATUS_BUS_MUX[5]	gpio7	GPIO[9]			tpsmp	HDATA_DIR
SD4_CLK	ALT5	usdhc4	CLK	rawnand	WRN	uart3	RXD_MUX			pcie_ctrl	DIAG_STATUS_BUS_MUX[6]	gpio7	GPIO[10]				
NANDF_D0	ALT5	rawnand	D0	usdhc1	DAT4	gpu3d	GPU_DEBUG_OUT[0]	usboh3	UH2_DFD_OUT[16]	usboh3	UH3_DFD_OUT[16]	gpio2	GPIO[0]	ipu1	IPU_DIAG_BUS[0]	ipu2	IPU_DIAG_BUS[0]
NANDF_D1	ALT5	rawnand	D1	usdhc1	DAT5	gpu3d	GPU_DEBUG_OUT[1]	usboh3	UH2_DFD_OUT[17]	usboh3	UH3_DFD_OUT[17]	gpio2	GPIO[1]	ipu1	IPU_DIAG_BUS[1]	ipu2	IPU_DIAG_BUS[1]
NANDF_D2	ALT5	rawnand	D2	usdhc1	DAT6	gpu3d	GPU_DEBUG_OUT[2]	usboh3	UH2_DFD_OUT[18]	usboh3	UH3_DFD_OUT[18]	gpio2	GPIO[2]	ipu1	IPU_DIAG_BUS[2]	ipu2	IPU_DIAG_BUS[2]
NANDF_D3	ALT5	rawnand	D3	usdhc1	DAT7	gpu3d	GPU_DEBUG_OUT[3]	usboh3	UH2_DFD_OUT[19]	usboh3	UH3_DFD_OUT[19]	gpio2	GPIO[3]	ipu1	IPU_DIAG_BUS[3]	ipu2	IPU_DIAG_BUS[3]
NANDF_D4	ALT5	rawnand	D4	usdhc2	DAT4	gpu3d	GPU_DEBUG_OUT[4]	usboh3	UH2_DFD_OUT[20]	usboh3	UH3_DFD_OUT[20]	gpio2	GPIO[4]	ipu1	IPU_DIAG_BUS[4]	ipu2	IPU_DIAG_BUS[4]
NANDF_D5	ALT5	rawnand	D5	usdhc2	DAT5	gpu3d	GPU_DEBUG_OUT[5]	usboh3	UH2_DFD_OUT[21]	usboh3	UH3_DFD_OUT[21]	gpio2	GPIO[5]	ipu1	IPU_DIAG_BUS[5]	ipu2	IPU_DIAG_BUS[5]
NANDF_D6	ALT5	rawnand	D6	usdhc2	DAT6	gpu3d	GPU_DEBUG_OUT[6]	usboh3	UH2_DFD_OUT[22]	usboh3	UH3_DFD_OUT[22]	gpio2	GPIO[6]	ipu1	IPU_DIAG_BUS[6]	ipu2	IPU_DIAG_BUS[6]
NANDF_D7	ALT5	rawnand	D7	usdhc2	DAT7	gpu3d	GPU_DEBUG_OUT[7]	usboh3	UH2_DFD_OUT[23]	usboh3	UH3_DFD_OUT[23]	gpio2	GPIO[7]	ipu1	IPU_DIAG_BUS[7]	ipu2	IPU_DIAG_BUS[7]
SD4_DAT0	ALT5	rawnand	D8	usdhc4	DAT0	rawnand	DQS	usboh3	UH2_DFD_OUT[24]	usboh3	UH3_DFD_OUT[24]	gpio2	GPIO[8]	ipu1	IPU_DIAG_BUS[8]	ipu2	IPU_DIAG_BUS[8]
SD4_DAT1	ALT5	rawnand	D9	usdhc4	DAT1	pwm3	PWMO	usboh3	UH2_DFD_OUT[25]	usboh3	UH3_DFD_OUT[25]	gpio2	GPIO[9]	ipu1	IPU_DIAG_BUS[9]	ipu2	IPU_DIAG_BUS[9]
SD4_DAT2	ALT5	rawnand	D10	usdhc4	DAT2	pwm4	PWMO	usboh3	UH2_DFD_OUT[26]	usboh3	UH3_DFD_OUT[26]	gpio2	GPIO[10]	ipu1	IPU_DIAG_BUS[10]	ipu2	IPU_DIAG_BUS[10]
SD4_DAT3	ALT5	rawnand	D11	usdhc4	DAT3			usboh3	UH2_DFD_OUT[27]	usboh3	UH3_DFD_OUT[27]	gpio2	GPIO[11]	ipu1	IPU_DIAG_BUS[11]	ipu2	IPU_DIAG_BUS[11]
SD4_DAT4	ALT5	rawnand	D12	usdhc4	DAT4	uart2	RXD_MUX	usboh3	UH2_DFD_OUT[28]	usboh3	UH3_DFD_OUT[28]	gpio2	GPIO[12]	ipu1	IPU_DIAG_BUS[12]	ipu2	IPU_DIAG_BUS[12]
SD4_DAT5	ALT5	rawnand	D13	usdhc4	DAT5	uart2	RTS	usboh3	UH2_DFD_OUT[29]	usboh3	UH3_DFD_OUT[29]	gpio2	GPIO[13]	ipu1	IPU_DIAG_BUS[13]	ipu2	IPU_DIAG_BUS[13]
SD4_DAT6	ALT5	rawnand	D14	usdhc4	DAT6	uart2	CTS	usboh3	UH2_DFD_OUT[30]	usboh3	UH3_DFD_OUT[30]	gpio2	GPIO[14]	ipu1	IPU_DIAG_BUS[14]	ipu2	IPU_DIAG_BUS[14]
SD4_DAT7	ALT5	rawnand	D15	usdhc4	DAT7	uart2	TXD_MUX	usboh3	UH2_DFD_OUT[31]	usboh3	UH3_DFD_OUT[31]	gpio2	GPIO[15]	ipu1	IPU_DIAG_BUS[15]	ipu2	IPU_DIAG_BUS[15]
SD1_DAT1	ALT5	usdhc1	DAT1	ecspi5	SS0	pwm3	PWMO	gpt	CAPIN2	pcie_ctrl	DIAG_STATUS_BUS_MUX[7]	gpio1	GPIO[17]	hdmi_tx	OPHYDTB[0]	anatop	ANATOP_TESTO[8]
SD1_DAT0	ALT5	usdhc1	DAT0	ecspi5	MISO	caam_wrapper	RNG_OSC_OBS	gpt	CAPIN1	pcie_ctrl	DIAG_STATUS_BUS_MUX[8]	gpio1	GPIO[16]	hdmi_tx	OPHYDTB[1]	anatop	ANATOP_TESTO[7]
SD1_DAT3	ALT5	usdhc1	DAT3	ecspi5	SS2	gpt	CMPOUT3	pwm1	PWMO	wdog2	WDOG_B	gpio1	GPIO[21]	wdog2	WDOG_RST_B_DEB	anatop	ANATOP_TESTO[6]
SD1_CMD	ALT5	usdhc1	CMD	ecspi5	MOSI	pwm4	PWMO	gpt	CMPOUT1			gpio1	GPIO[18]			anatop	ANATOP_TESTO[5]
SD1_DAT2	ALT5	usdhc1	DAT2	ecspi5	SS1	gpt	CMPOUT2	pwm2	PWMO	wdog1	WDOG_B	gpio1	GPIO[19]	wdog1	WDOG_RST_B_DEB	anatop	ANATOP_TESTO[4]
SD1_CLK	ALT5	usdhc1	CLK	ecspi5	SCLK	osc32k	32K_OUT	gpt	CLKIN			gpio1	GPIO[20]	phy	DTB[0]	sata_phy	DTB[0]
SD2_CLK	ALT5	usdhc2	CLK	ecspi5	SCLK	kpp	COL[5]	audmux	AUD4_RXFS	pcie_ctrl	DIAG_STATUS_BUS_MUX[9]	gpio1	GPIO[10]	phy	DTB[1]	sata_phy	DTB[1]
SD2_CMD	ALT5	usdhc2	CMD	ecspi5	MOSI	kpp	ROW[5]	audmux	AUD4_RXC	pcie_ctrl	DIAG_STATUS_BUS_MUX[10]	gpio1	GPIO[11]				
SD2_DAT3	ALT5	usdhc2	DAT3	ecspi5	SS3	kpp	COL[6]	audmux	AUD4_TXC	pcie_ctrl	DIAG_STATUS_BUS_MUX[11]	gpio1	GPIO[12]	sjc	DONE	anatop	ANATOP_TESTO[3]

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