FMN1xx5SBS(130ball) Datasheet

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Document Title

Stacked Multi-Chip Product(MCP)

Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	May. 21st, 2013	Preliminary

Stacked Multi-Chip Product(MCP)

1.8V NAND Flash Memory and Mobile SDR/DDR

1. MCP Features

- Supply Voltages : 1.8V Operation
  - VCC : 1.7V~1.95V for Core/IO Power
- Operating Temperature Range
  - Industrial Part : -40˚C ~ 85˚C
- Package Type :
  - 130-ball FBGA, 8x9mm^2, 1.0T, 0.65mm Ball Pitch
  - Lead & Halogen Free

2. MCP Selection Guide

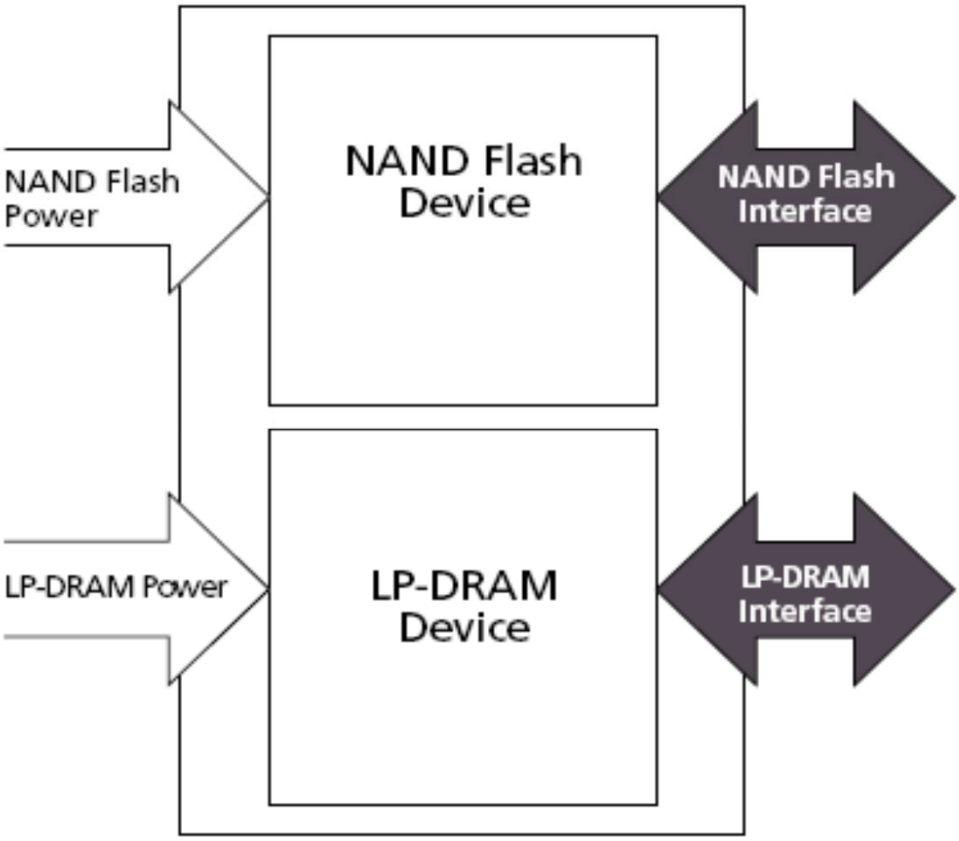
[1G NAND + 512Mb DDR SDRAM]

MCP Part Number	Flash	LP-DRAM	DRAM Freq.	Individual Datasheet		PKG Type
				Flash	LP-DRAM	
FMN1ED5SBS-50IA	1Gb(x8)	512Mb(x16)	200Mhz	FMND1G08S3S	FMD8C16LAW-25EI	130ball
FMN1SD5SBS-50IA	1Gb(x16)	512Mb(x16)	200Mhz	FMND1G16S3S	FMD8C16LAW-25EI	130ball

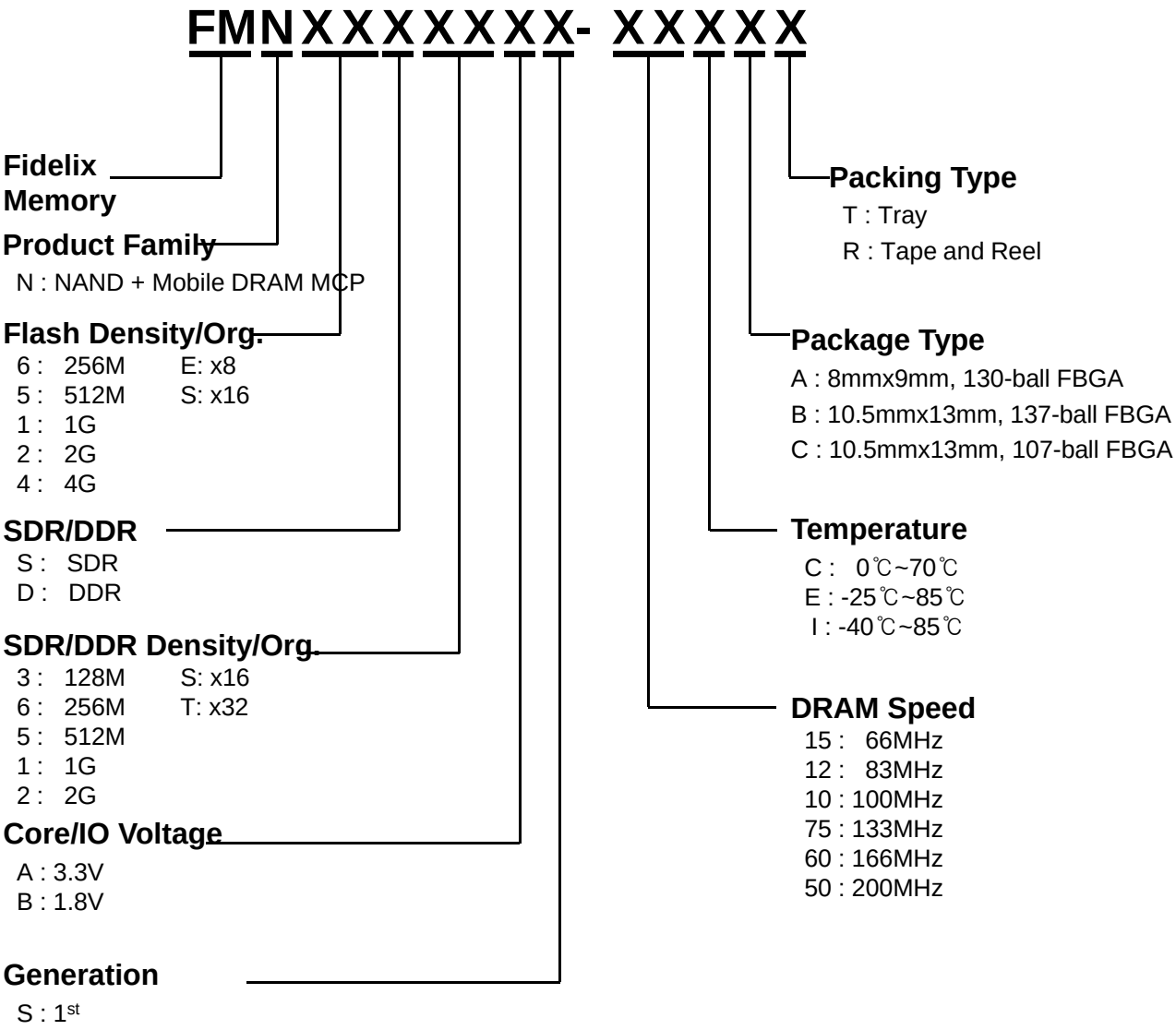
[1G NAND + 512Mb SDR SDRAM]

MCP Part Number	Flash	LP-DRAM	DRAM Freq.	Individual Datasheet		PKG Type
				Flash	LP-DRAM	
FMN1ES5SBS-60IA	1Gb(x8)	512Mb(x16)	166Mhz	FMND1G08S3S	FMS8C16LAW-60EI	130ball
FMN1SS5SBS-60IA	1Gb(x16)	512Mb(x16)	166Mhz	FMND1G16S3S	FMS8C16LAW-60EI	130ball

3. MCP Block Diagram

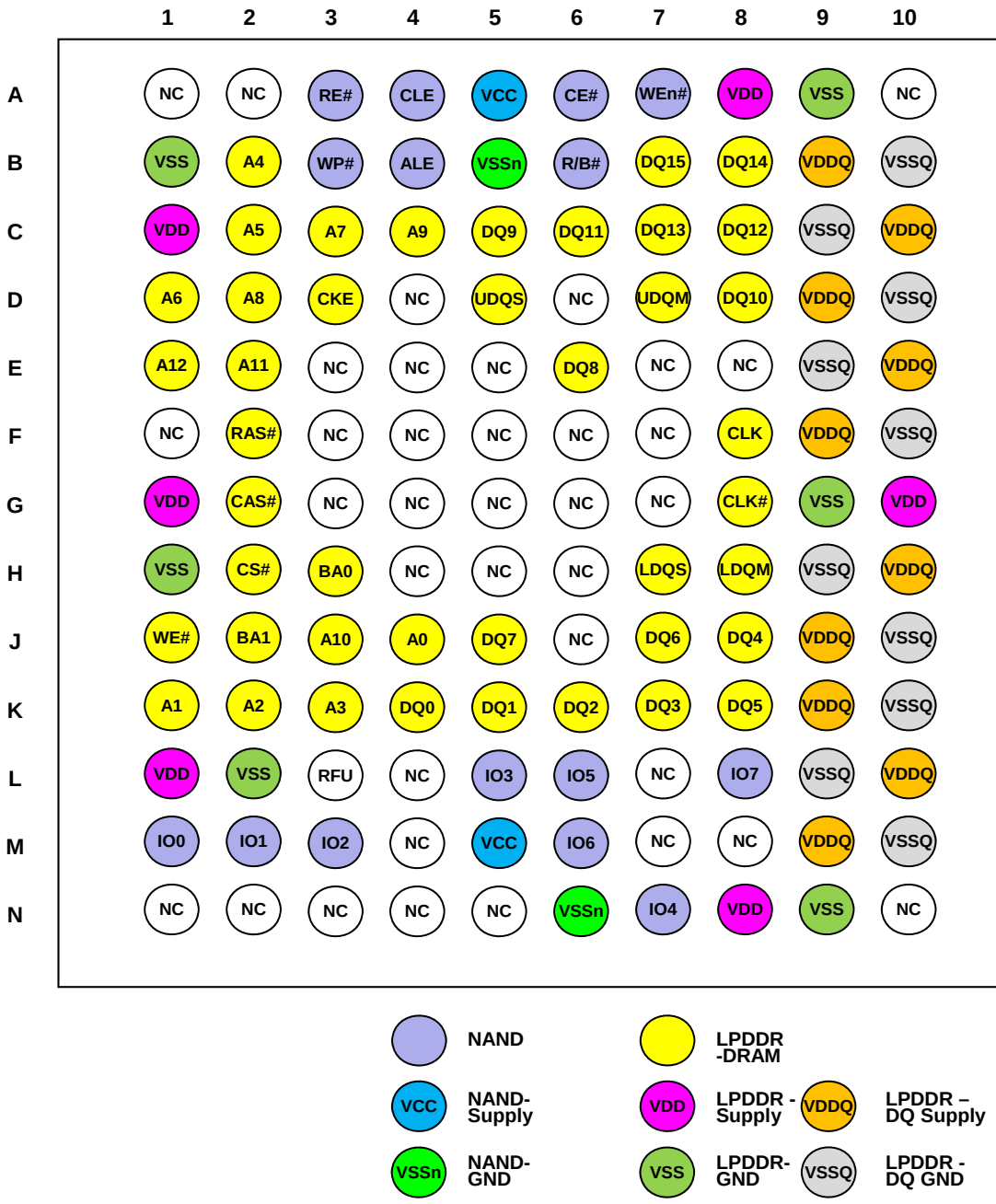


4. MCP Part Numbering System



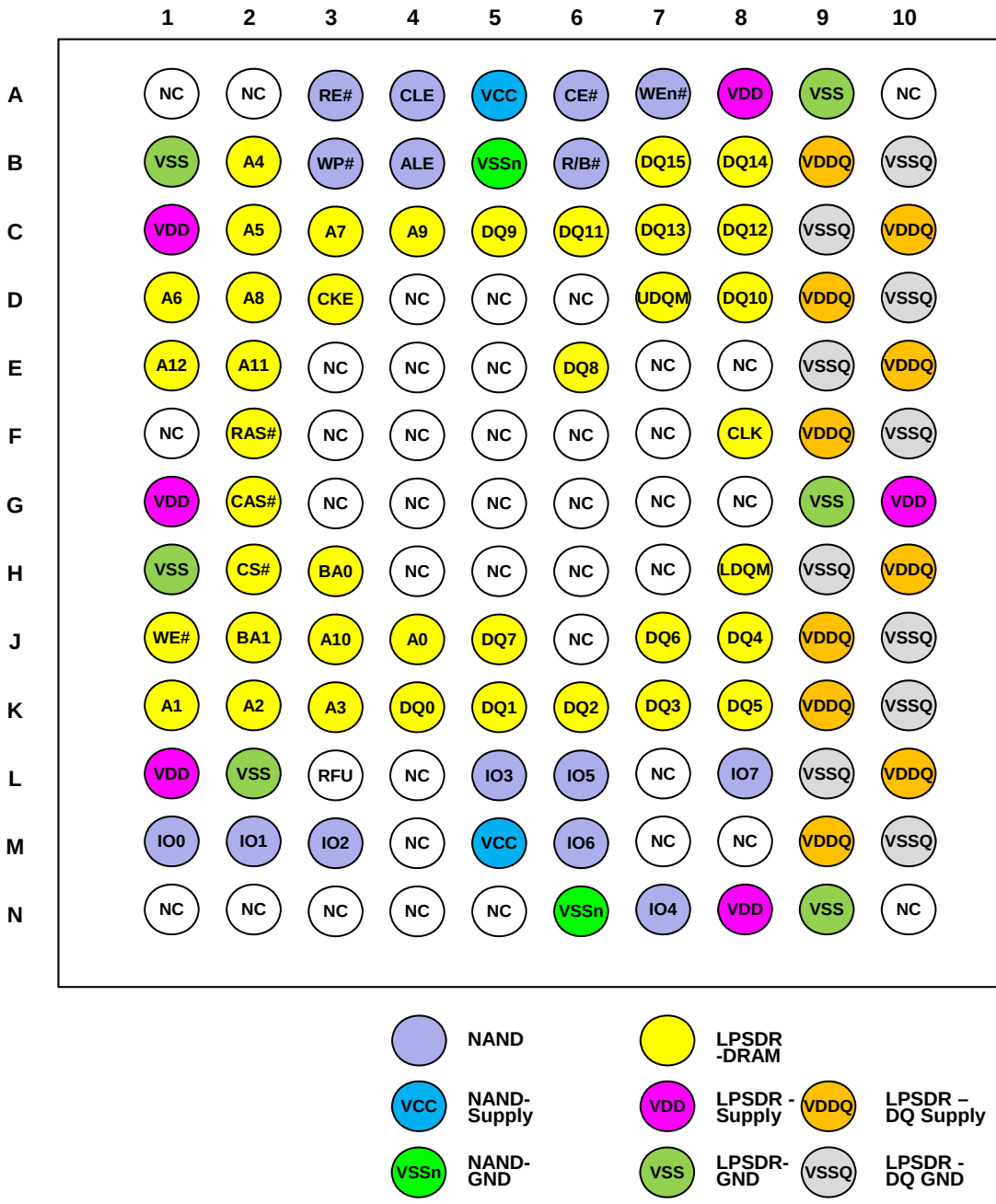
5-1. MCP Package Pin Configuration (130-ball FBGA, Top View)

NAND(x8) + DDR(x16)



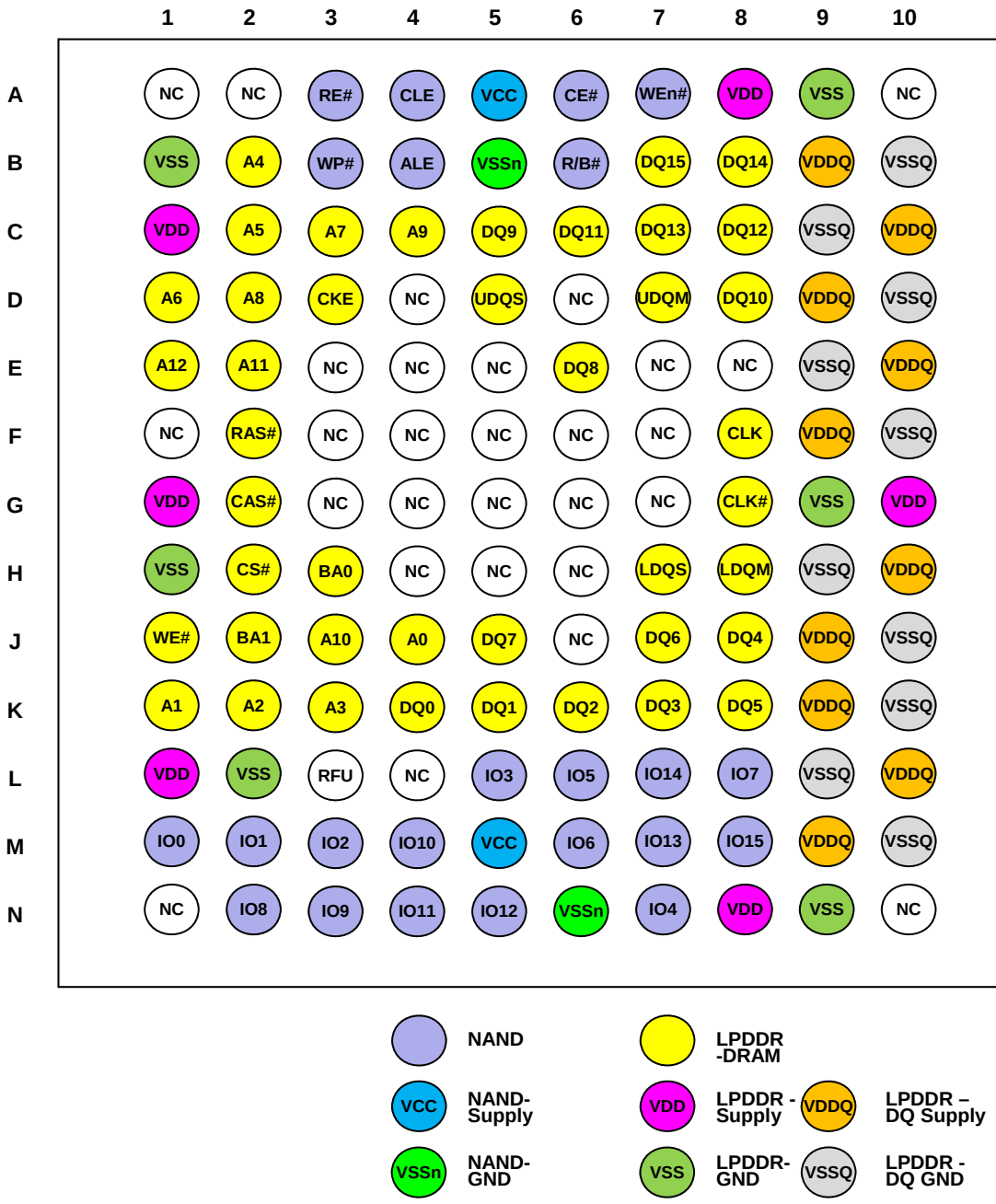
5-2. MCP Package Pin Configuration (130-ball FBGA, Top View)

NAND(x8) + SDR(x16)



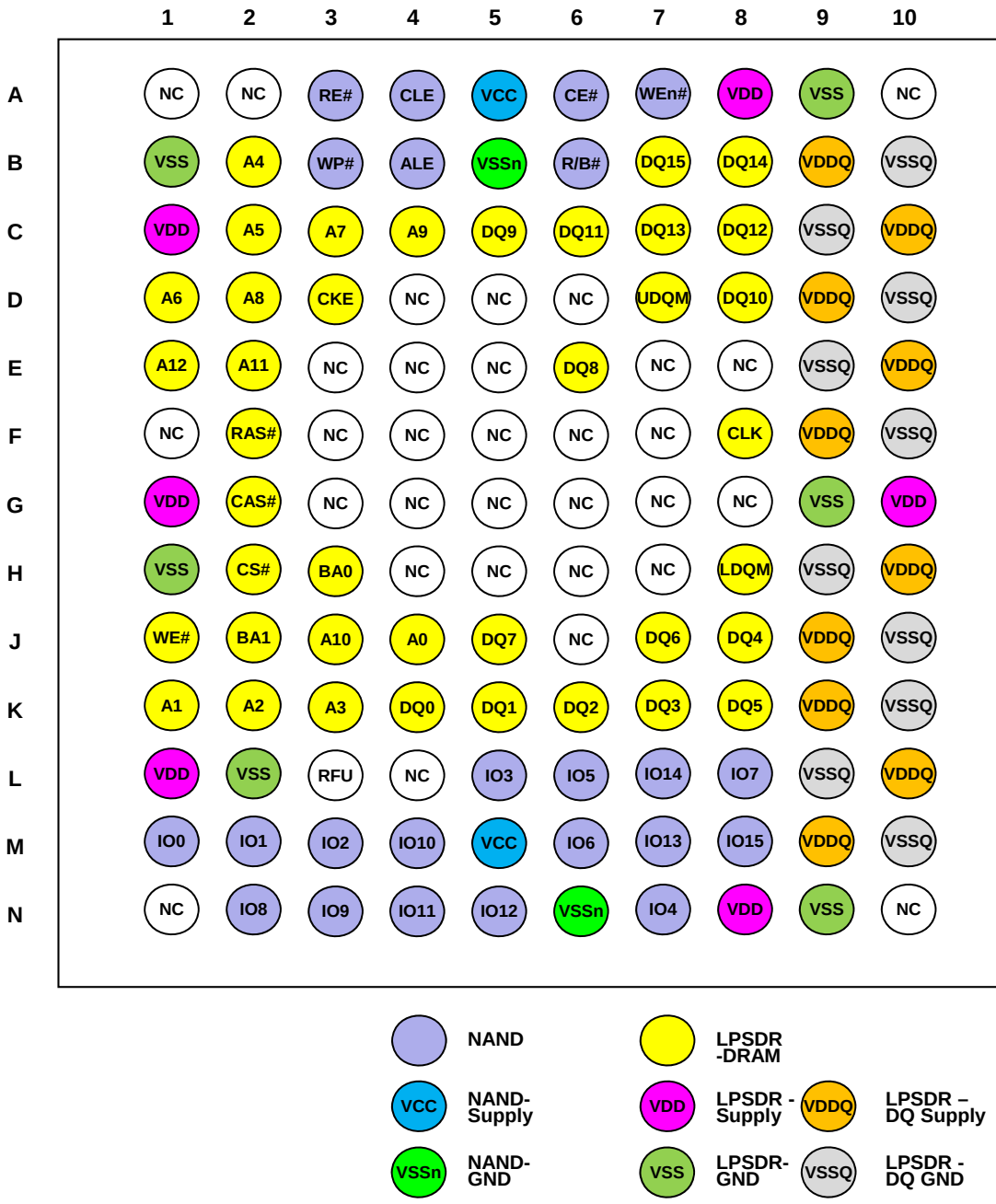
5-3. MCP Package Pin Configuration (130-ball FBGA, Top View)

NAND(x16) + DDR(x16)

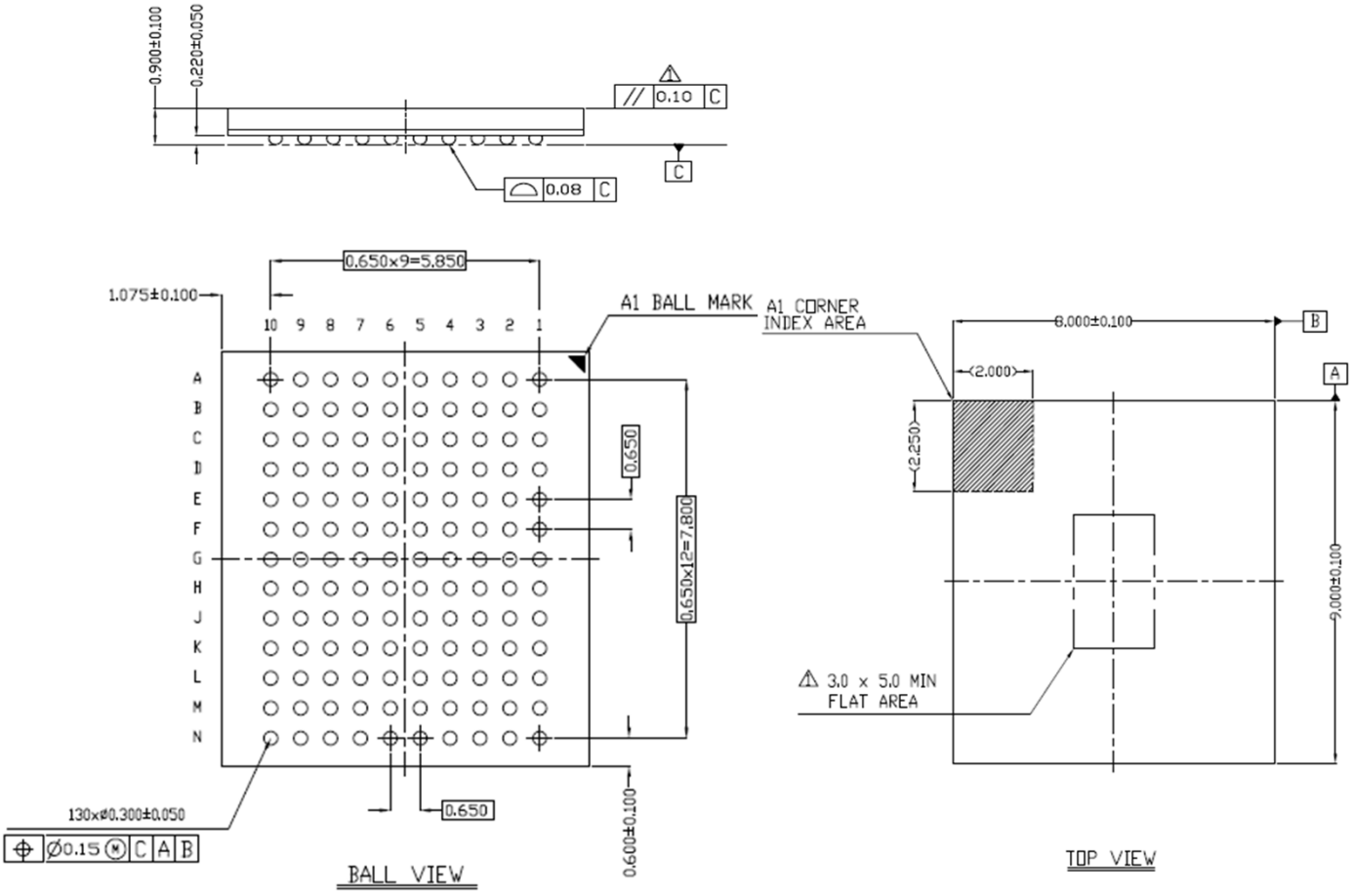


5-4. MCP Package Pin Configuration (130-ball FBGA, Top View)

NAND(x16) + SDR(x16)



5-5. 130-ball FBGA Package Dimension (8mm x 9mm)



SLC NAND FLASH

Document Title

1Gbit, 4Gbit SLC NAND FLASH

Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	May. 20th , 2013	Preliminary
0.1	Editorial Correction	Jun. 04th , 2013	Preliminary

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Distinctive Characteristics

- **Density**
  - 1 Gbit / 2 Gbit / 4 Gbit
- **Architecture**
  - Input / Output Bus Width: 8-bits / 16-bits
  - Page Size:
    - x8
      1 Gbit: (2048 + 64) bytes; 64-byte spare area
      2,4 Gbit: (2048 + 128) bytes; 128-byte spare area
    - x16
      1 Gbit: (1024 + 32) words; 32-word spare area
      2,4 Gbit: (1024 + 64) words; 64-word spare area
  - Block Size: 64 Pages
    - x8
      1 Gbit: (128k + 4k) bytes
      2,4 Gbit: (128k + 8k) bytes
    - x16
      1 Gbit: (64k + 2k) words
      2,4 Gbit: (64k + 4k) words
  - Plane Size:
    - x8
      1 Gbit: 1024 Blocks per Plane or (128M + 4M) bytes
      2 Gbit: 1024 Blocks per Plane or (128M + 8M) bytes
      4 Gbit: 2048 Blocks per Plane or (256M + 16M) bytes
    - x16
      1 Gbit: 1024 Blocks per Plane or (64M + 2M) words
      2 Gbit: 1024 Blocks per Plane or (64M + 4M) words
      4 Gbit: 2048 Blocks per Plane or (128M + 8M) words
  - Device Size:
    - 1 Gbit: 1 Plane per Device or 128 Mbyte
    - 2 Gbit: 2 Planes per Device or 256 Mbyte
    - 4 Gbit: 2 Planes per Device or 512 Mbyte
- **NAND Flash Interface**
  - Open NAND Flash Interface (ONFI) 1.0 compliant
  - Address, Data, and Commands multiplexed
- **Supply Voltage**
  - 1.8V device: VCC = 1.7V ~ 1.95V
- **Security**
  - One Time Programmable (OTP) area
  - Serial number (unique ID)
  - Hardware program/erase disabled during power transition
- **Additional Features**
  - 2Gb and 4 Gb parts support Multiplane Program and Erase commands
  - Supports Copy Back Program
  - 2/4 Gb parts support Multiplane Copy Back Program
  - Supports Read Cache
- **Electronic Signature**
  - Manufacturer ID: 01h
- **Operating Temperature**
  - Commercial: 0°C to 70°C
  - Extended: -30°C to 85°C
  - Industrial: -40°C to 85°C

Performance

- **Page Read / Program**
  - Random access: 25 µs (Max) (FMND1GxxS3S)
  - Random access: 30 µs (Max) (FMND2GxxS3S/FMND4GxxS3S)
  - Sequential access: 45 ns (Min)
  - Program time / Multiplane Program time: 300 µs (Typ)
- **Block Erase**
  - Block Erase time: 3.0 ms (Typ)
- **Block Erase / Multiplane Erase**
  (FMND2GxxS3S, FMND4GxxS3S)
  - Block Erase time: 3.5 ms (Typ)
- **Reliability**
  - 100,000 Program / Erase cycles (Typ)
    (with 4-bit ECC per 528 bytes (x8) or 264 words (x16))
  - 10 Year Data retention (Typ)
  - Block zero is a valid block and will be valid for at least 1000 program-erase cycles with ECC
- **Package Options**
  - 48-Pin TSOP 12 x 20 x 1.2 mm
  - 48-Ball BGA 9 x 9 x 1 mm

1. GENERAL DESCRIPTION

The Fidelix FMND1GxxS3S, FMND2GxxS3S, and FMND4GxxS3S series is offered in 1.8 VCC and VCCQ power supply, and with x8 or x16 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. The page size for x8 is (2048 + spare) bytes; for x16 (1024 + spare) words.

Each block can be programmed and erased up to 100,000 cycles with ECC (error correction code) on. To extend the lifetime of NAND flash devices, the implementation of an ECC is mandatory.

The chip supports CE# don't care function. This function allows the direct download of the code from the NAND flash memory device by a microcontroller, since the CE# transitions do not stop the read operation.

The devices have a Read Cache feature that improves the read throughput for large files. During cache reading, the devices load the data in a cache register while the previous data is transferred to the I/O buffers to be read.

Like all other 2-kB page NAND flash devices, a program operation typically writes 2 kbytes (x8), or 1 kword (x16) in 300 µs and an erase operation can typically be performed in 3 ms (FMND1GxxS3S) on a 128-kB block (x8) or 64-kword block (x16). In addition, thanks to multiplane architecture, it is possible to program two pages at a time (one per plane) or to erase two blocks at a time (again, one per plane). The multiplane architecture allows program time to be reduced by 40% and erase time to be reduced by 50%.

In multiplane operations, data in the page can be read out at 45 ns cycle time per byte. The I/O pins serve as the ports for command and address input as well as data input/output. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of the footprint.

Commands, Data, and Addresses are asynchronously introduced using CE#, WE#, ALE, and CLE control pins.

The on-chip Program/Erase Controller automates all read, program, and erase functions including pulse repetition, where required, and internal verification and margining of data. A WP# pin is available to provide hardware protection against program and erase operations.

The output pin R/B# (open drain buffer) signals the status of the device during each operation. It identifies if the program/erase/read controller is currently active. The use of an open-drain output allows the Ready/Busy pins from several memories to connect to a single pull-up resistor. In a system with multiple memories the R/B# pins can be connected all together to provide a global status signal.

The Reprogram function allows the optimization of defective block management — when a Page Program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

Multiplane Copy Back is also supported. Data read out after Copy Back Read (both for single and multiplane cases) is allowed.

In addition, Cache Program and Multiplane Cache Program operations improve the programing throughput by programing data using the cache register.

The devices provide two innovative features: Page Reprogram and Multiplane Page Reprogram. The Page Reprogram re-programs one page. Normally, this operation is performed after a failed Page Program operation. Similarly, the Multiplane Page Reprogram re-programs two pages in parallel, one per plane. The first page must be in the first plane while the second page must be in the second plane. The Multiplane Page Reprogram operation is performed after a failed Multiplane Page Program operation. The Page Reprogram and Multiplane Page Reprogram guarantee improved performance, since data insertion can be omitted during re-program operations.

The devices come with the following security features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently.
- Serial number (unique identifier), which allows the devices to be uniquely identified.

These security features are subject to an NDA (non-disclosure agreement) and are, therefore, not described in the data sheet. For more details about them, contact your nearest Fidelix sales office.

Device	Density (bits)		Number of Planes	Number of Blocks per Plane
	Main	Spare		
FMND1GxxS3S	128M x 8 64M x 16	4M x 8 2M x 16	1	1024
FMND2GxxS3S	256M x 8 128M x 16	16M x 8 8M x 16	2	1024
FMND4GxxS3S	512M x 8 256M x 16	32M x 8 16M x 16	2	2048

1.1 Logic Diagram

Figure 1.1 Logic Diagram

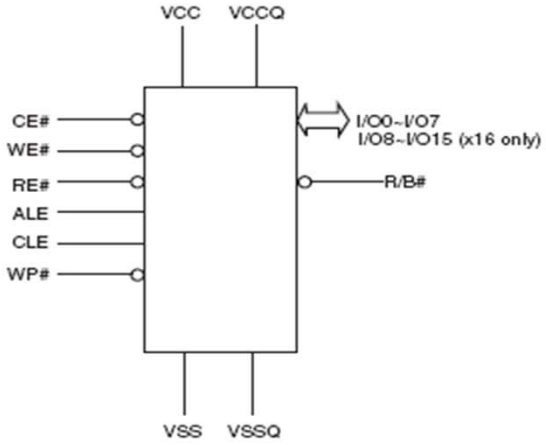


Table 1.1 Signal Names

I/O7 - I/O0 (x8)	Data Input / Outputs
I/O8 - I/O15 (x16)	
CLE	Command Latch Enable
ALE	Address Latch Enable
CE#	Chip Enable
RE#	Read Enable
WE#	Write Enable
WP#	Write Protect
R/B#	Read/Busy
VCC	Power Supply
VSS	Ground
NC	Not Connected

1.2 Connection Diagram

Figure 1.2 48-Pin TSOP1 Contact x8, x16 Devices

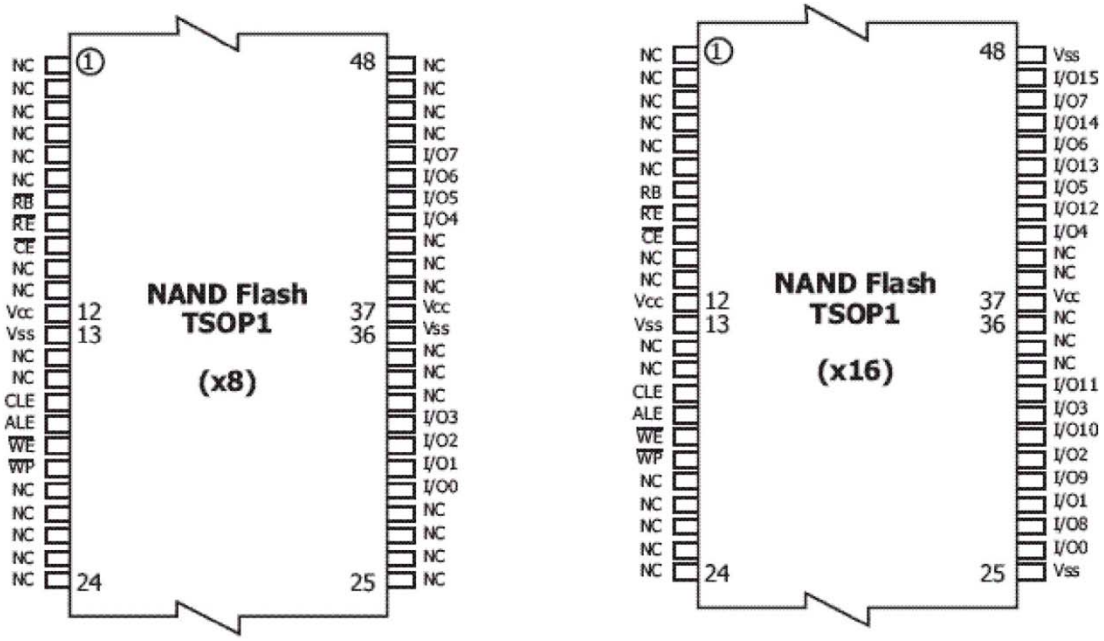


Figure 1.3 48-BGA Contact, x8 Device
(Balls Down, Top View)

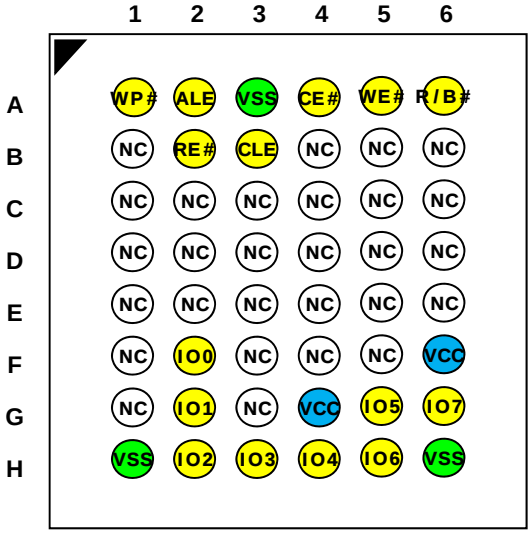
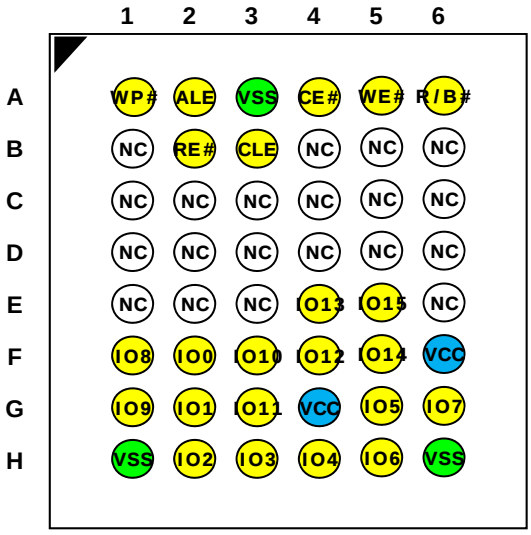


Figure 1.4 48-BGA Contact, x16 Device
(Balls Down, Top View)



1.3 Pin Description

Table 1.2 Pin Description

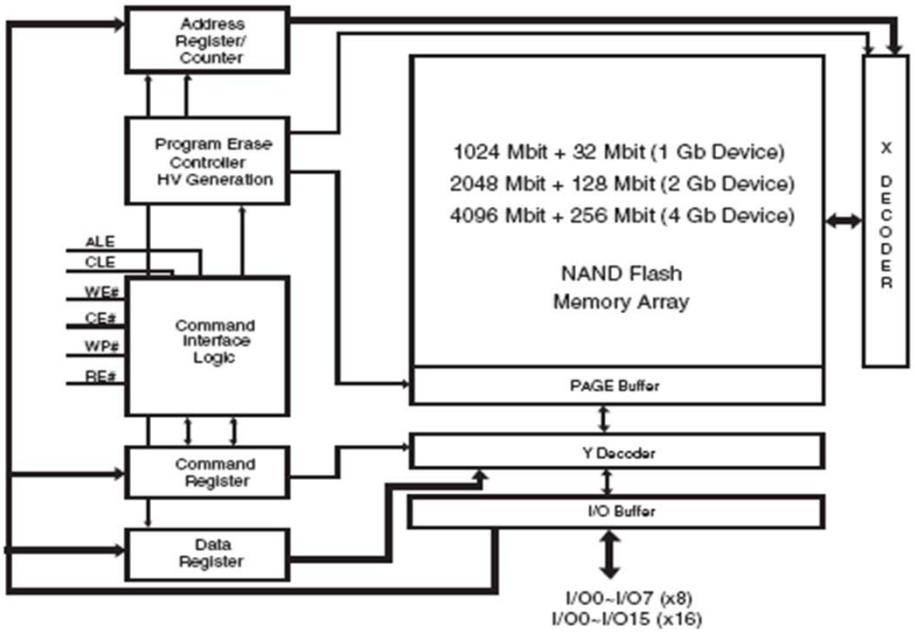
Pin Name	Description
I/O0 - I/O7 (x8) I/O8 - I/O15 (x16)	**Inputs/Outputs**. The I/O pins are used for command input, address input, data input, and data output. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
CLE	**Command Latch Enable.** This input activates the latching of the I/O inputs inside the Command Register on the rising edge of Write Enable (WE#).
ALE	**Address Latch Enable.** This input activates the latching of the I/O inputs inside the Address Register on the rising edge of Write Enable (WE#).
CE#	**Chip Enable.** This input controls the selection of the device. When the device is not busy CE# low selects the memory.
WE#	**Write Enable.** This input latches Command, Address and Data. The I/O inputs are latched on the rising edge of WE#.
RE#	**Read Enable.** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WP#	**Write Protect.** The WP# pin, when low, provides hardware protection against undesired data modification (program / erase).
R/B#	**Ready Busy**. The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	**Supply Voltage**. The V_{CC} supplies the power for all the operations (Read, Program, Erase). An internal lock circuit prevents the insertion of Commands when V_{CC} is less than V_{LKO}.
VSS	**Ground.**
NC	**Not Connected.**

Notes:

1. *A 0.1 µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.*
2. *An internal voltage detector disables all functions whenever V_{CC} is below 1.1V (1.8V device) to protect the device from any involuntary program/erase during power transitions.*

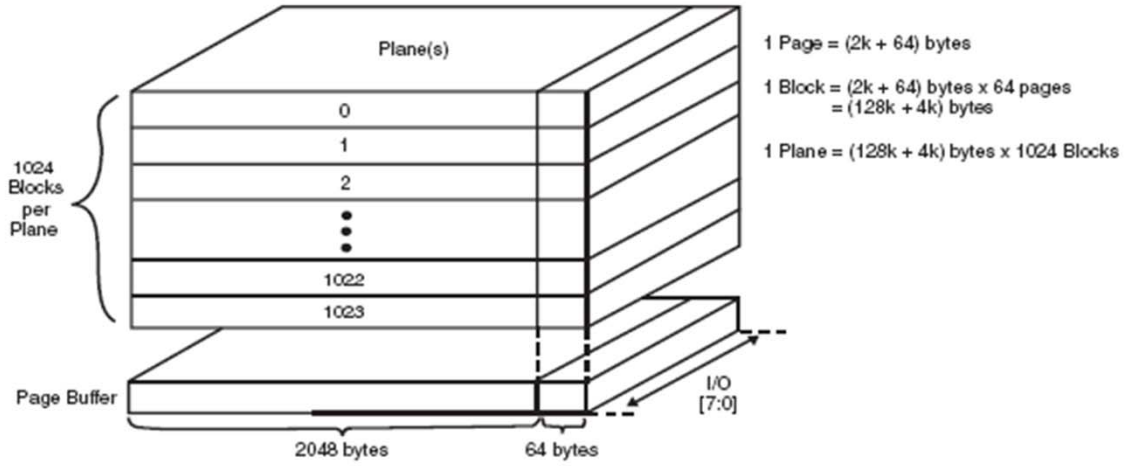
1.4 Block Diagram

Figure 1.5 Functional Block Diagram



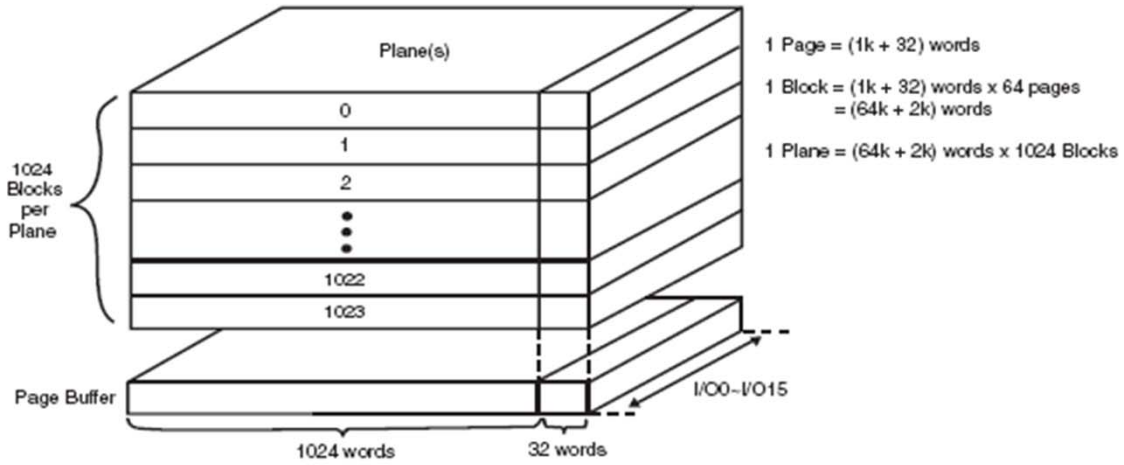
1.5 Array Organization

Figure 1.6 Array Organization – FMND1G08S3S (x8)



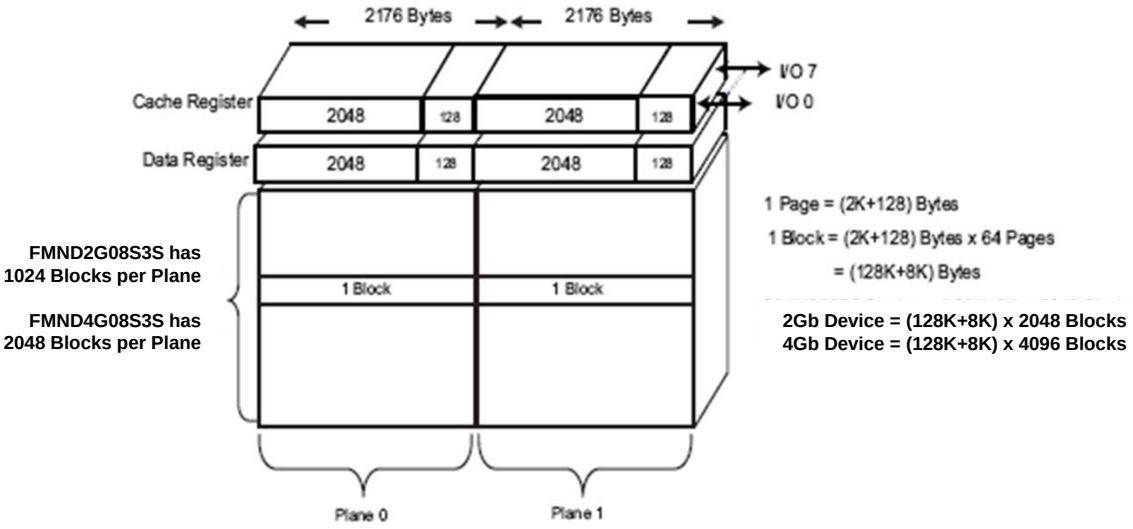
Array Organization (x8)

Figure 1.7 Array Organization – FMND1G16S3S (x16)



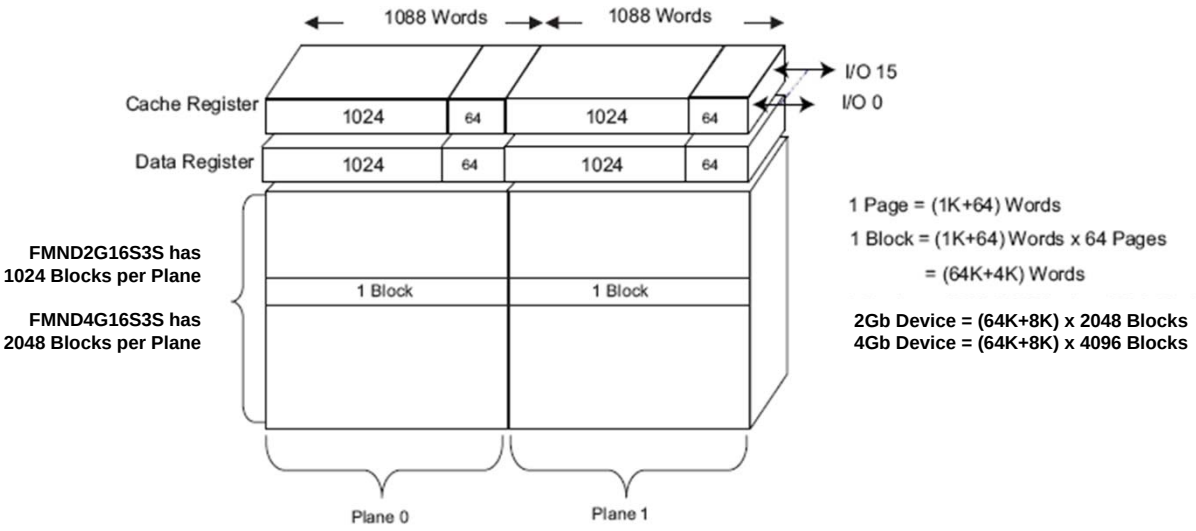
Array Organization (x16)

Figure 1.8 Array Organization – FMND2G08S3S and FMND4G08S3S (x8)



Array Organization (x8)

Figure 1.9 Array Organization – FMND2G16S3S and FMND4G16S3S (x16)



Array Organization(x16)

1.6 Addressing

1.6.1 FMND1GxxS3S

Table 1.3 Address Cycle Map — 1 Gb Device

Bus Cycle	I/O [15:8] (5)	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
x8									
1st	—	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd	—	A8 (CA8)	A9 (CA9)	A10 (CA10)	A11 (CA11)	Low	Low	Low	Low
3rd	—	A12 (PA0)	A13 (PA1)	A14 (PA2)	A15 (PA3)	A16 (PA4)	A17 (PA5)	A18 (BA0)	A19 (BA1)
4th	—	A20 (BA2)	A21 (BA3)	A22 (BA4)	A23 (BA5)	A24 (BA6)	A25 (BA7)	A26 (BA8)	A27 (BA9)
x16									
1st	Low	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd	Low	A8 (CA8)	A9 (CA9)	A10 (CA10)	Low	Low	Low	Low	Low
3rd	Low	A11 (PA0)	A12 (PA1)	A13 (PA2)	A14 (PA3)	A15 (PA4)	A16 (PA5)	A17 (BA0)	A18 (BA1)
4th	Low	A19 (BA2)	A20 (BA3)	A21 (BA4)	A22 (BA5)	A23 (BA6)	A24 (BA7)	A25 (BA8)	A26 (BA9)

Notes:

1. *CAx = Column Address bit.*
2. *PAx = Page Address bit.*
3. *BAx = Block Address bit.*
4. *Block address concatenated with page address = actual page address.*
5. *I/O[15:8] are not used during the addressing sequence and should be driven Low.*

For the x8 address bits, the following rules apply:

- A0 - A11: column address in the page
- A12 - A17: page address in the block
- A18 - A27: block address

For the x16 address bits, the following rules apply:

- A0 - A10: column address in the page
- A11 - A16: page address in the block
- A17 - A26: block address

1.6.2 FMND2GxxS3S

Table 1.4 Address Cycle Map — 2 Gb Device

Bus Cycle	I/O [15:8] (6)	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
x8									
1st	—	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd	—	A8 (CA8)	A9 (CA9)	A10 (CA10)	A11 (CA11)	Low	Low	Low	Low
3rd	—	A12 (PA0)	A13 (PA1)	A14 (PA2)	A15 (PA3)	A16 (PA4)	A17 (PA5)	A18 (PLA0)	A19 (BA0)
4th	—	A20 (BA1)	A21 (BA2)	A22 (BA3)	A23 (BA4)	A24 (BA5)	A25 (BA6)	A26 (BA7)	A27 (BA8)
5th	—	A28 (BA9)	Low	Low	Low	Low	Low	Low	Low
x16									
1st	Low	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd	Low	A8 (CA8)	A9 (CA9)	A10 (CA10)	Low	Low	Low	Low	Low
3rd	Low	A11 (PA0)	A12 (PA1)	A13 (PA2)	A14 (PA3)	A15 (PA4)	A16 (PA5)	A17 (PLA0)	A18 (BA0)
4th	Low	A19 (BA1)	A20 (BA2)	A21 (BA3)	A22 (BA4)	A23 (BA5)	A24 (BA6)	A25 (BA7)	A26 (BA8)
5th	Low	A27 (BA9)	Low	Low	Low	Low	Low	Low	Low

Notes:
1. *CAx = Column Address bit.*
2. *PAx = Page Address bit.*
3. *PLA0 = Plane Address bit zero.*
4. *BAx = Block Address bit.*
5. *Block address concatenated with page address and plane address = actual page address, also known as the row address.*
6. *I/O[15:8] are not used during the addressing sequence and should be driven Low.*

For the x8 address bits, the following rules apply:

- A0 - A11: column address in the page
- A12 - A17: page address in the block
- A18: plane address (for multiplane operations) / block address (for normal operations)
- A19 - A28: block address

For the x16 address bits, the following rules apply:

- A0 - A10: column address in the page
- A11 - A16: page address in the block
- A17: plane address (for multiplane operations) / block address (for normal operations)
- A18 - A27: block address

1.6.3 FMND4GxxS3S

Table 1.5 Address Cycle Map — 4 Gb Device

Bus Cycle	I/O [15:8] (6)	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
x8									
1st	—	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd	—	A8 (CA8)	A9 (CA9)	A10 (CA10)	A11 (CA11)	Low	Low	Low	Low
3rd	—	A12 (PA0)	A13 (PA1)	A14 (PA2)	A15 (PA3)	A16 (PA4)	A17 (PA5)	A18 (PLA0)	A19 (BA0)
4th	—	A20 (BA1)	A21 (BA2)	A22 (BA3)	A23 (BA4)	A24 (BA5)	A25 (BA6)	A26 (BA7)	A27 (BA8)
5th	—	A28 (BA9)	A29 (BA10)	Low	Low	Low	Low	Low	Low
x16									
1st	Low	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd	Low	A8 (CA8)	A9 (CA9)	A10 (CA10)	Low	Low	Low	Low	Low
3rd	Low	A11 (PA0)	A12 (PA1)	A13 (PA2)	A14 (PA3)	A15 (PA4)	A16 (PA5)	A17 (PLA0)	A18 (BA0)
4th	Low	A19 (BA1)	A20 (BA2)	A21 (BA3)	A22 (BA4)	A23 (BA5)	A24 (BA6)	A25 (BA7)	A26 (BA8)
5th	Low	A27 (BA9)	A28 (BA10)	Low	Low	Low	Low	Low	Low

Notes:
1. *CAx = Column Address bit.*
2. *PAx = Page Address bit.*
3. *PLA0 = Plane Address bit zero.*
4. *BAx = Block Address bit.*
5. *Block address concatenated with page address and plane address = actual page address, also known as the row address.*
6. *I/O[15:8] are not used during the addressing sequence and should be driven Low.*

For the x8 address bits, the following rules apply:

- A0 - A11: column address in the page
- A12 - A17: page address in the block
- A18: plane address (for multiplane operations) / block address (for normal operations)
- A19 - A29: block address

For the x16 address bits, the following rules apply:

- A0 - A10: column address in the page
- A11 - A16: page address in the block
- A17: plane address (for multiplane operations) / block address (for normal operations)
- A18 - A28: block address

1.7 Mode Selection

Table 1.6 Mode Selection

Mode		CLE	ALE	CE#	WE#	RE#	WP#
Read Mode	Command Input	High	Low	Low	Rising	High	X
	Address Input	Low	High	Low	Rising	High	X
Program or Erase Mode	Command Input	High	Low	Low	Rising	High	High
	Address Input	Low	High	Low	Rising	High	High
Data Input		Low	Low	Low	Rising	High	High
Data Output (on going)		Low	Low	Low	High	Falling	X
Data Output (suspended)		X	X	X	High	High	X
Busy Time in Read		X	X	X	X	High (3)	X
Busy Time in Program		X	X	X	X	X	High
Busy Time in Erase		X	X	X	X	X	High
Write Protect		X	X	X	X	X	Low
Stand By		X	X	High	X	X	0V / V_{CC} (2)

Notes:

1. *X can be V_{IL} or V_{IH}. High = Logic level high. Low = Logic level low.*
2. *WP# should be biased to CMOS high or CMOS low for stand-by mode.*
3. *During Busy Time in Read, RE# must be held high to prevent unintended data out.*

2. Bus Operation

There are six standard bus operations that control the device: Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby. (See Table 1.6.)
Typically glitches less than 5 ns on Chip Enable, Write Enable, and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input

The Command Input bus operation is used to give a command to the memory device. Commands are accepted with Chip Enable low, Command Latch Enable high, Address Latch Enable low, and Read Enable high and latched on the rising edge of Write Enable. Moreover, for commands that start a modify operation (program/erase) the Write Protect pin must be high. See Figure 6.1 on page 39 and Table 5.4 on page 36 for details of the timing requirements. Command codes are always applied on I/O7:0 regardless of the bus configuration (x8 or x16).

2.2 Address Input

The Address Input bus operation allows the insertion of the memory address. For the FMND2GxxS3S and FMND4GxxS3S devices, five write cycles are needed to input the addresses. For the FMND1GxxS3S, four write cycles are needed to input the addresses. If necessary, a 5th dummy address cycle can be issued to FMND1GxxS3S, which will be ignored by the NAND device without causing problems. Addresses are accepted with Chip Enable low, Address Latch Enable high, Command Latch Enable low, and Read Enable high and latched on the rising edge of Write Enable. Moreover, for commands that start a modify operation (program/erase) the Write Protect pin must be high. See Figure 6.2 on page 40 and Table 5.4 on page 36 for details of the timing requirements. Addresses are always applied on I/O7:0 regardless of the bus configuration (x8 or x16). Refer to Table 1.3 through Table 1.5 on page 13 for more detailed information.

2.3 Data Input

The Data Input bus operation allows the data to be programmed to be sent to the device. The data insertion is serial and timed by the Write Enable cycles. Data is accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable high, and Write Protect high and latched on the rising edge of Write Enable. See Figure 6.3 on page 40 and Table 5.4 on page 36 for details of the timing requirements.

2.4 Data Output

The Data Output bus operation allows data to be read from the memory array and to check the Status Register content, and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable high, Address Latch Enable low, and Command Latch Enable low. See Figure 6.4 on page 41 and Table 5.4 on page 36 for details of the timings requirements.

2.5 Write Protect

The Hardware Write Protection is activated when the Write Protect pin is low. In this condition, modify operations do not start and the content of the memory is not altered. The Write Protect pin is not latched by Write Enable to ensure the protection even during power up.

2.6 Standby

In Standby, the device is deselected, outputs are disabled, and power consumption is reduced.

3. Command Set

Table 3.1 Command Set

Command	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	Acceptable Command during Busy	Supported on FMND1GxxS3S
Page Read	00h	30h			No	Yes
Page Program	80h	10h			No	Yes
Random Data Input	85h				No	Yes
Random Data Output	05h	E0h			No	Yes
Multiplane Program	80h	11h	81h	10h	No	No
ONFI Multiplane Program	80h	11h	80h	10h	No	No
Page Reprogram	8Bh	10h			No	Yes
Multiplane Page Reprogram	8Bh	11h	8Bh	10h	No	No
Block Erase	60h	D0h			No	Yes
Multiplane Block Erase	60h	60h	D0h		No	No
ONFI Multiplane Block Erase	60h	D1h	60h	D0h	No	No
Copy Back Read	00h	35h			No	Yes
Copy Back Program	85h	10h			No	Yes
Multiplane Copy Back Program	85h	11h	81h	10h	No	No
ONFI Multiplane Copy Back Program	85h	11h	85h	10h	No	No
Special Read For Copy Back	00h	36h			No	No
Read Status Register	70h				Yes	Yes
Read Status Enhanced	78h				Yes	No
Reset	FFh				Yes	Yes
Read Cache	31h				No	Yes
Read Cache Enhanced	00h	31h			No	Yes
Read Cache End	3Fh				No	Yes
Cache Program (End)	80h	10h			No	Yes
Cache Program (Start) / (Continue)	80h	15h			No	Yes
Multiplane Cache Program (Start/Continue)	80h	11h	81h	15h	No	No
ONFI Multiplane Cache Program (Start/Continue)	80h	11h	80h	15h	No	No
Multiplane Cache Program (End)	80h	11h	81h	10h	No	No
ONFI Multiplane Cache Program (End)	80h	11h	80h	10h	No	No
Read ID	90h				No	Yes
Read ID2	30h-65h-00h	30h			No	Yes
Read ONFI Signature	90h				No	Yes
Read Parameter Page	ECh				No	Yes
One-time Programmable (OTP) Area Entry	29h-17h-04h-19h				No	Yes

3.1 Page Read

Page Read is initiated by writing 00h and 30h to the command register along with five address cycles (four or five cycles for FMND1GxxS3S). Two types of operations are available: random read and serial page read. Random read mode is enabled when the page address is changed. All data within the selected page are transferred to the data registers in less than 25 μs (tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of the R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 45 ns (x8) or 40 ns (x16) cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# signal makes the device output the data, starting from the selected column address up to the last column address.
The device may output random data in a page instead of the sequential data by writing Random Data Output command. The column address of next data, which is going to be out, may be changed to the address that follows Random Data Output command. Random Data Output can be performed as many times as needed.
After power up, the device is in read mode, so 00h command cycle is not necessary to start a read operation.
Any operation other than read or Random Data Output causes the device to exit read mode.
See Figure 6.6 on page 42 and Figure 6.12 on page 46 as references.

3.2 Page Program

A page program cycle consists of a serial data loading period in which up to 2112 bytes (x8) or 1056 words (x16) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.
The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs (four cycles for FMND1GxxS3S) and then serial data. The words other than those to be programmed do not need to be loaded. The device supports Random Data Input within a page. The column address of next data, which will be entered, may be changed to the address that follows the Random Data Input command (85h). Random Data Input may be performed as many times as needed.
The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks.
Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the Status Register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O0) may be checked. The internal write verify detects only errors for 1's that are not successfully programmed to 0's. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 6.9 on page 44 and Figure 6.11 on page 45 detail the sequence.
The device is programmable by page, but it also allows multiple partial page programming of a word or consecutive bytes up to the full page in a single page program cycle.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed the number indicated in Table 5.7 on page 38. Pages may be programmed in any order within a block.
If a Page Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted page is not used for further reading or programming operations until the next uninterrupted block erase is complete.

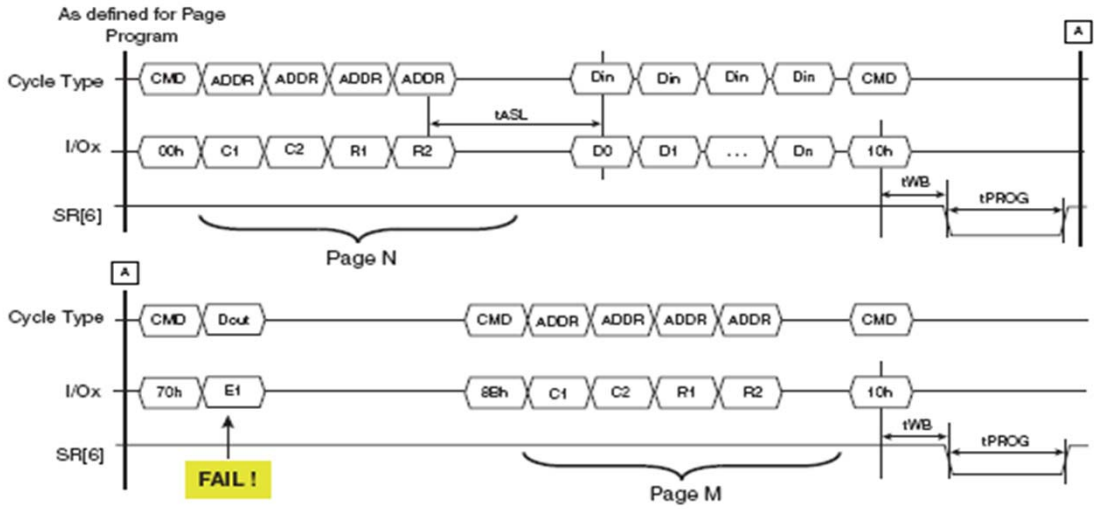
3.3 Multiplane Program – FMND2GxxS3S and FMND4GxxS3S

The FMND2GxxS3S and FMND4GxxS3S device support Multiplane Program, making it possible to program two pages in parallel, one page per plane.
A Multiplane Program cycle consists of a double serial data loading period in which up to 4352 bytes (x8) or 2176 words (x16) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1st page. The address for this page must be in the 1st plane (PLA0 = 0). The device supports Random Data Input exactly the same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY). Once it has become ready again, the '81h' command must be issued, followed by 2nd page address (5 cycles) and its serial data input. The address for this page must be in the 2nd plane (PLA0 = 1). The Program Confirm command (10h) starts parallel programming of both pages.
Figure 6.13 on page 46 describes the sequences using the legacy protocol. In this case, the block address bits for the first plane are all zero and the second address issued selects the block for both planes.
Figure 6.14 on page 47 describes the sequences using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.
The user can check operation status by monitoring R/B# pin or reading the Status Register (command 70h or 78h). The Read Status Register command is also available during Dummy Busy time (tDBSY). In case of failure in either page program, the fail bit of the Status Register will be set. Refer to Section 3.8 on page 22 for further info.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed the number indicated in Table 5.7 on page 38. In addition, pages must be programmed sequentially within a block.
If a Multiplane Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

3.4 Page Reprogram

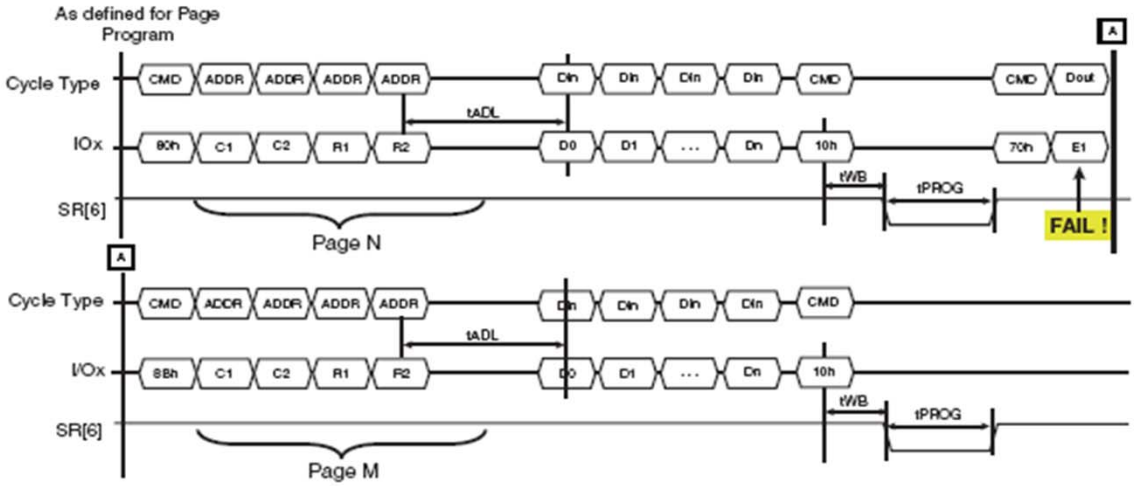
Page Program may result in a fail, which can be detected by Read Status Register. In this event, the host may call Page Reprogram. This command allows the reprogramming of the same pattern of the last (failed) page into another memory location. The command sequence initiates with reprogram setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle, as described in Figure 3.1.

Figure 3.1 Page Reprogram



On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm '10h', as described in Figure 3.2.

Figure 3.2 Page Reprogram with Data Manipulation



The device supports Random Data Input within a page. The column address of next data, which will be entered, may be changed to the address which follows the Random Data Input command (85h). Random Data Input may be operated multiple times regardless of how many times it is done in a page.
The Program Confirm command (10h) initiates the re-programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the Status Register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register.
Only the Read Status command and Reset command are valid when programming is in progress. When the Page Program is complete, the Write Status Bit (I/O0) may be checked. The internal write verify detects only errors for 1's that are not successfully programmed to 0's. The command register remains in Read Status command mode until another valid command is written to the command register.

The Page Reprogram must be issued in the same plane as the Page Program that failed. In order to program the data to a different plane, use the Page Program operation instead. The Multiplane Page Reprogram can re-program two pages in parallel, one per plane. The Multiplane Page Reprogram operation is performed after a failed Multiplane Page Program operation. The command sequence is very similar to Figure 6.13 on page 46, except that it requires the Page Reprogram Command (8Bh) instead of 80h and 81h.
If a Page Reprogram operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted page is not used for further reading or programming operations until the next uninterrupted block erase is complete.

3.5 Block Erase

The Block Erase operation is done on a block basis. Block address loading is accomplished in three cycles (two cycles for FMND1GxxS3S) initiated by an Erase Setup command (60h). Only the block address bits are valid while the page address bits are ignored.
The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by the execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase verify. Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the Status Register.
The system controller can detect the completion of an erase by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O0) may be checked. Figure 6.15 on page 47 details the sequence.
If a Block Erase operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted block is erased under continuous power conditions before that block can be trusted for further programming and reading operations.

3.6 Multiplane Block Erase – FMND2GxxS3S and FMND4GxxS3S

Multiplane Block Erase allows the erase of two blocks in parallel, one block per memory plane.
The Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. In this case, multiplane erase does not need any Dummy Busy Time between 1st and 2nd block insertion. See Table 5.7 on page 38 for performance information.
For the Multiplane Block Erase operation, the address of the first block must be within the first plane (PLA0 = 0) and the address of the second block in the second plane (PLA0 = 1). See Figure 6.16 on page 48 for a description of the legacy protocol. In this case, the block address bits for the first plane are all zero and the second address issued selects the block for both planes. Figure 6.17 on page 48 describes the sequences using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.
The user can check operation status by monitoring R/B# pin or reading the Status Register (command 70h or 78h). The Read Status Register command is also available during Dummy Busy time (tDBSY). In case of failure in either erase, the fail bit of the Status Register will be set. Refer to Section 3.8 on page 22 for further information.
If a Multiplane Block Erase operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted blocks are erased under continuous power conditions before those block can be trusted for further programming and reading operations.

3.7 Copy Back Program

The copy back feature is intended to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is greatly improved. The benefit is especially obvious when a portion of a block needs to be updated and the rest of the block also needs to be copied to the newly assigned free block. The operation for performing a copy back is a sequential execution of page-read (without mandatory serial access) and Copy Back Program with the address of destination page. A read operation with the '35h' command and the address of the source page moves the whole 2112-byte (x8) or 1056-word (x16) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE# (see Figure 6.18 on page 49), or Copy Back Program command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin programming.

The source and destination page in the Copy Back Program sequence must belong to the same device plane (same PLA0 for FMND2GxxS3S and FMND4GxxS3S). Copy Back Read and Copy Back Program for a given plane must be between odd address pages or between even address pages for the device to meet the program time (tPROG) specification. Copy Back Program may not meet this specification when copying from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page). The data input cycle for modifying a portion or multiple distinct portions of the source page is allowed as shown in Figure 6.19 on page 49.

If a Copy Back Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted page is not used for further reading or programming operations until the next uninterrupted block erase is complete.

3.7.1 Multiplane Copy Back Program – FMND2GxxS3S and FMND4GxxS3S

The device supports Multiplane Copy Back Program with exactly the same sequence and limitations as the Page Program. Multiplane Copy Back Program must be preceded by two single page Copy Back Read command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane). Multiplane Copy Back cannot cross plane boundaries — the contents of the source page of one device plane can be copied only to a destination page of the same plane.

The Multiplane Copy Back Program sequence represented in Figure 6.20 on page 50 shows the legacy protocol. In this case, the block address bits for the first plane are all zero and the second address issued selects the block for both planes. Figure 6.21 on page 51 describes the sequence using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.

If a Multiplane Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

3.7.2 Special Read for Copy Back – FMND2GxxS3S and FMND4GxxS3S

The device features the "Special Read for Copy Back." If Copy Back Read (described in Section 3.7 and Section 3.7.1 on page 21) is triggered with confirm command '36h' instead '35h', Copy Back Read from target page(s) will be executed with an increased internal (VPASS) voltage.

This special feature is used in order to minimize the number of read errors due to over-program or read disturb — it shall be used only if ECC read errors have occurred in the source page using Page Read or Copy Back Read sequences.

Excluding the Copy Back Read confirm command, all other features described in Section 3.7 and Section 3.7.1 for standard copy back remain valid (including the figures referred to in those sections).

3.8 Read Status Register

The Status Register is used to retrieve the status value for the last operation issued. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two-line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. Refer to Section 3.2 on page 17 for specific Status Register definition, and to Figure 6.22 on page 51 for timings.
If the Read Status Register command is issued during multiplane operations then Status Register polling will return the combined status value related to the outcome of the operation in the two planes according to the following table:

Status Register Bit	Composite Status Value
Bit 0, Pass/Fail	OR
Bit 1, Cache Pass/Fail	OR

In other words, the Status Register is dynamic; the user is not required to toggle RE# / CE# to update it.
The command register remains in Status Read mode until further commands are issued. Therefore, if the Status Register is read during a random read cycle, the read command (00h) should be given before starting read cycles.
Note: The Read Status Register command shall not be used for concurrent operations in multi-die stack configurations (single CE#). "Read Status Enhanced" shall be used instead.

3.9 Read Status Enhanced – FMND2GxxS3S and FMND4GxxS3S

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation in the case of multiplane operations in the same die.
Figure 6.23 on page 52 defines the Read Status Enhanced behavior and timings. The plane and die address must be specified in the command sequence in order to retrieve the status of the die and the plane of interest. Refer to Table 3.2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued.
The Status Register is dynamic; the user is not required to toggle RE# / CE# to update it.

3.10 Read Status Register Field Definition

Table 3.2 below lists the meaning of each bit of the Read Status Register and Read Status Enhanced (FMND2GxxS3S and FMND4GxxS3S).

Table 3.2 Status Register Coding

ID	Page Program / Page Reprogram	Block Erase	Read	Read Cache	Cache Program / Cache Reprogram	Coding
0	Pass / Fail	Pass / Fail	NA	NA	Pass / Fail (N)	N Page Pass: 0 Fail: 1
1	NA	NA	NA	NA	Pass / Fail (N-1)	N - 1 Page Pass: 0 Fail: 1
2	NA	NA	NA	NA	NA	—
3	NA	NA	NA	NA	NA	—
4	NA	NA	NA	NA	NA	—
5	Ready / Busy	Ready / Busy	Ready / Busy	P/E/R Controller Bit	Ready / Busy	Ready / Busy Busy: 0 Ready: 1
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy: 0 Ready: 1
7	Write Protect	Write Protect	Write Protect	NA	Write Protect	Protected: 0 Not Protected: 1

3.11 Reset

The Reset feature is executed by writing FFh to the command register. If the device is in Busy state during random read, program, or erase mode, the Reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data may be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high or value 60h when WP# is low. If the device is already in reset state a new Reset command will not be accepted by the command register. The R/B# pin transitions to low for tRST after the Reset command is written. Refer to Figure 6.24 on page 52 for further details. The Status Register can also be read to determine the status of a Reset operation.

3.12 Read Cache

Read Cache can be used to increase the read operation speed, as defined in Section 3.1 on page 17, and it cannot cross a block boundary. As soon as the user starts to read one page, the device automatically loads the next page into the cache register. Serial data output may be executed while data in the memory is read into the cache register. Read Cache is initiated by the Page Read sequence (00-30h) on a page M.
After random access to the first page is complete (R/B# returned to high, or Read Status Register I/O6 switches to high), two command sequences can be used to continue read cache:

- Read Cache (command '31h' only): once the command is latched into the command register (see Figure 6.26 on page 53), device goes busy for a short time (tCBSYR), during which data of the first page is transferred from the data register to the cache register. At the end of this phase, the cache register data can be output by toggling RE# while the next page (page address M+1) is read from the memory array into the data register.
- Read Cache Enhanced (sequence '00h' <page N address> '31'): once the command is latched into the command register (see Figure 6.27 on page 54), device goes busy for a short time (tCBSYR), during which data of the first page is transferred from the data register to the cache register. At the end of this phase, cache register data can be output by toggling RE# while page N is read from the memory array into the data register.
  Note: The FMND1GxxS3S device does not support Read Cache Enhanced.

Subsequent pages are read by issuing additional Read Cache or Read Cache Enhanced command sequences. If serial data output time of one page exceeds random access time (tR), the random access time of the next page is hidden by data downloading of the previous page.
On the other hand, if 31h is issued prior to completing the random access to the next page, the device will stay busy as long as needed to complete random access to this page, transfer its contents into the cache register, and trigger the random access to the following page.
To terminate the Read Cache operation, 3Fh command should be issued (see Figure 6.28 on page 54). This command transfers data from the data register to the cache register without issuing next page read.
During the Read Cache operation, the device doesn't allow any other command except for 00h, 31h, 3Fh, Read SR, or Reset (FFh). To carry out other operations, Read Cache must be terminated by the Read Cache End command (3Fh) or the device must be reset by issuing FFh.
Read Status command (70h) may be issued to check the status of the different registers and the busy/ready status of the cached read operations.

- The Cache-Busy status bit I/O6 indicates when the cache register is ready to output new data.
- The status bit I/O5 can be used to determine when the cell reading of the current data register contents is complete.
  Note: The Read Cache and Read Cache End commands reset the column counter, thus, when RE# is toggled to output the data of a given page, the first output data is related to the first byte of the page (column address 00h). Random Data Output command can be used to switch column address.

3.13 Cache Program

Cache Program can improve the program throughput by using the cache register. The Cache Program operation cannot cross a block boundary. The cache register allows new data to be input while the previous data that was transferred to the data register is programmed into the memory array.
After the serial data input command (80h) is loaded to the command register, followed by five cycles of address, a full or partial page of data is latched into the cache register.
Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in the Busy state for a short time (tCBSYW). After all data of the cache register is transferred into the data register, the device returns to the Ready state and allows loading the next data into the cache register through another cache program command sequence (80h-15h).
The Busy time following the first sequence 80h - 15h equals the time needed to transfer the data from the cache register to the data register. Cell programming the data of the data register and loading of the next data into the cache register is consequently processed through a pipeline model.
In case of any subsequent sequence 80h - 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete; till this moment the device will stay in a busy state (tCBSYW).
Read Status commands (70h or 78h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations.

- The Cache-Busy status bit I/O6 indicates when the cache register is ready to accept new data.
- The status bit I/O5 can be used to determine when the cell programming of the current data register contents is complete.
- The cache program error bit I/O1 can be used to identify if the previous page (page N-1) has been successfully programmed or not in a cache program operation. The status bit is valid upon I/O6 status bit changing to 1.
- The error bit I/O0 is used to identify if any error has been detected by the program/erase controller while programming page N. The status bit is valid upon I/O5 status bit changing to 1.

I/O1 may be read together with I/O0.
If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O5 must be polled to find out if the last programming is finished before starting any other operation. See Table 3.2 on page 22 and Figure 6.29 on page 55 for more details.
If a Cache Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

3.14 Multiplane Cache Program – FMND2GxxS3S and FMND4GxxS3S

The Multiplane Cache Program enables high program throughput by programming two pages in parallel, while exploiting the data and cache registers of both planes to implement cache.
The command sequence can be summarized as follows:

- Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (PLA0 = 0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports Random Data Input exactly like Page Program operation.
- The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).

- Once device returns to ready again, 81h command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (PLA0 = 1). The data of 2nd page other than those to be programmed do not need to be loaded.
- Cache Program confirm command (15h). Once the cache write command (15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in the Busy state for a short time (tCBSYW). After all data from the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence.

The sequence 80h-...- 11h...-...81h...-...15h can be iterated, and each time the device will be busy for the tCBSYW time needed to complete programming the current data register contents, and transferring the new data from the cache registers. The sequence to end Multiplane Cache Program is 80h-...- 11h...-...81h...-...10h.
The Multiplane Cache Program is available only within two paired blocks in separate planes. Figure 6.30 on page 56 shows the legacy protocol for the multiplane cache program operation. In this case, the block address bits for the first plane are all zero and the second address issued selects the block for both planes. Figure 6.31 on page 57 shows the ONFI protocol for the multiplane cache program operation. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.
The user can check operation status by R/B# pin or Read Status Register commands (70h or 78h). If the user opts for 70h, Read Status Register will provide "global" information about the operation in the two planes.

- I/O6 indicates when both cache registers are ready to accept new data.
- I/O5 indicates when the cell programming of the current data registers is complete.
- I/O1 identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. This status bit is valid upon I/O6 status bit changing to 1.
- I/O0 identifies if any error has been detected by the program/erase controller while programming the two pages N. This status bit is valid upon I/O5 status bit changing to 1.

See Table 3.2 on page 22 for more details.
If the system monitors the progress of the operation only with R/B#, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O5 must be polled to find out if the last programming is finished before starting any other operation. Refer to Section 3.8 on page 22 for further information.
If a Multiplane Cache Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

3.15 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.
Note: If you want to execute Read Status command (0x70) after Read ID sequence, you should input dummy command (0x00) before Read Status command (0x70).
For the FMND2GxxS3S and FMND4GxxS3S device, five read cycles sequentially output the manufacturer code (01h), and the device code and 3rd, 4th, and 5th cycle ID, respectively. For the FMND1GxxS3S device, four read cycles sequentially output the manufacturer code (01h), and the device code and 80h, 4th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 6.32 on page 58 shows the operation sequence, while Table 3.3 to Table 3.8 explain the byte meaning.

Table 3.3 Read ID for Supported Configurations

Density	Org	V_{CC}	1st	2nd	3rd	4th	5th
1 Gb	x8	1.8V	01h	A1h	80h	15h	—
2 Gb			01h	AAh	90h	15h	46h
4 Gb			01h	ACh	90h	15h	56h
1 Gb	x16		01h	B1h	80h	55h	—
2 Gb			01h	BAh	90h	55h	46h
4 Gb			01h	BCh	90h	55h	56h

Table 3.4 Read ID Bytes

Device Identifier Byte	Description
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell type, etc.
4th	Page Size, Block Size, Spare Size, Organization
5th (FMND2GxxS3S, FMND4GxxS3S)	ECC, Multiplane information

3rd ID Data

Table 3.5 Read ID Byte 3 Description

	Description	I/O7	I/O6	I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Internal Chip Number	1					0 0
	2					0 1
	4					1 0
	8					1 1
Cell type	2-level cell				0 0	
	4-level cell				0 1	
	8-level cell				1 0	
	16-level cell				1 1	
Number of simultaneously programmed pages	1			0 0		
	2			0 1		
	4			1 0		
	8			1 1		
Interleave program Between multiple chips	Not supported		0			
	Supported		1			
Cache Program	Not supported	0				
	Supported	1				

4th ID Data

Table 3.6 Read ID Byte 4 Description – FMND1GxxS3S

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page size (without spare area)	1 kB						0 0
	2 kB						0 1
	4 kB						1 0
	8 kB						1 1
Block Size (without spare area)	64 kB			0 0			
	128 kB			0 1			
	256 kB			1 0			
	512 kB			1 1			
Spare Area Size (byte / 512 byte)	8					0	
	16					1	
Serial Access Time	45 ns	0			0		
	25 ns	0			1		
	Reserved	1			0		
	Reserved	1			1		
Organization	x8		0				
	x16		1				

Table 3.7 Read ID Byte 4 Description – FMND2GxxS3S and FMND4GxxS3S

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page size (without spare area)	1 kB						0 0
	2 kB						0 1
	4 kB						1 0
	8 kB						1 1
Block Size (without spare area)	64 kB			0 0			
	128 kB			0 1			
	256 kB			1 0			
	512 kB			1 1			
Spare Area size (byte / 512 byte)	16					0	
	32					1	
Serial Access Time	45 ns	0			0		
	25 ns	1			0		
	Reserved	0			1		
	Reserved	1			1		
Organization	x8		0				
	x16		1				

5th ID Data

Table 3.8 Read ID Byte 5 Description — FMND2GxxS3S and FMND4GxxS3S

	Description	I/O7	I/O6 I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
ECC Level	1 bit / 512 bytes				0 0
	2 bit / 512 bytes				0 1
	4 bit / 512 bytes				1 0
	8 bit / 512 bytes				1 1
Plane Number	1			0 0	
	2			0 1	
	4			1 0	
	8			1 1	
Plane Size (without spare area)	64 Mb		0 0 0		
	128 Mb		0 0 1		
	256 Mb		0 1 0		
	512 Mb		0 1 1		
	1 Gb		1 0 0		
	2 Gb		1 0 1		
	4 Gb		1 1 0		
Reserved		0			

3.16 Read ID2

The device contains an alternate identification mode, initiated by writing 30h-65h-00h to the command register, followed by address inputs, followed by command 30h. The address for FMND1GxxS3S will be 00h-02h-02h-00h. The address for FMND2GxxS3S and FMND4GxxS3S will be 00h-02h-02h-00h-00h. The ID2 data can then be read from the device by pulsing RE#. The command register remains in Read ID2 mode until further commands are issued to it. Figure 6.33 on page 58 shows the Read ID2 command sequence. Read ID2 values are all 0xFs, unless specific values are requested when ordering from Fidelix.

3.17 Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. Figure 6.34 on page 59 shows the operation sequence.

3.18 Read Parameter Page

The device supports the ONFI Read Parameter Page operation, initiated by writing ECh to the command register, followed by an address input of 00h. The command register remains in Parameter Page mode until further commands are issued to it. Figure 6.35 on page 59 shows the operation sequence, while Table 3.9 explains the parameter fields.

For x16 device, upper eight I/Os are not used and are 0xFF.

Note: For 32 nm Fidelix NAND, for a particular condition, the Read Parameter Page command does not give the correct values. If the previous address has A23/A24/A25 = High, the output is 00h instead of the correct values. To overcome this issue, the host must issue a Reset command before the Read Parameter Page command. Issuance of Reset before the Read Parameter Page command will provide the correct values and will not output 00h values.

Table 3.9 Parameter Page Description (Sheet 1 of 3)

Byte	O/M	Description	Values
Revision Information and Features Block			
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	4Fh, 4Eh, 46h, 49h
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02h, 00h
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	FMND1G08S3S (x8): 14h, 00h FMND2G08S3S (x8): 1Ch, 00h FMND4G08S3S (x8): 1Ch, 00h FMND1G16S3S (x16): 15h, 00h FMND2G16S3S (x16): 1Dh, 00h FMND4G16S3S (x16): 1Dh, 00h
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command	FMND1GxxS3S: 13h, 00h FMND2GxxS3S: 3Bh, 00h FMND4GxxS3S: 1Bh, 00h
10-31		Reserved (0)	00h
Manufacturer Information Block			
32-43	M	Device manufacturer (12 ASCII characters)	53h, 50h, 41h, 4Eh, 53h, 49h, 4Fh, 4Eh, 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters)	FMND1GxxS3S: 53h, 33h, 34h, 4Dh, 53h, 30h, 31h, 47h, 32h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h FMND2GxxS3S: 53h, 33h, 34h, 4Dh, 53h, 30h, 32h, 47h, 32h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h FMND4GxxS3S: 53h, 33h, 34h, 4Dh, 53h, 30h, 34h, 47h, 32h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	M	JEDEC manufacturer ID	01h
65-66	O	Date code	00h
67-79		Reserved (0)	00h
Memory Organization Block			
80-83	M	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	M	Number of spare bytes per page	FMND1GxxS3S: 40h, 00h FMND2GxxS3S: 80h, 00h FMND4GxxS3S: 80h, 00h
86-89	M	Number of data bytes per partial page	00h, 00h, 00h, 00h
90-91	M	Number of spare bytes per partial page	00h, 00h
92-95	M	Number of pages per block	40h, 00h, 00h, 00h
96-99	M	Number of blocks per logical unit (LUN)	FMND1GxxS3S: 00h, 04h, 00h, 00h FMND2GxxS3S: 00h, 08h, 00h, 00h FMND4GxxS3S: 00h, 10h, 00h, 00h
100	M	Number of logical units (LUNs)	01h

Table 3.9 Parameter Page Description (Sheet 2 of 3)

Byte	O/M	Description	Values
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	FMND1GxxS3S: 22h FMND2GxxS3S: 23h FMND4GxxS3S: 23h
102	M	Number of bits per cell	01h
103-104	M	Bad blocks maximum per LUN	FMND1GxxS3S: 14h, 00h FMND2GxxS3S: 28h, 00h FMND4GxxS3S: 50h, 00h
105-106	M	Block endurance	01h, 05h
107	M	Guaranteed valid blocks at beginning of target	01h
108-109	M	Block endurance for guaranteed valid blocks	01h, 03h
110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	04h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	FMND1GxxS3S: 00h FMND2GxxS3S: 01h FMND4GxxS3S: 01h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	04h
115-127		Reserved (0)	00h
Electrical Parameters Block			
128	M	I/O pin capacitance	0Ah
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	03h, 00h
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0	03h, 00h
133-134	M	tPROG Maximum page program time (µs)	BCh, 02h
135-136	M	tBERS Maximum block erase time (µs)	10h, 27h
137-138	M	tR Maximum page read time (µs)	FMND1GxxS3S: 19h, 00h FMND2GxxS3S: 1Eh, 00h FMND4GxxS3S: 1Eh, 00h
139-140	M	tCCS Minimum Change Column setup time (ns)	C8h, 00h
141-163		Reserved (0)	00h
Vendor Block			
164-165	M	Vendor specific Revision number	00h
166-253		Vendor specific	00h

Table 3.9 Parameter Page Description (Sheet 3 of 3)

Byte	O/M	Description	Values
254-255	M	Integrity CRC	FMND1G08S3S (x8): F1h, F9h FMND2G08S3S (x8): 28h, C6h FMND4G08S3S (x8): 56h, 8Dh FMND1G16S3S (x16): 83h, 8Fh FMND2G16S3S (x16): 5Ah, B0h FMND4G16S3S (x16): 24h, FBh
Redundant Parameter Pages			
256-511	M	Value of bytes 0-255	Repeat Value of bytes 0-255
512-767	M	Value of bytes 0-255	Repeat Value of bytes 0-255
768+	O	Additional redundant parameter pages	FFh

Note:
1. O" Stands for Optional, "M" for Mandatory.

3.19 Read Unique ID

The device supports the ONFI Read Unique ID function, initiated by writing EDh to the command register, followed by an address input of 00h. The host must monitor the R/B# pin or wait for the maximum data transfer time (tR) before reading the Unique ID data. The first sixteen bytes returned by the flash is a unique value. The next sixteen bytes returned are the bit-wise complement of the unique value. The host can verify the Unique ID was read correctly by performing an XOR of the two values. The result should be all ones. The command register remains in Unique ID mode until further commands are issued to it. Figure 6.36 on page 60 shows the operation sequence, while Table 3.10 shows the Unique ID data contents.

Table 3.10 Unique ID Data Description (Sheet 1 of 2)

Byte	Description
0-15	Unique ID
16-31	ID Complement
32-47	Unique ID
48-63	ID Complement
64-79	Unique ID
80-95	ID Complement
96-111	Unique ID
112-127	ID Complement
128-143	Unique ID
144-159	ID Complement
160-175	Unique ID
176-191	ID Complement
192-207	Unique ID
208-223	ID Complement
224-239	Unique ID
240-255	ID Complement
256-271	Unique ID
272-287	ID Complement
288-303	Unique ID
304-319	ID Complement
320-335	Unique ID
336-351	ID Complement
352-367	Unique ID
368-383	ID Complement
384-399	Unique ID
400-415	ID Complement

Table 3.10 Unique ID Data Description (Sheet 2 of 2)

Byte	Description
416-431	Unique ID
432-447	ID Complement
448-463	Unique ID
464-479	ID Complement
480-495	Unique ID
496-511	ID Complement

3.20 One-Time Programmable (OTP) Entry

The device contains a one-time programmable (OTP) area, which is accessed by writing 29h-17h-04h-19h to the command register. The device is then ready to accept Page Read and Page Program commands (refer to Page Read and Page Program on page 17). The OTP area is of a single erase block size (64 pages), and hence only row addresses between 00h and 3Fh are allowed. The host must issue the Reset command (refer to Reset on page 23) to exit the OTP area and access the normal flash array. The Block Erase command is not allowed in the OTP area. Refer to Figure 6.37 on page 60 for more detail on the OTP Entry command.

4. Signal Descriptions

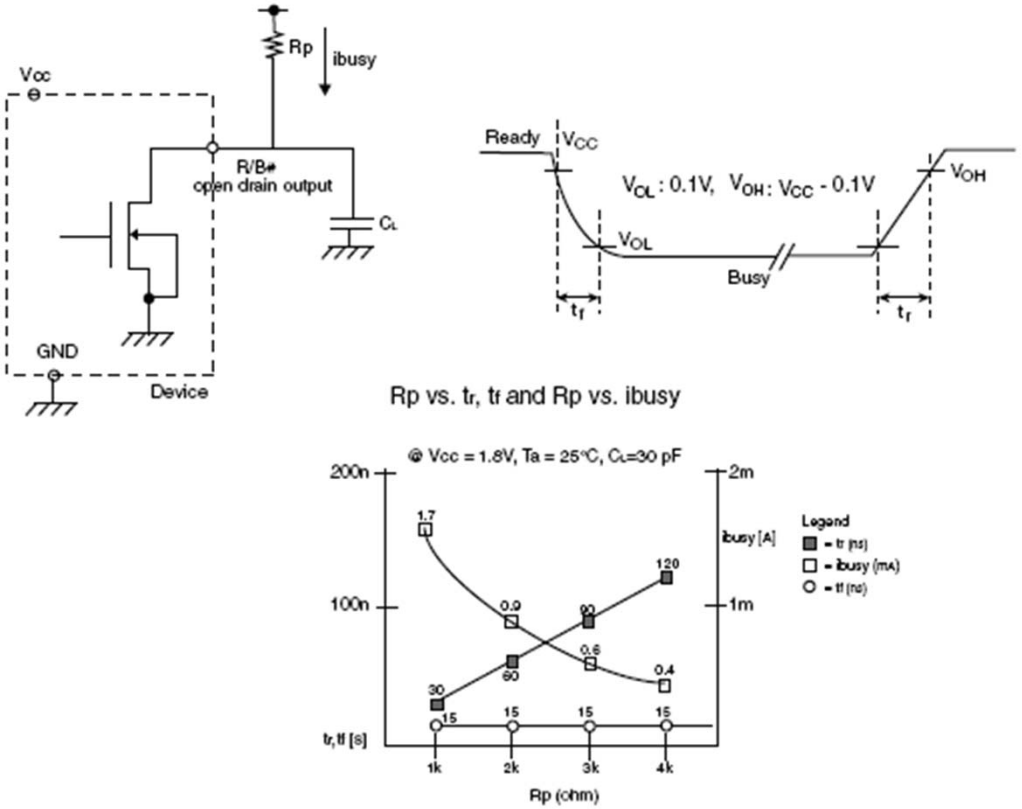
4.1 Data Protection and Power On/Off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 1.1V.
The power-up and power-down sequence is shown in Figure 6.38 on page 61, in this case VCC and VCCQ on the one hand (and VSS and VSSQ on the other hand) are shorted together at all times.
The Ready/Busy signal shall be valid within 100 µs after the power supplies have reached the minimum values (as specified on), and shall return to one within 5 ms (max).
During this busy time, the device executes the initialization process (cam reading), and dissipates a current ICC0 (30 mA max), in addition, it disregards all commands excluding Read Status Register (70h).
At the end of this busy time, the device defaults into "read setup", thus if the user decides to issue a page read command, the 00h command may be skipped.
The WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 100 µs is required before the internal circuit gets ready for any command sequences as shown in Figure 6.38 on page 61. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy

The Ready/Busy output provides a method of indicating the completion of a page program, erase, copyback, or read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tr (R/B#) and the current drain during busy (ibusy), and output load capacitance is related to tf, an appropriate value can be obtained with the reference chart shown in Figure 4.1.

Figure 4.1 Ready/Busy Pin Electrical Application



Rp value guidence

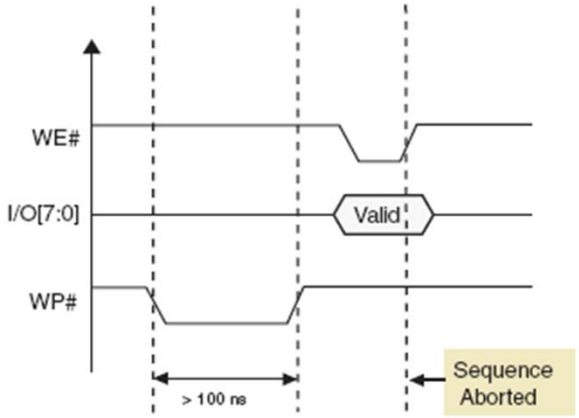
$$Rp\ (min.) = \frac{Vcc\ (Max.) - VoL\ (Max.)}{IoL + \sum IL} = \frac{1.85V}{3mA + \sum IL}$$

where I_L is the sum of the input currents of all devices tied to the R/B# pin.
Rp(max) is determined by maximum permissible limit of tr.

4.3 Write Protect Operation

Erase and program operations are aborted if WP# is driven low during busy time, and kept low for about 100 ns. Switching WP# low during this time is equivalent to issuing a Reset command (FFh). The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/B# pin will stay low for tRST (similarly to Figure 6.24 on page 52). At the end of this time, the command register is ready to process the next command, and the Status Register bit I/O6 will be cleared to 1, while I/O7 value will be related to the WP# value. Refer to Table 3.2 on page 22 for more information on device status. Erase and program operations are enabled or disabled by setting WP# to high or low respectively, prior to issuing the setup commands (80h or 60h). The level of WP# shall be set tWW ns prior to raising the WE# pin for the set up command, as explained in Figure 6.39 and Figure 6.40 on page 62.

Figure 4.2 WP# Low Timing Requirements during Program/Erase Command Sequence



5. Electrical Characteristics

5.1 Valid Blocks

Table 5.1 Valid Blocks

Device	Symbol	Min	Typ	Max	Unit
FMND1GxxS3S	NVB	1004	-	1024	Blocks
FMND2GxxS3S	NVB	2008	-	2048	Blocks
FMND4GxxS3S	NVB	4016	-	4096	Blocks

5.2 Absolute Maximum Ratings

Table 5.2 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Ambient Operating Temperature (Commercial Temperature Range)	T_A	0 to 70	°C
Ambient Operating Temperature (Extended Temperature Range)		-25 to +85	°C
Ambient Operating Temperature (Industrial Temperature Range)		-40 to +85	°C
Temperature under Bias	T_{BIAS}	-50 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Input or Output Voltage	V_{IO} (2)	-0.6 to +2.7	V
Supply Voltage	V_{CC}	-0.6 to +2.7	V

Notes:

1. *Except for the rating "Operating Temperature Range", stresses above those listed in the table Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.*
2. *Minimum Voltage may undershoot to -2V during transition and for less than 20 ns during transitions.*
3. *Maximum Voltage may overshoot to V_{CC} +2.0V during transition and for less than 20 ns during transitions.*

5.3 AC Test Conditions

Table 5.3 AC Test Conditions

Parameter	Value
Input Pulse Levels	0.0V to V_{CC}
Input Rise And Fall Times	5 ns
Input And Output Timing Levels	V_{CC} / 2
Output Load (1.7V - 1.95V)	1 TTL Gate and CL = 30 pF

5.4 AC Characteristics

Table 5.4 AC Characteristics

Parameter	Symbol	Min	Max	Unit
ALE to RE# delay	tAR	10	-	ns
ALE hold time	tALH	10	-	ns
ALE setup time	tALS	25	-	ns
Address to data loading time	tADL	100	-	ns
CE# Access Time (FMND1GxxS3S)	tCEA (4)	-	45	ns
CE# low to RE# low	tCR	10	-	ns
CE# hold time	tCH	10	-	ns
CE# high to output High-Z (FMND1GxxS3S) CE# high to output High-Z (FMND2GxxS3S, FMND4GxxS3S)	tCHZ	-	50 30	ns
CLE hold time	tCLH	10	-	ns
CLE to RE# delay	tCLR	10	-	ns
CLE setup time	tCLS	25	-	ns
CE# high to output hold	tCOH (3)	15	-	ns
CE# high to ALE or CLE don't care	tCSD	10	-	ns
CE# setup time	tCS	35	-	ns
Data hold time	tDH	10	-	ns
Data setup time	tDS	20	-	ns
Data transfer from cell to register (FMND1GxxS3S) Data transfer from cell to register (FMND2GxxS3S, FMND4GxxS3S)	tR	-	25 30	?
Output High-Z to RE# low	tIR	0	-	ns
Read cycle time	tRC	45	-	ns
RE# access time	tREA	-	30	ns
RE# high hold time	tREH	15	-	ns
RE# high to output hold	tRHOH (3)	15	-	ns
RE# high to WE# low	tRHW	100	-	ns
RE# high to output High-Z	tRHZ	-	100	ns
RE# low to output hold	tRLOH (5)	-	-	ns
RE# pulse width	tRP	25	-	ns
Ready to RE# low	tRR	20	-	ns
Device resetting time (Read/Program/Erase)	tRST	-	5/10/500 (2)	?
WE# high to busy	tWB	-	100	ns
Write cycle time	tWC	45	-	ns
WE# high hold time	tWH	15	-	ns
WE# high to RE# low	tWHR	60	-	ns
WE# high to RE# low for Random data out	tWHR2	200	-	ns
WE# pulse width	tWP	25	-	ns
Write protect time	tWW	100	-	ns

Notes:

1. *The time to Ready depends on the value of the pull-up resistor tied to R/B# pin.*
2. *If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5 µs.*
3. *CE# low to high or RE# low to high can be at different times and produce three cases. Depending on which signal comes high first, either t_{COH} or t_{RHOH} will be met.*
4. *During data output, t_{CEA} depends partly on t_{CR} (CE# low to RE# low). If t_{CR} exceeds the minimum value specified, then the maximum time for t_{CEA} may also be exceeded ($t_{CEA} = t_{CR} + t_{REA}$).*
5. *t_{RLOH} is only relevant for EDO timing ($t_{RC} < 30$ ns), which does not apply for this device.*

5.5 DC Characteristics

Table 5.5 DC Characteristics and Operating Conditions

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Power-On-Reset Current		ICC0	FFh command input after power on	-	-	50 per device	mA
Operating Current	Read	ICC1	tRC = tRC (min) CE#=VIL, IOUT = 0 mA (FMND1GxxS3S, FMND4GxxS3S)	-	15	30	mA
			tRC = tRC (min) CE# =VIL, IOUT = 0 mA (FMND2GxxS3S)	-	TBD	TBD	mA
	Program	ICC2	Normal (FMND1GxxS3S, FMND4GxxS3S)	-	15	30	mA
			Cache (FMND1GxxS3S, FMND4GxxS3S)	-	15	30	mA
			Normal (FMND2GxxS3S)	-	TBD	TBD	mA
			Cache (FMND2GxxS3S)	-	TBD	TBD	mA
	Erase	ICC3	- (FMND1GxxS3S, FMND4GxxS3S)	-	15	30	mA
			- (FMND2GxxS3S)	-	TBD	TBD	mA
Standby Current, (TTL)		ICC4	CE# = VIH, WP# = 0V/Vcc	-	-	1	mA
Standby Current, (CMOS)		ICC5	CE# = VCC –0.2, WP# = 0/VCC	-	10	50	µA
Input Leakage Current		ILI	VIN = 0 to VCC(max)	-	-	±10	µA
Output Leakage Current		ILO	VOUT = 0 to VCC(max)	-	-	±10	µA
Input High Voltage		VIH	-	VCC x 0.8	-	VCC + 0.3	V
Input Low Voltage		VIL	-	-0.3	-	VCC x 0.2	V
Output High Voltage		VOH	IOH = -100 µA	VCC - 0.1	-	-	V
Output Low Voltage		VOL	IOL = 100 µA			0.1	V
Output Low Current (R/B#)		IOL(R/B#)	VOL = 0.1V	3	4	-	mA
VCC Supply Voltage (erase and program lockout)		VLKO	-	-	1.1	-	V

Notes:

1. All VCCQ and VCC pins, and VSS and VSSQ pins respectively are shorted together.

2. Values listed in this table refer to the complete voltage range for VCC and VCCQ and to a single device in case of device stacking.

3. All current measurements are performed with a 0.1 µF capacitor connected between the VCC Supply Voltage pin and the VSS Ground pin.

4. Standby current measurement can be performed after the device has completed the initialization process at power up. Refer to Section 4.1 for more details.

5.6 Pin Capacitance

Table 5.6 Pin Capacitance (TA = 25°C, f=1.0 MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input	C_{IN}	V_{IN} = 0V	—	10	pF
Input / Output	C_{IO}	V_{IL} = 0V	—	10	pF

Note:
1. *For the stacked devices version the Input is 10 pF x [number of stacked chips] and the Input/Output is 10 pF x [number of stacked chips].*

5.7 Program / Erase Characteristics

Table 5.7 Program / Erase Characteristics

Parameter	Description	Min	Typ	Max	Unit
Program Time / Multiplane Program Time (2)	tPROG	-	300	700	us
Dummy Busy Time for Multiplane Program (FMND2GxxS3S, FMND4GxxS3S)	tDBSY	-	0.5	1	us
Cache Program short busy time	tCBSYW	-	5	tPROG	us
Number of partial Program Cycles in the same page (Main+Spare)	NOP	-	-	4	Cycle
Block Erase Time (FMND1GxxS3S)	tBERS	-	3	10	ms
Block Erase Time (FMND2GxxS3S, FMND4GxxS3S)	tBERS	-	3.5	10	ms
Read Cache busy time (FMND1GxxS3S)	tCBSYR	-	3	tR	us
Read Cache busy time (FMND2GxxS3S, FMND4GxxS3S)	tCBSYR	-	5	tR	us

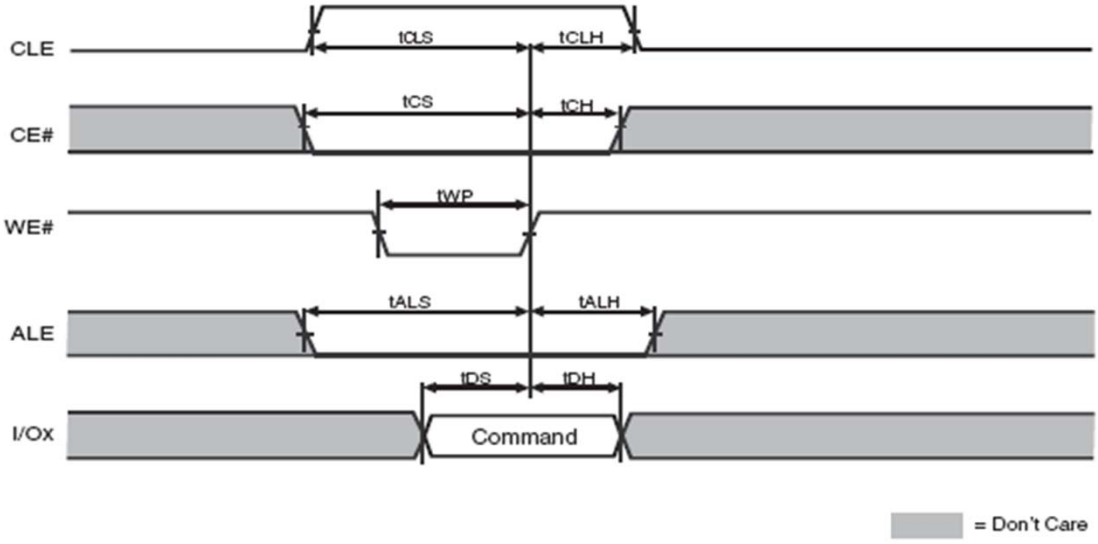
Notes:
1. *Typical program time is defined as the time within which more than 50% of the whole pages are programmed (VCC = 1.8V, 25°C).*
2. *Copy Back Read and Copy Back Program for a given plane must be between odd address pages or between even address pages for the device to meet the program time (tPROG) specification. Copy Back Program may not meet this specification when copying from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page(target page).*

6. Timing Diagram

6.1 Command Latch Cycle

Command Input bus operation is used to give a command to the memory device. Commands are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low, and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/ erase) the Write Protect pin must be high.

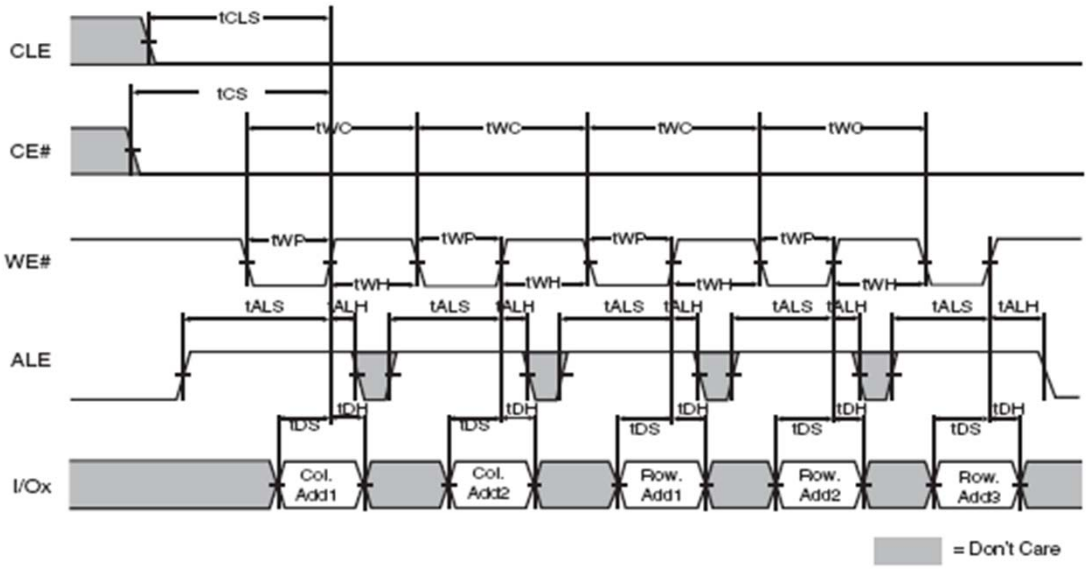
Figure 6.1 Command Latch Cycle



6.2 Address Latch Cycle

Address Input bus operation allows the insertion of the memory address. To insert the 27 (x8 Device) addresses needed to access the 1 Gb, four write cycles are needed. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low, and Read Enable High and latched on the rising edge of Write Enable. Moreover, for commands that start a modify operation (write/ erase) the Write Protect pin must be high.

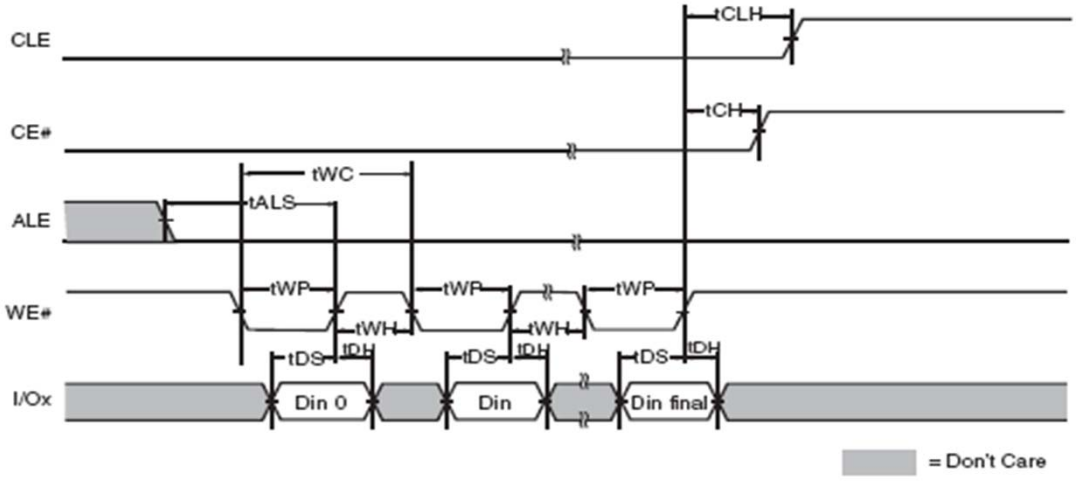
Figure 6.2 Address Latch Cycle



6.3 Data Input Cycle Timing

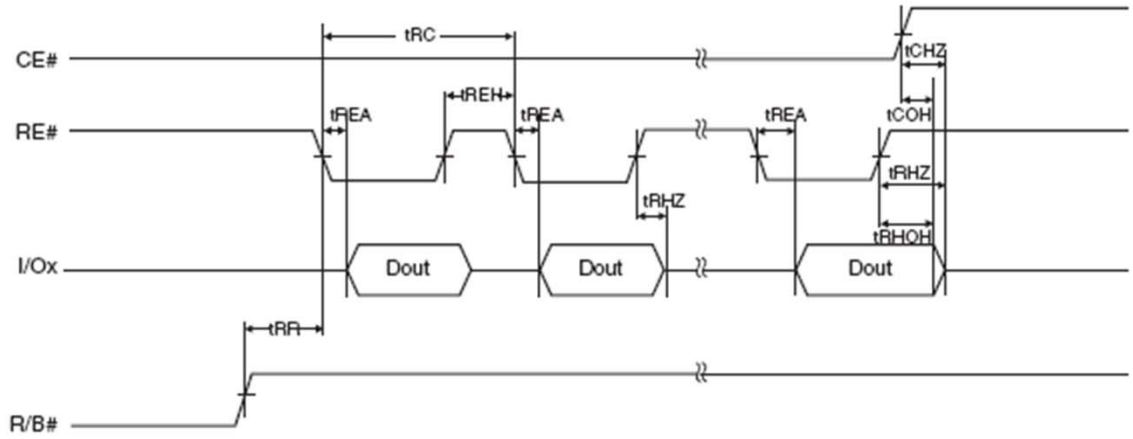
Data Input bus operation allows the data to be programmed to be sent to the device. The data insertion is serially, and timed by the Write Enable cycles. Data is accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable.

Figure 6.3 Input Data Latch Cycle



6.4 Data Output Cycle Timing (CLE=L, WE#=H, ALE=L, WP#=H)

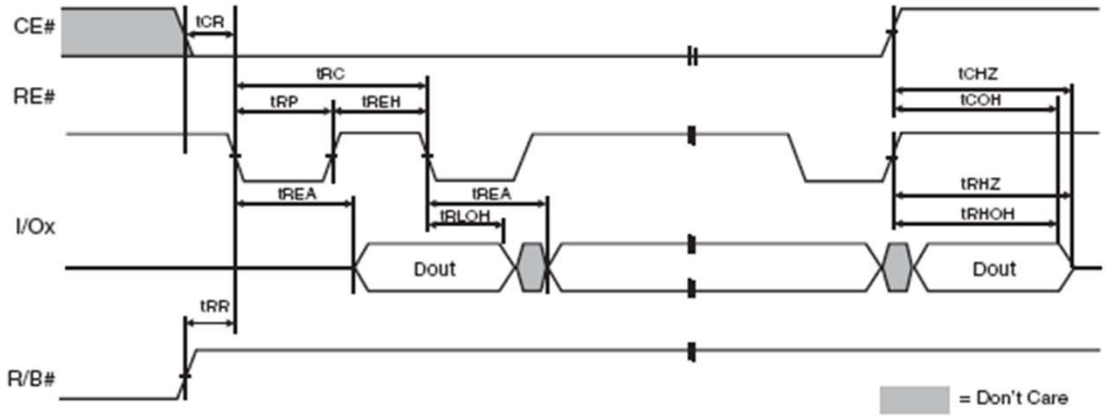
Figure 6.4 Data Output Cycle Timing



Notes:
1. *Transition is measured at ± 200 mV from steady state voltage with load.*
2. *This parameter is sampled and not 100% tested.*
3. t_{RHOH} *starts to be valid when frequency is lower than 33 MHz.*

6.5 Data Output Cycle Timing (EDO Type, CLE=L, WE#=H, ALE=L)

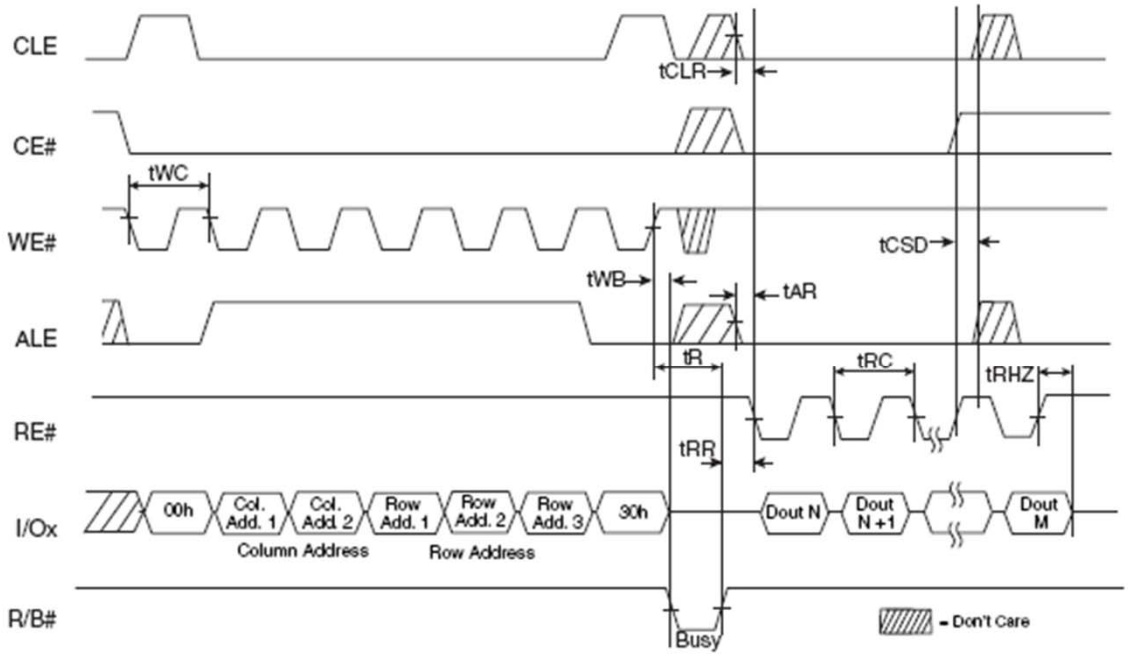
Figure 6.5 Data Output Cycle Timing (EDO)



Notes:
1. *Transition is measured at ± 200 mV from steady state voltage with load.*
2. *This parameter is sampled and not 100% tested.*
3. t_{RLOH} *is valid when frequency is higher than 33 MHz.*
4. t_{RHOH} *starts to be valid when frequency is lower than 33 MHz.*

6.6 Page Read Operation

Figure 6.6 Page Read Operation (Read One Page)

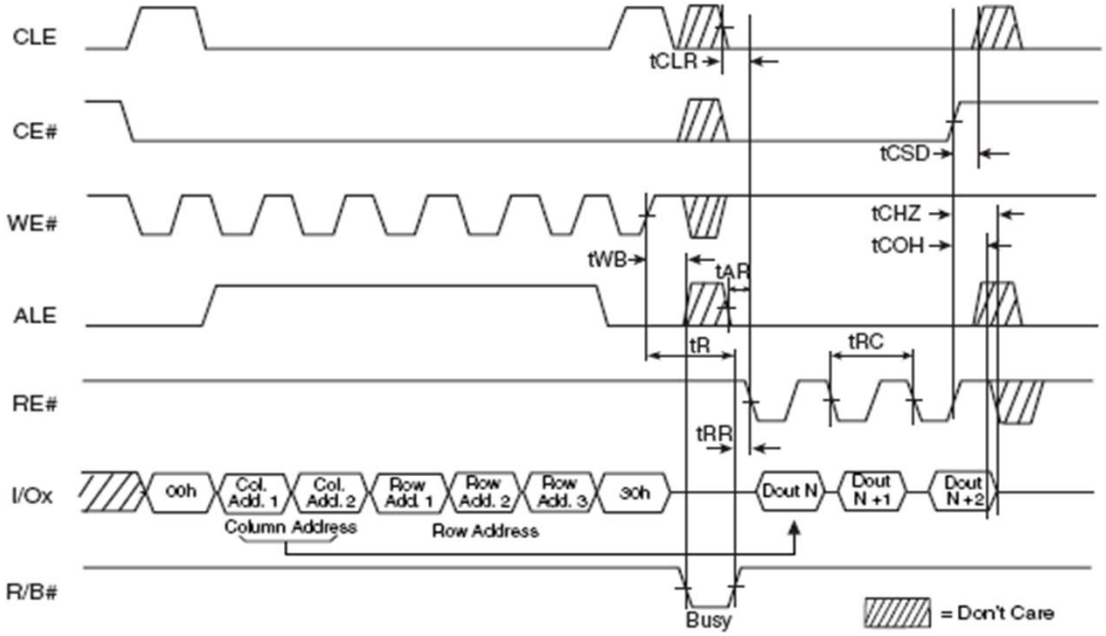


Note:

1. *If Status Register polling is used to determine completion of the read operation, the Read Command (00h) must be issued before data can be read from the page buffer.*

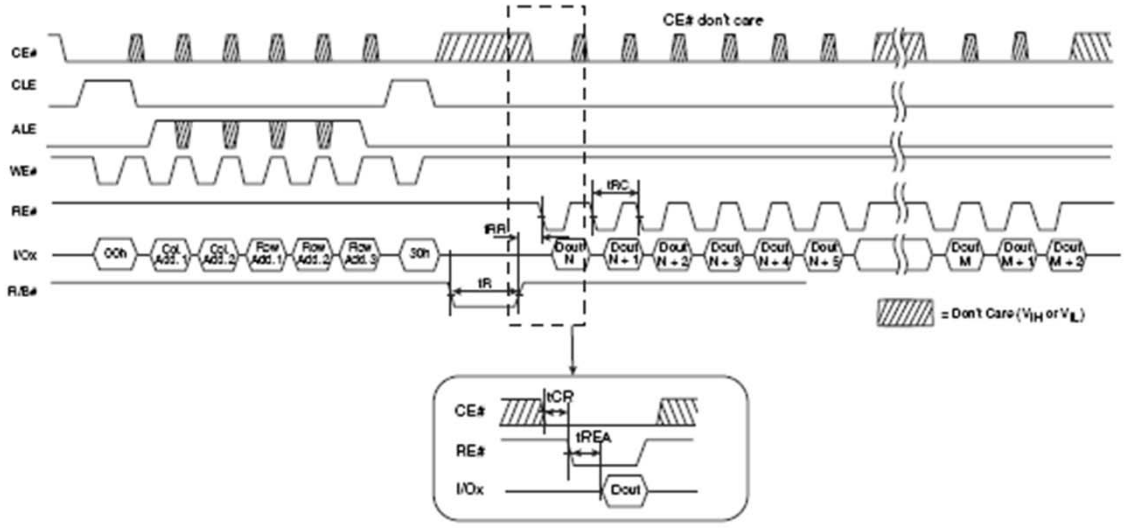
6.7 Page Read Operation (Interrupted by CE#)

Figure 6.7 Page Read Operation Interrupted by CE#



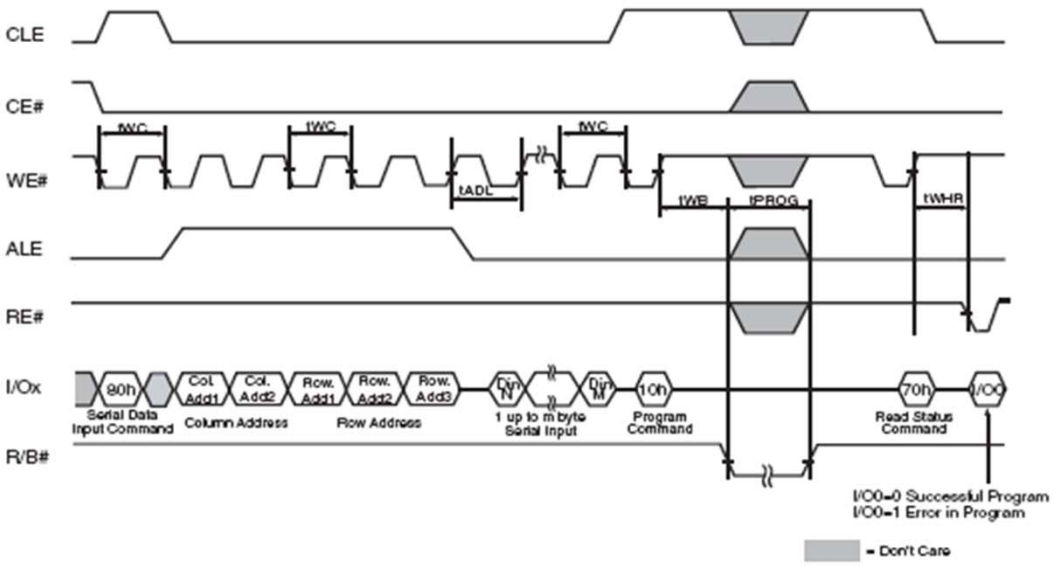
6.8 Page Read Operation Timing with CE# Don't Care

Figure 6.8 Page Read Operation Timing with CE# Don't Care



6.9 Page Program Operation

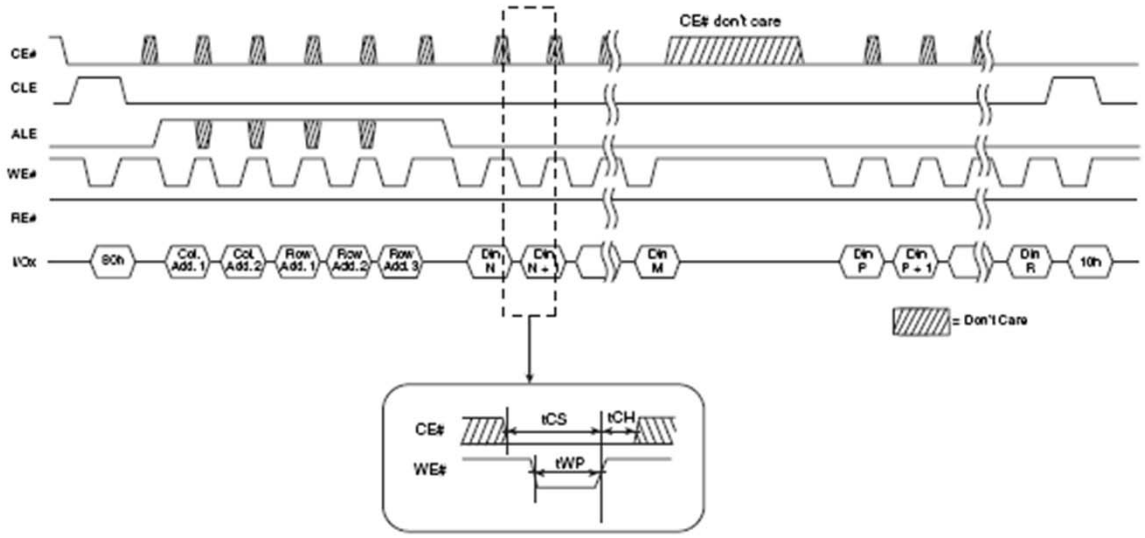
Figure 6.9 Page Program Operation



Note:
1. t_{ADL} *is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.*

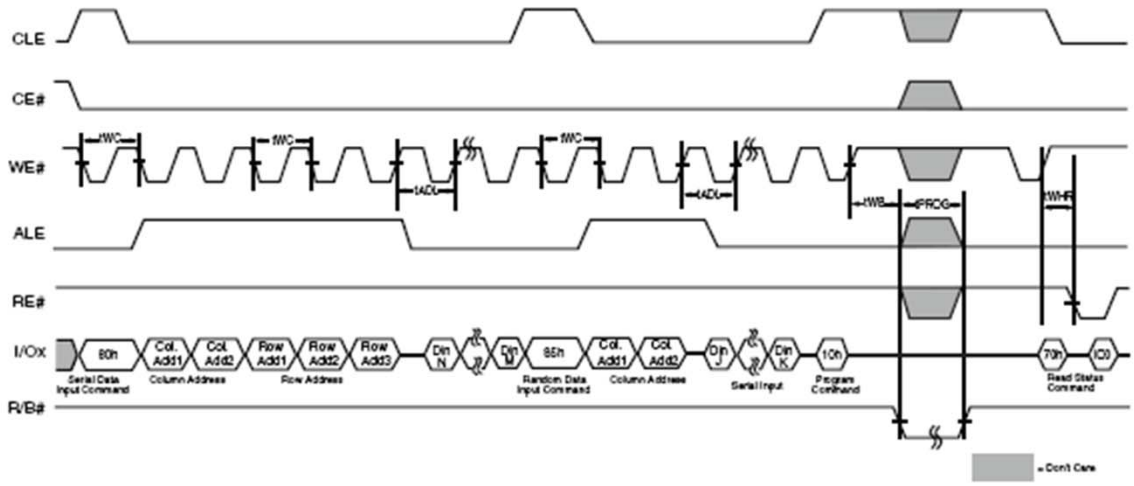
6.10 Page Program Operation Timing with CE# Don't Care

Figure 6.10 Page Program Operation Timing with CE# Don't Care



6.11 Page Program Operation with Random Data Input

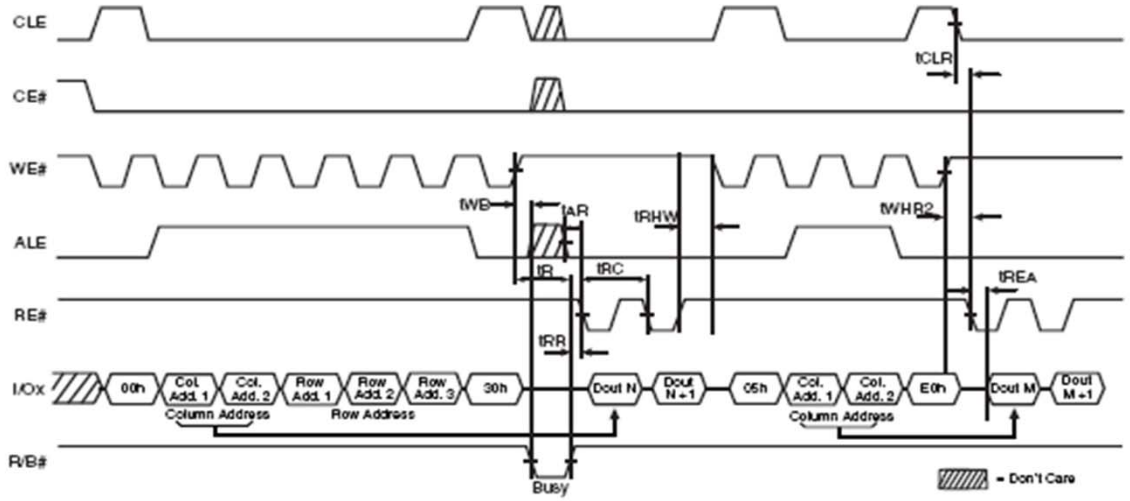
Figure 6.11 Random Data Input



Note:
1. t_{ADL} *is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.*

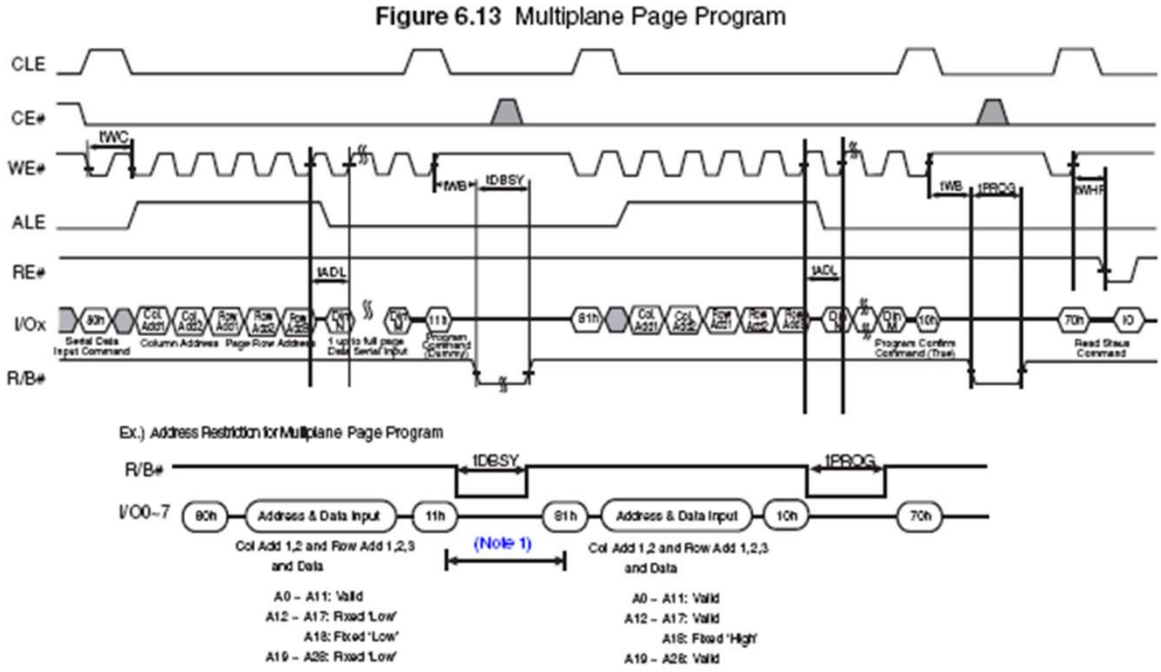
6.12 Random Data Output In a Page

Figure 6.12 Random Data Output



6.13 Multiplane Page Program Operation — FMND2GxxS3S and FMND4GxxS3S

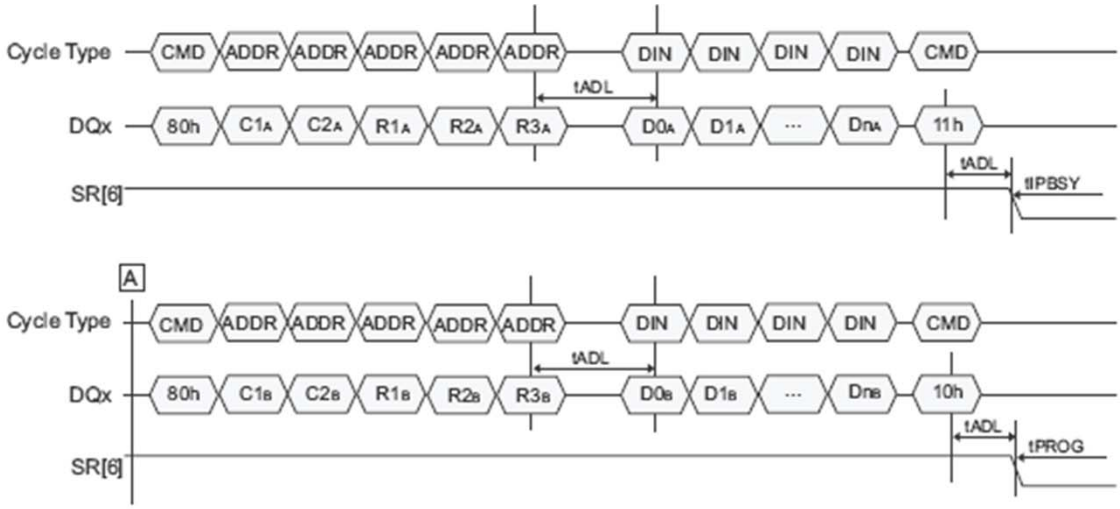
Figure 6.13 Multiplane Page Program



Notes:

1. *Any command between 11h and 81h is prohibited except 70h, 78h, and FFh.*
2. *A18 is the plane address bit for x8 devices. A17 is the plane address bit for x16 devices.*

Figure 6.14 Multiplane Page Program (ONFI 1.0 Protocol)

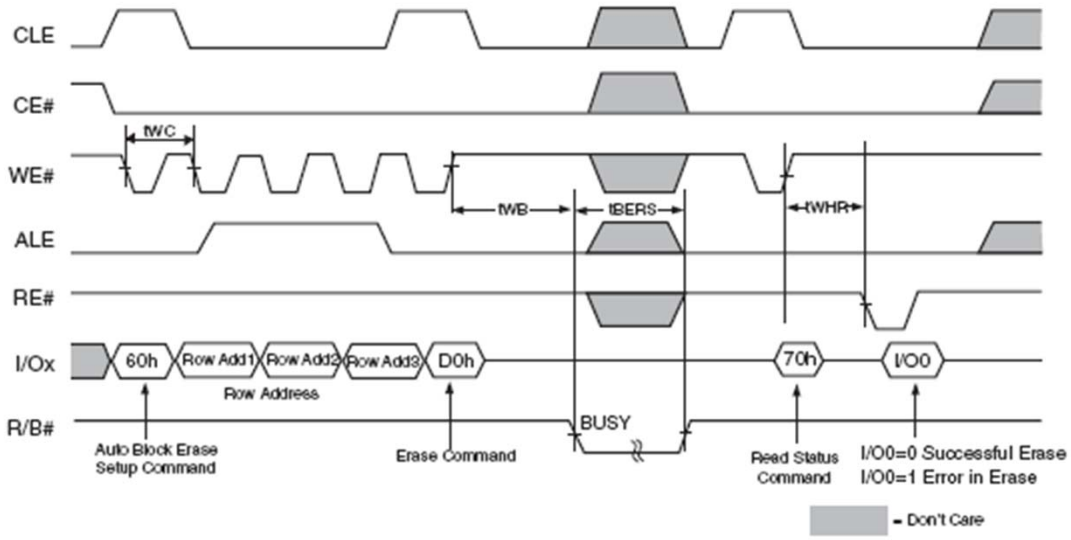


Notes:

1. *C1A-C2A Column address for page A. C1A is the least significant byte.*
2. *R1A-R3A Row address for page A. R1A is the least significant byte.*
3. *D0A-DnA Data to program for page A.*
4. *C1B-C2B Column address for page B. C1B is the least significant byte.*
5. *R1B-R3B Row address for page B. R1B is the least significant byte.*
6. *D0B-DnB Data to program for page B.*
7. *The block address bits must be the same except for the bit(s) that select the plane.*

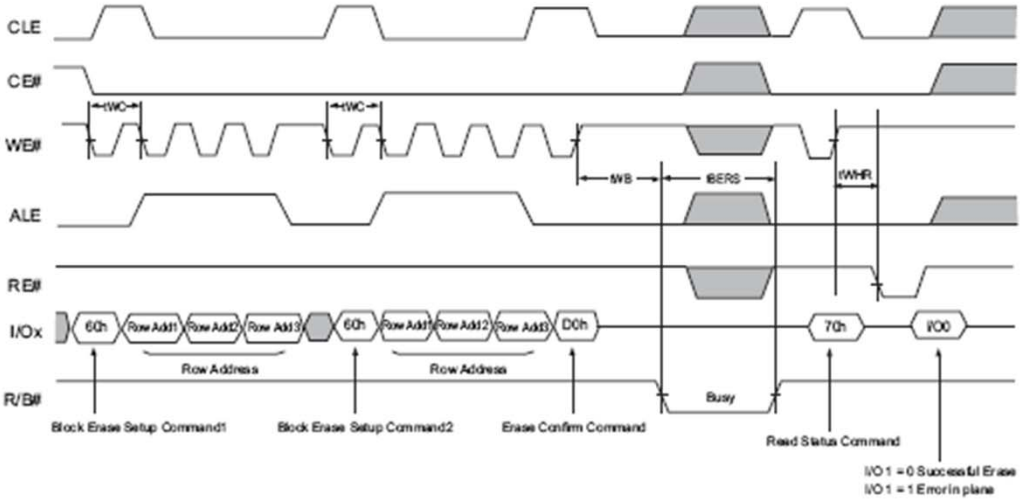
6.14 Block Erase Operation

Figure 6.15 Block Erase Operation (Erase One Block)

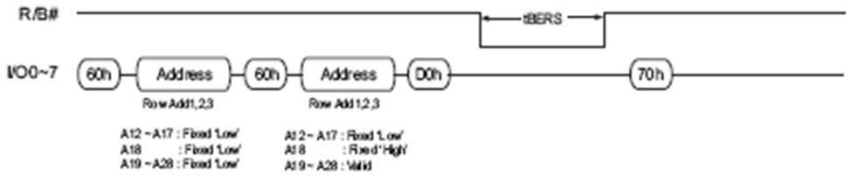


6.15 Multiplane Block Erase — FMND2GxxS3S and FMND4GxxS3S

Figure 6.16 Multiplane Block Erase



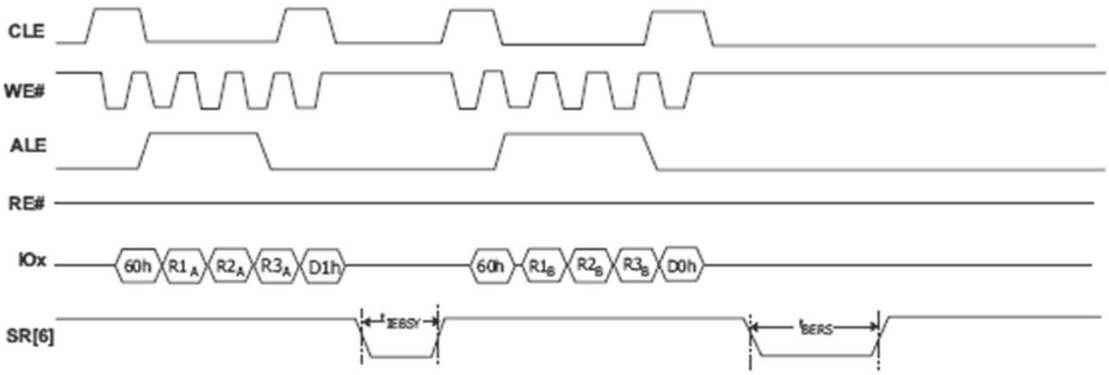
Ex.) Address Restriction for Multiplane Block Erase Operation



Note:

1. *A18 is the plane address bit for x8 devices. A17 is the plane address bit for x16 devices.*

Figure 6.17 Multiplane Block Erase (ONFI 1.0 Protocol)

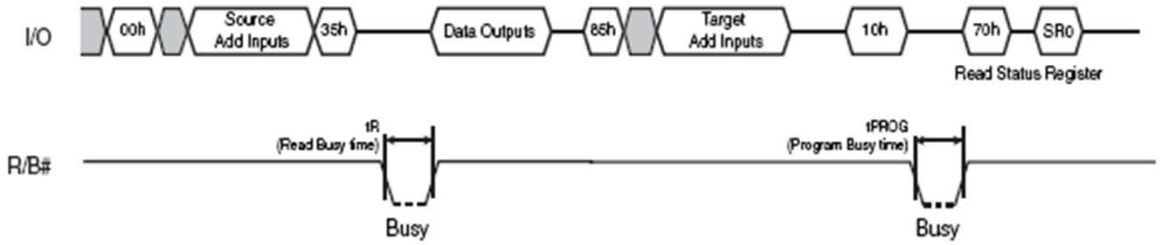


Notes:

1. *R1A-R3A Row address for block on plane 0. R1A is the least significant byte.*
2. *R1B-R3B Row address for block on plane 1. R1B is the least significant byte.*
3. *The block address bits must be the same except for the bit(s) that select the plane.*

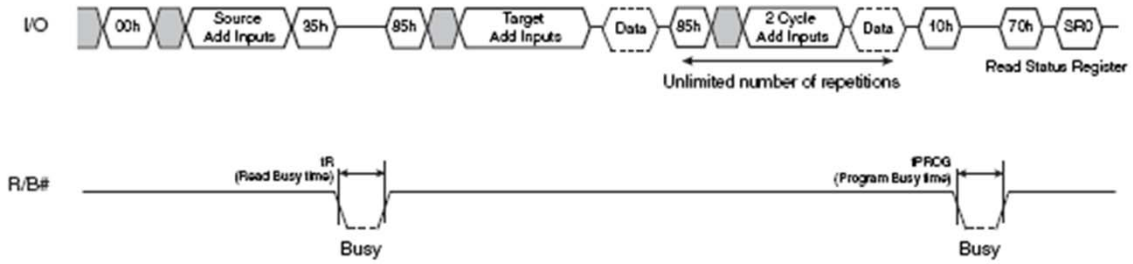
6.16 Copy Back Read with Optional Data Readout

Figure 6.18 Copy Back Read with Optional Data Readout



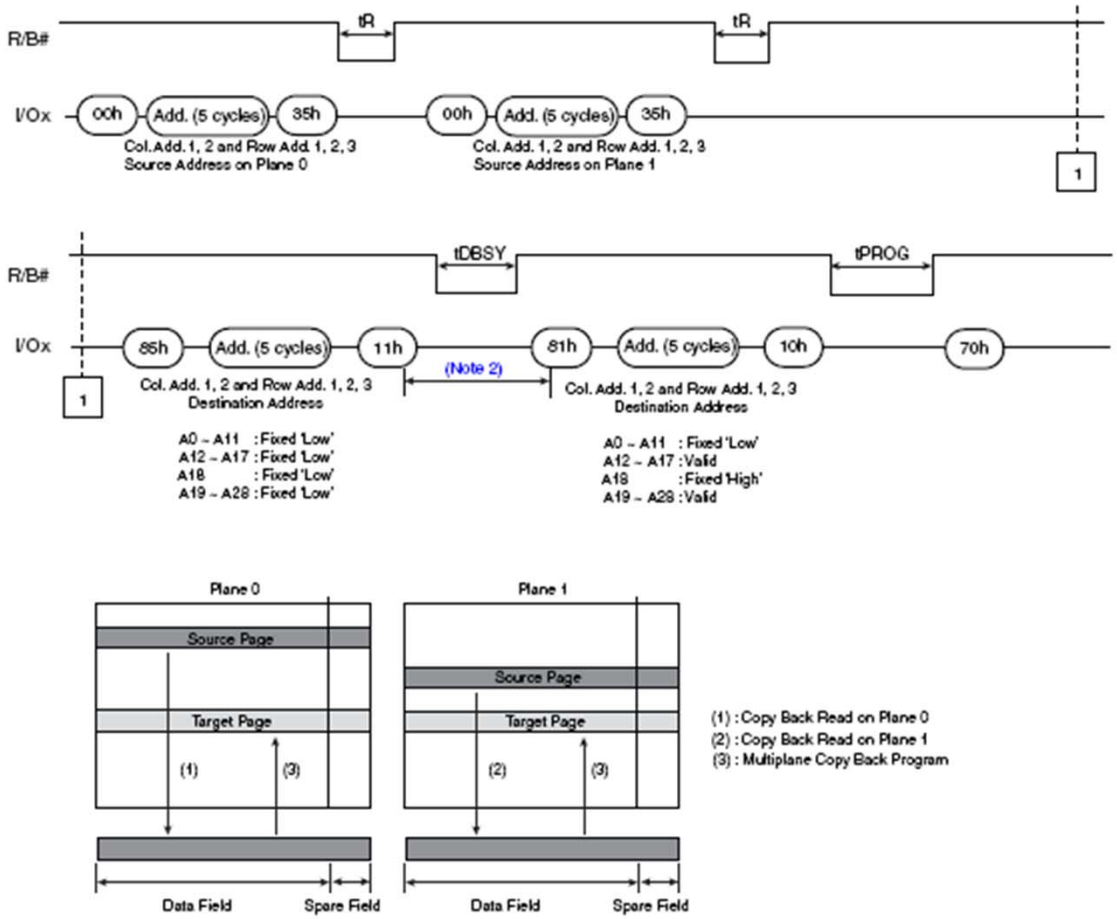
6.17 Copy Back Program Operation With Random Data Input

Figure 6.19 Copy Back Program with Random Data Input



6.18 Multiplane Copy Back Program — FMND2GxxS3S and FMND4GxxS3S

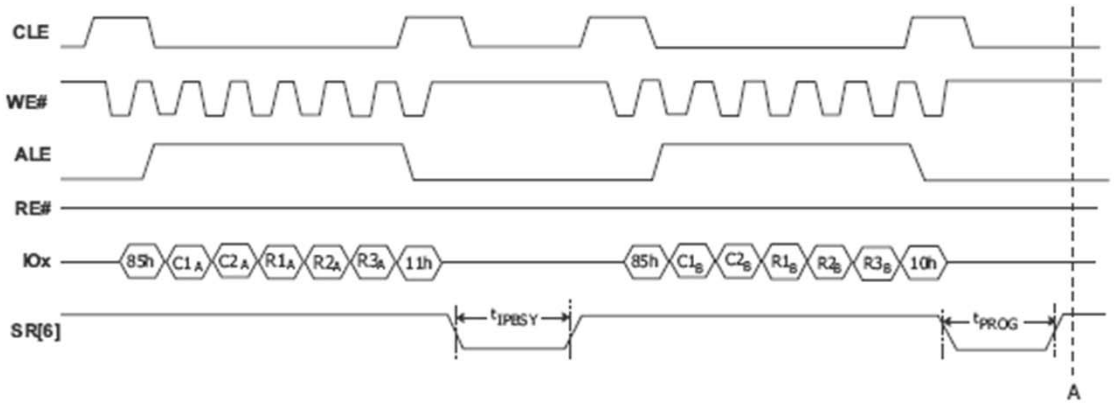
Figure 6.20 Multiplane Copy Back Program



Notes:

1. *Copy Back Program operation is allowed only within the same memory plane.*
2. *Any command between 11h and 81h is prohibited except 70h, 78h, and FFh.*
3. *A18 is the plane address bit for x8 devices. A17 is the plane address bit for x16 devices.*

Figure 6.21 Multiplane Copy Back Program (ONFI 1.0 Protocol)

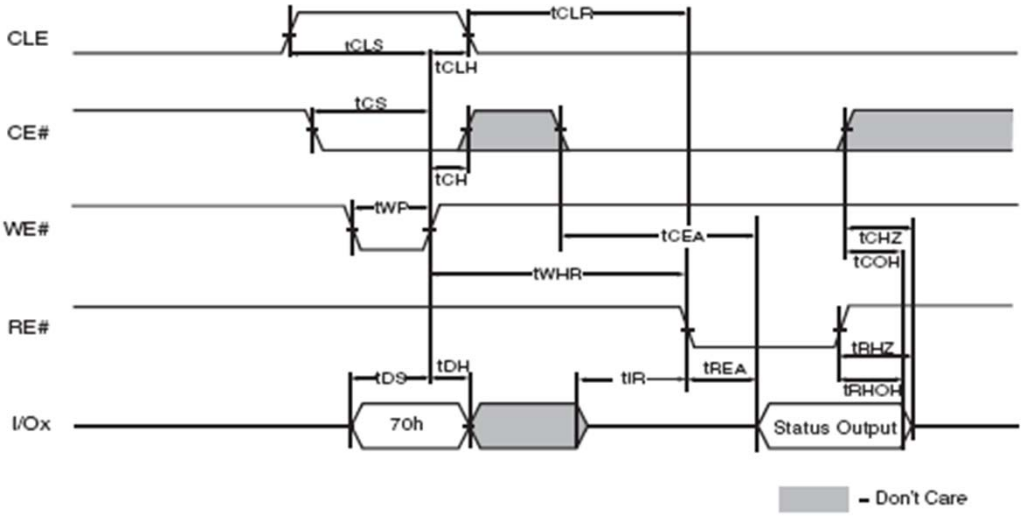


Notes:

1. *C1A-C2A Column address for page A. C1A is the least significant byte.*
2. *R1A-R3A Row address for page A. R1A is the least significant byte.*
3. *C1B-C2B Column address for page B. C1B is the least significant byte.*
4. *R1B-R3B Row address for page B. R1B is the least significant byte.*
5. *The block address bits must be the same except for the bit(s) that select the plane.*

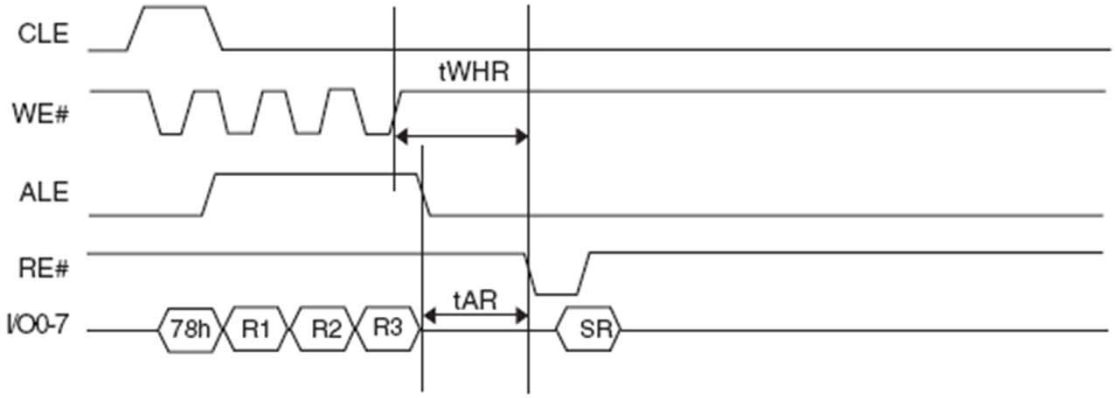
6.19 Read Status Register Timing

Figure 6.22 Status Read Cycle



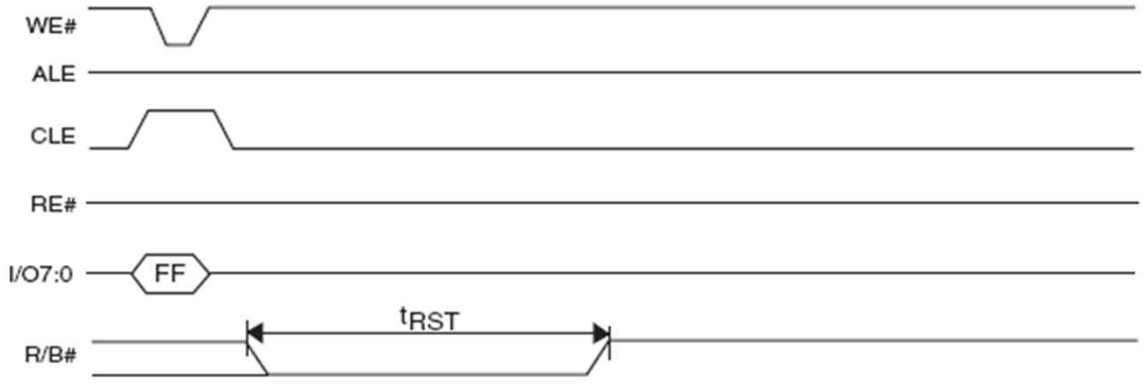
6.20 Read Status Enhanced Timing

Figure 6.23 Read Status Enhanced Timing



6.21 Reset Operation Timing

Figure 6.24 Reset Operation Timing



6.22 Read Cache

Figure 6.25 Read Cache Operation Timing

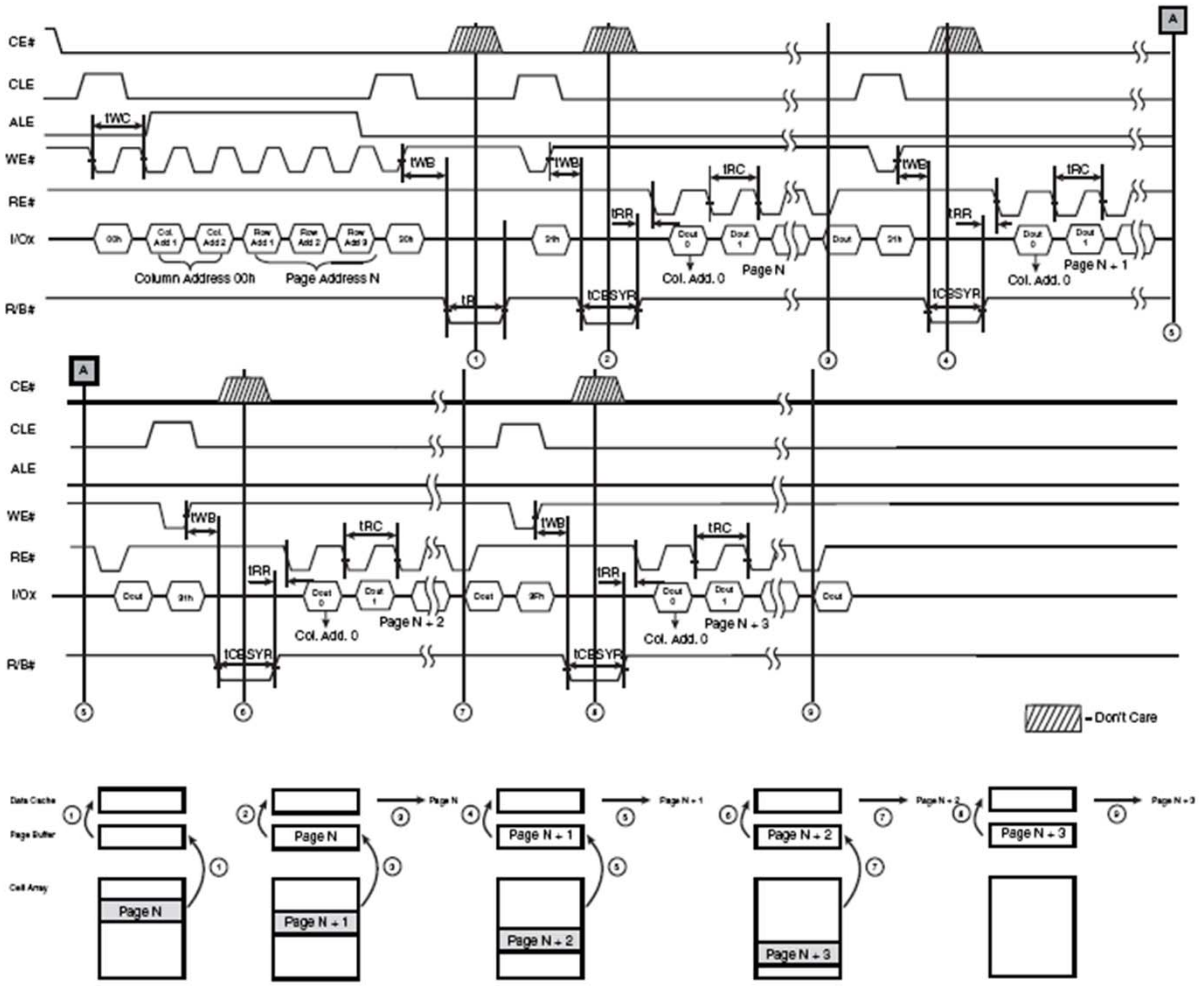


Figure 6.26 "Sequential" Read Cache Timing, Start (and Continuation) of Cache Operation

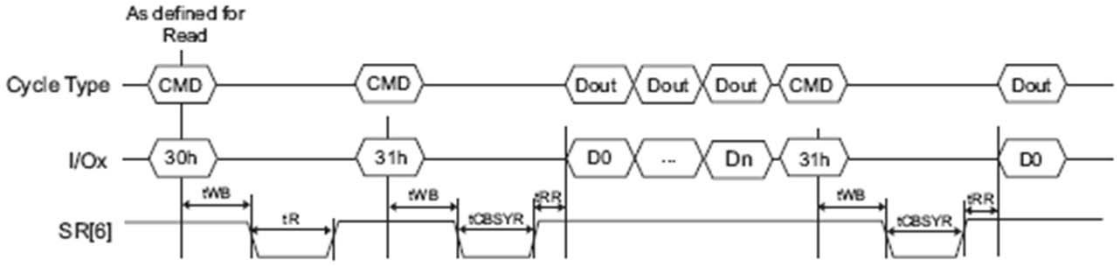


Figure 6.27 "Random" Read Cache Timing, Start (and Continuation) of Cache Operation

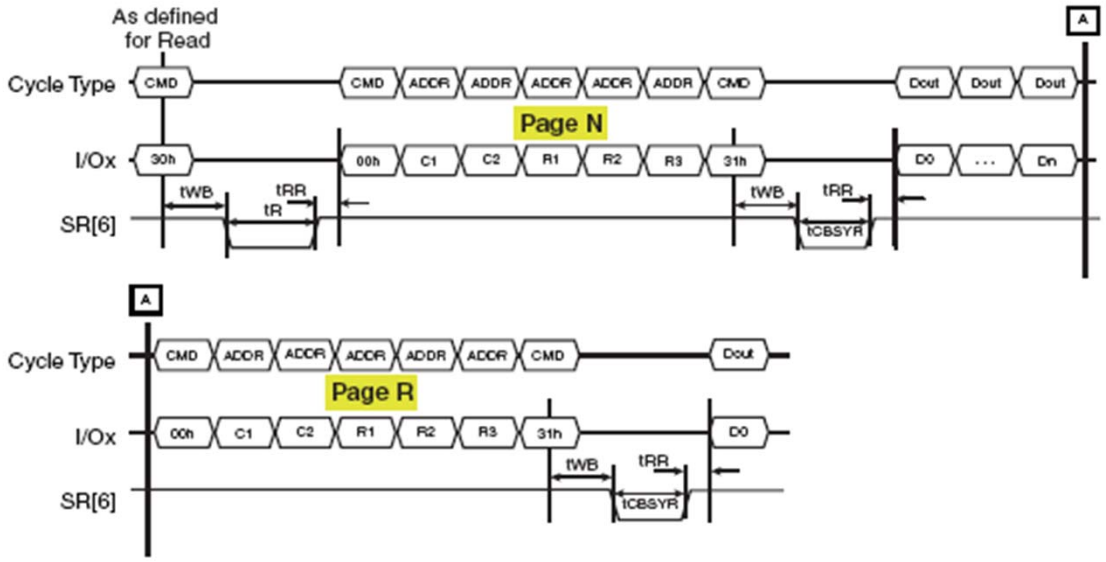
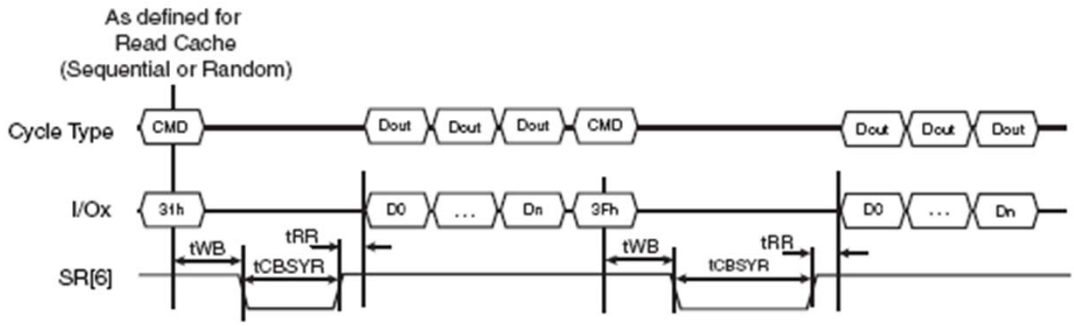
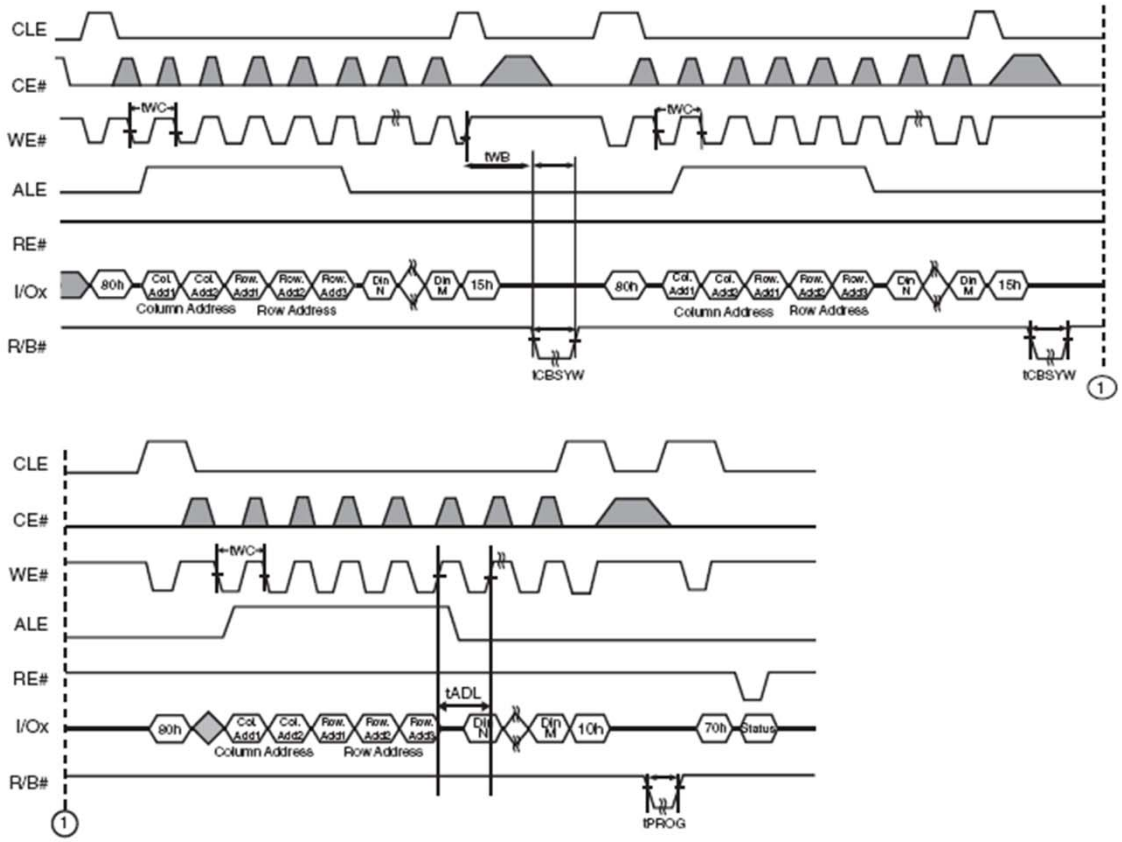


Figure 6.28 Read Cache Timing, End Of Cache Operation



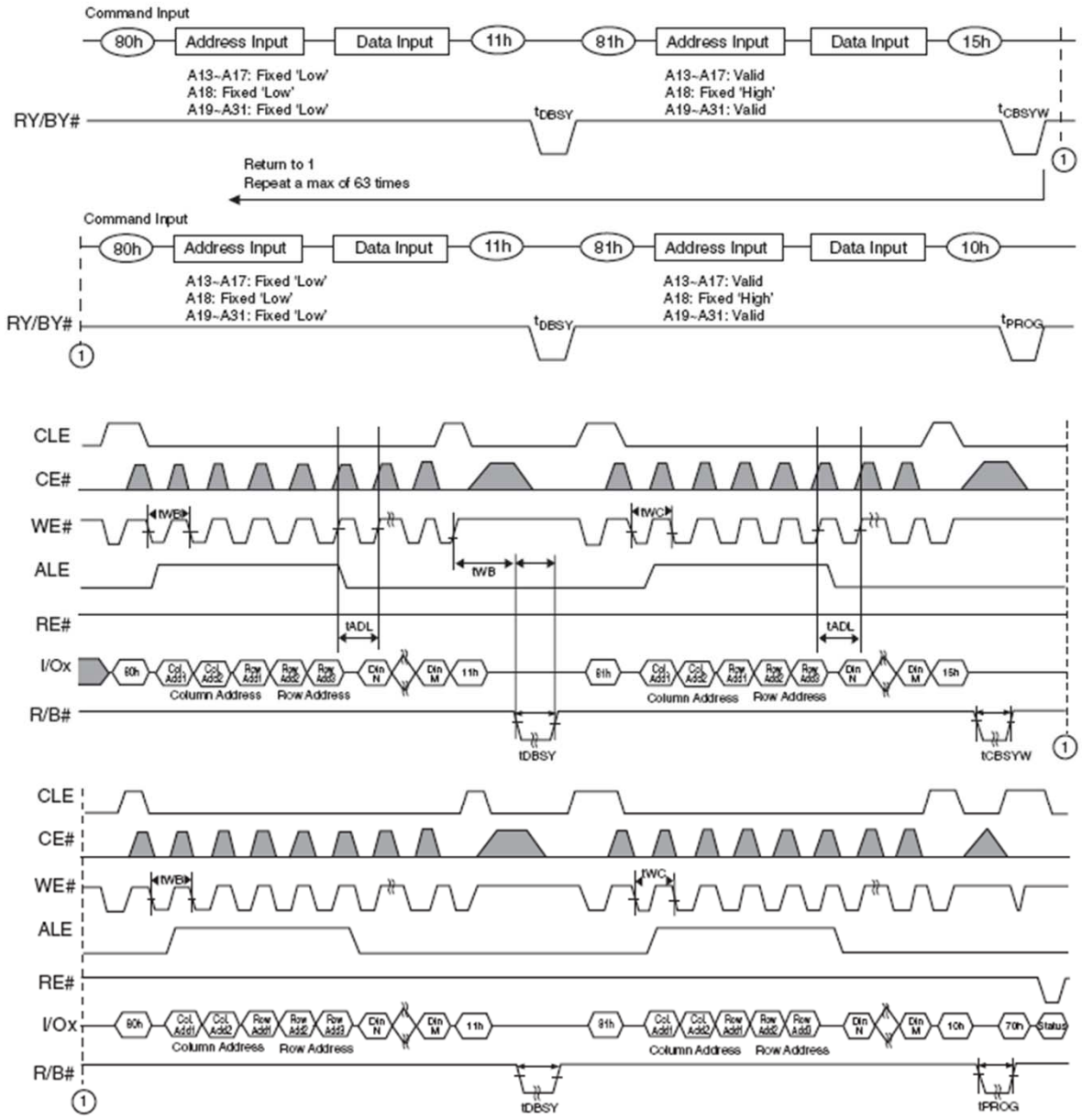
6.23 Cache Program

Figure 6.29 Cache Program



6.24 Multiplane Cache Program — FMND2GxxS3S and FMND4GxxS3S

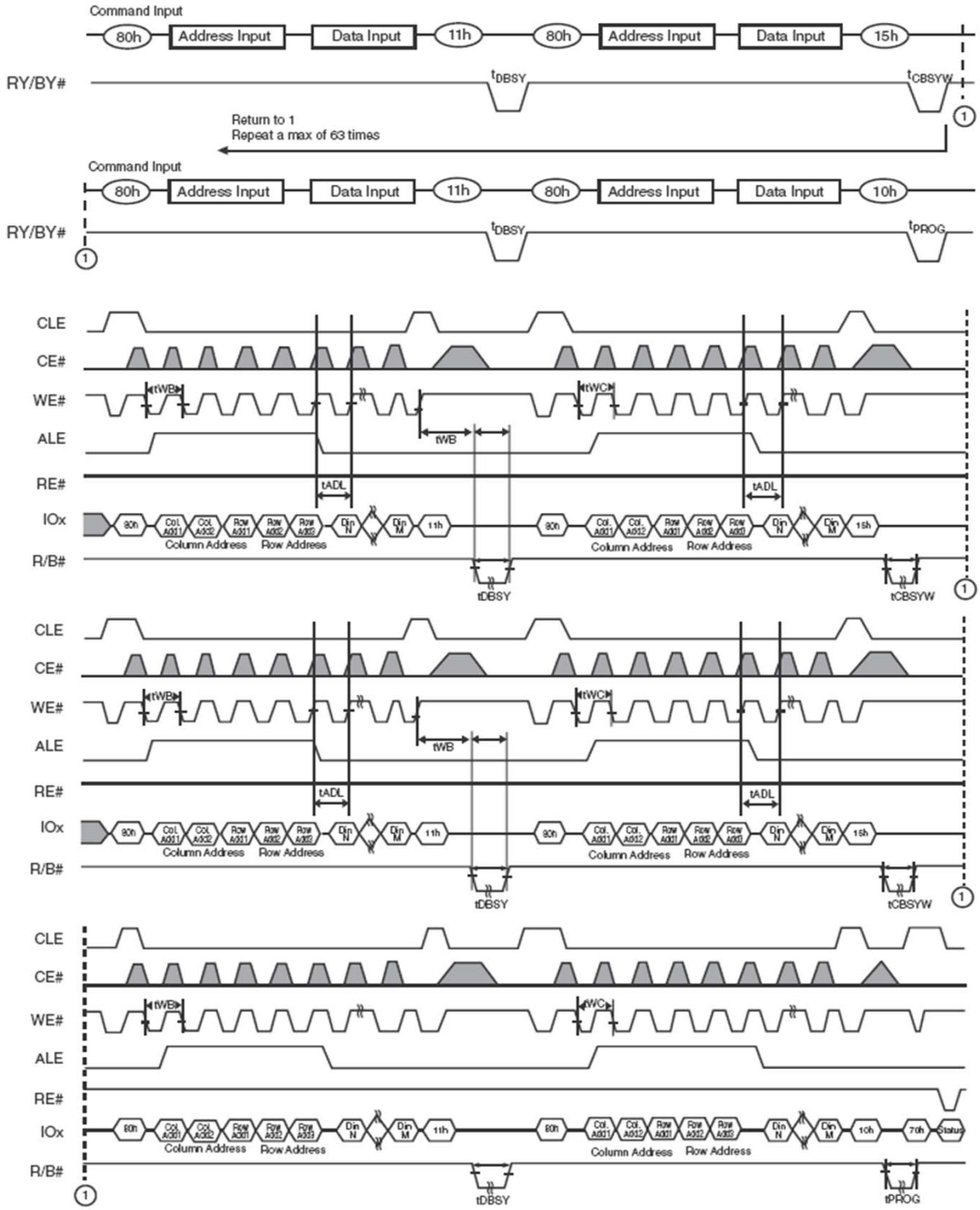
Figure 6.30 Multiplane Cache Program



Notes:

1. *Read Status Register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.*
2. *A18 is the plane address bit for x8 devices. A17 is the plane address bit for x16 devices.*

Figure 6.31 Multiplane Cache Program (ONFI 1.0 Protocol)

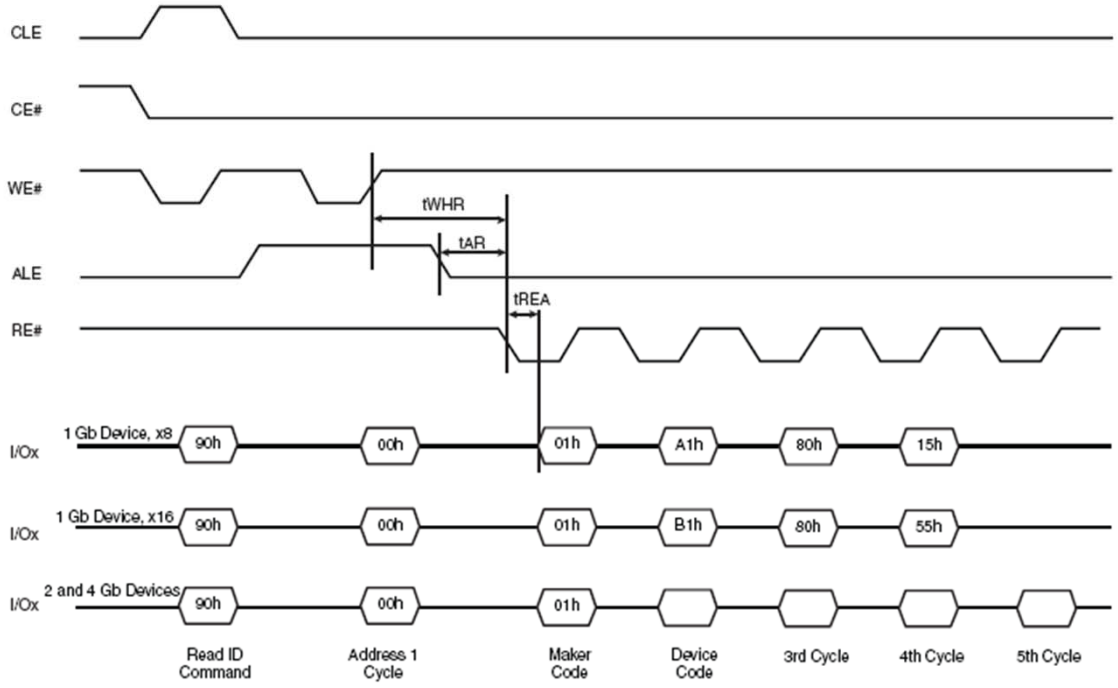


Notes:

1. *The block address bits must be the same except for the bit(s) that select the plane.*
2. *Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.*

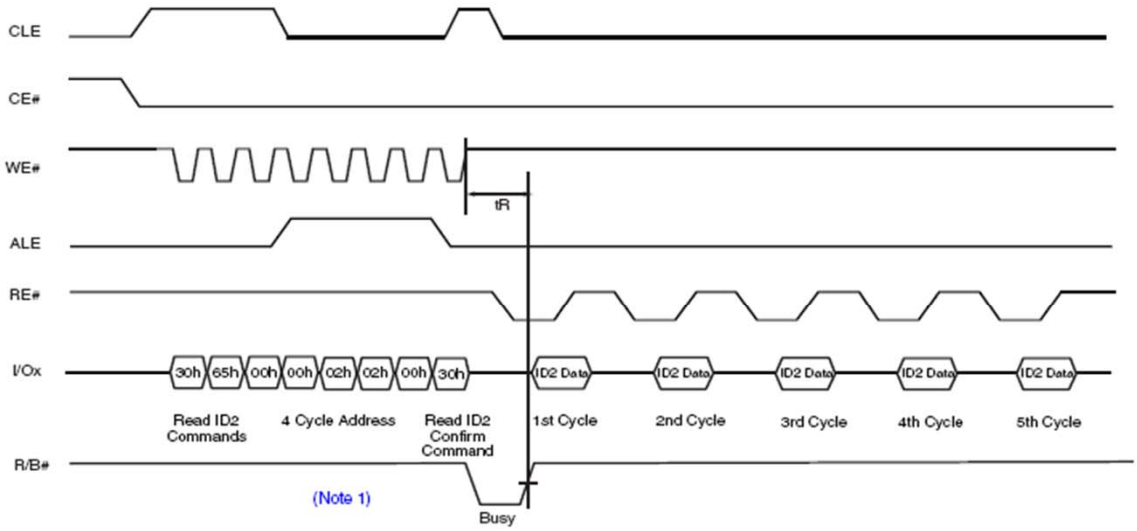
6.25 Read ID Operation Timing

Figure 6.32 Read ID Operation Timing



6.26 Read ID2 Operation Timing

Figure 6.33 Read ID2 Operation Timing

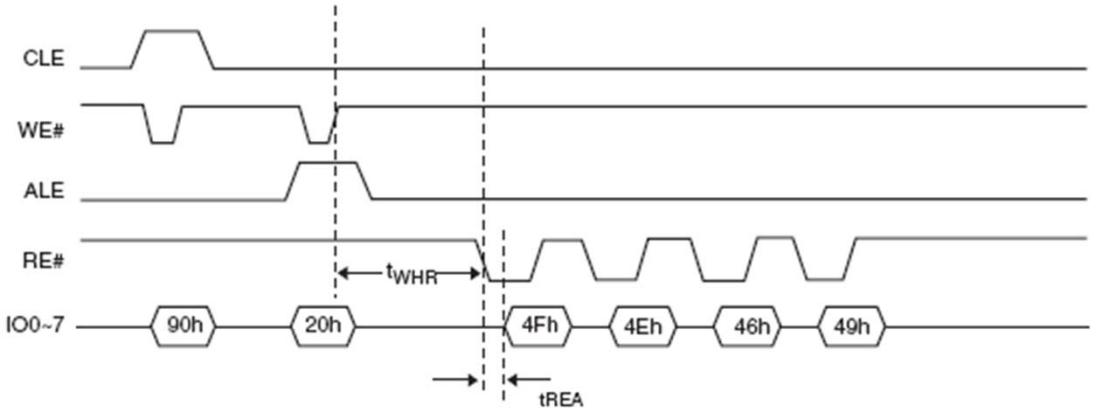


Notes:

1. *4-cycle address is shown for the S34MS01G2. For S34MS02G2 and S34MS04G2, insert an additional address cycle of 00h.*
2. *If Status Register polling is used to determine completion of the Read ID2 operation, the Read Command (00h) must be issued before ID2 data can be read from the flash.*

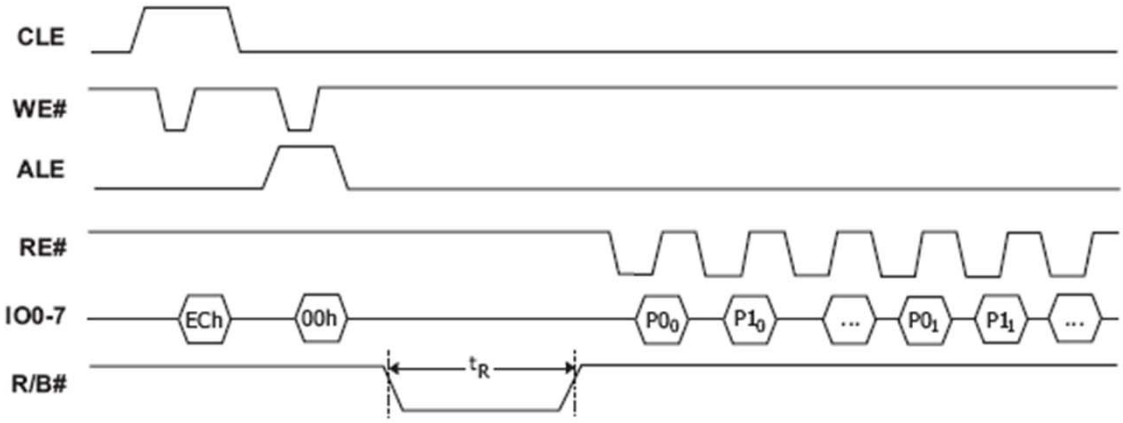
6.27 Read ONFI Signature Timing

Figure 6.34 ONFI Signature Timing



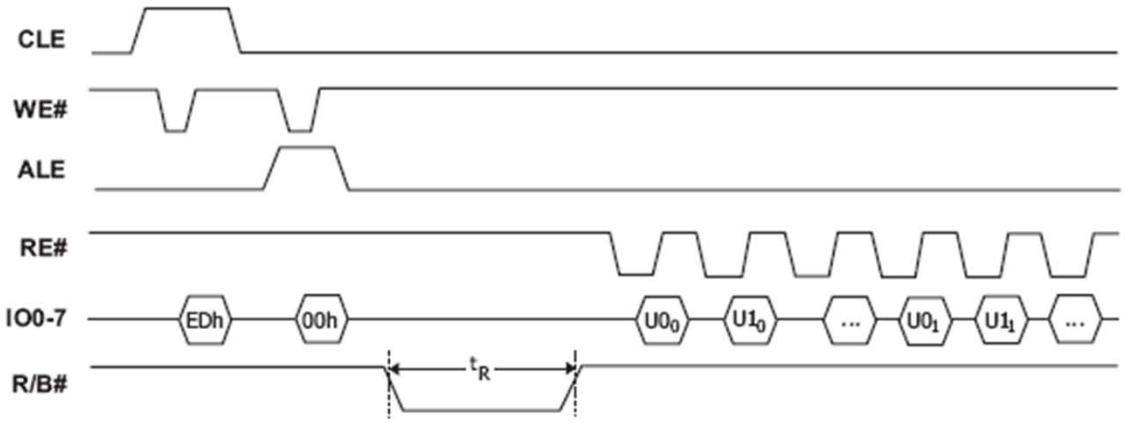
6.28 Read Parameter Page Timing

Figure 6.35 Read Parameter Page Timing



6.29 Read Unique ID Timing

Figure 6.36 Read Unique ID Timing

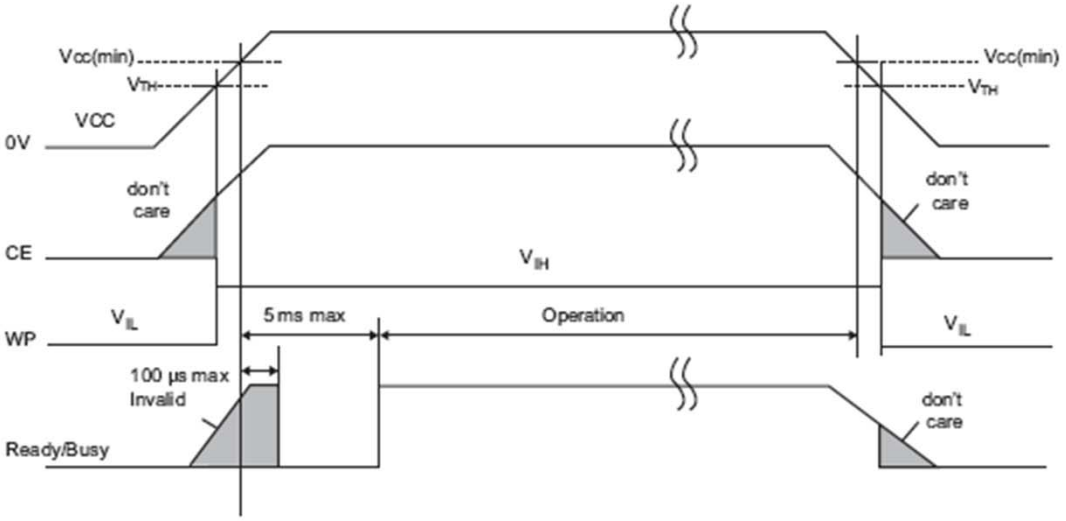


6.30 OTP Entry Timing

Figure 6.37 OTP Entry Timing

6.31 Power On and Data Protection Timing

Figure 6.38 Power On and Data Protection Timing



Note:
1. V_{TH} = 1.2 volts.

6.32 WP# Handling

Figure 6.39 Program Enabling / Disabling Through WP# Handling

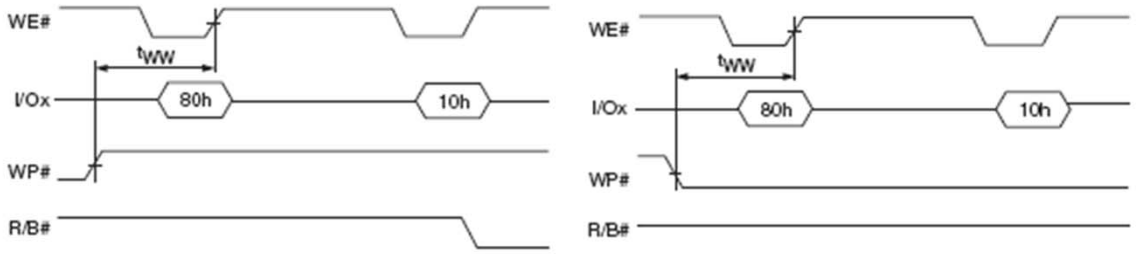
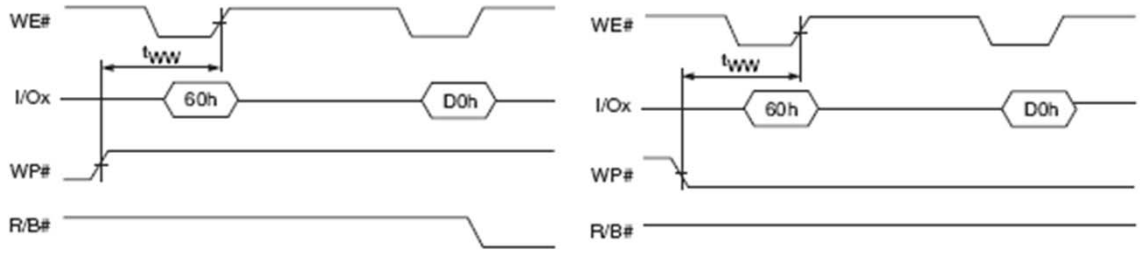


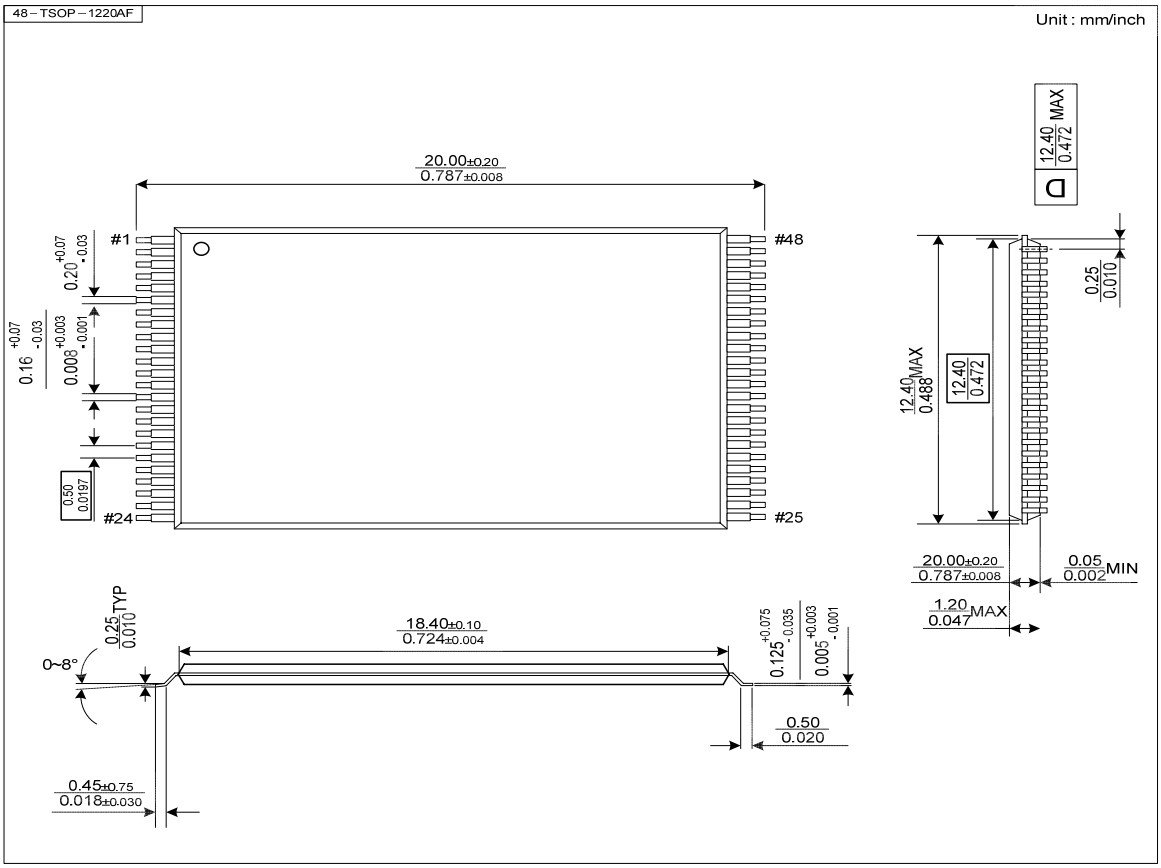
Figure 6.40 Erase Enabling / Disabling Through WP# Handling



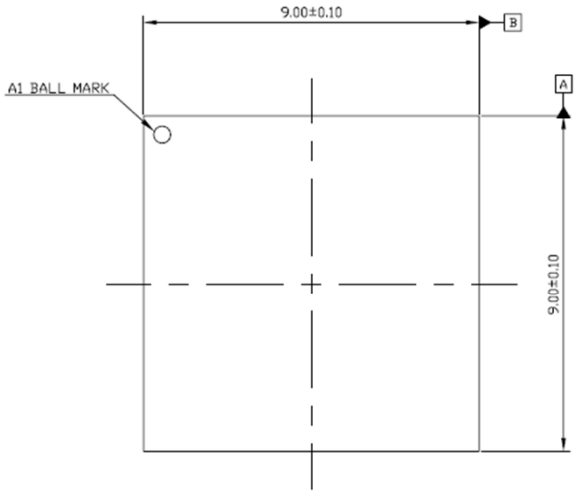
7. Physical Interface

7.1 Physical Diagram

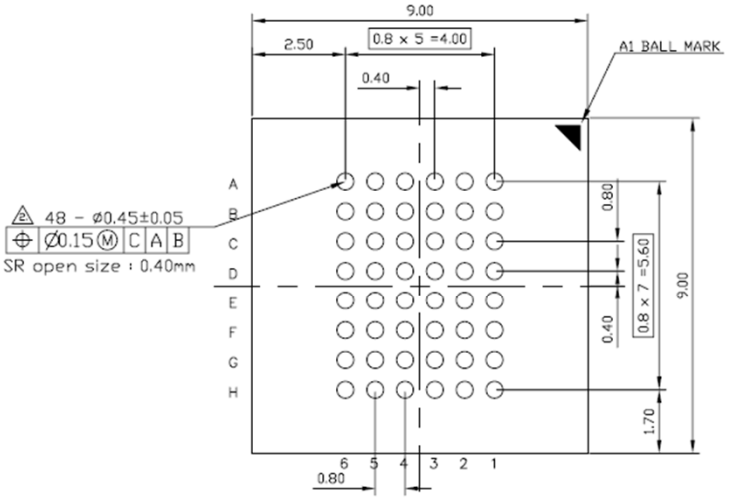
7.1.1 48-Pin TSOP1



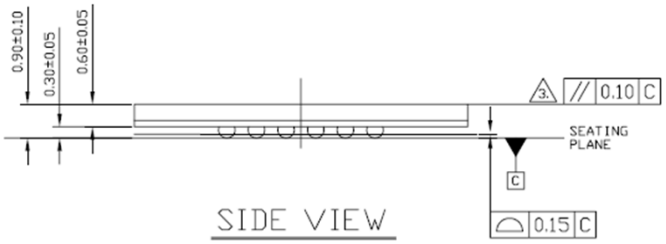
7.1.2 48-Pin BGA



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Description
FBGA 48BALL
Dimension
9.0mm x 9.0mm x 0.90mm (Max. 1.0mm T)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

8. System Interface

To simplify system interface, CE# may be unasserted during data loading or sequential data reading as shown in Figure 8.1. By operating in this way, it is possible to connect NAND flash to a microprocessor. Contrary to standard NAND, CE# don't care devices do not allow sequential read function.

Figure 8.1 Program Operation with CE# Don't Care

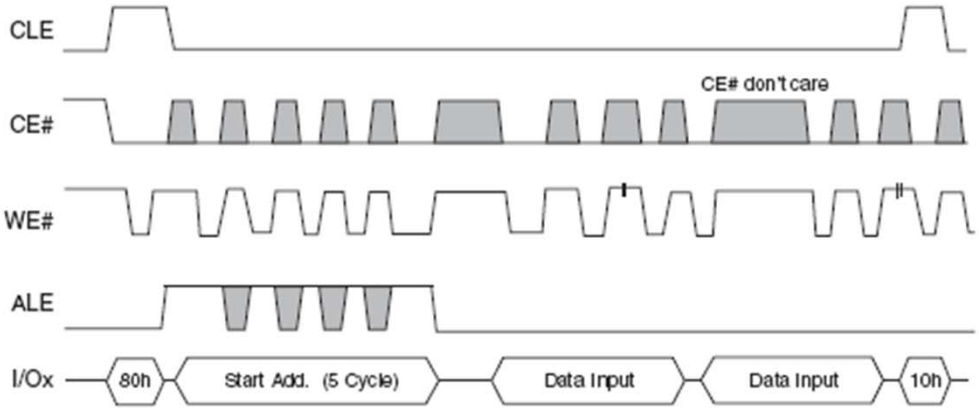


Figure 8.2 Read Operation with CE# Don't Care

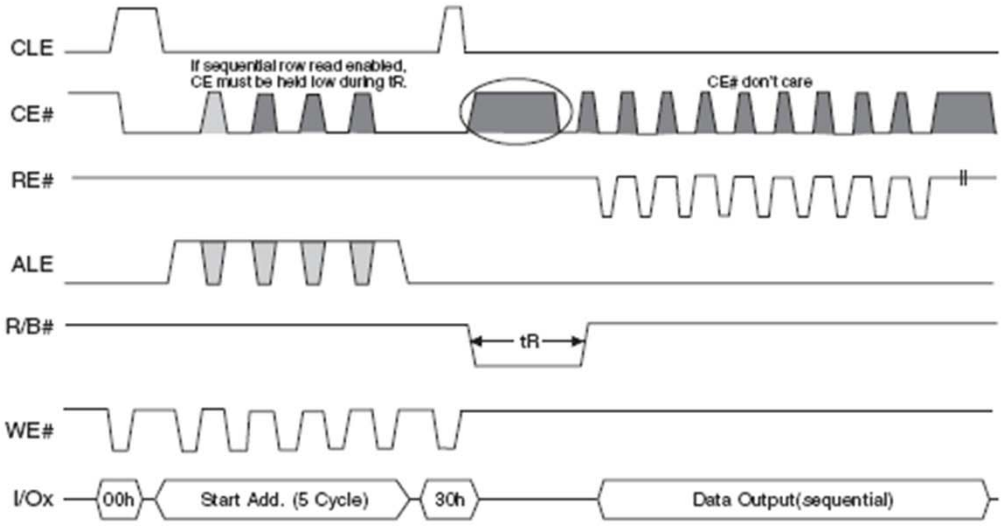
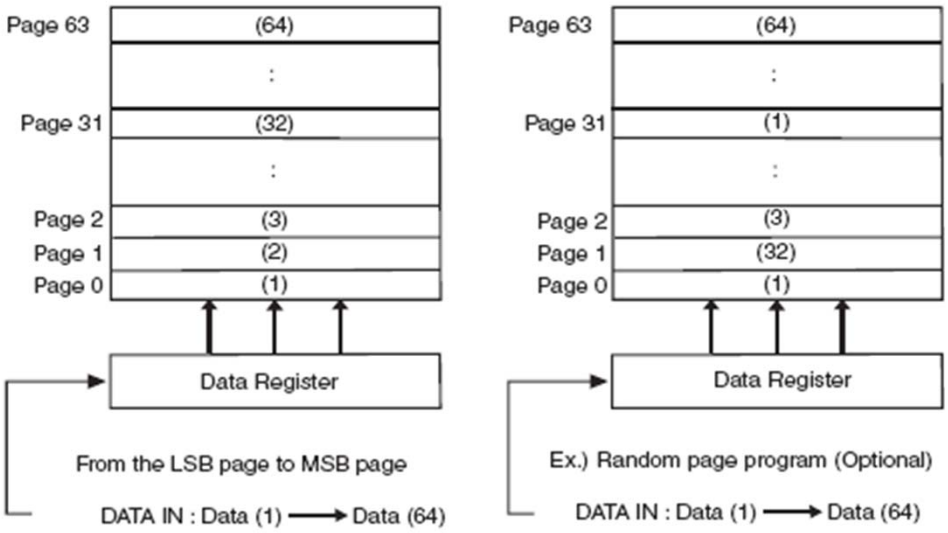


Figure 8.3 Page Programming Within a Block



9. Error Management

9.1 System Bad Block Replacement

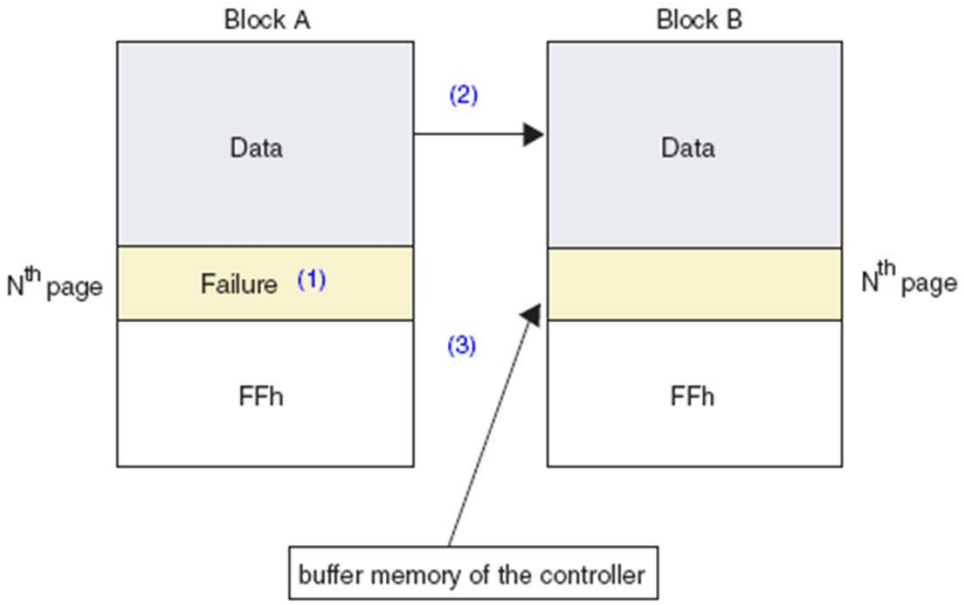
Over the lifetime of the device, additional Bad Blocks may develop. In this case, each bad block has to be replaced by copying any valid data to a new block. These additional Bad Blocks can be identified whenever a program or erase operation reports "Fail" in the Status Register.

The failure of a page program operation does not affect the data in other pages in the same block, thus the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. Refer to Table 9.1 and Figure 9.1 for the recommended procedure to follow if an error occurs during an operation.

Table 9.1 Block Failure

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (4 bit / 512+16 byte)

Figure 9.1 Bad Block Replacement



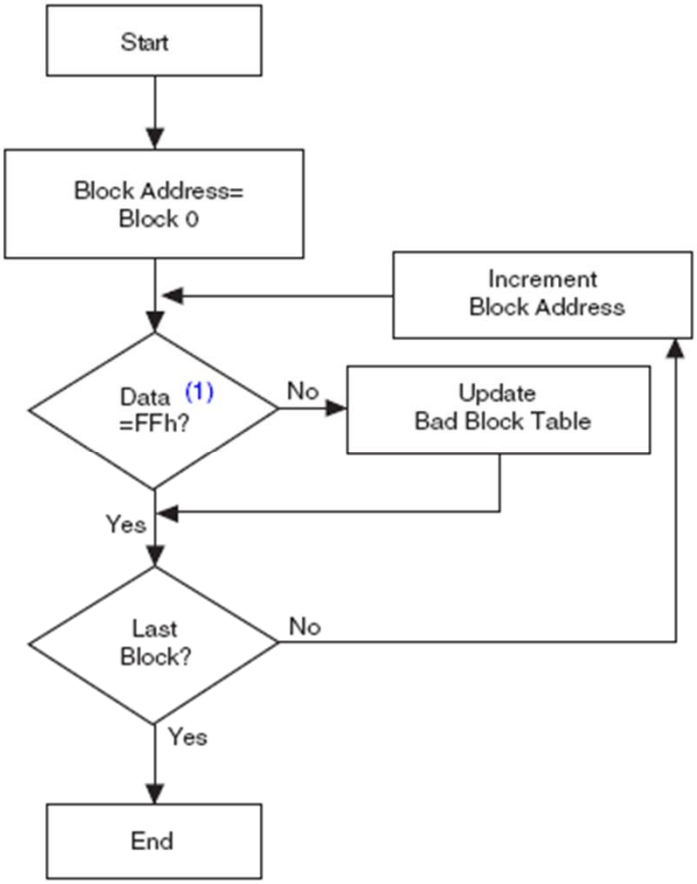
Notes:

1. *An error occurs on the Nth page of Block A during a program operation.*
2. *Data in Block A is copied to the same location in Block B, which is a valid block.*
3. *The Nth page of block A, which is in controller buffer memory, is copied into the Nth page of Block B.*
4. *Bad block table should be updated to prevent from erasing or programming Block A.*

9.2 Bad Block Management

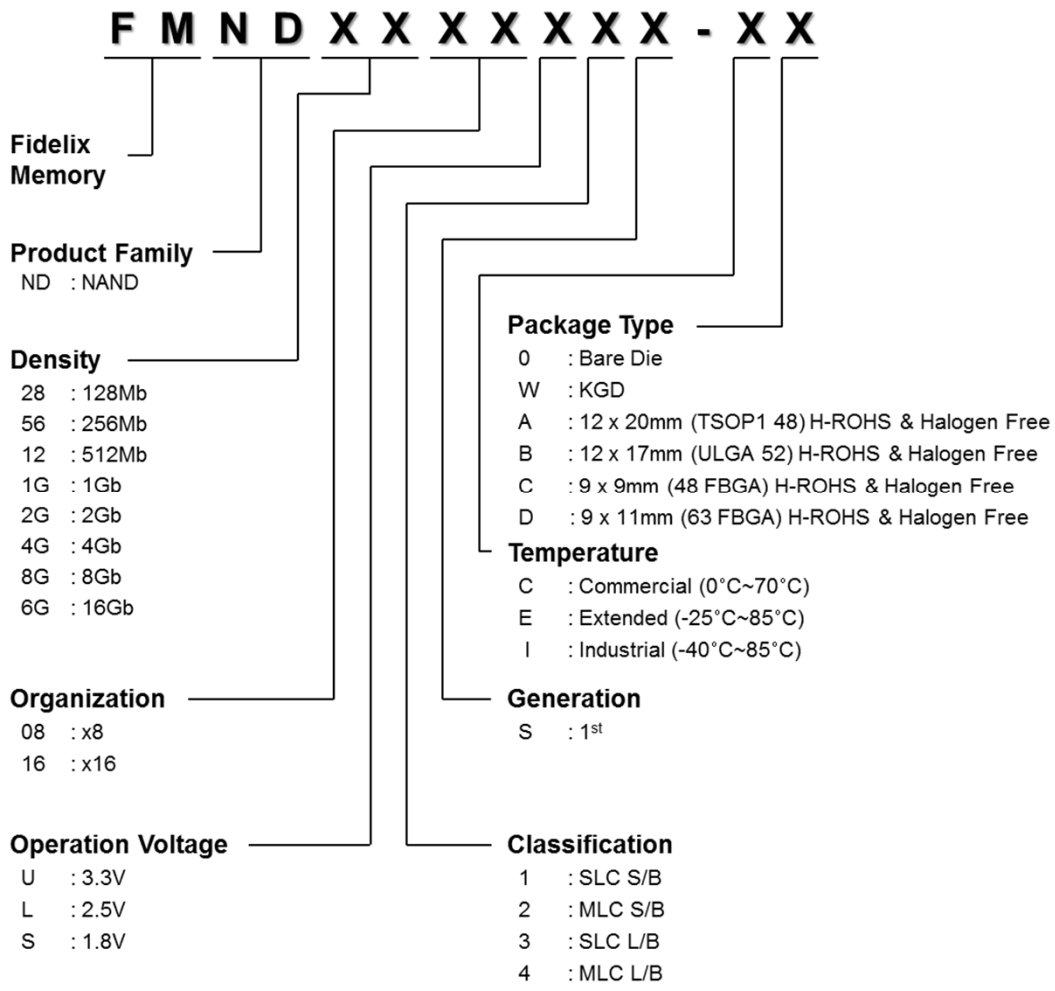
Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 1st byte in the spare area of the 1st or 2nd or last page does not contain FFh is a Bad Block. That is, if the first page has an FF value and should have been a non-FF value, then the non-FF value in the second page or the last page will indicate a bad block. The Bad Block Information must be read before any erase is attempted, as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information, it is recommended to create a Bad Block table following the flowchart shown in Figure 9.2. The host is responsible to detect and track bad blocks, both factory bad blocks and blocks that may go bad during operation. Once a block is found to be bad, data should not be written to that block. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

Figure 9.2 Bad Block Management Flowchart



Note:
1. Check for FFh at the 1st byte in the spare area of the 1st, 2nd, and last pages.

10. Part Numbering System



512M(32Mx16) Low Power DDR SDRAM

Revision 0.3

Jun. 2013

Document Title

512M(32Mx16) Low Power DDR SDRAM

Revision History

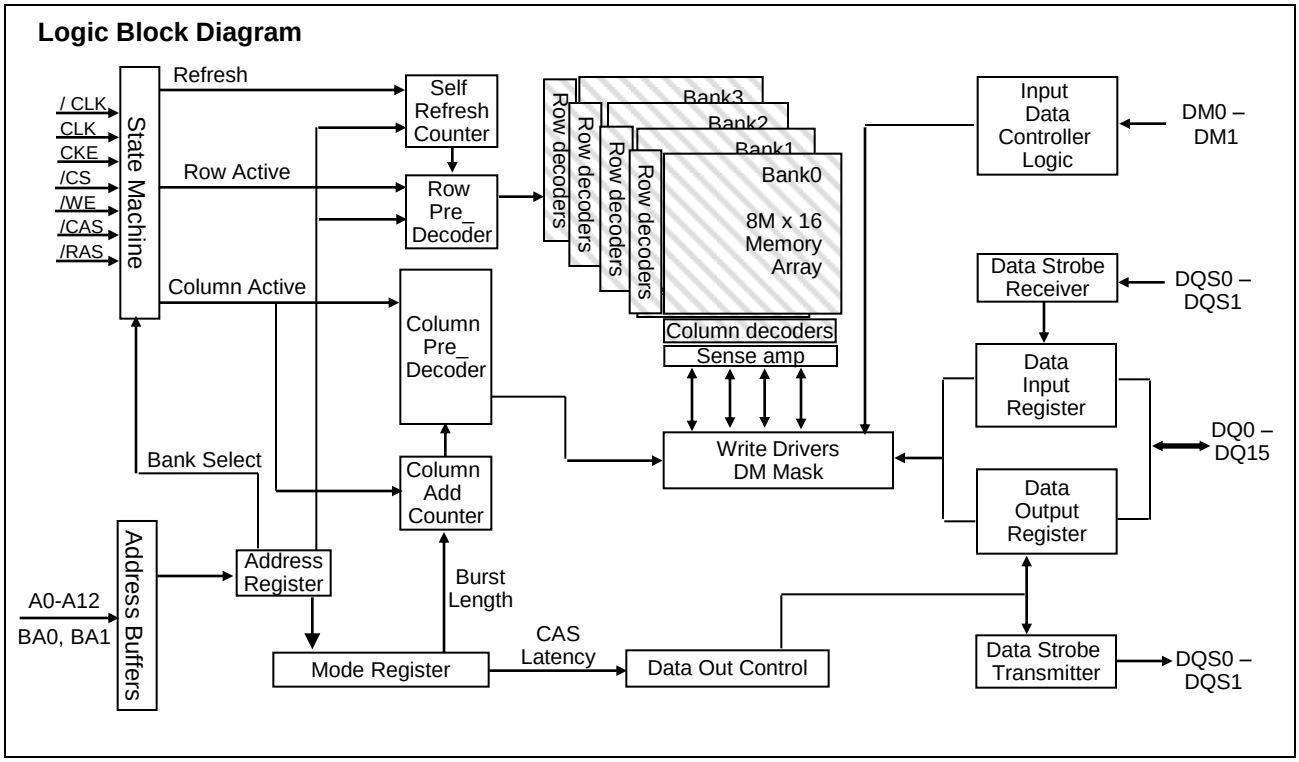
Revision No.	History	Draft date	Remark
0.0	Initial Draft	Dec. 15th, 2011	Preliminary
0.1	Adjusted DC parameters(IDD0, IDD4R, IDD4W, IDD6)	Jun. 28th, 2012	
0.2	Changed tWTR (1CLK → 2CLKs)	Jul. 27th, 2012	
0.3	Revise typo(remove max of tSRR, tSRC)	Jun. 17th, 2013	Final

DDR Sync DRAM Features

- **Functionality**
  - Double-data-rate architecture ; two data transfers per CLK cycle.
  - Bidirectional data strobe per byte data (DQS).
  - No DLL ; CLK to DQS is not Synchronized.
  - Differential CLK inputs(CLK and /CLK).
  - Commands entered on each positive CLK edge.
  - DQS edge-aligned with data for Reads; center-aligned with data for Writes.
  - Four internal banks for concurrent operation.
  - Data masks (DM) for masking write data-one mask per byte.
  - Programmable burst lengths : 2, 4, 8, 16.
  - Programmable CAS Latency : 2, 3.
  - Concurrent auto pre-charge option is supported.
  - Auto refresh and self refresh modes.
  - Status read register (SRR)
  - LVCMOS-compatible inputs.
- **Configuration**
  - 32 Meg X 16 (8 Meg X 16 X 4Bank).
- **Low Power Features**
  - Low voltage power supply.
  - Auto TCSR (Temperature Compensated Self Refresh).
  - Partial Array Self Refresh power-saving mode.
  - Deep Power Down Mode.
  - Driver Strength Control.
- **Operating Temperature Ranges**
  - Commercial (0℃ to +70℃).
  - Extended (-25℃ to +85℃).
  - Industrial (-40℃ to +85℃).
- **Package**
  - 60-Ball FBGA (8 X 9 X 0.8mm)
- **Functional Description**

The FMD8B16LBx Family is high-performance CMOS Dynamic RAMs (DRAM) organized as 32M x 16. These devices feature advanced circuit design to provide low active current and extremely low standby current. The device is compatible with the JEDEC standard Low Power DDR SDRAM specifications.

Logic Block Diagram



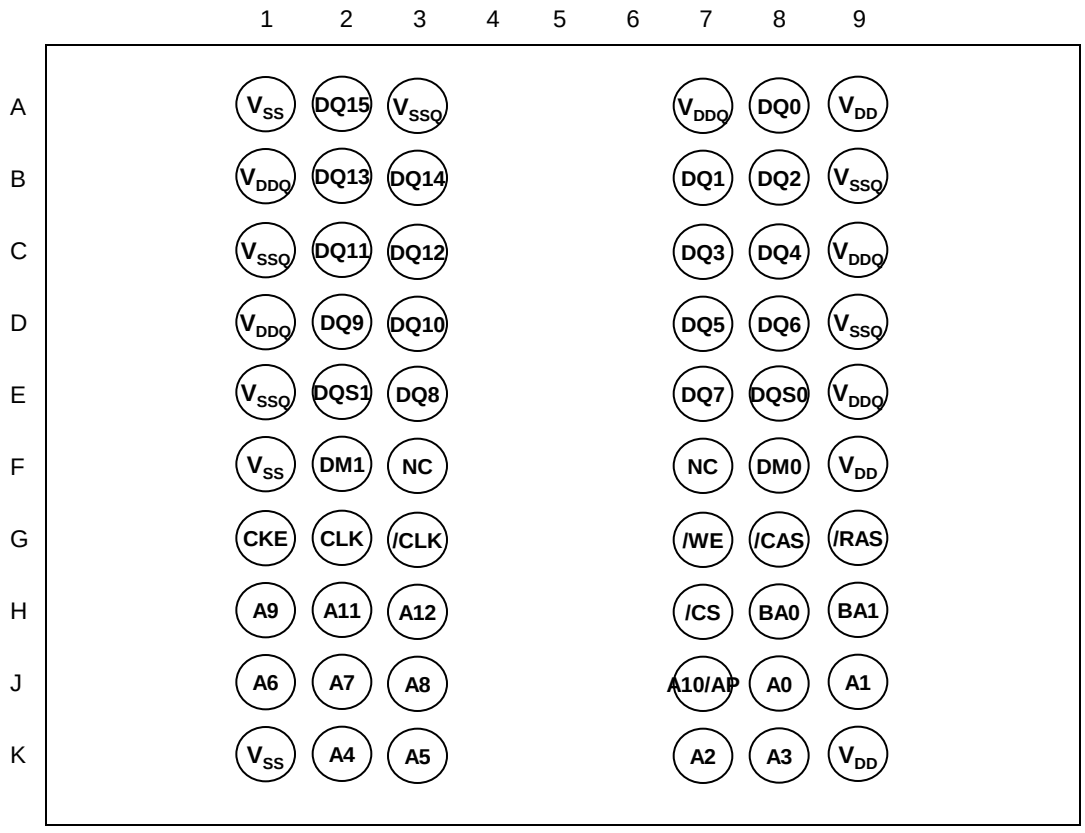
Selection Guide

Device	Voltage		Clock Frequency	Access Time(t_{AC})		tRCD	tRP
	V_{DD}	V_{DDQ}		CL=2	CL=3		
FMD8C16LAx-25Ex	1.70-1.95V	1.70-V_{DD}	200MHz		5.0ns	15ns	15ns
			83MHz	6.0ns		15ns	15ns

Pin Configuration

60 ball 0.8mm pitch FBGA(8mm x 9mm)

Top View



General Description

The 512Mb Low Power DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the 134,217,728-bit banks is organized as 8,192 rows by 1,024 columns by 16 bits.

The 512Mb Low Power DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer four data words per clock cycle at the I/O balls. A single read or write access for the 512Mb DDR SDRAM effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the Low Power DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes.

The 512Mb Low Power DDR SDRAM operates from a differential clock (CLK and /CLK); the crossing of CLK going HIGH and /CLK going LOW will be referred to as the positive edge of CLK. Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

Read and write accesses to the Low Power DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The Low Power DDR SDRAM provides for programmable READ or WRITE burst lengths of 2,4,8 or 16. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of Low Power DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto-refresh mode is provided, along with a power saving power-down mode. Self refresh mode offers temperature compensation through an on-chip temperature sensor and partial array self refresh, which allow users to achieve additional power saving. The temperature sensor is enabled by default and the partial array self refresh can be programmed through the extended mode register.

Notes :

1. Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes. For the first byte (DQ0–DQ7) DM refers to DM0 and DQS refers to DQS0. For the second byte (DQ8–DQ15) DM refers to DM1 and DQS refers to DQS1.
2. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
3. Any specific requirement takes precedence over a general statement.

Pin Description

Symbol	Type	Description
CLK, /CLK	Input	Clock: CLK is the system clock input. CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK. Input and output data is referenced to the crossing of CLK and /CLK (both directions of the crossing).
CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW allows PRECHARGE power-down and SELF REFRESH operations (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions expect SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes.
/CS	Input	Chip select: /CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
/RAS, /CAS, /WE	Input	Command inputs: /RAS, /CAS, and /WE (along with /CS) define the command being entered.
DM0–DM1	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x16, DM0 corresponds to DQ0 – DQ7, DM1 corresponds to DQ8–DQ15.
BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is applied. BA0 and BA1 also determine which mode register (standard mode register or extended mode register) is loaded during a LOAD MODE REGISTER command.
A0-A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto pre-charge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. For 512Mb(X16), Row Address : A0 ~ A12, Column Address: A0 ~ A9.
DQ0-DQ15	I/O	Data input/output: Data bus for x16.
DQS0-DQS1	I/O	Data strobe: Output with read data, input with write data. DQS is edge aligned with read data, centered in write data. It is used to capture data. For the x16, DQS0 corresponds to DQ0 – DQ7, DQS1 corresponds to DQ8–DQ15.
TQ	Output	Temperature sensor output : TQ High when LPDDR Tj exceeds 85℃. When TQ is 'High', self refresh is not supported.
VDDQ	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
VSSQ	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
VDD	Supply	Power Supply: Voltage dependant on option.
VSS	Supply	Ground.

Functional Description

The 512Mb Low Power DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the 67,108,864-bit banks is organized as 8,192 rows by 1,024 columns by 16 bits.

The 512Mb Low Power DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture, with an interface designed to transfer four data words per clock cycle at the I/O balls. single read or write access for the 512Mb Low Power DDR SDRAM consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O balls.

Read and write accesses to the Low Power DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command.

The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

It should be noted that the DLL signal that is typically used on standard DDR devices is not necessary on the Low Power DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the Low Power DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

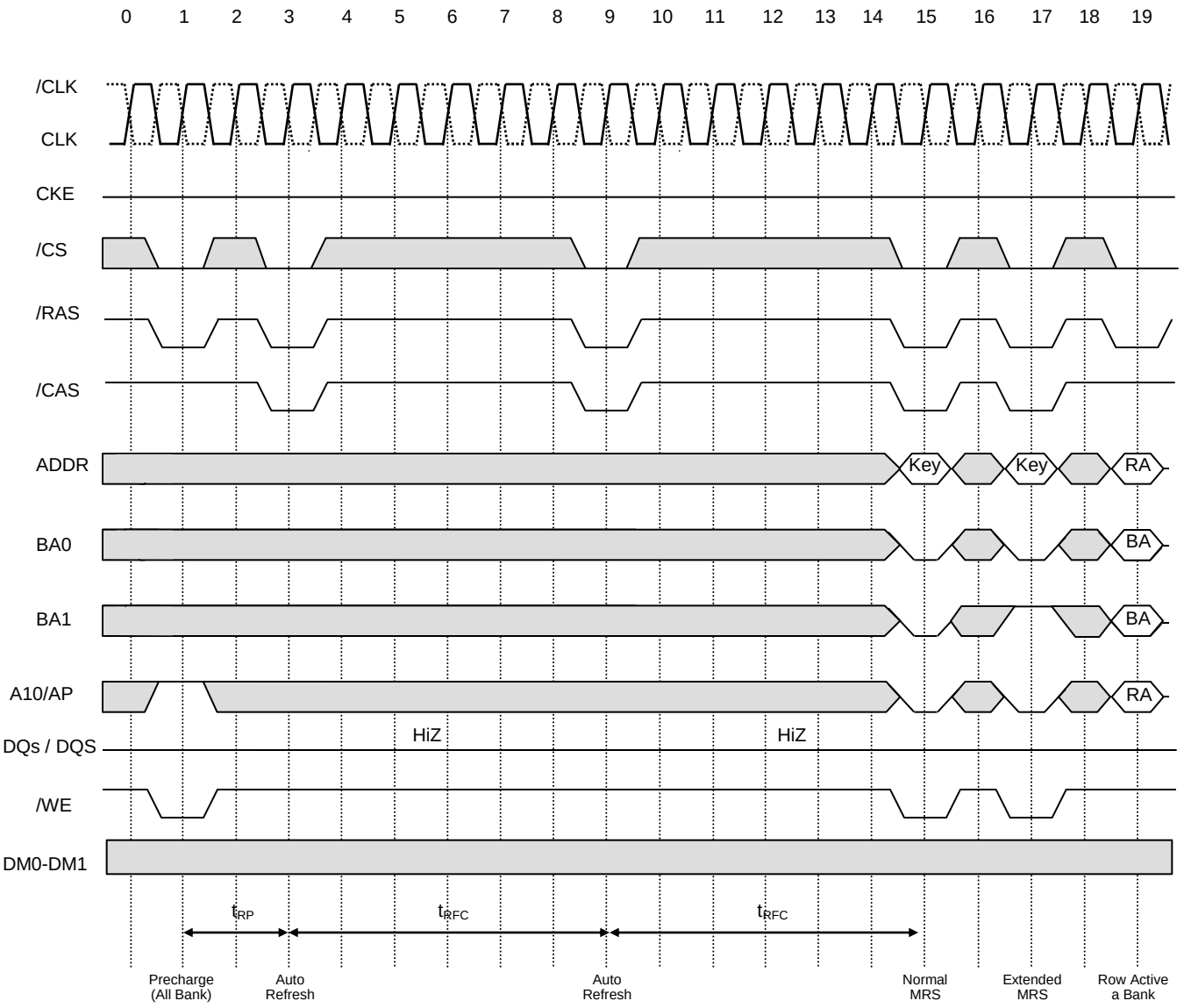
Low Power DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

If there is an interruption to the device power, the initialization routine should be followed to ensure proper functionality of the Low Power DDR SDRAM. The clock stop feature is not available until the device has been properly initialized.

To properly initialize the Low Power DDR SDRAM, this sequence must be followed:

1. To prevent device latch-up, it is recommended the core power (VDD) and I/O power (VDDQ) be from the same power source and brought up simultaneously. If separate power sources are used, VDD must lead VDDQ.
2. Once power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. Once the clock is stable, a 200µs (minimum) delay is required by the Low Power DDR SDRAM prior to applying an executable command. During this time, NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue NOP or DESELECT commands for at least tRP time.
6. Issue an AUTO REFRESH command followed by NOP or DESELECT commands for at least tRFC time. Issue a second AUTO REFRESH command followed by NOP or DESELECT commands for at least tRFC time. As part of the individualization sequence, two AUTO REFRESH commands must be issued. Typically, both of these commands are issued at this stage as described above. Alternately, the second AUTO-REFRESH command and NOP or DESELECT sequence can be issued between steps 10 and 11.
7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.
8. Issue NOP or DESELECT commands for at least tMRD time.
9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or DESELECT commands for at least tMRD time.
11. The Low Power DDR SDRAM has been properly initialized and is ready to receive any valid command.

Figure 1. Initialize and Load Mode Register[1.2.3.]



Note :

1. The two AUTO REFRESH commands at T3 and T9 may be applied before either LOAD MODE REGISTER (LMR) command.
2. PRE = PRECHARGE command, LMR = LOAD MODE REGISTER command, AR = AUTO REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address
3. The Load Mode Register for both MR/EMR and 2 Auto Refresh commands can be in any order; However, all must occur prior to an Active command.
4. NOP or DESELECT commands are required for at least 200μs.
5. Other valid commands are possible.
6. NOPs or DESELECTs are required during this time.

Register Definition

Mode Registers

The mode registers are used to define the specific mode of operation of the Low Power DDR SDRAM. There are two mode registers used to specify the operational characteristics of the device. The standard mode register, which exists for all Low Power DDR SDRAM devices, and the extended mode register, which exists on all Low Power DDR SDRAM devices.

Standard Mode Register

The standard mode register definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Table 1 on page 10. The standard mode register is programmed via the LOAD MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again. Reprogramming the standard mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.
Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A12 specify the operating mode.

Note: Standard refers to meeting JEDEC-standard mode register definitions.

Burst Length

Read and write accesses to the Low Power DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Table 1 on page 10. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2,4,8 or 16 are available for both the sequential and the interleaved burst types.
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap until a boundary is reached. The block is uniquely selected by A1–Ai when BL = 2, by A2–Ai when BL = 4, by A3–Ai when BL = 8, by A4–Ai when BL=16(where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block.
The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.
The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address. See Table 2 on page 11 for more information.

READ Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 3 clocks, as shown in Table 1 on page 10. For CL = 3, if the READ command is registered at clock edge n, then the data will nominally be available at (2 clocks + tAC). For CL = 2, if the READ command is registered at clock edge n, then the data will be nominally be available at (1 clock + tAC).

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Table 1: Standard Mode Register Definition

M14-BA1	M13-BA0	M12-A12	M11-A11	M10-A10	M9-A9	M8-A8	M7-A7	M6-A6	M5-A5	M4-A4	M3-A3	M2-A2	M1-A1	M0-A0
0	0	Operation Mode						CAS Latency			BT	Burst Length		

M14	M13	Mode Register Definition
0	**0**	**Standard Mode Register**
0	1	Status Read Register
1	0	Extended Mode Register
1	1	Reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M12	M11	M10	M9	M8	M7		Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
-	-	-	-	-	-	-	All other states reserved

M3	Burst Type
0	Sequential
1	Interleaved

Table 2: Burst Definition

Burst Length			Starting Column Address		Order of Accesses Within a Burst	
					Type = Sequential	Type = Interleaved
2				A0		
				0	0-1	0-1
				1	1-0	1-0
4			A1	A0		
			0	0	0-1-2-3	0-1-2-3
			0	1	1-2-3-0	1-0-3-2
			1	0	2-3-0-1	2-3-0-1
			1	1	3-0-1-2	3-2-1-0
8		A2	A1	A0		
		0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
		0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
		0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
		0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
		1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
		1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
		1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
		1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
16	A3	A2	A1	A0		
	0	0	0	0	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15
	0	0	0	1	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-0-3-2-5-4-7-6-9-8-11-10-13-12-15-14
	0	0	1	0	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-0-1-6-7-4-5-10-11-8-9-14-15-12-13
	0	0	1	1	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-2-1-0-7-6-5-4-11-10-9-8-15-14-13-12
	0	1	0	0	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-0-1-2-3-12-13-14-15-8-9-10-11
	0	1	0	1	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-4-7-6-1-0-3-2-13-12-15-14-9-8-11-10
	0	1	1	0	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-4-5-2-3-0-1-14-15-12-13-10-11-8-9
	0	1	1	1	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-15-14-13-12-11-10-9-8
	1	0	0	0	8-9-10-11-12-13-14-15-0-1-2-3-4-5-6-7	8-9-10-11-12-13-14-15-0-1-2-3-4-5-6-7
	1	0	0	1	9-10-11-12-13-14-15-0-1-2-3-4-5-6-7-8	9-8-11-10-13-12-15-14-1-0-3-2-5-4-7-6
	1	0	1	0	10-11-12-13-14-15-0-1-2-3-4-5-6-7-8-9	10-11-8-9-14-15-12-13-2-3-0-1-6-7-4-5
	1	0	1	1	11-12-13-14-15-0-1-2-3-4-5-6-7-8-9-10	11-10-9-8-15-14-13-12-3-2-1-0-7-6-5-4
	1	1	0	0	12-13-14-15-0-1-2-3-4-5-6-7-8-9-10-11	12-13-14-15-8-9-10-11-4-5-6-7-0-1-2-3
	1	1	0	1	13-14-15-0-1-2-3-4-5-6-7-8-9-10-11-12	13-12-15-14-9-8-11-10-5-4-7-6-1-0-3-2
	1	1	1	0	14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-12-13-10-11-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-14-13-12-11-10-9-8-7-6-5-4-3-2-1-0

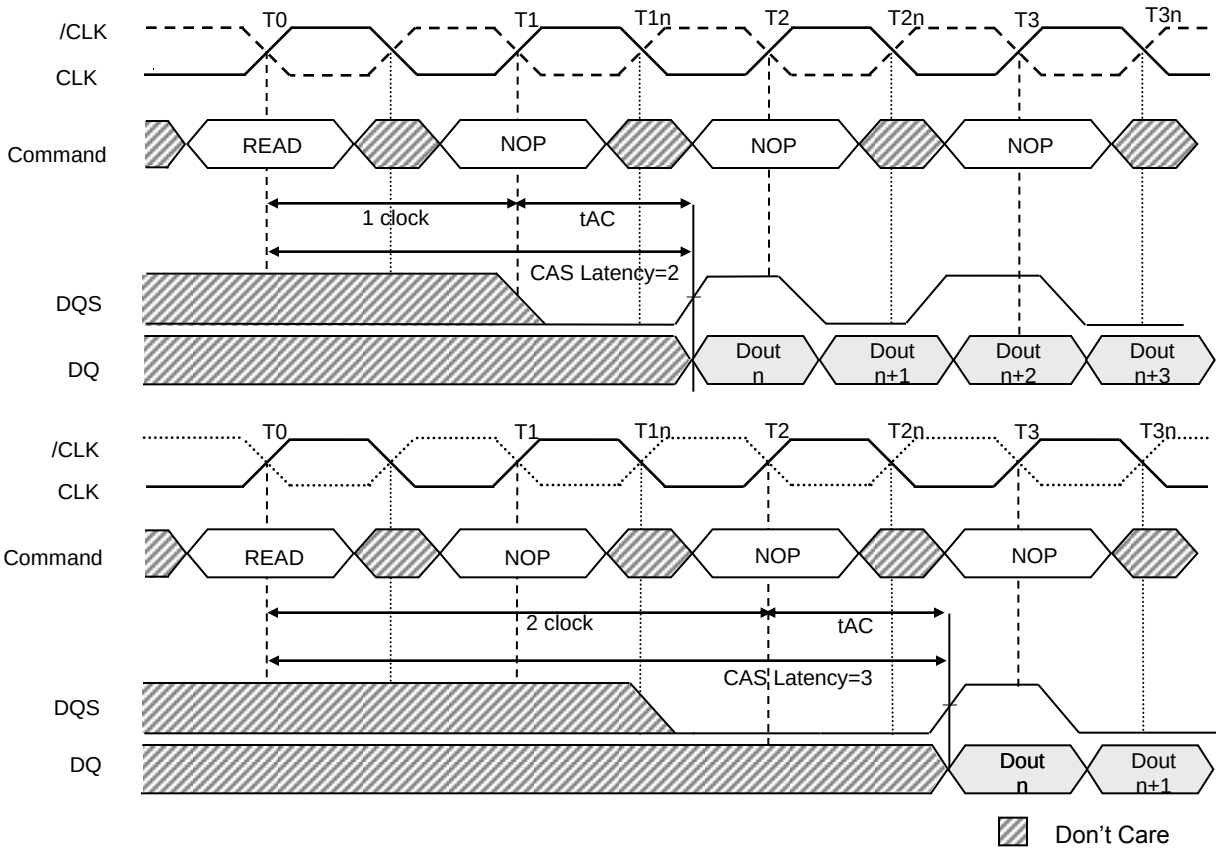
Notes:

1. For BL = 2, A1–A*i* select the two-data-element block; A0 selects the first access within the block.
2. For BL = 4, A2–A*i* select the four-data-element block; A0–A1 select the first access within the block.
3. For BL = 8, A3–A*i* select the eight-data-element block; A0–A2 select the first access within the block.
4. For BL=16, A4–A*i* select the sixteen-data-element block; A0–A3 select the first access within the block.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. A*i* = the most significant column address bit for a given configuration.

Table 3: CAS Latency

Speed	Allowable Operating Clock Frequency (MHz)	
	CL = 2	CL = 3
-25	f ≤83	f ≤200

Figure 2: CAS Latency



Notes:

1. BL = 4 in the cases shown.
2. Shown with nominal tAC and nominal tDQSCLK.

Operating Mode

The normal operating mode is selected by issuing a LOAD MODE REGISTER SET command with bits A7–A12 each set to zero, and bits A0–A6 set to the desired values. All other combinations of values for A7–A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions specific to low power operation. These additional functions include drive strength, temperature compensated self refresh, and partial array self refresh. This device has default values for the extended mode register (if not programmed, the device will operate with the default values – PASR = Full Array, DS = Full Drive).

Temperature Compensated Self Refresh

A temperature sensor is implemented for automatic control of the self refresh oscillator on the device. Programming of the temperature compensated self refresh (TCSR) bits will have no effect on the device.The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Partial Array Self Refresh

For further power savings during SELF REFRESH, the PASR feature allows the controller to select the mount of memory that will be refreshed during SELF REFRESH. The refresh options are as follows:

- Full array: banks 0, 1, 2, and 3
- Half array: banks 0 & 1
- Quarter array: bank 0
- One Eighth array: Half of Bank0
- One Sixteenth array: Quarter of Bank0

WRITE and READ commands can still occur during standard operation, but only the selected banks will be refreshed during SELF REFRESH. Data in banks that are disabled will be lost.

Output Driver Strength

Because the Low Power DDR SDRAM is designed for use in smaller systems that are mostly point to point, an option to control the drive strength of the output buffers is available. Drive strength should be selected based on the expected loading of the memory bus. Bits A5 ~ A7 of the extended mode register can be used to select the driver strength of the DQ outputs. There are five allowable settings for the output drivers.

Table 4: Extended Mode Register Table[1.2.].

EM14-BA1	EM13-BA0	EM12-A12	EM11-A11	EM10-A10	EM9-A9	EM8-A8	EM7-A7	EM6-A6	EM5-A5	EM4-A4	EM3-A3	EM2-A2	EM1-A1	EM0-A0
1	0	All must be set to '0'					Driver Strength			0	0	PASR		

EM14	EM13	Mode Register Definition
0	0	Standard Mode Register
0	1	Status Read Register
1	**0**	**Extended Mode Register**
1	1	Reserved

A2	A1	A0	Self Refresh Coverage
0	0	0	All Banks
0	0	1	Half of Total Bank(BA1=0)
0	1	0	Quarter of Total Bank(BA1=BA0=0)
0	1	1	RFU
1	0	0	RFU
1	0	1	One Eighth of Total Bank (BA1=BA0=Row Address MSB=0)
1	1	0	One Sixteenth of Total Bank (BA1=BA0=Row Address2 MSBs=0)
1	1	1	RFU

A7	A6	A5	Driver Strength
0	0	0	100%
0	0	1	50%
0	1	0	25%
0	1	1	12.5%
1	0	0	75%
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Note :

1. EM14 and EM13 (BA1 and BA0) must be "1, 0" to select the Extended Mode Register(vs. the base Mode Register).
2. RFU: Reserved for Future Use

Status Read Registers

The status read register (SRR) is used to read the manufacturer ID, revision ID, refresh multiplier, width type, and density of the device, as shown in Table 5 (page 14). The SRR is read via the LOAD MODE REGISTER command with BA0 = 1 and BA1 = 0. The sequence to perform an SRR command is as follows:

- The device must be properly initialized and in the idle or all banks precharged state.
- Issue a LOAD MODE REGISTER command with BA[1:0] = 01 and all address pins set to 0.
- Wait tSRR; only NOP or DESELECT commands are supported during the tSRR time.
- Issue a READ command.
- Subsequent commands to the device must be issued tSRC after the SRR READ command is issued; only NOP or DESELECT commands are supported during tSRC.

SRR output is read with a burst length of 2. SRR data is driven to the outputs on the first

bit of the burst, with the output being “Don’t Care” on the second bit of the burst.

Table 5: Status Register Table.

S31~S16[1]	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
Reserved	Density			Type	Width	Refresh Rate			Revision ID				Manufacturer ID			

S15	S14	S13	Density
0	0	0	128Mb
0	0	1	256Mb
0	1	0	512Mb
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

S12	Device Type
0	LPDDR
1	Reserve

S11	Device Width
0	16 bits
1	32 bits

S10	S9	S8	Refresh Multiplier[2]
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	2X
1	0	0	1X
1	0	1	Reserved
1	1	0	0.25X
1	1	1	Reserved

S3	S2	S1	S0	Manufacturer ID
0	0	0	0	Fidelix
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

S7	S6	S5	S4	Revision ID
0	0	0	0	The manufacturer’s revision number starts at ‘0000’ and increments by ‘0001’ each time a change in the specification (AC timings or feature set), IBIS (pull-up or pull-down characteristics), or process occurs.
~				
1	1	1	1	

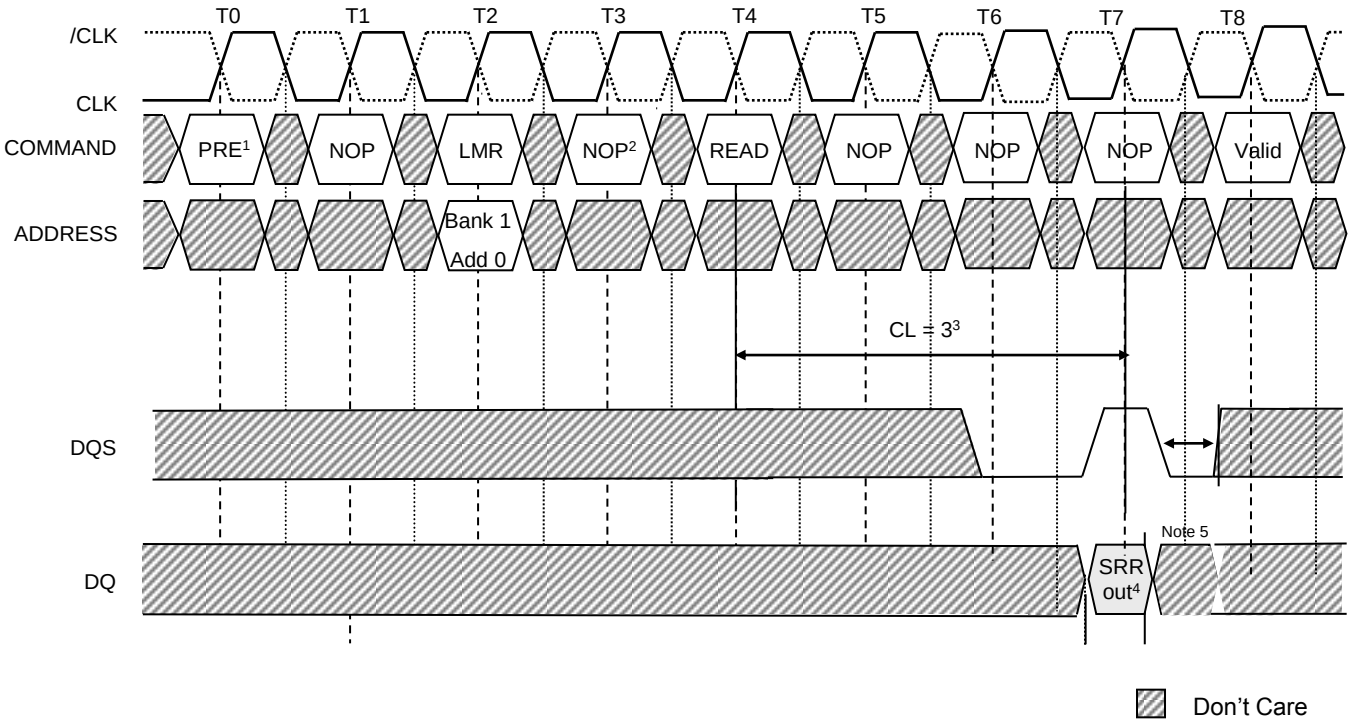
Note : 1. Reserved bits should be set to 0 for future compatibility.

2. Refresh multiplier is based on the device on-board temperature sensor.

Requited periodic refresh interval = tREFI X multiplier.

Self refresh is not supported for automotive device at high temperature. (85℃ to 105℃)

Figure 3: Status Read Register Timing



Note : 1. All banks must be idle prior to status register read.

2. NOP or DESELECT commands are required between the LMR and READ commands(tSRR), and between the READ and the next VALID command (tSRC).
3. CAS latency is predetermined by the programming of the mode register. CL = 3 is shown as an example only.
4. Burst length is fixed to 2 for SRR regardless of the value programmed by the mode register.
5. The second bit of the data-out burst is a "Don't Care."

Stopping the External Clock

One method of controlling the power efficiency in applications is to throttle the clock which controls the Low Power DDR SDRAM. There are two basic ways to control the clock:

1. Change the clock frequency, when the data transfers require a different rate of speed.
2. Stopping the clock altogether.

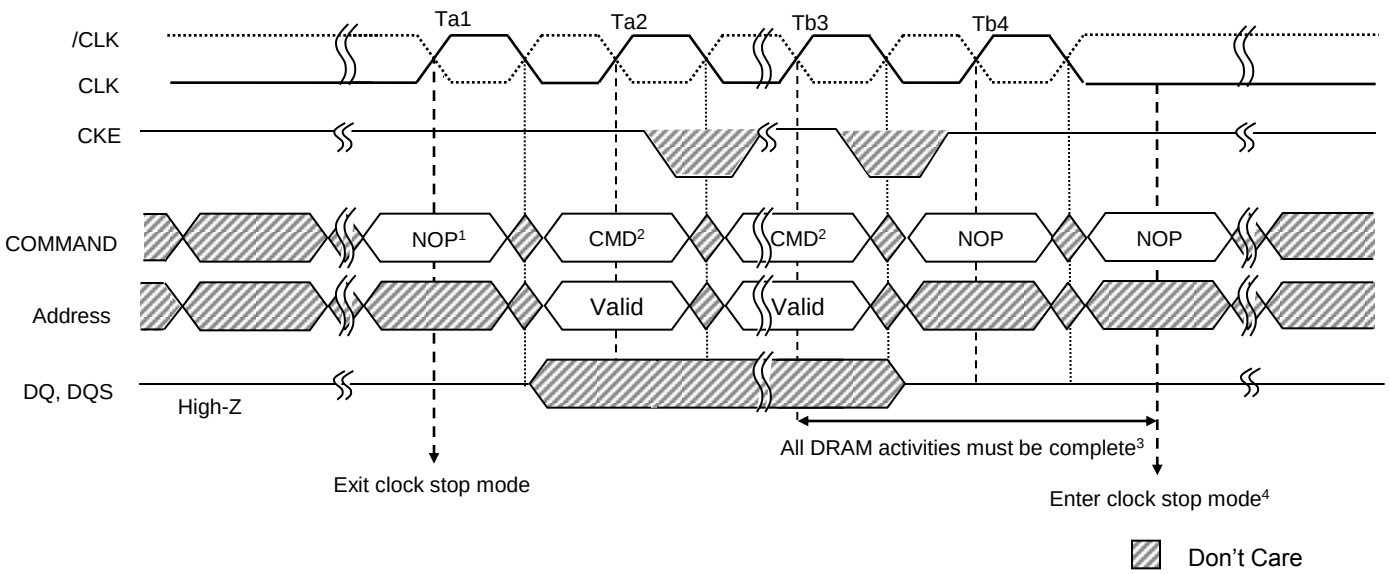
Both of these are specific to the application and its requirements and both allow power savings due to possible less transitions on the clock path.

The Low Power DDR SDRAM allows the clock to change frequency during operation, only if all the timing parameters are met with respect to that change and all refresh requirements are satisfied.

The clock can also be stopped all together, if there are no data accesses in progress, either WRITEs or READs that would be effected by this change; i.e., if a WRITE or a READ is in progress the entire data burst must be through the pipeline prior to stopping the clock. CKE must be held HIGH with CLK = LOW and /CLK = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP is required after the clock is restarted before a valid command can be issued. Figure 4 on page 16 illustrates the clock stop mode.

It is recommended that the Low Power DDR SDRAM should be in a precharged state if any changes to the clock frequency are expected. This will eliminate timing violations that may otherwise occur during normal operational accesses.

Figure 4: Clock Stop Mode



Notes:

1. Prior to Ta1 the device is in clock stop mode. To exit, at least one NOP is required before any valid command.
2. Any valid command is allowed, device is not in clock suspend mode.
3. Any DRAM operation already in process must be completed before entering clock stop mode. This includes tRCD, tRP, tRFC, tMRD, tWR, all data-out for READ bursts. This means the DRAM must be either in the idle or precharge state before clock suspend mode can be entered.
4. To enter and maintain a clock stop mode: CLK = LOW, /CLK = HIGH, CKE = HIGH.

Commands

Table 6 and Table 7 provide quick references of available commands. This is followed by a written description of each command. Three additional Truth Tables (Table 13 on page 46, Table 14 on page 47, and Table 15 on page 49) provide CKE commands and current/ next state information.

Table 6: Truth Table – Commands

Notes : 1 and 11 apply to all commands

Name (Function)	/CS	/RAS	/CAS	/WE	ADDR	Notes
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8, 10
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH (refresh all or single bank) or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER (standard or extended mode registers)	L	L	L	L	Op-Code2	2
Deep Power Down(Enter DPD Mode)	L	H	H	L	Op-Code2	11

Notes:

1. CKE is HIGH for all commands shown except SELF REFRESH and Deep Power Down.
2. BA0–BA1 select either the standard mode register or the extended mode register (BA0 = 0, BA1 = 0 select the standard mode register; BA0 = 0, BA1 = 1 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A12 provide the op- code to be written to the selected mode register.
3. BA0–BA1 provide bank address and A0–A12 provide row address.
4. BA0–BA1 provide bank address; A0–A9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. A10 LOW : BA0–BA1 determine which bank is precharged. A10 HIGH: all banks are precharged and BA0–BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
9. DESELECT and NOP are functionally interchangeable.
10. This command is a BURST TERMINATE if CKE is HIGH.
11. This command is a Deep Power Down if CKE is Low.
12. All states and sequences not shown are reserved and/or illegal.

Table 7: Truth Table – DM Operation

Name (Function)	DM	DQ
Write enable	L	Valid
Write inhibit	H	X

Note: Used to mask write data; provided coincident with corresponding data.

DESELECT

The DESELECT function (/CS HIGH) prevents new commands from being executed by the Low Power DDR SDRAM. The Low Power DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (/CS = LOW, /RAS = /CAS = /WE = HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0–A12. See mode register descriptions in “Register Definition” on page 9. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This “earliest valid stage” is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating tRAS (MIN), as described for each burst type in “Operations” on page 24. The user must not issue another command to the same bank until the precharge time (tRP) is completed.

BURST TERMINATE

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in “Operations” on page 24. The open page which the READ burst was terminated from remains open.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the Low Power DDR SDRAM and is analogous to /CAS-BEFORE-/RAS (CBR) REFRESH in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during an AUTO REFRESH command. The 512Mb Low Power DDR SDRAM requires AUTO REFRESH cycles at an average interval of 7.8125µs (maximum).To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (HIGH) during the auto refresh period. The auto refresh period begins when the AUTO REFRESH command is registered and ends tRFC later.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the Low Power DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the Low Power DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). All command and address input signals except CKE are “Don’t Care” during SELF REFRESH.

During SELF REFRESH, the device is refreshed as identified in the external mode register (see PASR setting). For a the full array refresh, all four banks are refreshed simultaneously with the refresh frequency set by an internal self refresh oscillator. This oscillator changes due to the temperature sensors input. As the case temperature of the Low Power DDR SDRAM increases, the oscillation frequency will change to accommodate the change of temperature. This happens because the DRAM capacitors lose charge faster at higher temperatures. To ensure efficient power dissipation during self refresh, the oscillator will change to refresh at the slowest rate possible to maintain the devices data.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the Low Power DDR SDRAM must have NOP commands issued for tXSR is required for the completion of any internal refresh in progress. Self refresh is not supported for automotive device at high temperature.(85℃ to 105℃)

DEEP POWER DOWN

Deep Power Down Mode is an operating mode to achieve extreme power reduction by cutting the power of the whole memory array of the device. Data will not be retained once the device enters DPD Mode. Full initialization is required when the device exits from DPD Mode. [Figure 38,39]

Maximum Ratings

Voltage on V_{DD}/V_{DDQ} Supply
Relative to V_{SS} ……..-0.5V to + 2.3V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} …….. –0.5V to +2.3V
Storage Temperature (plastic) …….. -55℃ to + 150℃
Power Dissipation ……..……1W

*Stresses greater than those listed under “Maximum Ratings” may cause permanent damage to the device.This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Device	Range	Ambient Temperature	V_{DD}	V_{DDQ}
FMD8C16LAx-xxEC	Commercial	0℃ to +70℃	1.7V ~ 1.95V	1.7V ~ V_{DD}
FMD8C16LAx-xxEE	Extended	-25℃ to +85℃		
FMD8C16LAx-xxEI	Industrial	-40℃ to +85℃		

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS [1,2]

Parameter / Condition	Symbol	Min	Max	Units
Supply Voltage	V_{DD}	1.7	1.95	V
I/O Supply Voltage	V_{DDQ}	1.7	V_{DD}	V
Input High Voltage : Logic 1 All Inputs [3.]	V_{IH}	0.7* V_{DDQ}	V_{DDQ} +0.3	V
Input Low Voltage : Logic 0 All Inputs [3.]	V_{IL}	-0.3	0.3*V_{DDQ}	V
Data Output High Voltage : Logic 1 : All Inputs(-0.1mA)	V_{OH}	0.9* V_{DDQ}		V
Data Output Low Voltage : Logic 0 : All Inputs(0.1mA)	V_{OL}		0.1* V_{DDQ}	V
Input Leakage Current : Any Input 0V=V_{IN}=V_{DD} (All other pins not under test=0V)	II	-5	5	μA
Output Leakage Current : DQs are disabled ; 0V= V_{OUT}=V_{DDQ}	I_{OZ}	-5	5	μA

Table 8. AC Operating Conditions[1,2,3,4,5,6]

Parameter / Condition	Value	Units
AC input levels (Vih / Vil)	0.8 x VDDQ / 0.2 x VDDQ	V
Input timing measurement reference level	0.5 x VDDQ	V
Input signal minimum slew rate	1.0	V/ns
Output timing measurement reference level	0.5 x VDDQ	V
Output load condition	AC Output Load Circuit on page 21	V

Note :

1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-40°C ≤ TA ≤ +85°C for IT parts) is ensured.
2. An initial pause of 200μs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
3. All states and sequences not shown are illegal or reserved.
4. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. t_{HZ} defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet t_{OH} before going High-Z.
6. AC timing and I_{DD} tests have V_{IL} and V_{IH}, with timing referenced to V_{IH}/2 = crossover point. If the input transition time is longer than t_T (MAX), then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the V_{IH}/2 crossover point.

Table 9: IDD Specifications and Conditions

Parameter/Condition		Symbol	Max -25	Units	Notes
Operating one bank active precharge current: tRC = tRC(MIN); tCLK = tCLK(MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD0	60	mA	1, 6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2P	300	µA	2, 4
Precharge power-down standby current with CLK stopped: All banks idle; CKE is LOW, CS is HIGH; CLK = LOW, /CLK = HIGH; Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2PS	300	µA	2, 4
Precharge non power-down standby current: All banks idle; CKE = HIGH; CS = HIGH; tCLK =tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2N	15	mA	5
Precharge non power-down standby current: CLK stopped; All banks idle; CKE = HIGH; CS = HIGH; CLK = LOW; /CLK = HIGH Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2NS	8	mA	5
Active power-down standby current: One bank active; CKE = LOW; CS = HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD3P	3	mA	2, 4
Active power-down standby current: CLK stopped; One bank active; CKE = LOW; CS = HIGH; CLK = LOW; /CLK = HIGH; Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD3PS	2	mA	2, 4
Active non power-down standby: One bank active; CKE = HIGH; CS = HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two cycles; Data bus inputs are stable.		IDD3N	15	mA	1
Active non-power-down standby: CLK stopped; One bank active; CKE = HIGH; CS = HIGH; CLK = LOW; /CLK = HIGH; Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD3NS	8	mA	1
Operating burst read : One bank active; BL = 4; tCLK = tCLK(MIN); Continuous READ bursts; Address inputs are switching; 50 percent data changing each burst.		IDD4R	80	mA	1, 6
Operating burst write: One bank active; BL = 4; tCLK = tCLK(MIN); Continuous WRITE bursts; Address inputs are switching; 50 percent data changing each burst.		IDD4W	80	mA	1, 6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable.	tRC = tRFC(138ns)	IDD5	95	mA	7
Precharge power-down standby current: All banks idle, CKE is LOW; CS is HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.	tRC = 7.8125µs	IDD5a	3	mA	3, 7
Self refresh: CKE = LOW; tCLK = tCLK(MIN); Address and control inputs are stable; Data bus inputs are Stable.	Full Array, 85˚C	IDD6a	600	µA	8, 9
	Full Array, 45˚C	IDD6a	450	µA	8, 9
	Half Array, 85˚C	IDD6b	500	µA	8, 9
	¼ Array, 85˚C	IDD6c	400	µA	8, 9
Deep Power Down Current ; Address, control and data bus inputs are STABLE		IDD7	10	µA	10

Notes :

1. MIN (tRC or tRFC) for IDD measurements is the smallest multiple of tCLK that meets the minimum absolute value for the respective parameter. tRAS (MAX) for IDD measurements is the largest multiple of tCLK that meets the maximum absolute value for tRAS.
2. The refresh period equals 64ms. This equates to an average refresh rate of 7.8125µs.
3. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (tRFC [MIN]) else CKE is LOW (i.e., during standby).
4. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/ DM/DQS slew rate is less than 0.5V/ns, timing must be derated: ***50ps (pending) must be added to tDS and tDH for each 100mv/ns reduction in slew rate.*** If slew rate exceeds 4V/ns, functionality is uncertain.

5. IDD2N specifies DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level.
6. Switching is defined as :
   - address and command: inputs changing between HIGH and LOW once per two clock cycles;
   - data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.
7. CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising CLK edge, until tRFC later.
8. With the inclusion of the temperature sensor on the low-power DDR device, these numbers are shown as examples only, and will change due to the junction temperature that the device is sensing. They are expected to be maximum values at this time.
9. Enables on-chip refresh and address counters.
10. Device must be in the all banks idle state prior to entering Deep Power Down.

Table 10: Capacitance

Parameter	Symbol	Min	Max	Units
Input capacitance (A0-A12, BA0~BA1, CKE, /CS, /RAS, /CAS, /WE)	CIN1	1.5	3.0	pF
Input capacitance (CLK, /CLK)	CIN2	1.5	3.0	pF
Data & DQS input / output capacitance	COUT	3.0	5.0	pF
Input capacitance(DM)	CIN3	3.0	5.0	pF

AC Output Load Circuit

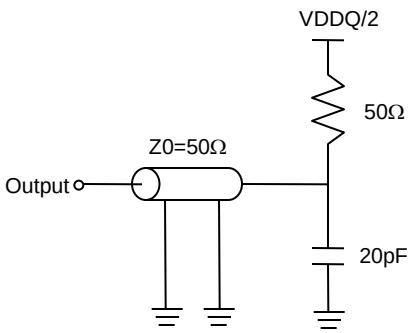


Table 11: Electrical Characteristics and Recommended AC Operating Conditions

AC Characteristics		Symbol	-25		Units	Notes
Parameter			Min	Max		
Access window of DQ from CLK & /CLK	CL=3	tAC(3)	2.0	5.0	ns	
	CL=2	tAC(2)	2.0	6.0		
CLK high-level width		tCH	0.45	0.55	tCLK	
CLK low-level width		tCL	0.45	0.55	tCLK	
System Clock cycle time	CL=3	tCLK(3)	5	100	ns	1
	CL=2	tCLK(2)	12	-	ns	
Auto precharge write recovery + precharge time		tDAL	5	-	tCLK	16
DQ and DM input hold time relative to DQS		tDH	0.48	-	ns	9, 13, 15
DQ and DM input setup time relative to DQS		tDS	0.48	-	ns	17
DQ and DM input pulse width (for each input)		tDIPW	1.6	-	ns	
Access window of DQS from CLK & /CLK		tDQSCLK	2.0	5.0	ns	
DQS input high-pulse width		tDQSH	0.4	0.6	tCLK	
DQS input low-pulse width		tDQSL	0.4	0.6	tCLK	
Data strobe edge to Dout edge		tDQSQ	-	0.4	ns	8, 9
WRITE command to first DQS latching transition		tDQSS	0.75	1.25	tCLK	
DQS falling edge to CLK rising – setup time		tDSS	0.2	-	tCLK	
DQS falling edge from CLK rising – hold time		tDSH	0.2	-	tCLK	
Half-CLK period		tHP	tCH, tCL	-	ns	12
Data-out High-Z window from CLK & /CLK		tHZ	-	5.0	ns	3, 11
Data-out Low-Z window from CLK & /CLK		tLZ	1.0	-	ns	3, 11
Transition Time		t_T	0.5	1.2	ns	
Address and control input hold time		tIH	0.9	-	ns	2, 15
Address and control input setup time		tIS	0.9	-	ns	2, 15
Address and control input pulse width		tIPW	2.2	-	ns	17
LOAD MODE REGISTER command cycle time		tMRD	2	-	tCLK	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		tQH	tHP -tQHS	-	ns	8, 9
Data hold skew factor		tQHS	-	0.5	ns	
ACTIVE-to-PRECHARGE command		tRAS	42	70,000	ns	10
ACTIVE-to-ACTIVE command period		tRC	55	-	ns	
AUTO REFRESH command period		tRFC	80	-	ns	14
ACTIVE-to-READ or WRITE delay		tRCD	15	-	ns	
PRECHARGE command period		tRP	15	-	ns	
DQS read preamble	CL=3	tRPRE(3)	0.9	1.1	tCLK	11
	CL=2	tRPRE(2)	0.5	1.1	tCLK	11
DQS read postamble		tRPST	0.4	0.6	tCLK	
Read of SRR to next valid command		tSRC	CL+1	-	tCLK	
SRR to Read		tSRR	2	-	tCLK	
Internal temperature sensor valid temperature output enable		tTQ	2	2	ms	
ACTIVE bank *a* to ACTIVE bank *b* Delay		tRRD	10	-	ns	

Table 12: Electrical Characteristics and Recommended AC Operating Conditions (continued)

AC Characteristics	Symbol	-25		Units	Notes
Parameter		Min	Max		
DQS write preamble	tWPRE	0.25	-	tCLK	
DQS write preamble setup time	tWPRES	0	-	ns	5, 6
DQS write postamble	tWPST	0.4	0.6	tCLK	4
Write recovery time	tWR	15	-	ns	
Internal WRITE to READ command delay	tWTR	2	-	tCLK	
Average periodic refresh interval	tREFI	-	7.8	µs	7
Exit SELF REFRESH to first valid command	tXSR	120	-	ns	18
Exit power-down mode to first valid command	tPDX	25	-	ns	19
Minimum tCKE HIGH/LOW time	tCKE	1	-	tCLK	

Notes

1. CAS latency definition: for CL = 2, the first data element is valid at (tCLK + tAC) after the CLK at which the READ command was registered; for CL = 3, the first data element is valid at (2 × tCLK + tAC) after the first CLK at which the READ command was registered.
2. Fast command/address input slew rate ≥ 1V/ns. Slow command/address input slew rate ≥ 0.5V/ns. If the slew rate is less than 0.5V/ns, timing must be derated: tIS has ***an additional 50ps (pending) per each 100mV/ns*** reduction in slew rate from the 0.5V/ns. ***tIH has 0ps added (pending);*** that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
3. tHZ and tLZ transitions occur in the same access time windows as valid data transitions.These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
4. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
5. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
6. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command.
7. The refresh period equals 64ms. This equates to an average refresh rate of 7.8125µs.
8. The valid data window is derived by achieving other specifications: tHP (tCLK/2), tDQSQ, and tQH (tHP - tQHS). The data valid window derates directly proportional with the CLK duty cycle and a practical data valid window can be derived. The CLK is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio.
9. Referenced to each output group: DQS0 with DQ0–DQ7; and DQ1 with DQ8–DQ1
10. READs and WRITEs with auto precharge are allowed to be issued before tRAS (MIN) can be satisfied prior to the internal PRECHARGE command being issued.
11. tHZ (MAX) will prevail over tDQSCLK (MAX) + tRPST (MAX) condition.
12. tHP (MIN) is the lesser of tCL minimum and tCH minimum actually applied to the device CLK and /CLK inputs, collectively.
13. Random addressing changing 50 percent of data changing at every transfer.
14. CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising CLK edge, until tRFC later.
15. The transition time for input signals (/CAS, CKE, /CS, DM, DQ, DQS, /RAS, /WE, and addresses) are measured between VIL(DC) to VIH(AC) for rising input signals and VIH(DC) to VIL(AC) for falling input signals.
16. tDAL = (tWR/tCLK) + (tRP/tCLK): for each term, if not already an integer, round to the next higher integer.
17. These parameters guarantee device timing but they are not necessarily tested on each device.
18. CLK must be toggled a minimum of two times during this period.
19. CLK must be toggled a minimum of one time during this period.
20. This device can support 45/55 of duty rate for tDQSCLK in case of 50/50 of CLK input.

Operations

Bank/row Activation

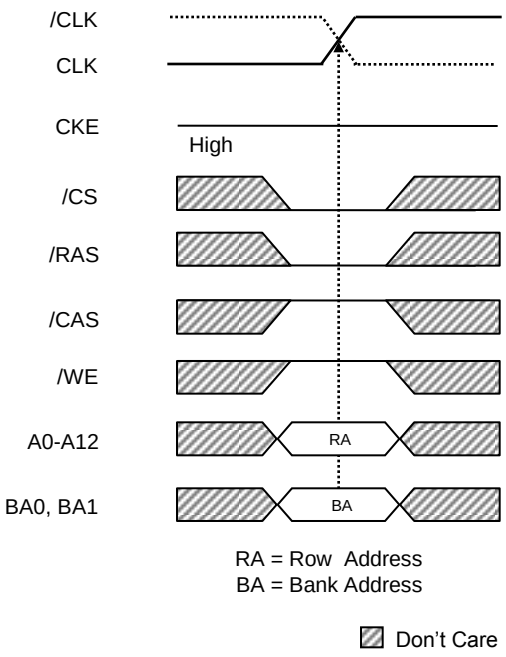
Before any READ or WRITE commands can be issued to a bank within the Low Power DDR SDRAM, a row in that bank must be “opened.” This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 5.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a tRCD specification of 18ns with a 133 MHz clock (7.5ns period) results in 2.4 clocks rounded to 3.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

Figure 5: Activating a Specific Row in a Specific Bank



READ

READ bursts are initiated with a READ command, as shown in Figure 6 on page 26.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CLK and /CLK). Figure 7 on page 27 shows general timing for each possible CAS latency setting. DQS is driven by the Low Power DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of tDQSCLK (DQS transition skew to CLK) and tAC (data-out transition skew to CLK) is depicted in Figure 28 on page 52.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued ***x*** cycles after the first READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture). This is shown in Figure 8 on page 28.

A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is shown for illustration in Figure 9 on page 29. Full speed random read accesses within a page (or pages) can be performed as shown in Figure 10 on page 30.

Figure 6: READ Command

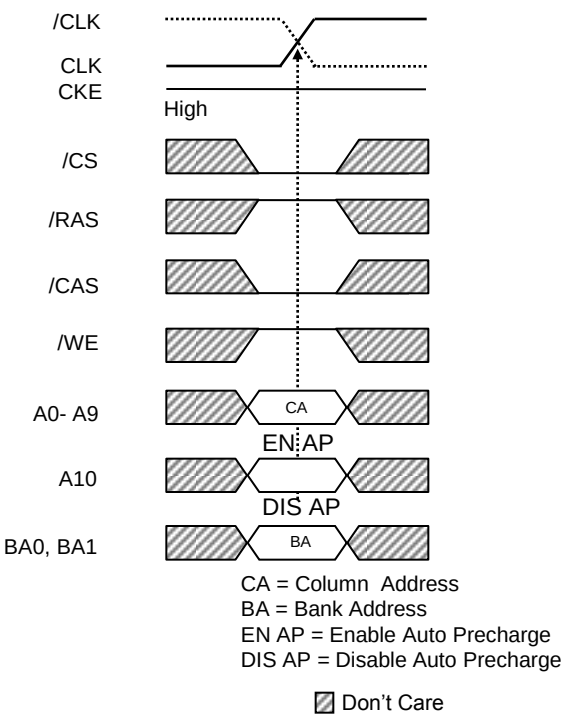
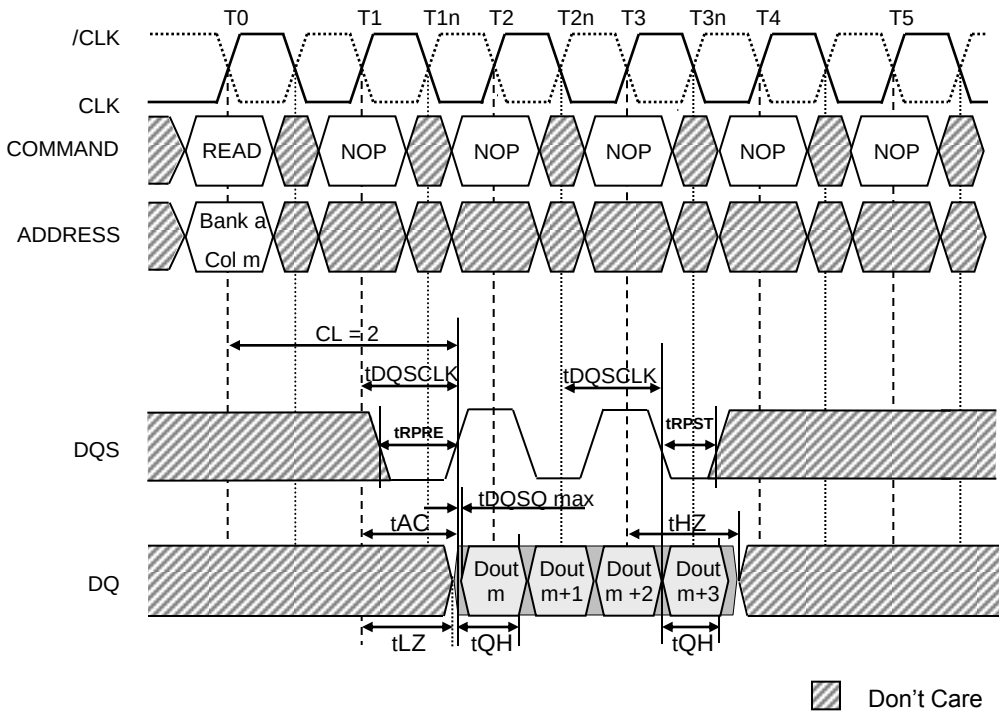


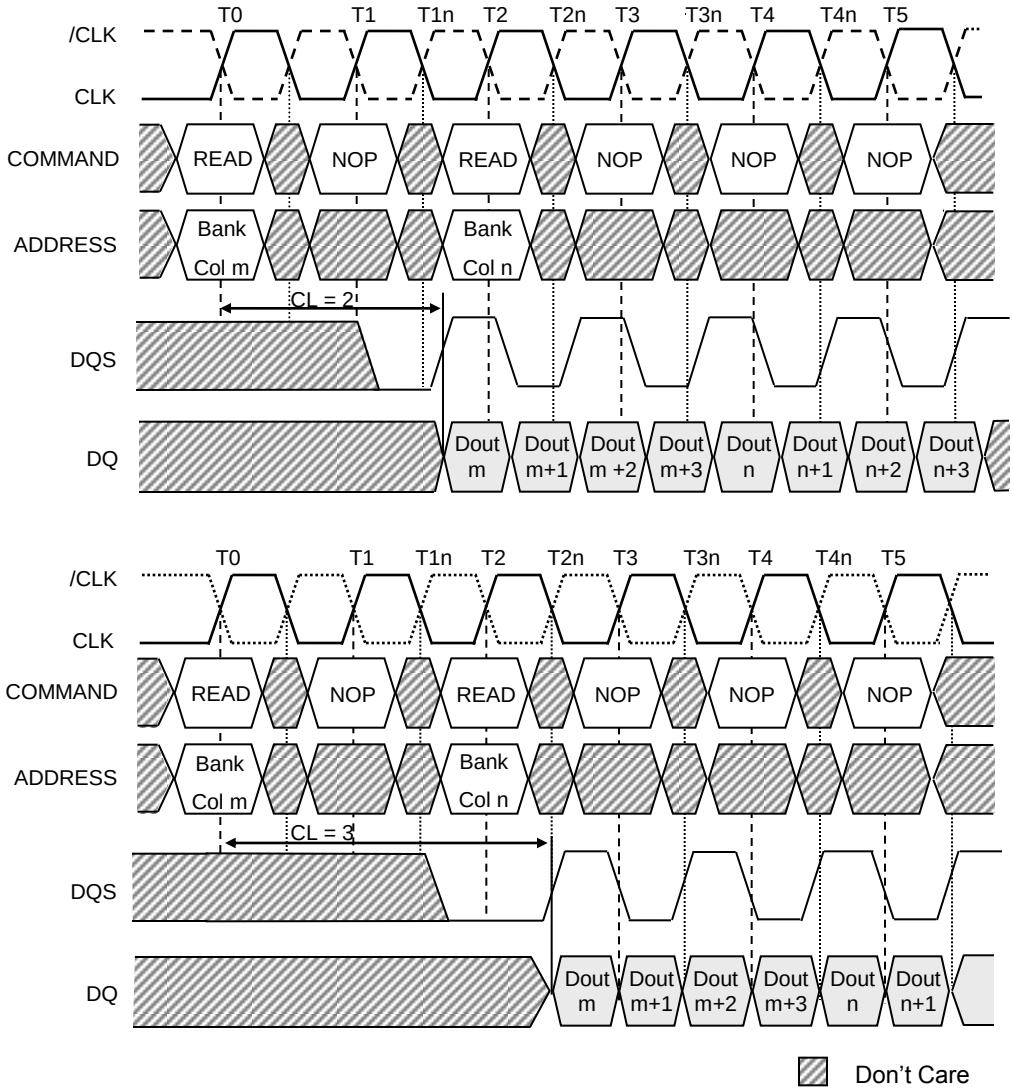
Figure 7: READ Operation



Notes :

1. Dout m = data-out from column m.
2. BL = 4.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.

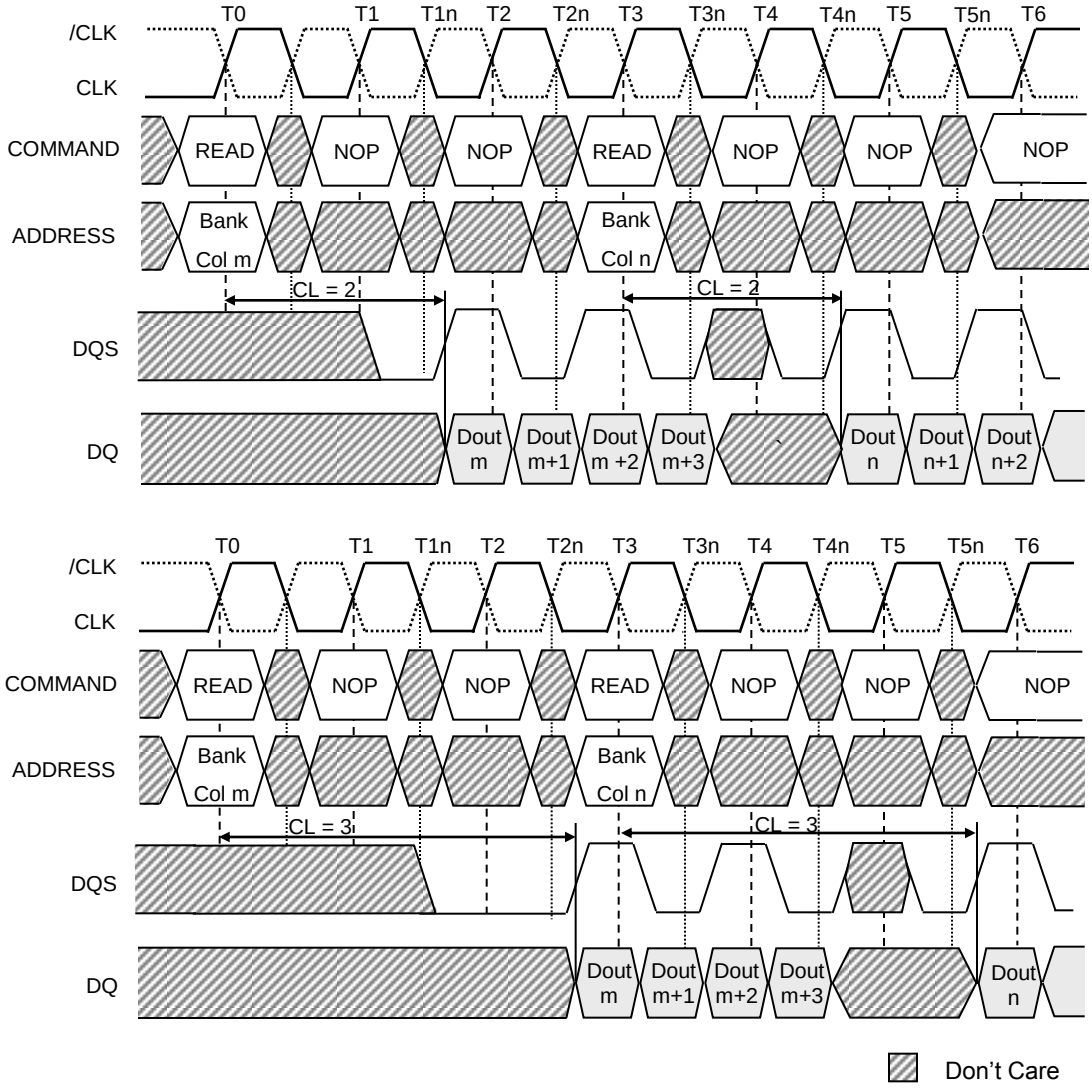
Figure 8: Consecutive Read Bursts



Notes :

1. Dout m (or n) = data-out from column m (or column n).
2. BL = 4 in the cases shown.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. This example represents consecutive READ commands issued to the device.

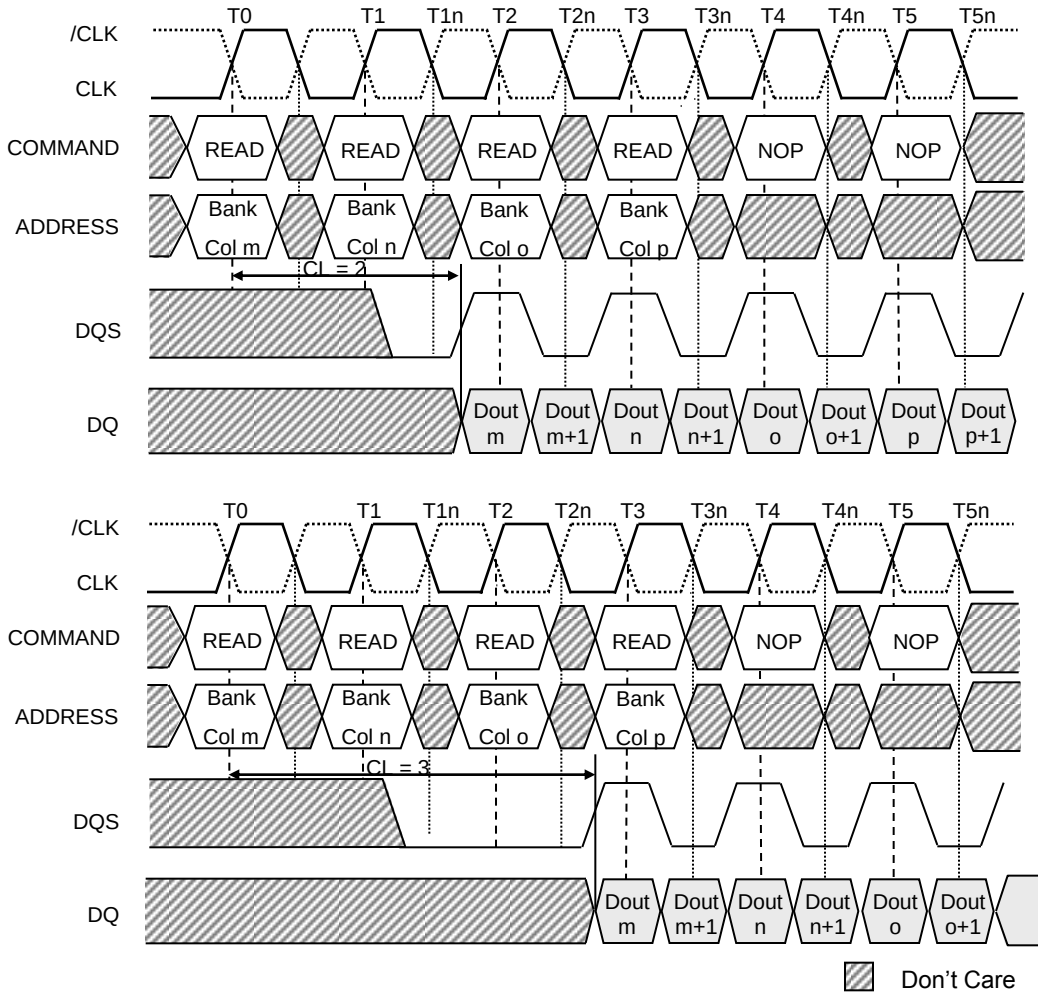
Figure 9: Read-to-Read Operation



Notes :

1. Dout m (or n) = data-out from column m (or column n).
2. BL = 4 in the cases shown
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. This example represents nonconsecutive READ commands issued to the device.

Figure 10: Random READ Accesses



Notes :

1. Dout m (or n, o, p) = data-out from column m *(*or column n, column o, column p).
2. BL = 4 in the cases shown.
3. READs are to an active row in any bank.
4. Shown with nominal tAC, tDQSCLK, and tDQSQ.

Truncated READs

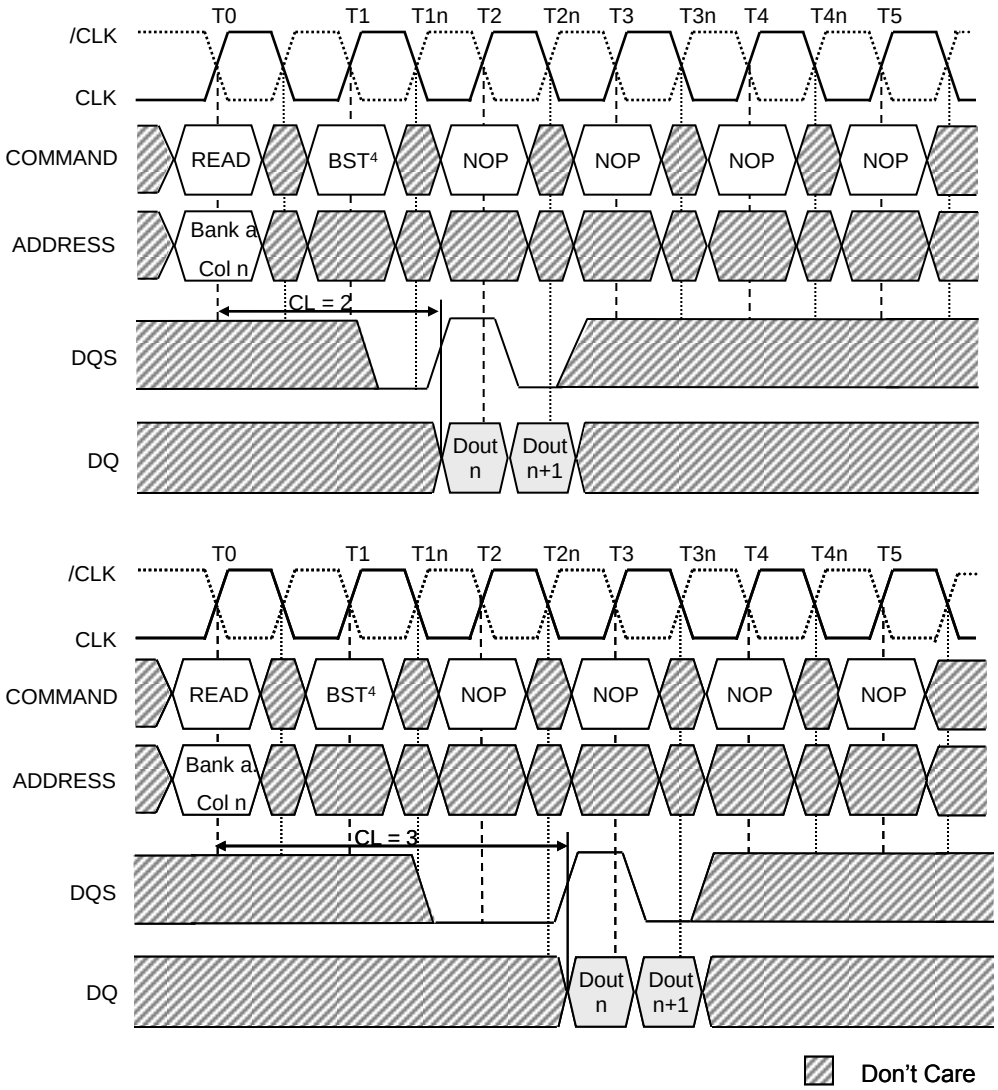
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 11 on page 31. The BURST TERMINATE latency is equal to the READ (CAS) latency, i.e., the BURST TERMINATE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 12 on page 32. The tDQSS (MIN) case is shown; the tDQSS (MAX) case has a longer bus idle time. (tDQSS [MIN] and tDQSS [MAX] are defined in the section on WRITEs.)

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated. The PRECHARGE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the *n*-prefetch architecture). This is shown in Figure 13 on page 33. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

Note: Part of the row precharge time is hidden during the access of the last data elements

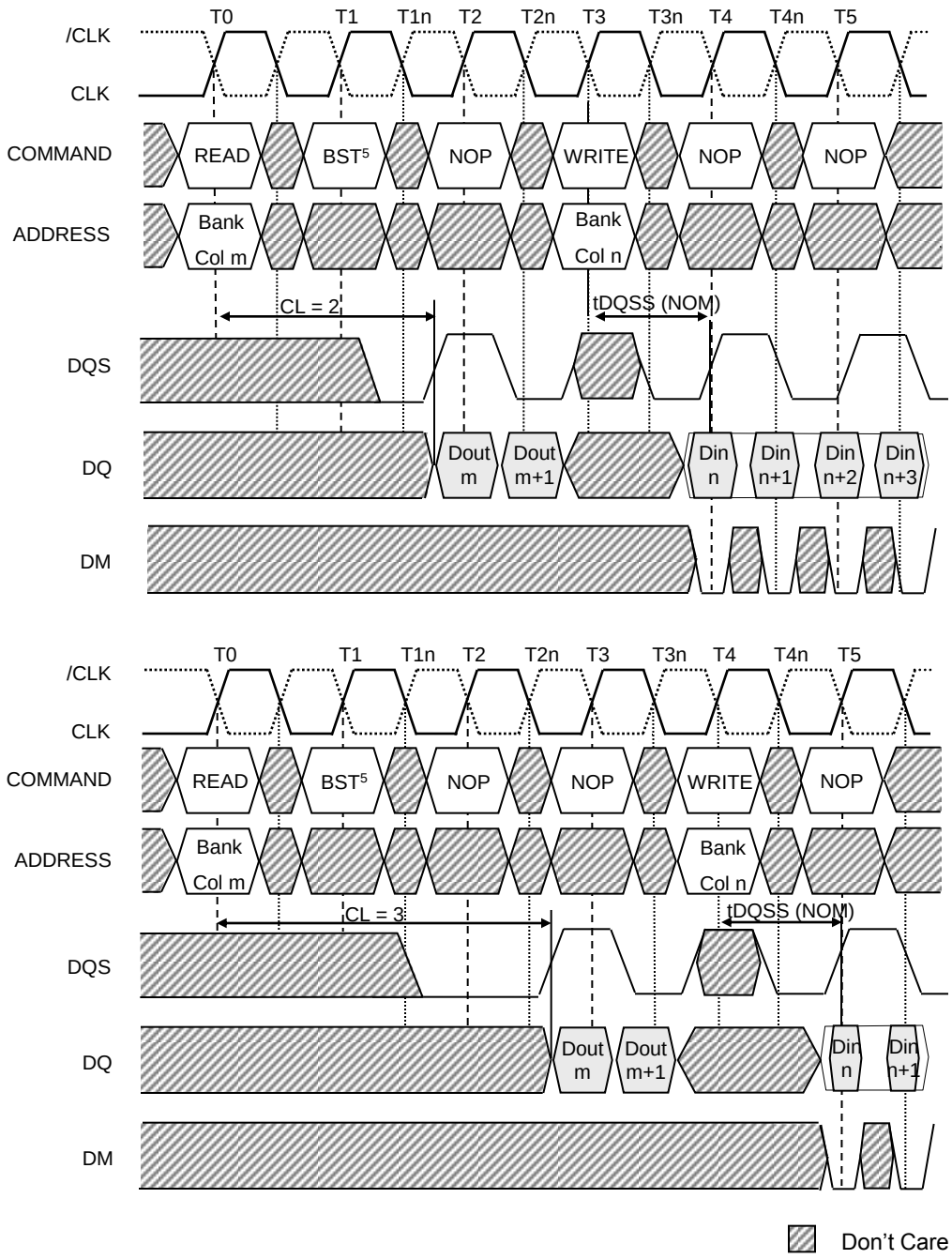
Figure 11: READ Burst Terminated



Notes :

1. Dout n = data-out from column n.
2. Only valid for BL = 4 and BL = 8.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. BST = BURST TERMINATE command; page remains open.
5. CKE = HIGH.

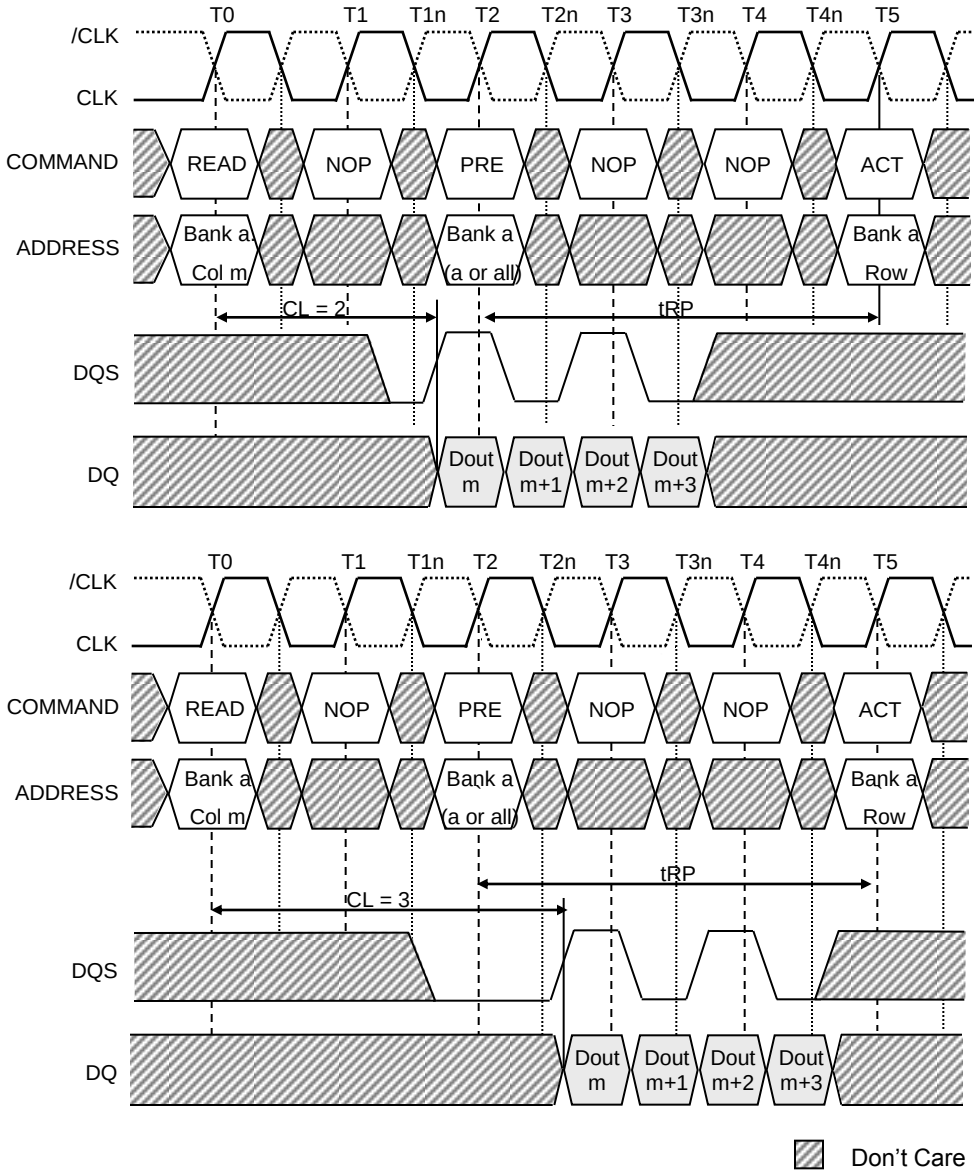
Figure 12: READ-to-WRITE Operation



Notes :

1. Dout m = data-out from column m.
2. Din n = data-in from column n.
3. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
4. Shown with nominal tAC, tDQSCLK, and tDQSQ.
5. BST = BURST TERMINATE command; page remains open.
6. CKE = HIGH.

Figure 13: READ-to-PRECHARGE Operation



Notes :

1. Dout m = data-out from column m.
2. BL = 4 or an interrupted burst of 8.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. READ-to-PRECHARGE equals 2 clocks, which allows 2 data pairs of data-out.
5. A READ command with auto precharge enabled, provided tRAS (MIN) is met, would cause a precharge to be performed at *x* number of clock cycles after the READ command, where *x* = BL / 2.
6. PRE = PRECHARGE command; ACT = ACTIVE command.

WRITE

WRITE bursts are initiated with a WRITE command, as shown in Figure 14 on page 35. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75 percent to 125 percent of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., tDQSS [MIN] and tDQSS [MAX]) might not be intuitive, they have also been included. Figure 15 on page 36 shows the nominal case and the extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

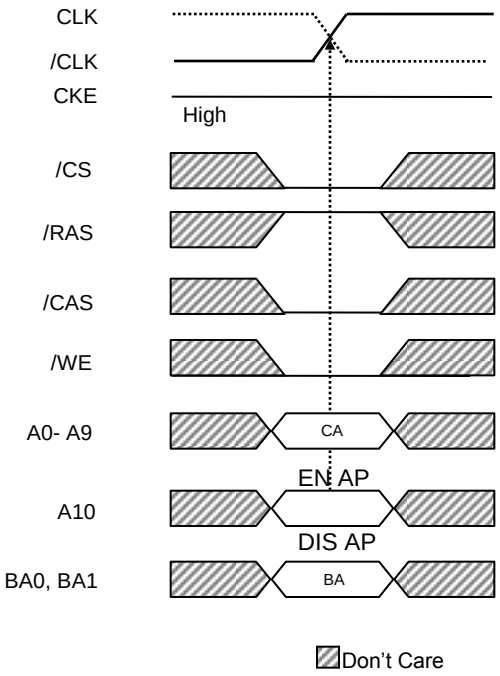
Figure 16 on page 37 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 17 on page 37. Full-speed random write accesses within a page or pages can be performed, as shown in Figure 18 on page 38. Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst, tWTR should be met, as shown in Figure 19 on page 39.

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figure 20 on page 40. Note that only the data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 21 on page 41.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, tWR should be met, as shown in Figure 22 on page 42.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure 23 on page 43 and Figure 24 on page 44. Note that only the data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 23 on page 43 and Figure 24 on page 44. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

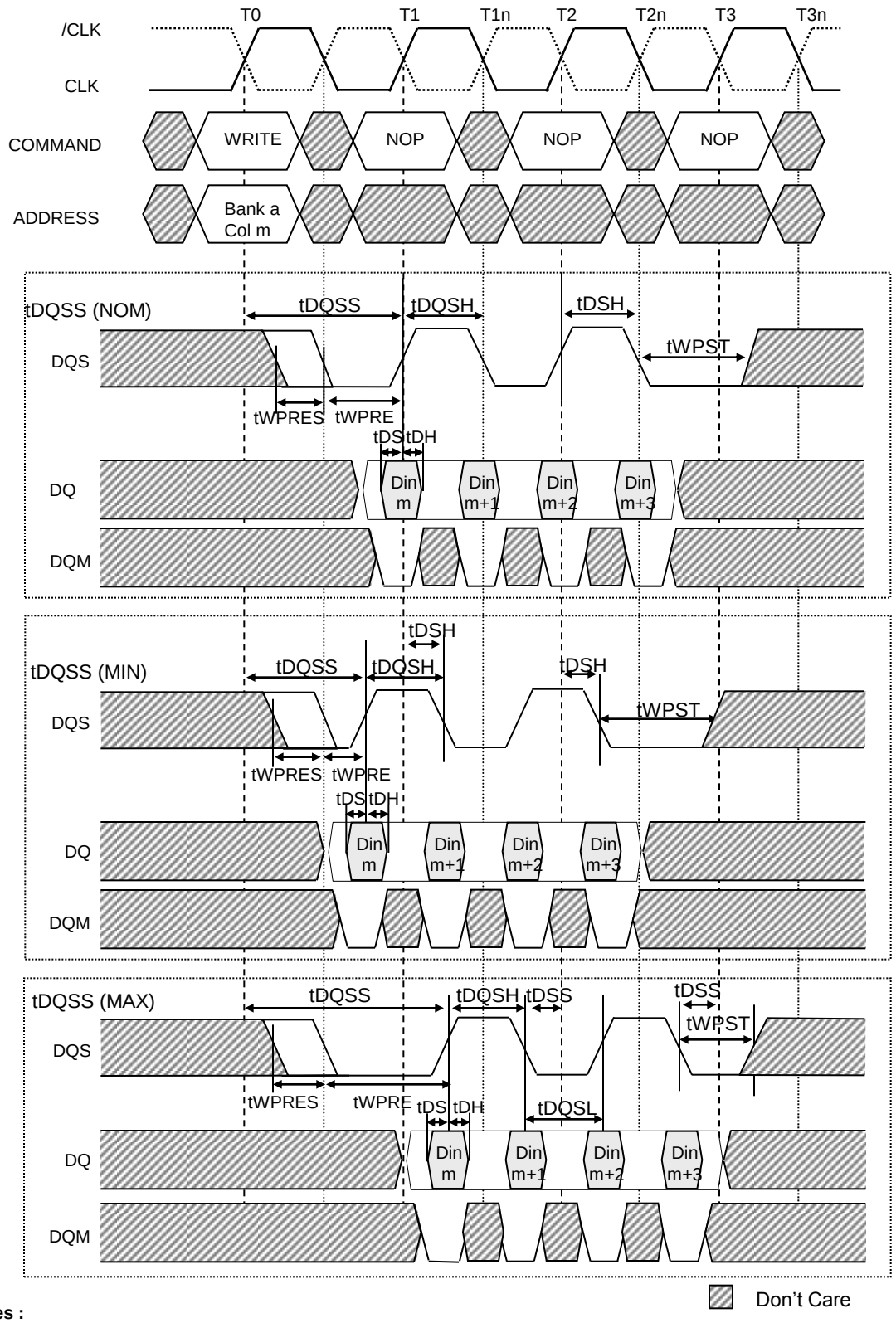
Figure 14: WRITE Command



Note :

1. DIS AP = Disable Auto Precharge
2. EN AP = Enable Auto Precharge
3. BA = Bank Address
4. CA = Column Address

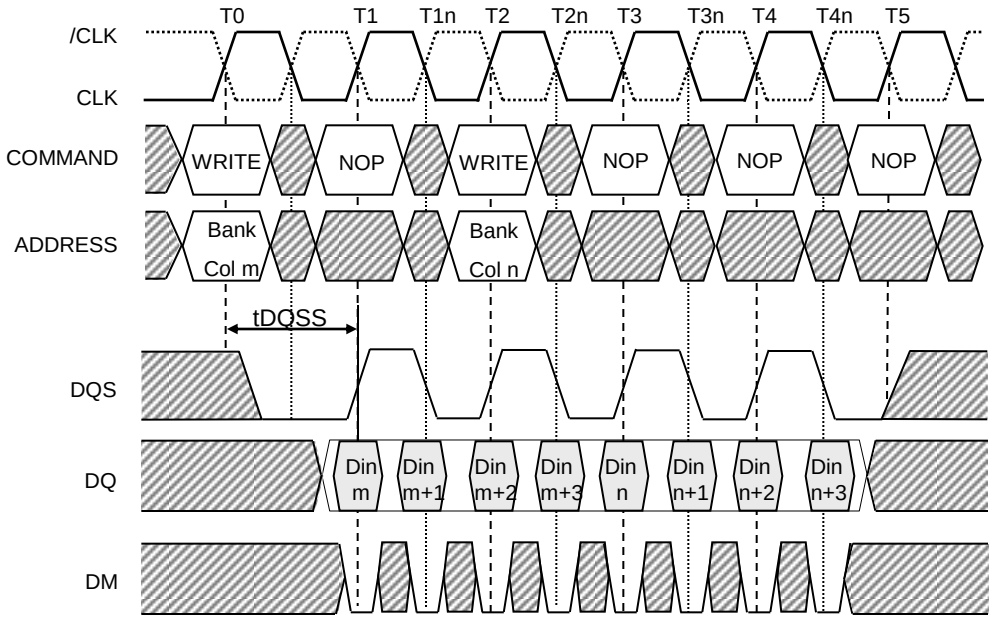
Figure 15: WRITE Operation



Notes :

1. Din m = data-in for column m.
2. An uninterrupted burst of 4 is shown.
3. A10 is LOW with the WRITE command (auto precharge is disabled).

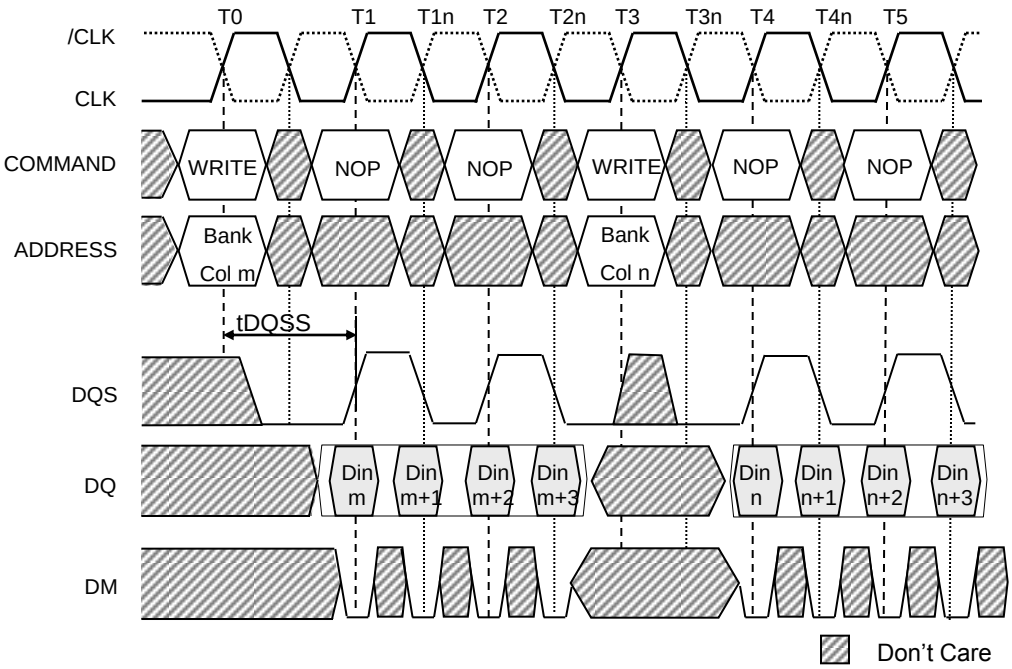
Figure 16: Consecutive WRITE-to-WRITE



Notes :

1. Din m (n) = data-in for column m (n).
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.

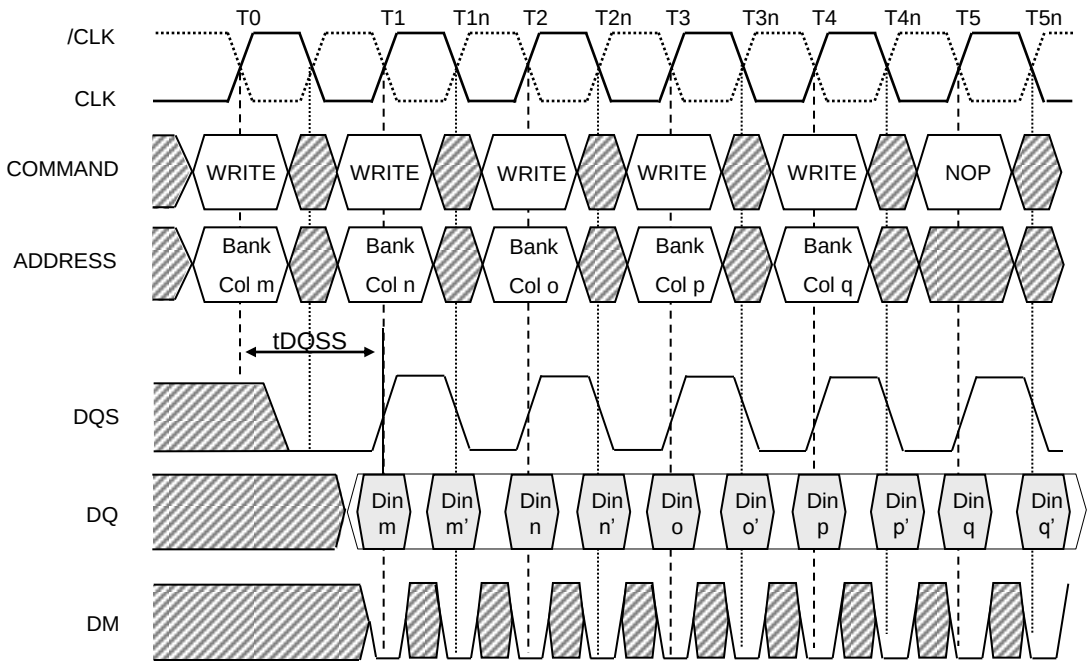
Figure 17: WRITE-to-WRITE Operation



Notes :

1. Din m (n) = data-in for column m (n).
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.

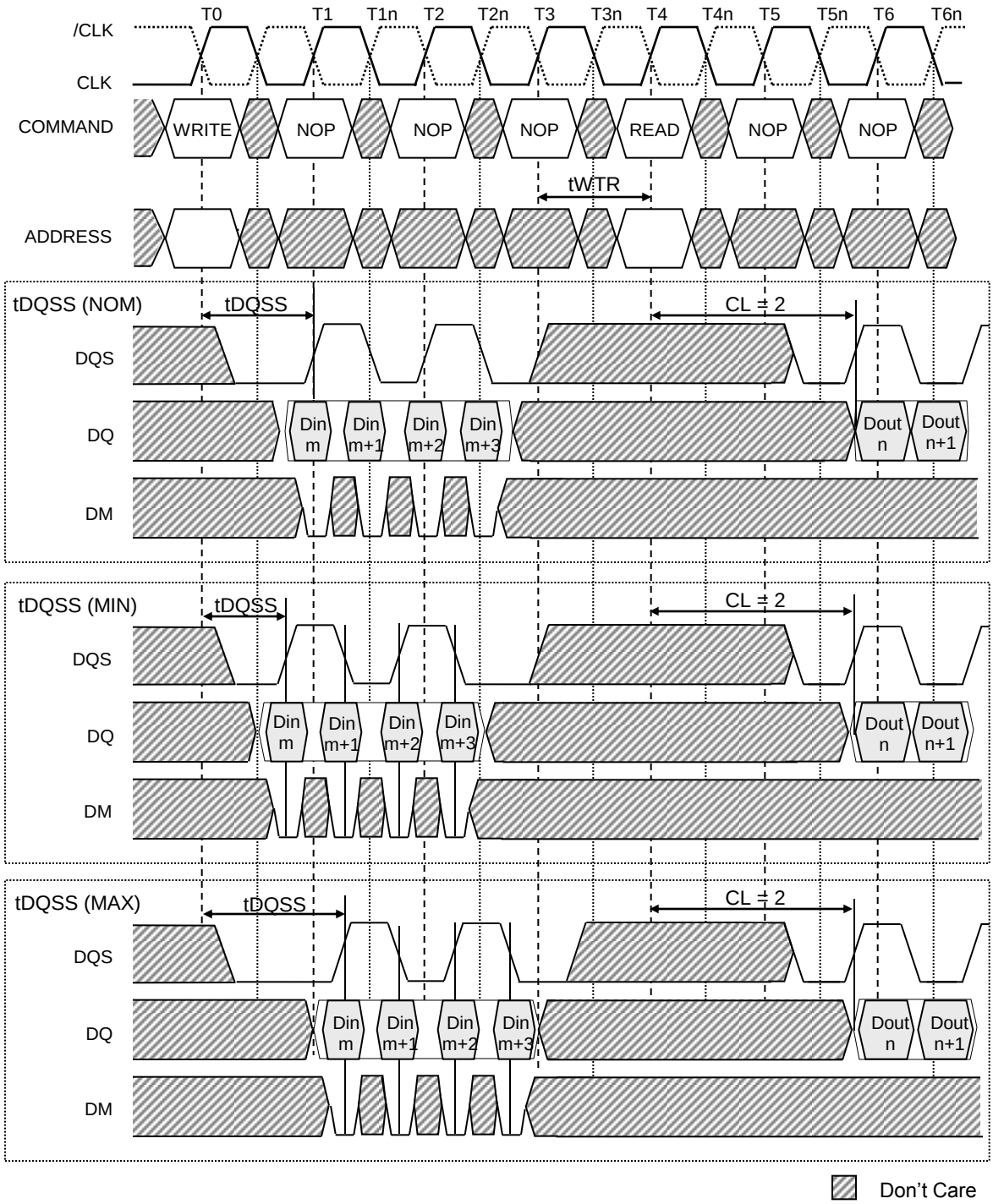
Figure 18: Random WRITE Cycles



Notes :

1. Din m (or n, o, p, q) = data-in for column m (or n, o, p, q)
2. m' (or n, o, p, q) = the next data-in following Din m (or n, o, p, q), according to the programmed burst order.
3. Programmed BL = 2, 4, or 8 in cases shown.
4. Each WRITE command may be to any bank.

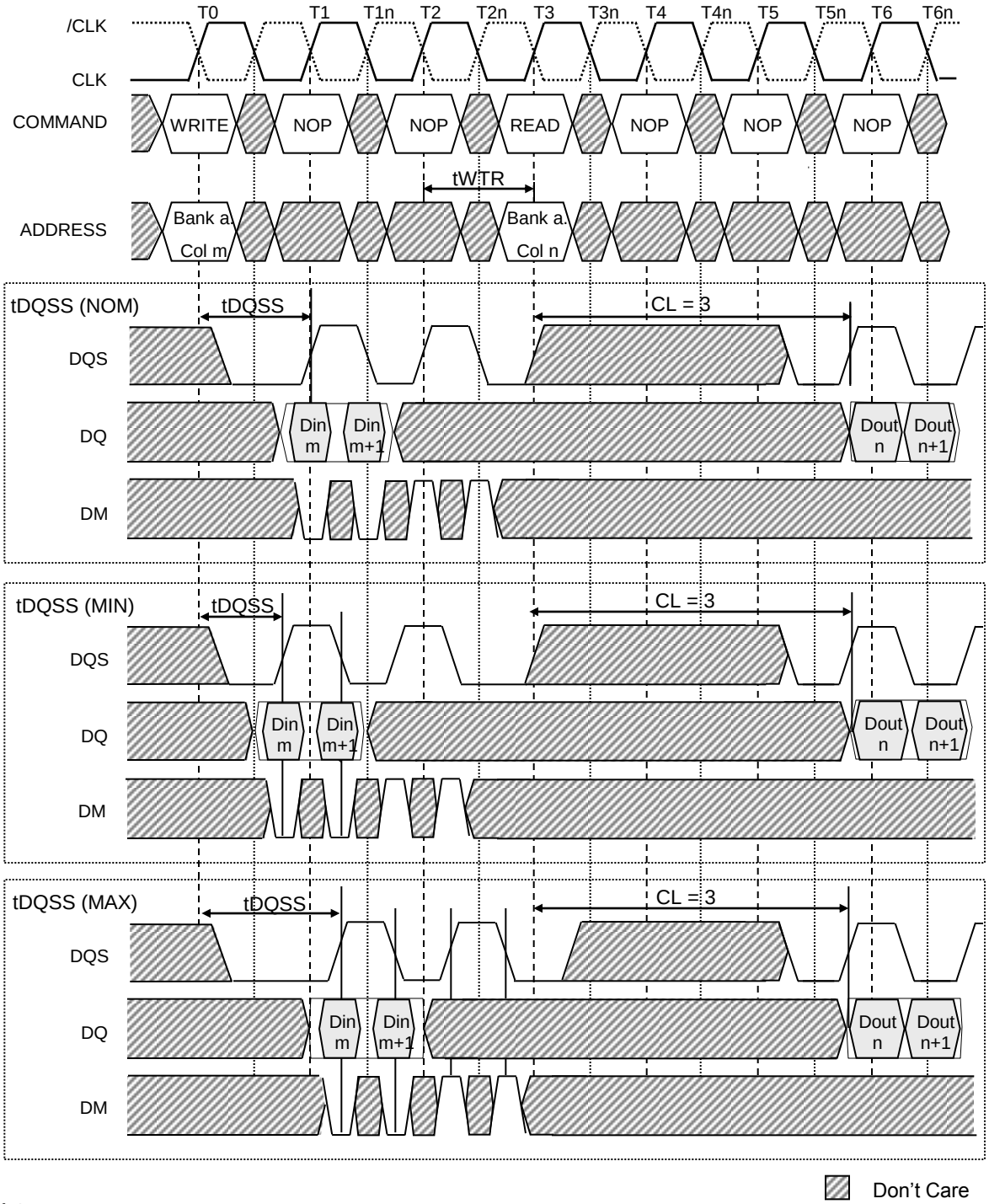
Figure 19: WRITE-to-READ – Uninterrupting



Notes :

1. Din m = data-in for column m; Dout n = data-out for column n.
2. An uninterrupted burst of 4 is shown.
3. tWTR is referenced from the first positive CLK edge after the last data-in pair.
4. The READ and WRITE commands are to same device. However, the READ and WRITE commands may be to different devices, in which case tWTR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).

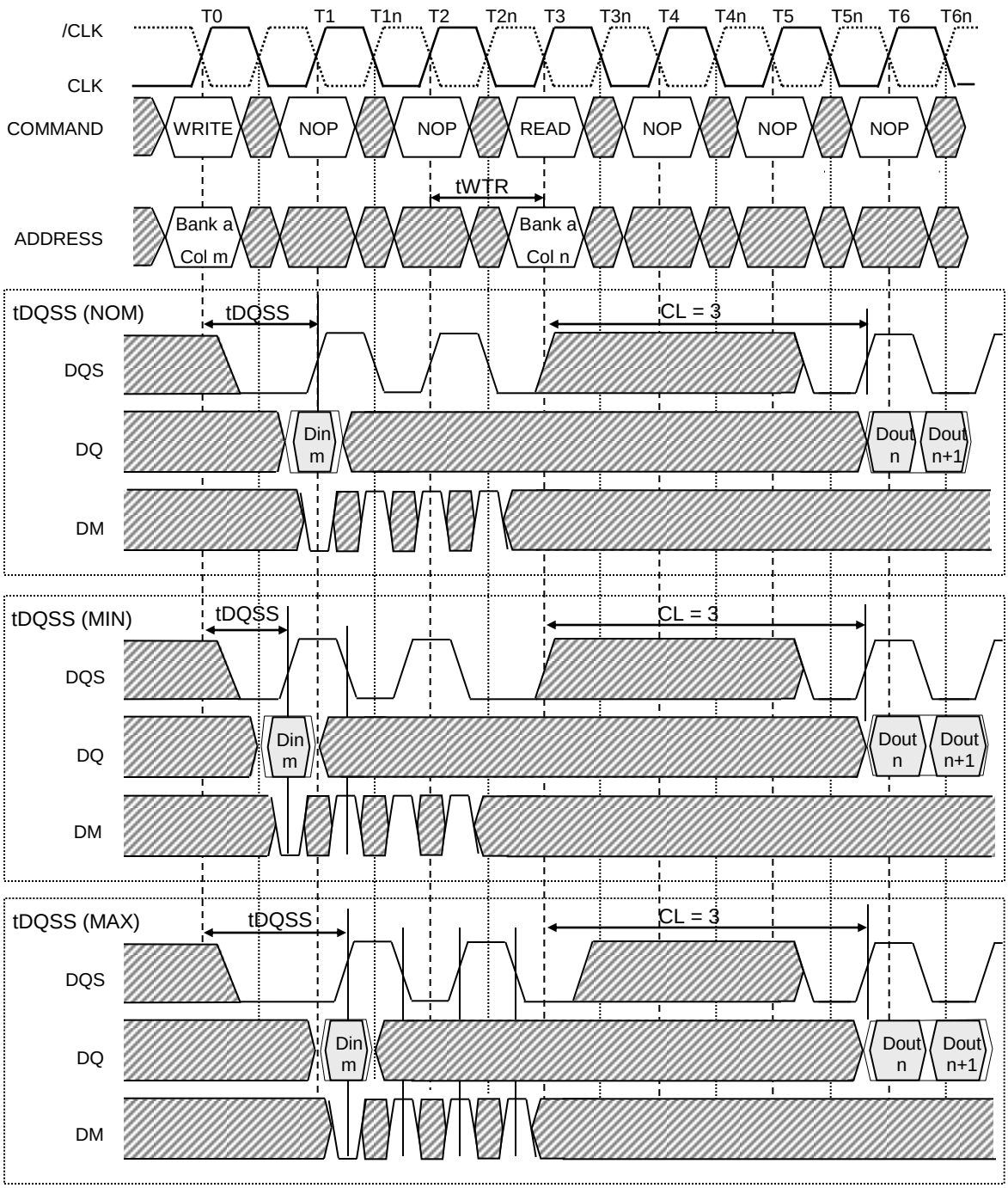
Figure 20: WRITE-to-READ – Interrupting



Notes :

1. Din m = data-in for column m; Dout n = data-out for column n.
2. An interrupted burst of 4 is shown; two data elements are written.
3. tWTR is referenced from the first positive CLK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used and RD is required at T5, DM and DQS would be required at T4 and T4n because the READ command would not mask these two data elements.

Figure 21: WRITE-to-READ – Odd Number of Data, Interrupting

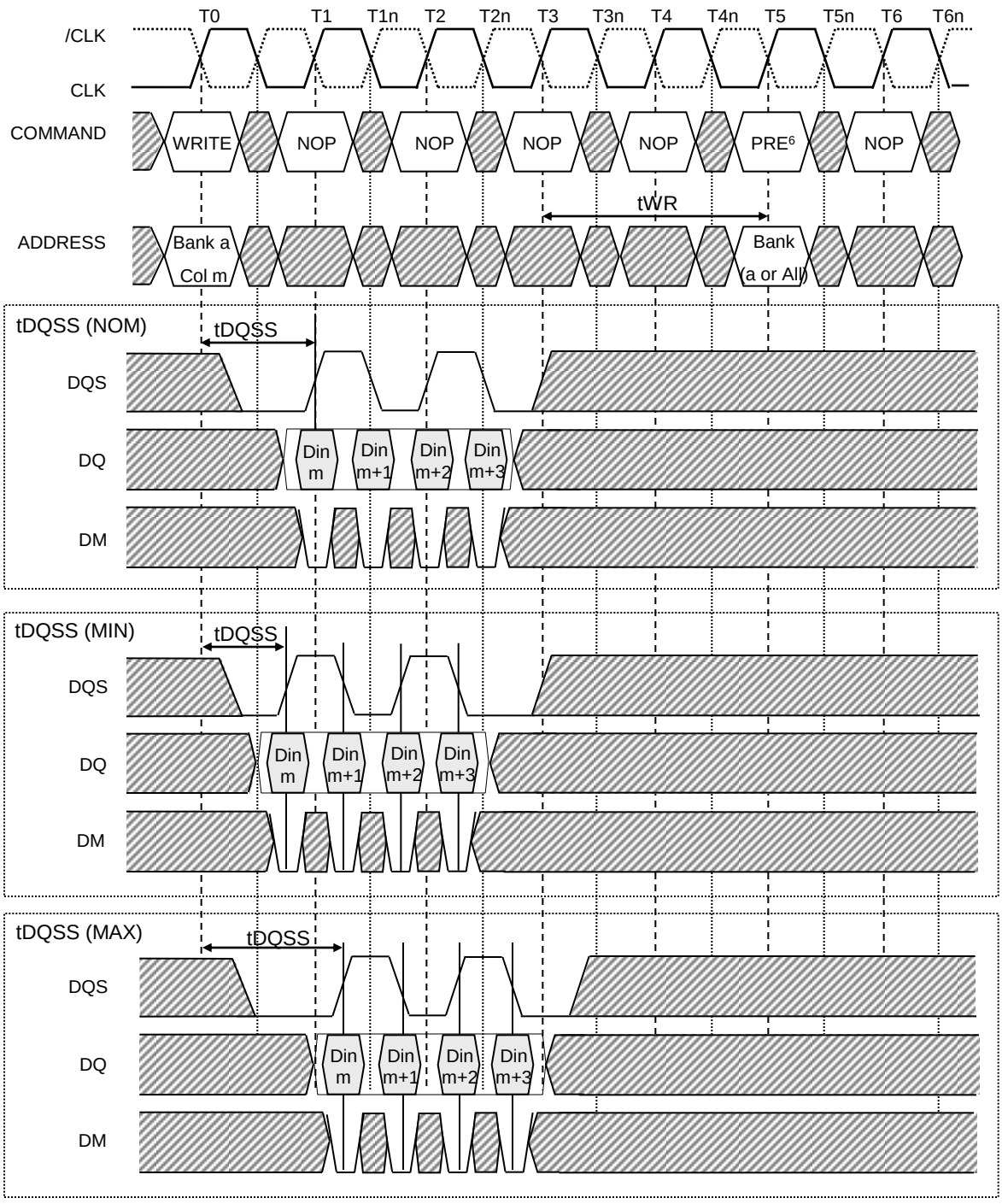


Notes :

Don't Care

1. Din m = data-in for column m; Dout n = data-out for column n.
2. An interrupted burst of 4 is shown; two data elements are written, three are masked.
3. tWTR is referenced from the first positive CLK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used and RD is required at T5, DM and DQS would be required at T4 and T4n because the READ command would not mask these two data elements.

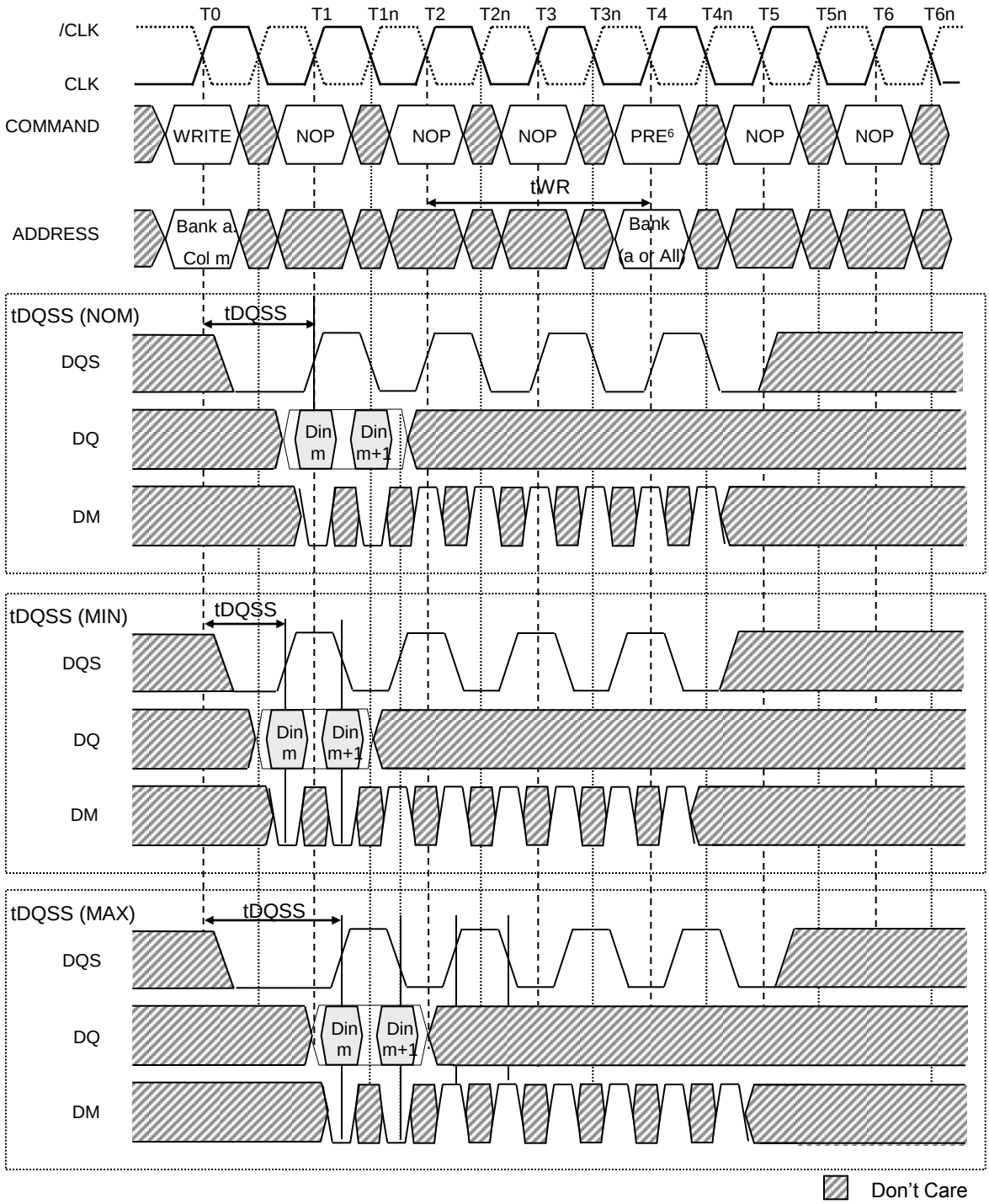
Figure 22: WRITE-to-PRECHARGE – Uninterrupting



Notes :

1. Din m = data-in for column m.
2. An uninterrupted burst of 4 is shown.
3. tWR is referenced from the first positive CLK edge after the last data-in pair.
4. The PRECHARGE and WRITE commands are to same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case tWR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. PRE = PRECHARGE command.

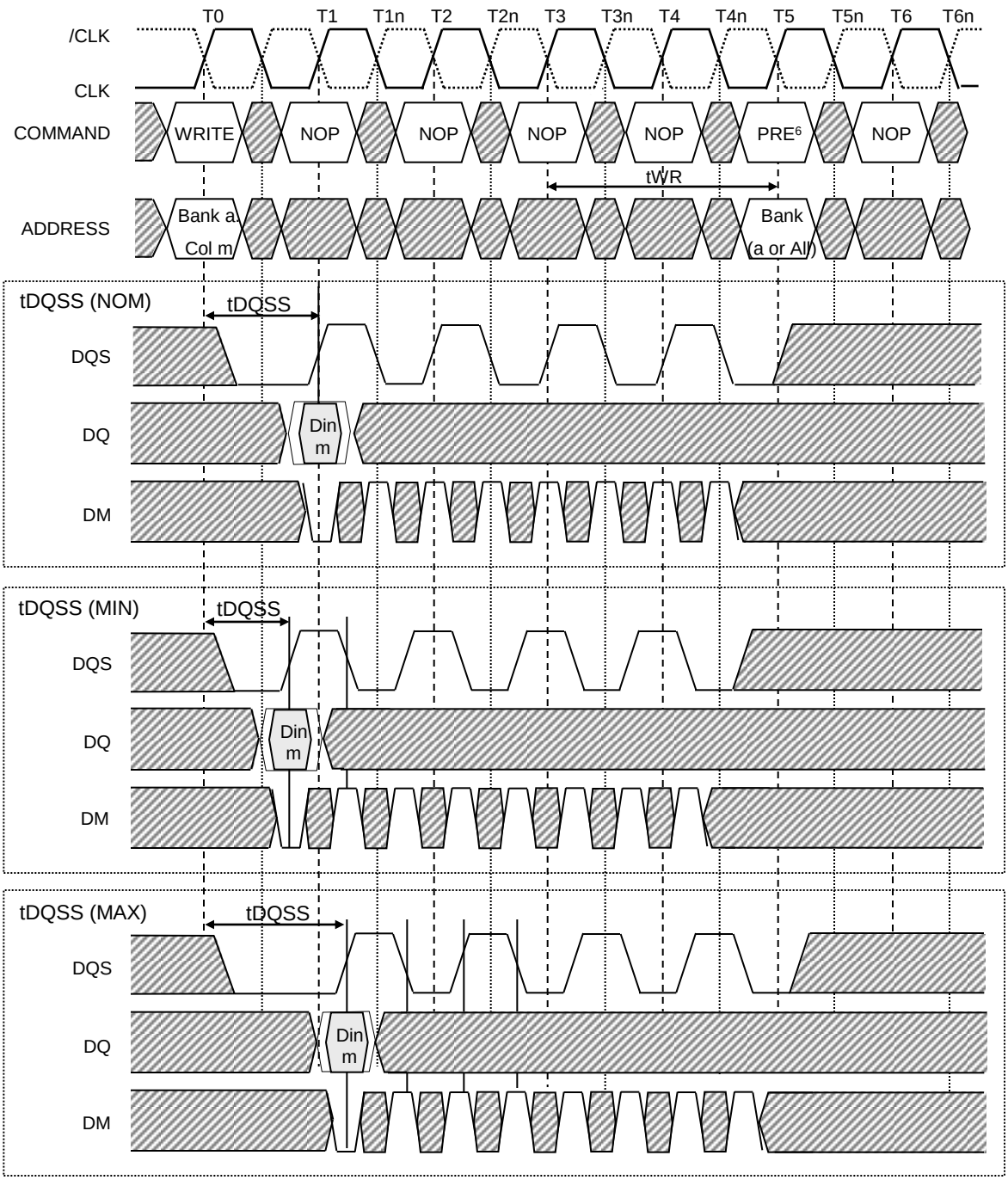
Figure 23: WRITE-to-PRECHARGE – Interrupting



Notes :

1. Din m = data-in for column m.
2. An interrupted burst of 8 is shown.
3. tWR is referenced from the first positive CLK edge after the last data-in pair.
4. The PRECHARGE and WRITE commands are to same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case tWR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. PRE = PRECHARGE command.

Figure 24: WRITE-to-PRECHARGE – Odd Number of Data, Interrupting



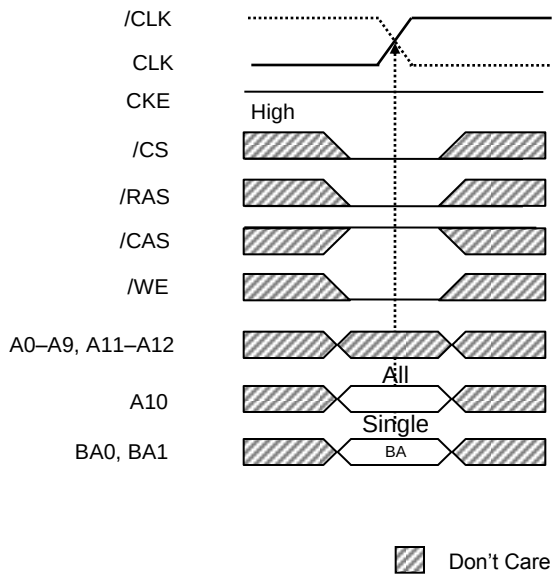
Notes :

1. Din m = data-in for column m.
2. An interrupted burst of 8 is shown.
3. tWR is referenced from the first positive CLK edge after the last data-in pair.
4. The PRECHARGE and WRITE commands are to same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case tWR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. PRE = PRECHARGE command.

PRECHARGE

The PRECHARGE command (Figure 25) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 25: PRECHARGE Command



Note :

1. BA = Bank Address.
2. All = All banks to be Precharged, BA1, BA0 are “Don't Care.”
3. Single = Only bank selected by BA1 and BA0 will be precharged.

Power-Down (CKE Not Active)

Unlike SDR SDRAMs, DDR SDRAMs require CKE to be active at all times an access is in progress: from the issuing of a READ or WRITE command until completion of the burst; thus a clock suspend is not supported. For READs, a burst completion is defined when the read postamble is satisfied; For WRITEs, a burst completion is defined when the write postamble is satisfied.

Power-Down (Active or Precharge)

Power-down (Figure 27) is entered when CKE is registered LOW. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, including CLK and /CLK. Exiting power-down requires the device to be at the same voltage as when it entered power-down and a stable clock.

Note :

The power-down duration is limited by the refresh requirements of the device. While in power-down, CKE LOW must be maintained at the inputs of the Low Power DDR SDRAM, while all other input signals are “Don’t Care.” The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). NOPs or DESELECT commands must be maintained on the command bus until tPDX is satisfied.

Figure 26: Power-Down Command (Active or Precharge)

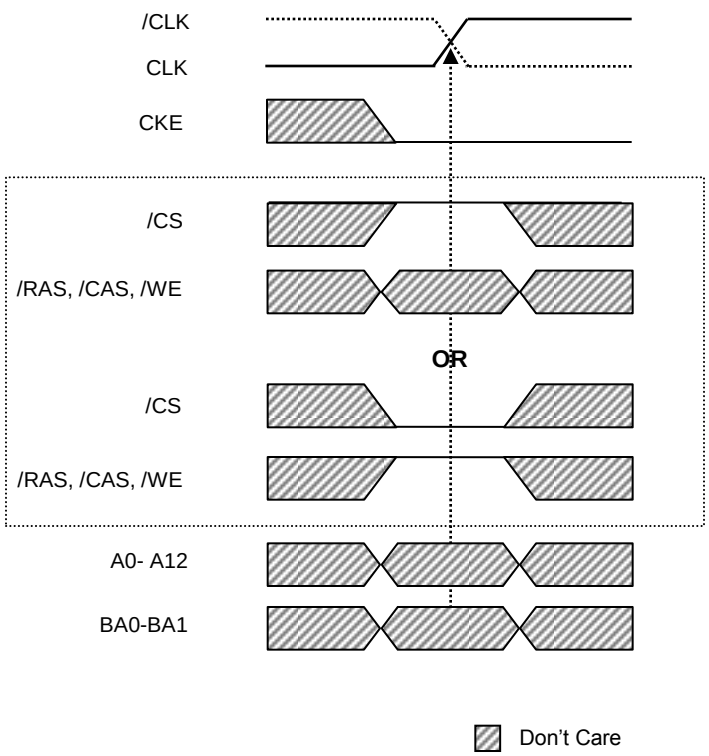
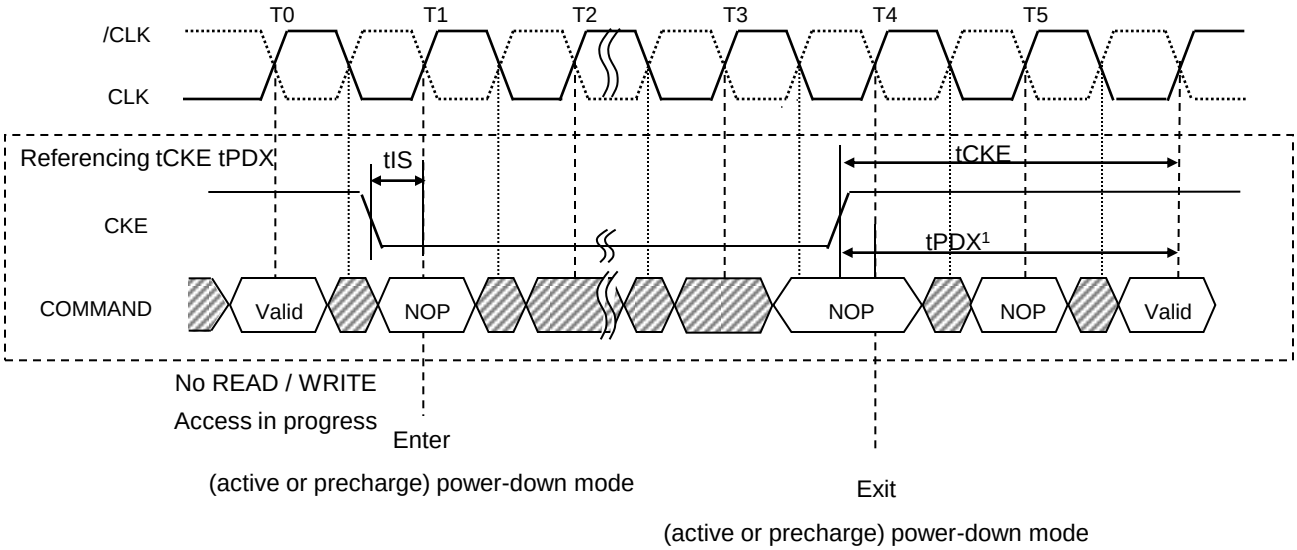


Figure 27: Power-Down (Active or Precharge)



Notes: 1. Clock must toggle a minimum of once during this time.

Truth Tables

Table 13: Truth Table – CKE

Notes: 1–5

CKEn-1	CKEn	Current State	COMMANDn	ACTIONn	Notes
L	L	(Active) Power-Down	X	Maintain (active) power-down	
L	L	(Precharge) Power-Down	X	Maintain (precharge) power-down	
L	L	Self refresh	X	Maintain self refresh	
L	H	(Active) Power-Down	DESELECT or NOP	Exit (active) power-down	6, 7
L	H	(Precharge) Power-Down	DESELECT or NOP	Exit (precharge) power-down	6, 7
L	H	Self refresh	DESELECT or NOP	Exit self refresh	8, 9
H	L	Bank(s) active	DESELECT or NOP	(Active) power-down entry	
H	L	All banks idle	DESELECT or NOP	(Precharge) power-down entry	
H	L	All banks idle	AUTO REFRESH	Self refresh entry	
H	H		See Table 15 on page 49		
H	H		See Table 15 on page 49		

Notes :

1. CKEn is the logic state of CKE at clock edge *n*; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge *n*.
3. COMMANDn is the command registered at clock edge *n,* and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. tCKE pertains.
6. DESELECT or NOP commands should be issued on any clock edges occurring during the tPDX period.
7. The clock must toggle at least once during the tPDX period.
8. DESELECT or NOP commands should be issued on any clock edges occurring during the tXSR period.
9. The clock must toggle at least once during the tXSR period.

Table 14 Truth Table – Current State Bank *n* - Command to Bank *n*

Notes : 1–6; notes appear below and on next page

Current State	/CS	/RAS	/CAS	/WE	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
Row active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8, 11

Notes :

1. This table applies when CKEn-1 was HIGH and CKEn is HIGH and after tXSR has been met (if the previous state was self refresh) and after tPDX has been met (if the previous state was power-down).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 14, and according to Table15.

   Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the row active state.

   Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

   Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRFC is met. Once tRFC is met, the DDR SDRAM will be in the all banks idle state.

   Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command and ends when tMRD has been met. Once tMRD is met, the Low Power DDR SDRAM will be in the all banks idle state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.

10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Table 15: Truth Table – Current State Bank *n* - Command to Bank *m*

Notes : 1–6; notes appear below and on next page

Current State	/CS	/RAS	/CAS	/WE	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command allowed to bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (auto precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start WRITE burst)	7. 9, 3a
	L	L	H	L	PRECHARGE	
Write (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 3a
	L	L	H	L	PRECHARGE	

Notes :

1. This table applies when CKE*n*-1 was HIGH and CKEn is HIGH and after tXSR has been met (if the previous state was self refresh) or after tPDX has been met (if the previous state was power-down).
2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Read with auto precharge enabled: See following text – 3a

   Write with auto precharge enabled: See following text – 3a

3a. The read with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when tWR ends, with tWR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins.

   This device supports concurrent auto precharge such that when a read with auto precharge enabled or a write with auto precharge is enabled any command to other banks is allowed, long as that command does not interrupt the read or write data transfer already in process. either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

3b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized below.

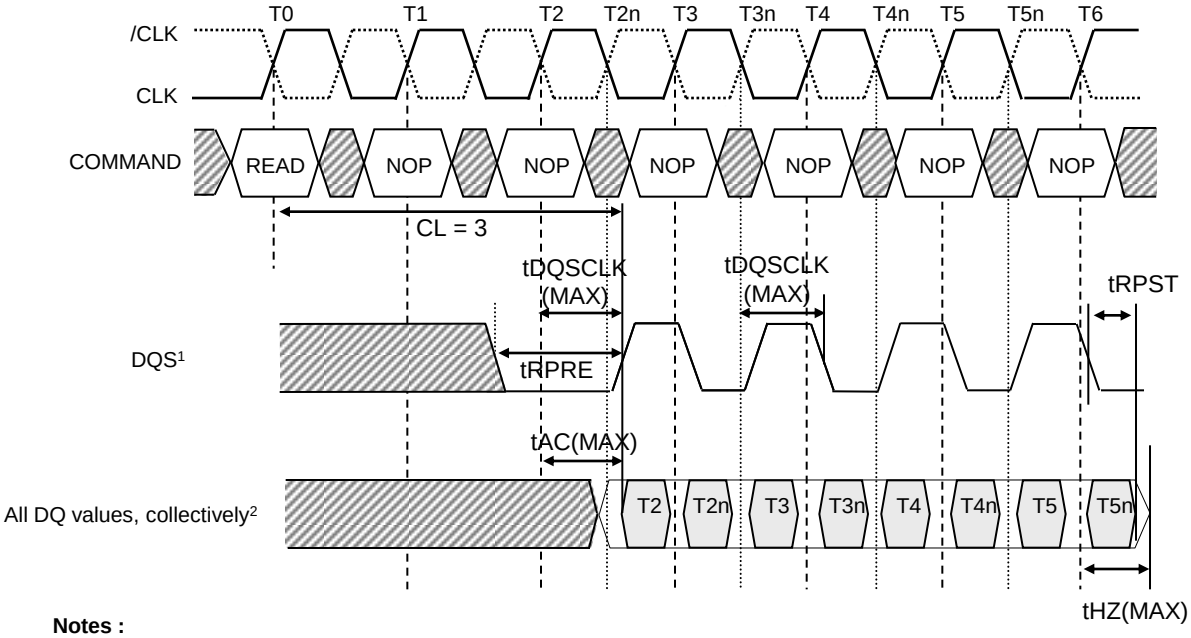
From Command	To Command	Minimum Delay (with Concurrent Auto Precharge)
WRITE w/AP	READ or READ w/AP	[1 + (BL/2)] tCLK + tWTR
	WRITE or WRITE w/AP	(BL/2) tCLK
	PRECHARGE	1 tCLK
	ACTIVE	1 tCLK
READ w/AP	READ or READ w/AP	(BL/2) × tCLK
	WRITE or WRITE w/AP	[CLRU + (BL/2)] tCLK
	PRECHARGE	1 tCLK
	ACTIVE	1 tCLK

CLRU = CAS Latency (CL) rounded up to the next integer

BL = Burst Length

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

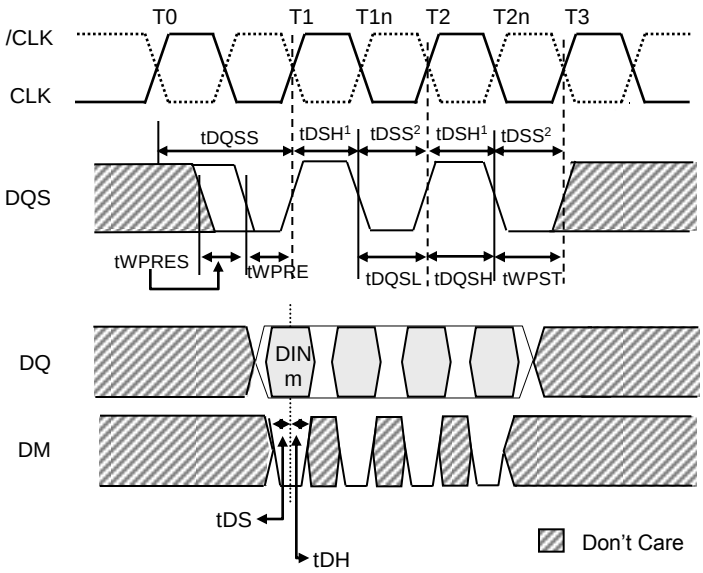
Figure 28: Data Output Timing – tAC and tDQSCLK



Notes :

1. DQ transitioning after DQS transition define tDQSQ window.
2. All DQ must transition by tDQSQ after DQS transitions, regardless of tAC.
3. tAC is the DQ output window relative to CLK, and is the “long term” component of DQ skew.

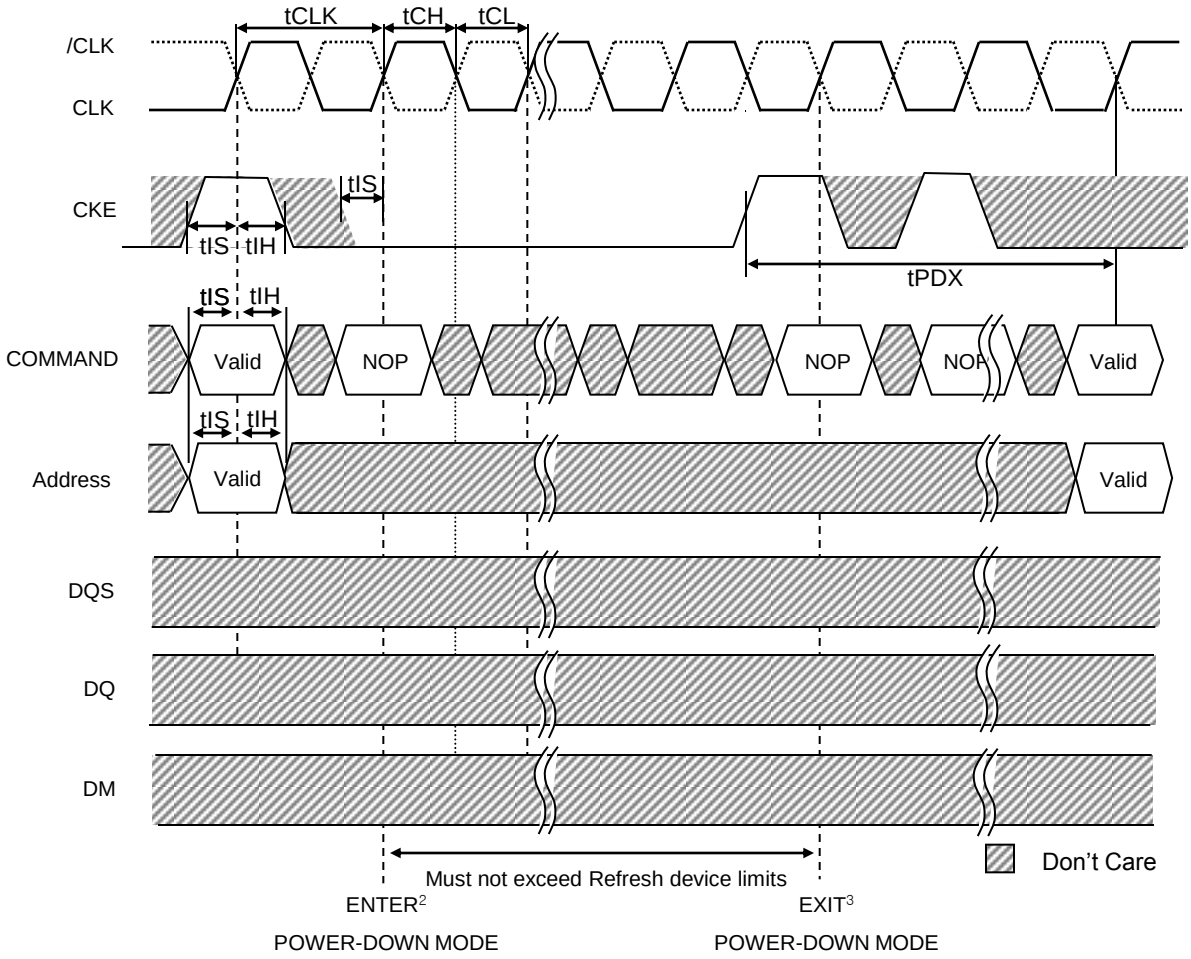
Figure 29: Data Input Timing



Notes :

1. tDSH (MIN) generally occurs during tDQSS (MIN).
2. tDSS (MIN) generally occurs during tDQSS (MAX).
3. WRITE command issued at T0.

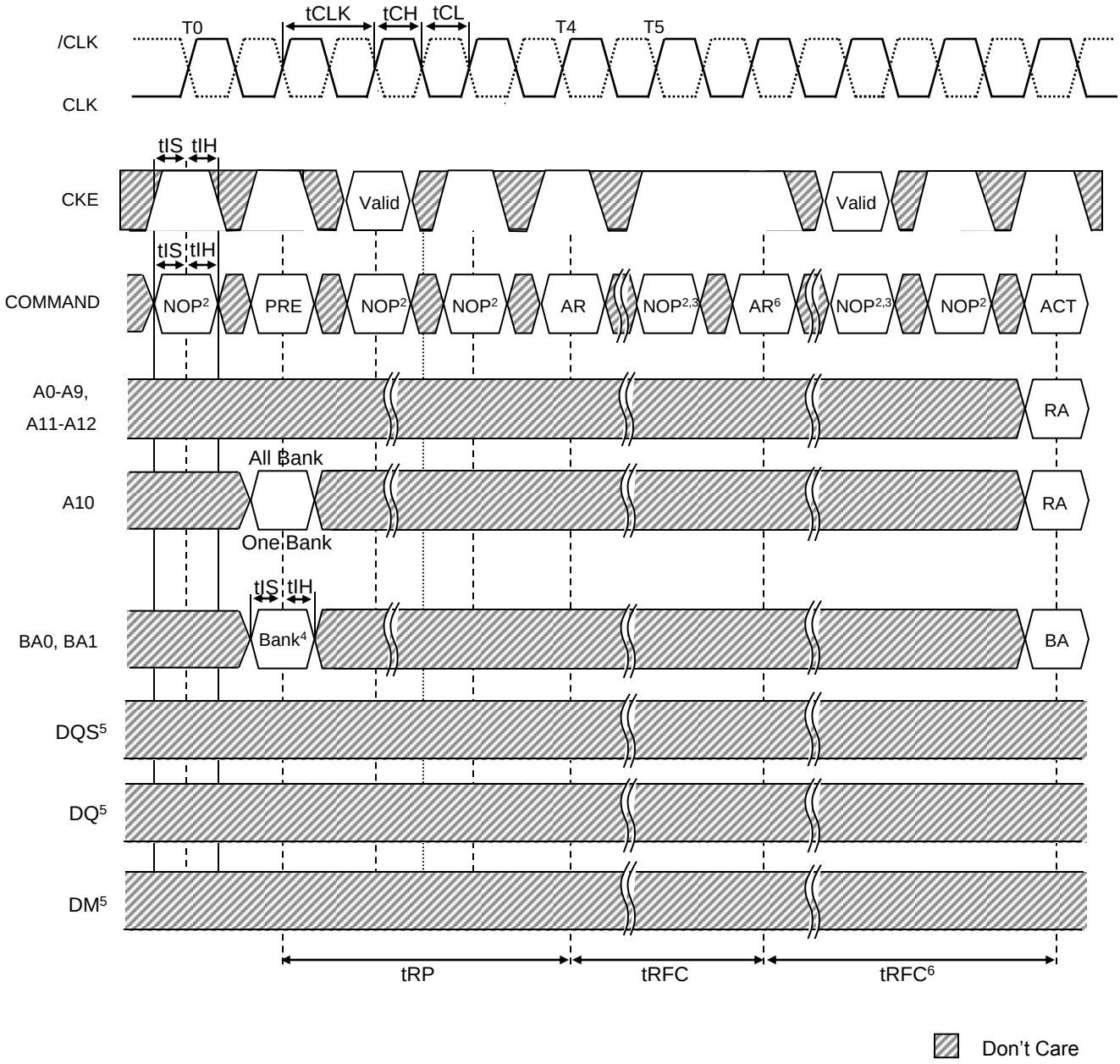
Figure 30: Power-Down Mode (Active or Precharge)



Notes :

1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. No column accesses are allowed to be in progress at the time power-down is entered.
3. There must be at least one clock pulse during tPDX time.

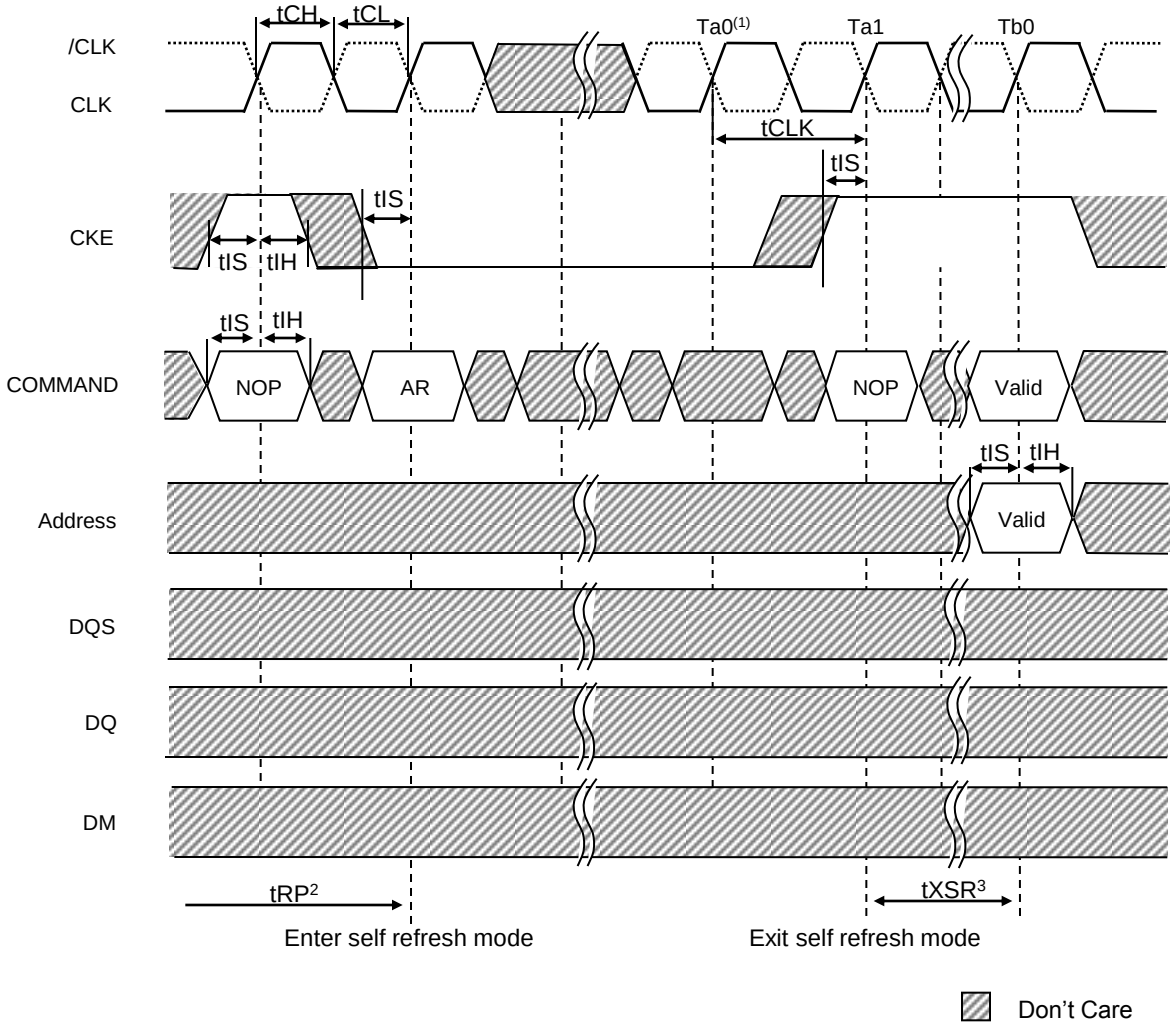
Figure 31: Auto Refresh Mode



Notes :

1. PRE = PRECHARGE, ACT = ACTIVE, AR = AUTO REFRESH, RA = Row address, BA = Bank address.
2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
3. NOP or COMMAND INHIBIT are the only commands allowed until after tRFC time, CKE must be active during clock positive transitions.
4. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks).
5. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.
6. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.

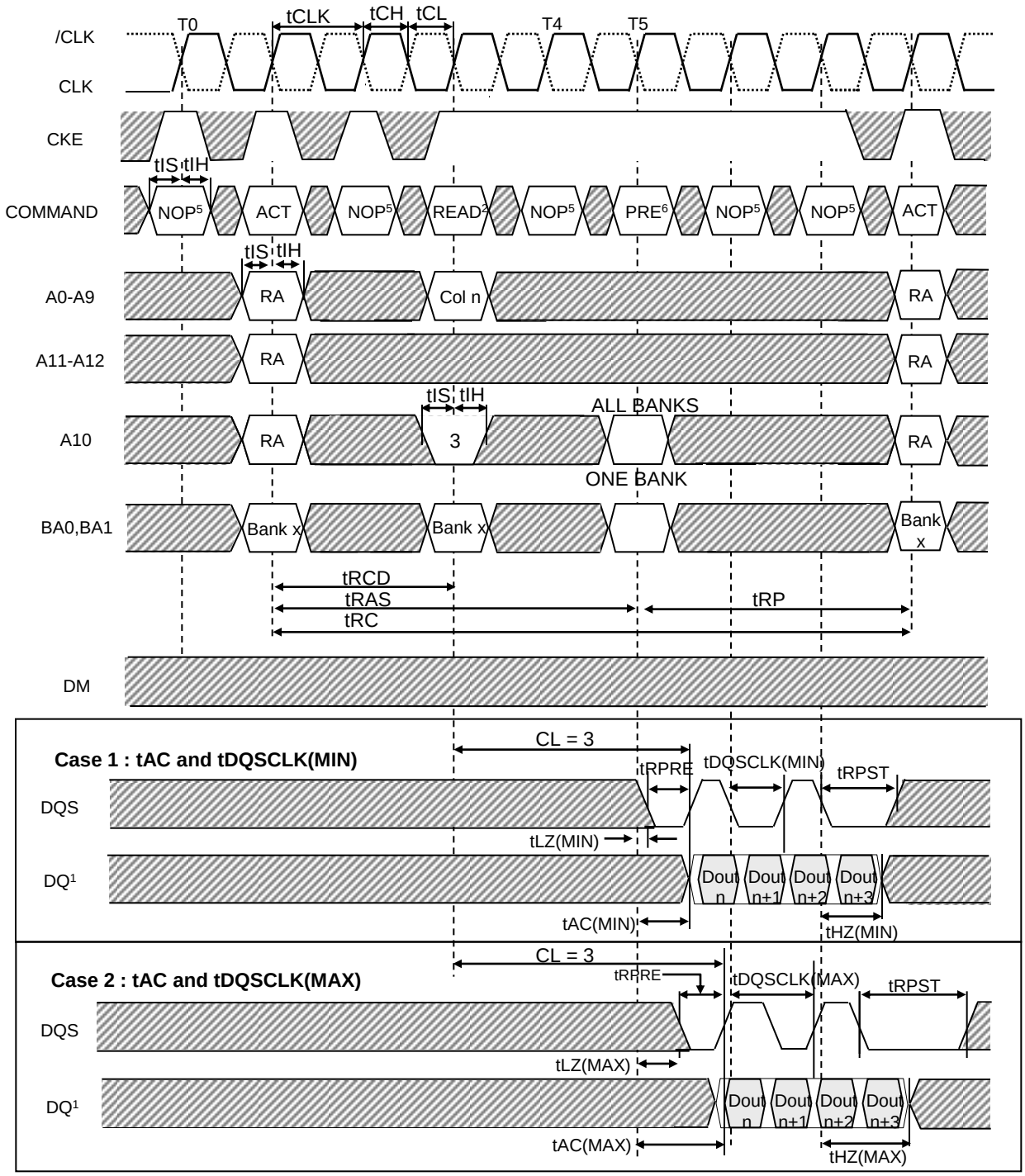
Figure 32: Self Refresh Mode



Notes :

1. Clock must be stable before exiting self refresh mode. That is, the clock must be cycling within specifications by Ta0.
2. Device must be in the all banks idle state prior to entering self refresh mode.
3. NOPs or DESELECT are required for tXSR time with at least two clock pulses.
4. AR = AUTO REFRESH command.

Figure 33: Bank Read – Without Auto Precharge

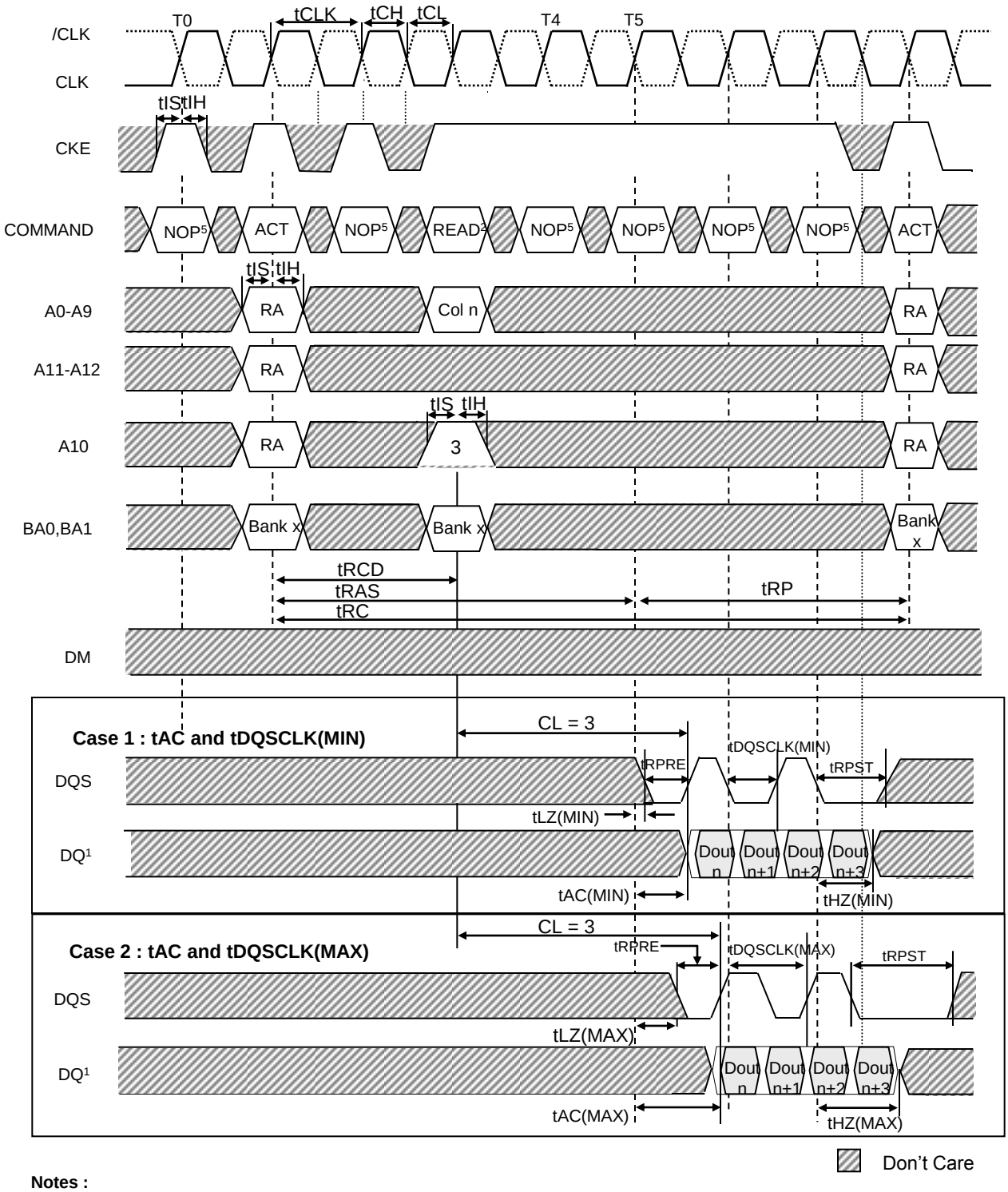


Notes :

1. Dout n = data-out from column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. The PRECHARGE command can only be applied at T5 if tRAS minimum is met.

▨ Don't Care

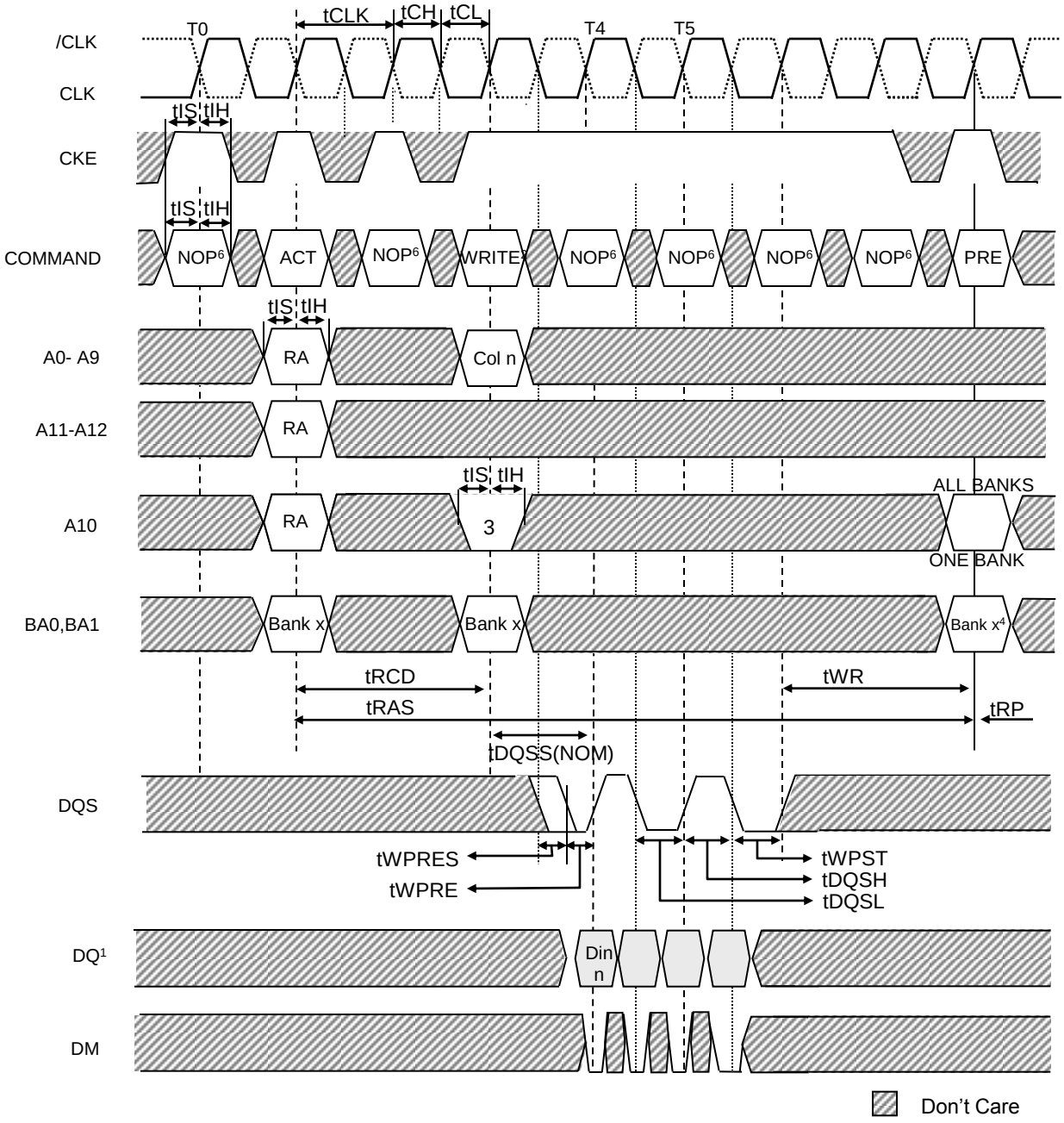
Figure 34: Bank Read – With Auto Precharge



Notes :

1. Dout n = data-out from column n.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.

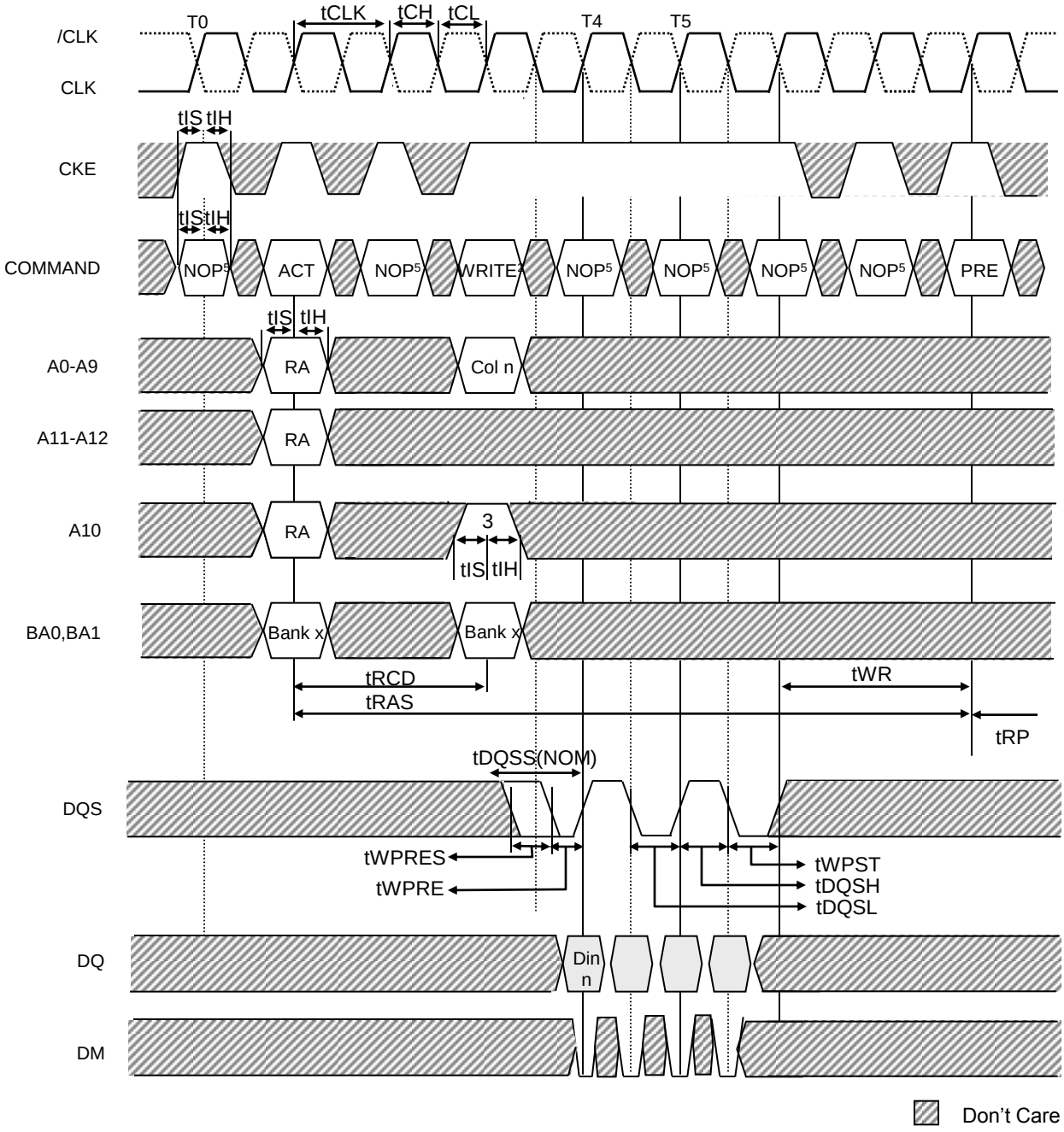
Figure 35: Bank Write – Without Auto Precharge



Notes :

1. Din n = data-in for column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T8.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. tDSH is applicable during tDQSS (MIN) and is referenced from tCLK T4 or T5.
8. tDSH is applicable during tDQSS (MAX) and is referenced from tCLK T5 or T6.

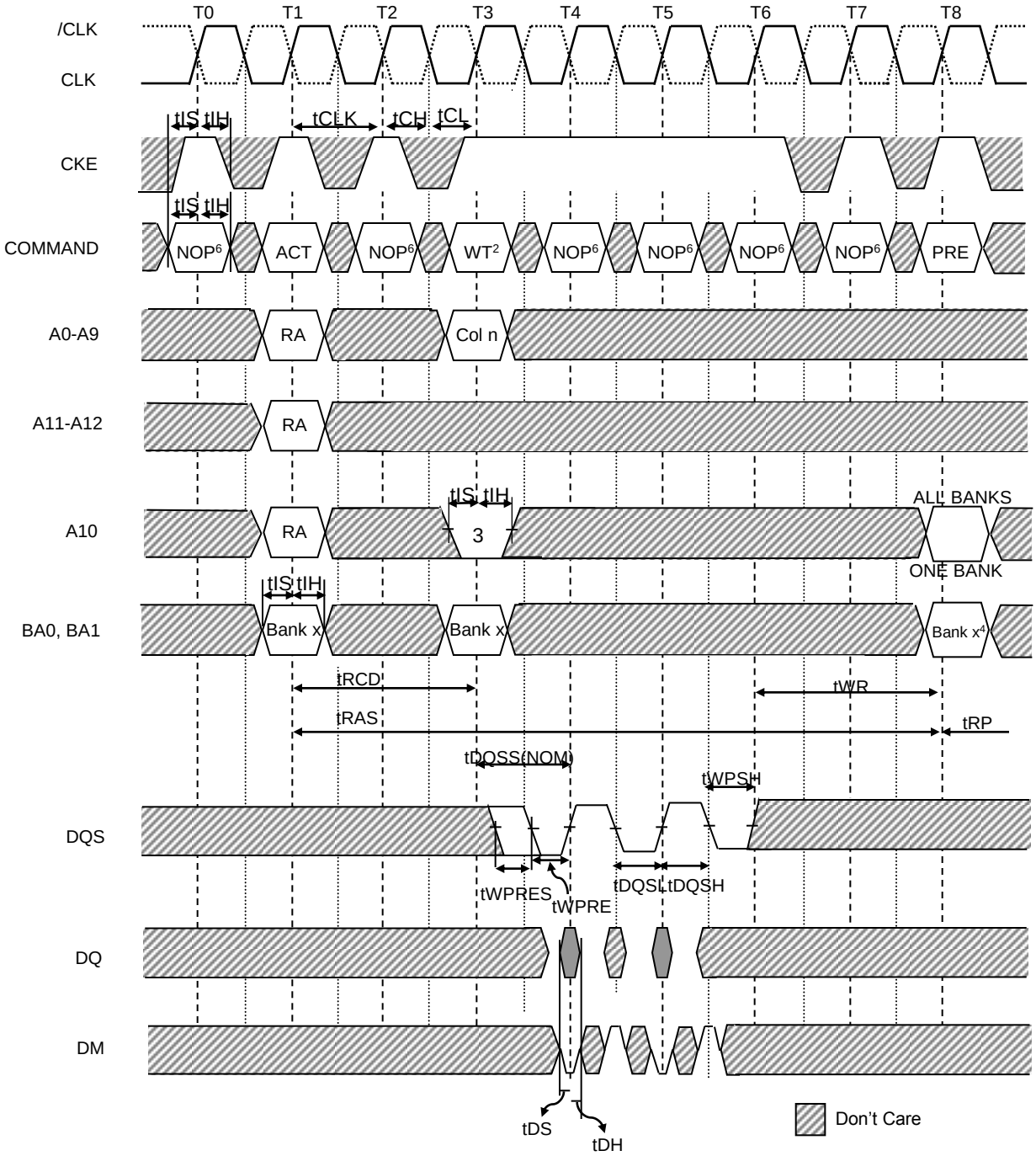
Figure 36: Bank Write – With Auto Precharge



Notes :

1. Din n = data-in for column n.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. tDSH is applicable during tDQSS (MIN) and is referenced from tCLK T4 or T5.
7. tDSH is applicable during tDQSS (MAX) and is referenced from tCLK T5 or T6.

Figure 37: Write – DM Operation



Notes :

1. Din n = data-in for column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T8.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. tDSH is applicable during tDQSS (MIN) and is referenced from tCLK T4 or T5.
8. tDSH is applicable during tDQSS (MAX) and is referenced from tCLK T5 or T6.

DEEP POWER DOWN MODE ENTRY

The Deep Power Down Mode is entered by having burst termination command, while CKE is low. The Deep Power Down Mode has to be maintained for a minimum of 100us. The following diagram illustrates Deep Power Down mode entry.

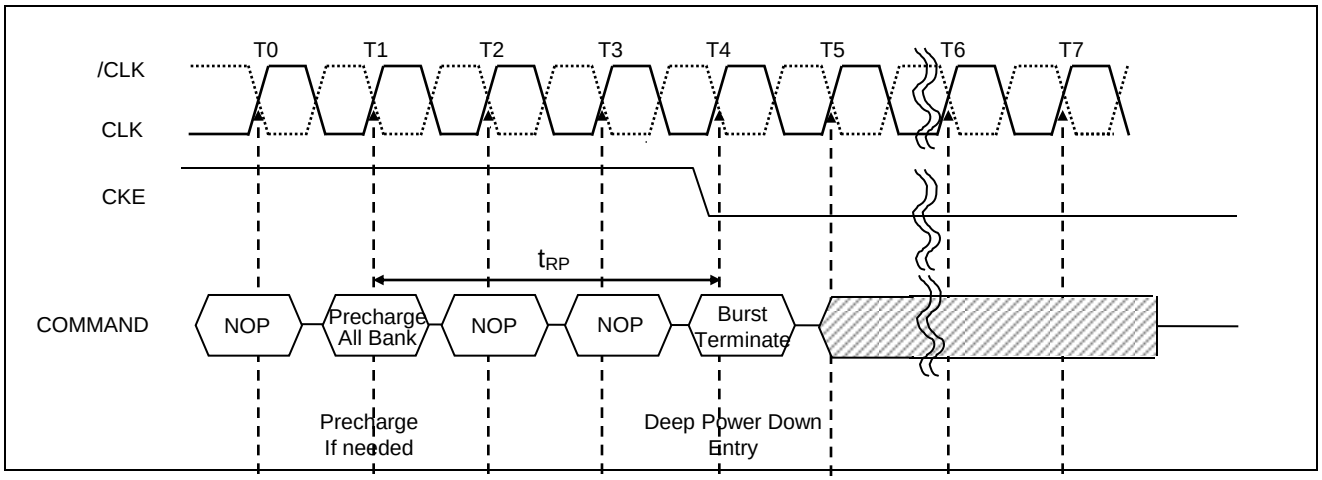


Figure 38. Deep Power Down Mode Entry

DEEP POWER DOWN MODE EXIT SEQUENCE

The Deep Power Down Mode is exited by asserting CKE high.
After the exit, the following sequence is needed to enter a new command

1. Maintain NOP input conditions for a minimum of 200us
2. Issue precharge commands for all banks of the device
3. Issue 2 or more auto refresh commands
4. Issue a mode register set command to initialize the mode register
5. Issue a extended mode register set command to initialize the extended mode register

The following timing diagram illustrates deep power down exit sequence

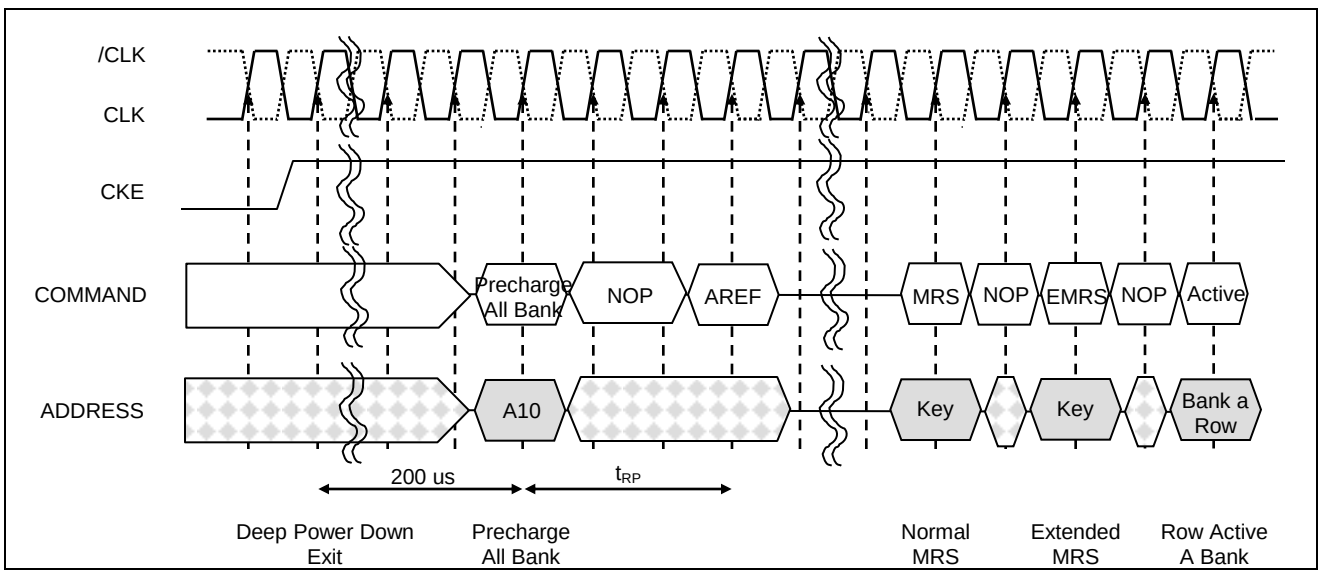


Figure 39. Deep Power Down Mode Exit