i.MX28 EVK Board, Rev. D

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Multimedia Application Division,
Wireless & Mobile System Group

ICAP Classification: FCP: FIUO: X PUBI:

Designer:	Drawing Title: i.MX28 EVK	
Drawn by: DRAWN_BY	Page Title: Cover	
Approved:	Size: Custom	Document Number: SCH-26241 PDF: SPF-26241 — Rev: D
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Revision History

REVA: 11/04/2009

Original Release

REVB: 04/15/2010

1.Changed all the boot mode resistors (R244, R246, R248, R250, R345, R346, R347, R352, R336, R337, R335, R338) to 10 Kohms.
2.C180 (reset pin external capacitor) changed to 0.01uF. This is to ensure the reset persistent bit is reset properly to 0 after startup after a power cycle.
3.Change the USB5V and WALL 5V selection method to use S16 to switch the sources onto the VDD5V pin.
4.Changed the LCD Backlight supply to be powered from VDD4P2 by default. Added a FET (switched by VDD_5V) from LI-ION_BATTERY to VDD4P2 to improve efficiency. Also added an option to power the LCD backlight from WALL_5V_IN for very large displays (with very high backlight current requirements).
5.Changed the 5V reset circuit to disconnect the 5V supply from the VDD5V pin when the RESET pin is pressed.
6.Changed the COM pin of the LTC2495 to 1/2 of the VCC_ID supply by adding a 47K resistor divider circuit between VDD_ID and COM and GND and COM. This is to fix the ADC readings and to increase the ADC range to the full supply voltage.
7.On U63, connected pins 7 and 8 (VREF2 and EN) together and then connected these two pins to the VDDIO_ID net with a 200k resistor. If pins 7 and 8 (VREF2 and EN) are connected directly to VDDIO_ID, U63 could potentially back-power the VDDIO_3V3 rail.
8.The current GND test points are small and alligator clips easily fall off. Changed TP12, TP14, TP11, and TP13 to larger GND test points and labeled as "GND" on the top silkscreen with large font. Added one GND test point in the middle of the board.
9.Added 0.02 ohm (1%) resistors in series with the main power supply signals for current measurement.
10.Added SPDIF RCA connector.
11.Added GPMI_CE2, GPMI_CE3, GPMI_READY2, and GPMI_READY3 signal connections to NAND flash connector, J93.
12.Changed USB Host and USB OTG power from WALL 5V net to 5V net. This is to meet the software debugging requirement so the system is able to provide a Host 5V supply (from USB0) when connected to a battery power supply (no WALL 5V supply).
13.Rotated the NAND flash connector 180 degrees to be compatible with the legacy NAND flash d-cards.
14.Changed to the LTC2495, 16 channel ADC, (same as on the Armadillo 2 board) so that the CPU_ID0 and CPU_ID1 ADC channels could be added. In addition, a 10K pull-down resistor was added on the CPU_ID1 (ADC channel 13), to identify the board as the MX28 DDR2 rev B EVK.
15.Added a 5 pin header (J96) to allow the customer to test various types of 4 and 5 wire resistive touch panels.
16.Added the same DC adapter overvoltage protection circuit as on the Armadillo 2 main board.
17.Add TVS diodes at the VDD5V input pin of the MX28 and at the 5V adapter input for transient overvoltage protection.
18.Connected the following pins on the NAND flash connector (J93) to GND: 1, 2, 11, 12, 21, 22, 31, 32, 41, 42, 51, 52.
19.Added a 10K pull-up resistor to USB0_ID.
20.Added GPMI_READY2, READY3, CE2, CE3 connections to the MX28 (shared with CAN0 and CAN1 pins).

REV C: 6/11/2010

1. Added common mode choke and EMI capacitive filter at the input of the 5V DC adapter for EMI suppression.
2. Swapped the pin 1 and 3 connections on J85.
3. Increased the voltage rating of C159 to avoid damaging the capacitor when a high voltage adapter is plugged in.
4. Added additional 10uF capacitor on the WALL_5V_IN net after Q15.
5. Added a ferrite bead on the HEADPHONE_DETECT line of J80 to reduce the board radiated emissions.
6. Changed the FB1-FB6 ferrite beads to higher impedance and wider bandwidth frequency performance ferrites to reduce the board radiated emissions.
7. Added a ferrite bead on the USB_0_ID signal near the USB OTG connector (J82).
8. Added ferrite beads on the RS232 port connector signals.

REV D: 8/04/2010

1. Connected pin 5 of J83 to GND.

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Drawing Title: **i.MX28 EVK**

Page Title: **Revison History**

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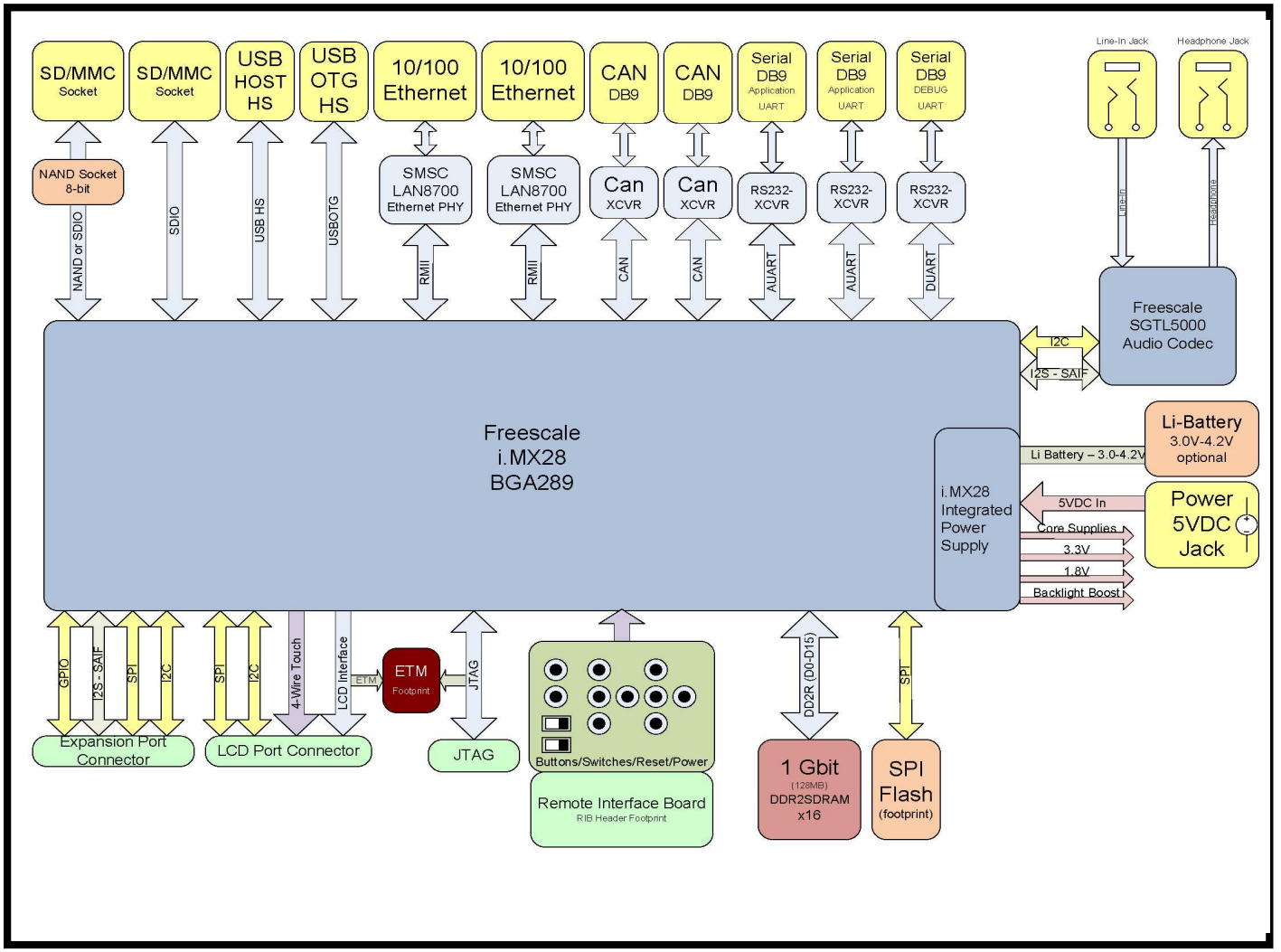

Block Diagram

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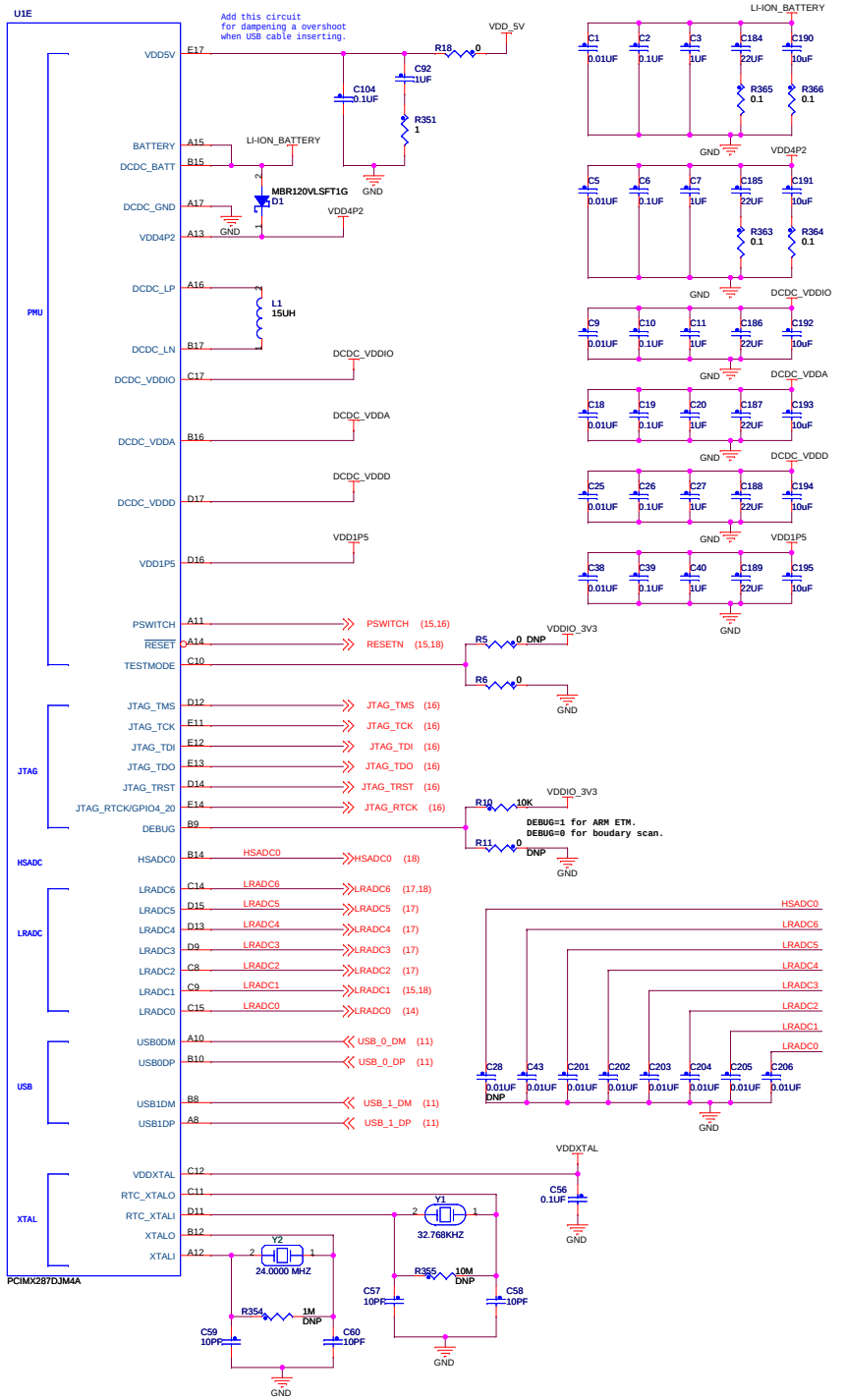
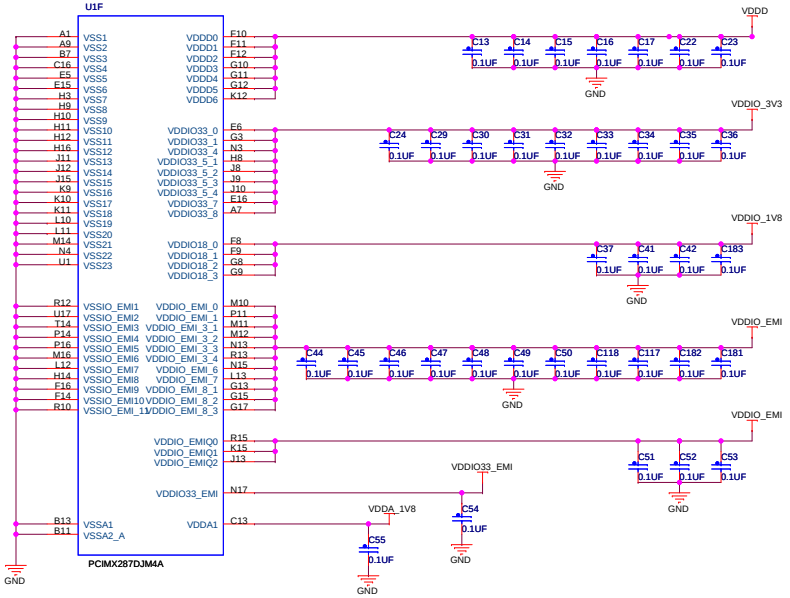


DC-DC &JTAG&ADC



CPU Power

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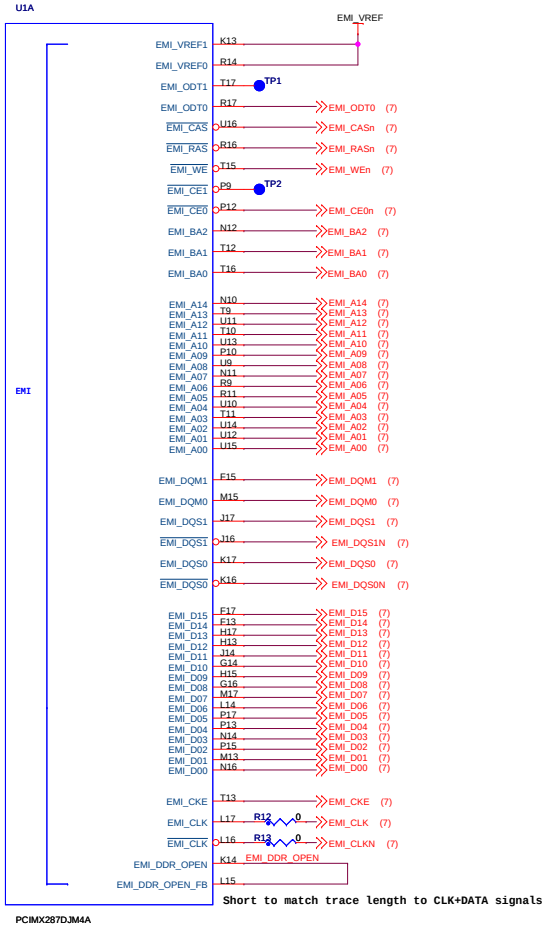
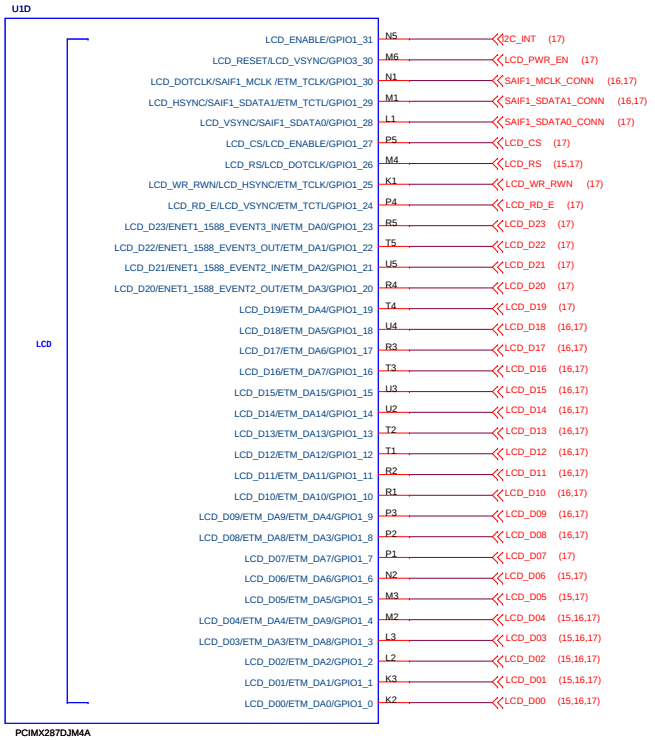


EMI DDR2



LCD&SAIF1

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Page Title: **CPU_EMI&LCD**

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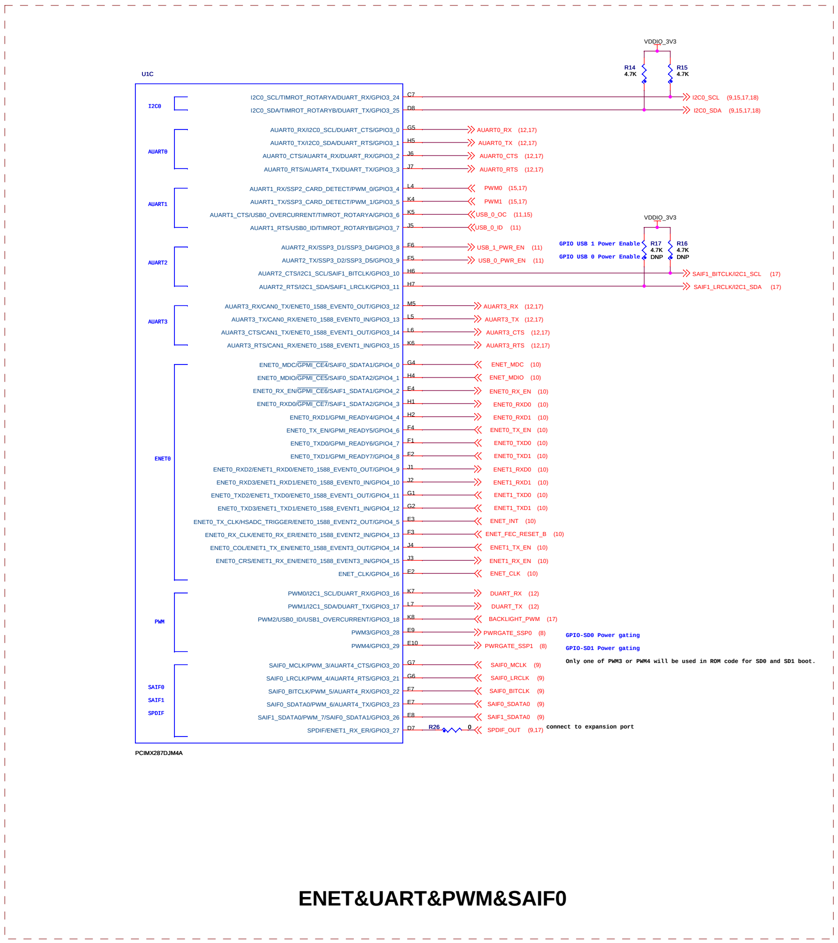

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Drawing Title: **i.MX28 EVK**

Page Title: **CPU_GPMI&ENET&UART&SSP&SAIF**

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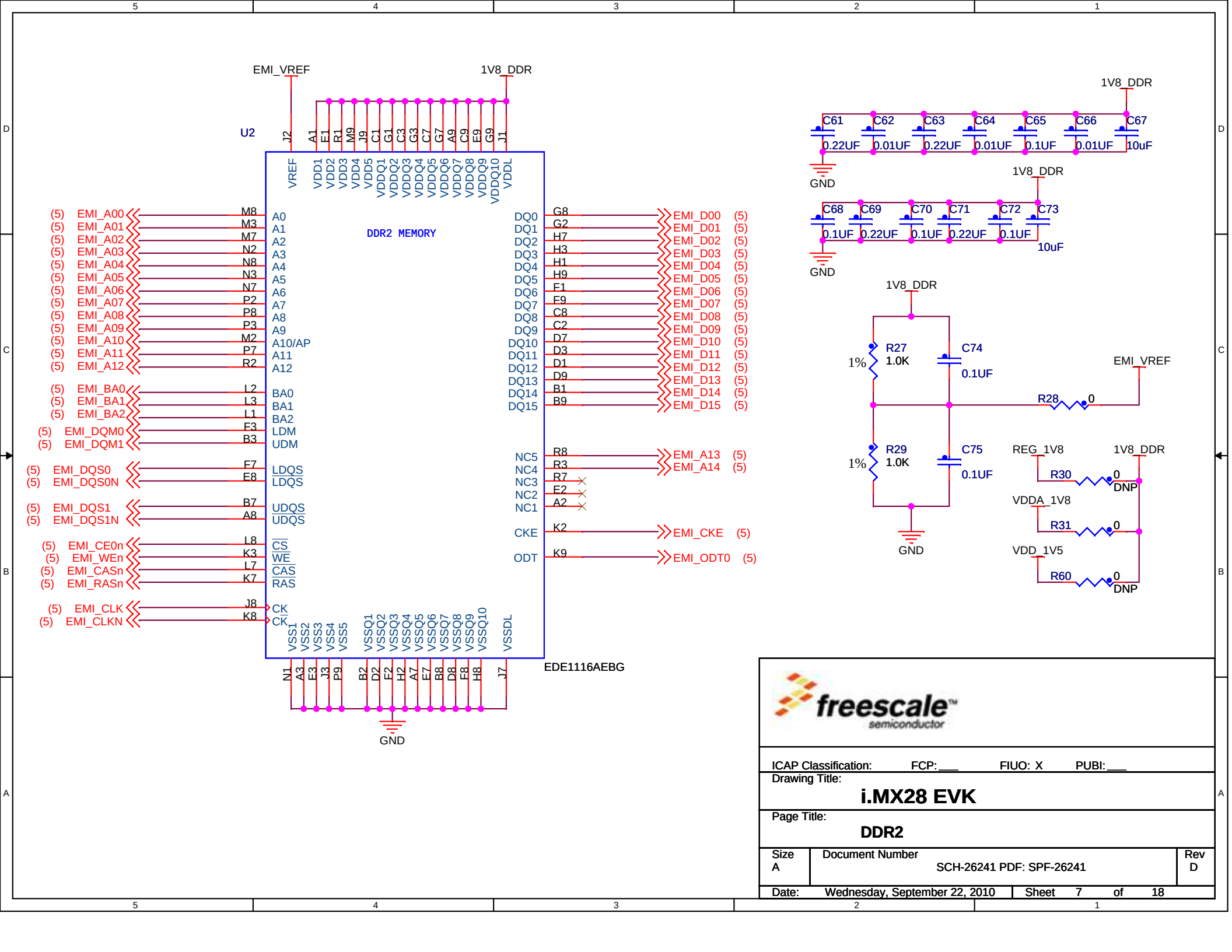

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DDR2

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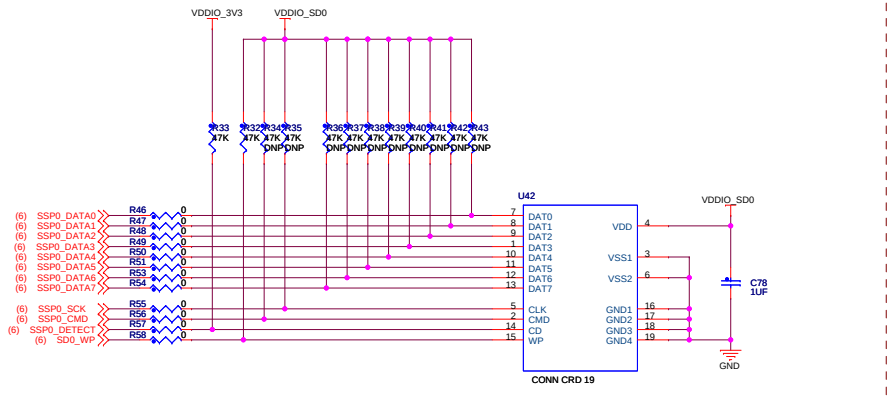
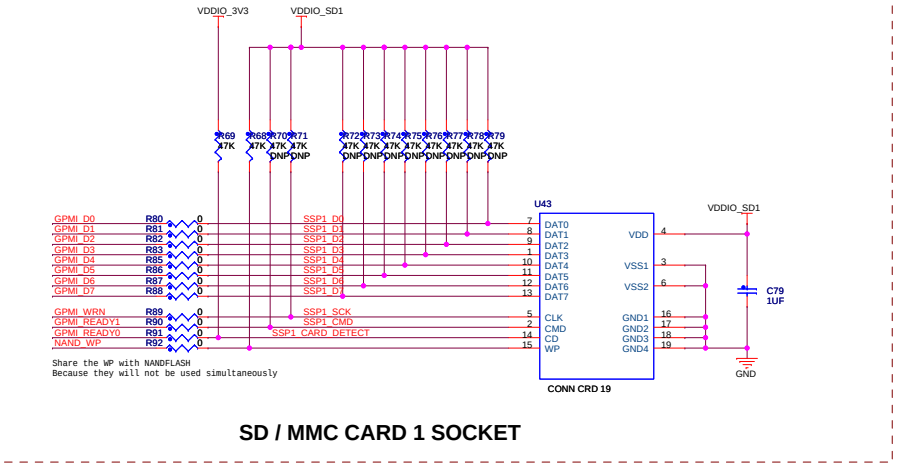


SD / MMC CARD 0 SOCKET-Default Boot Card



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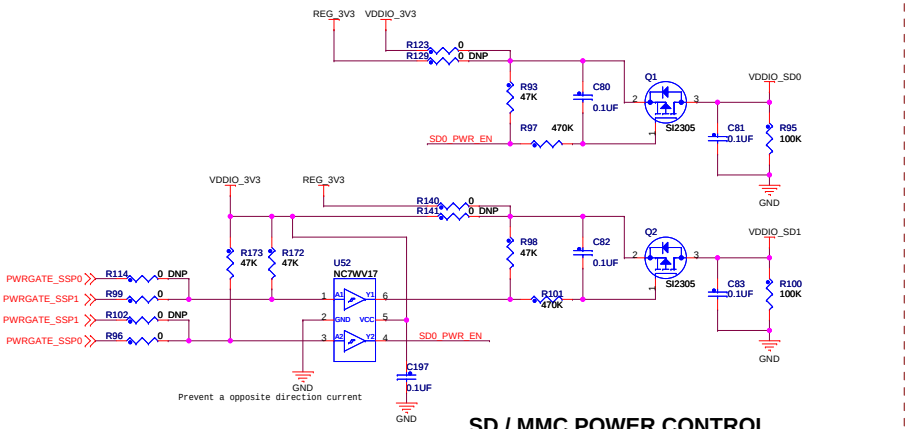
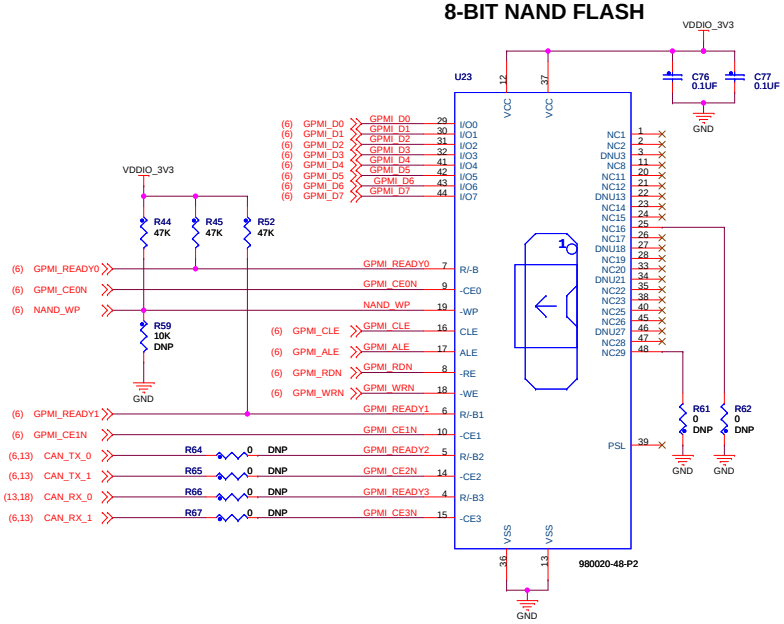
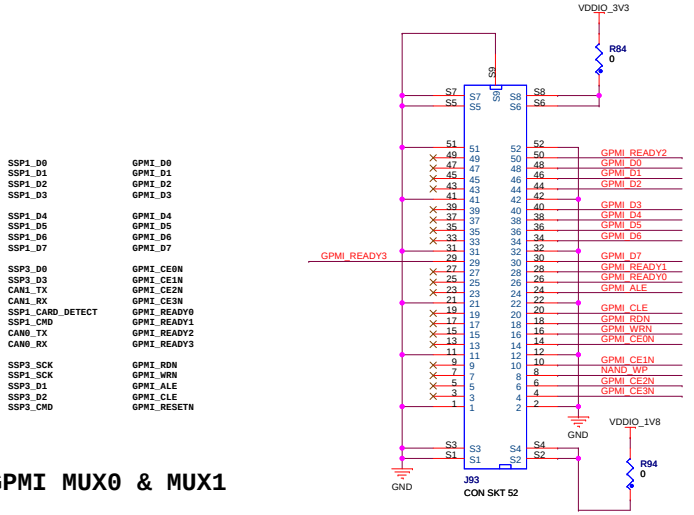


SD / MMC POWER CONTROL

8-BIT NAND FLASH



NAND FLASH SOCKET



GPMI MUX0 & MUX1

NAND FLASH CONNECTOR

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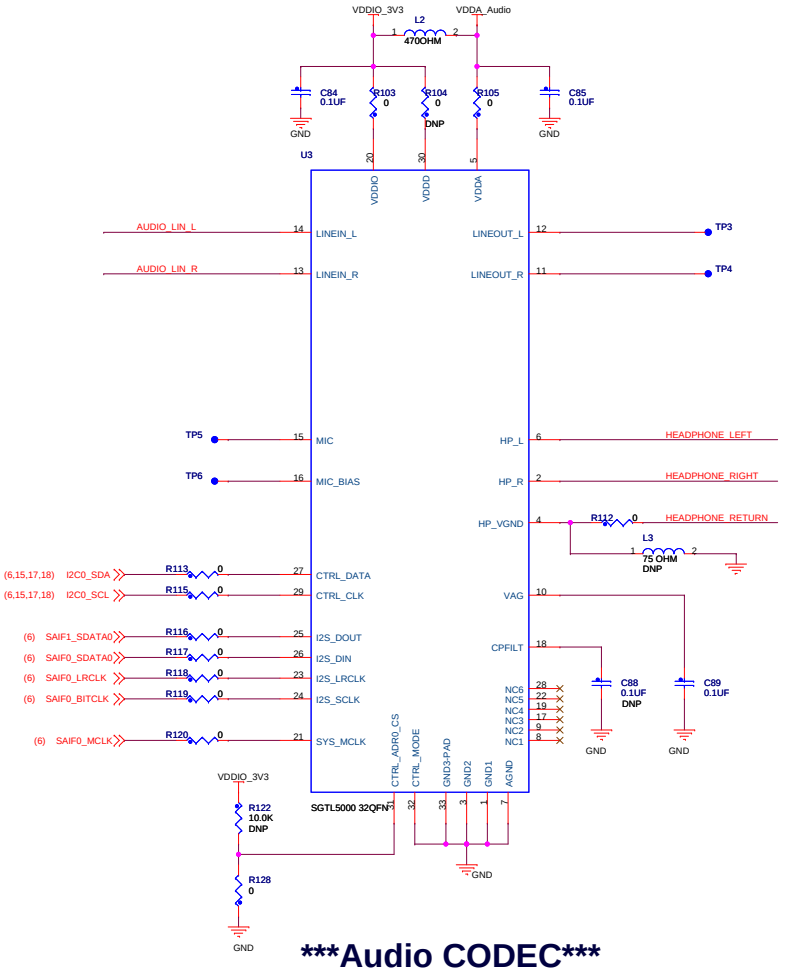
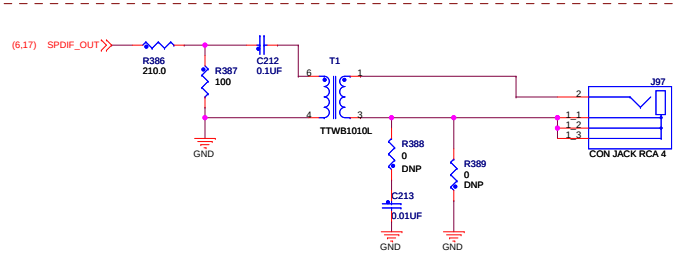
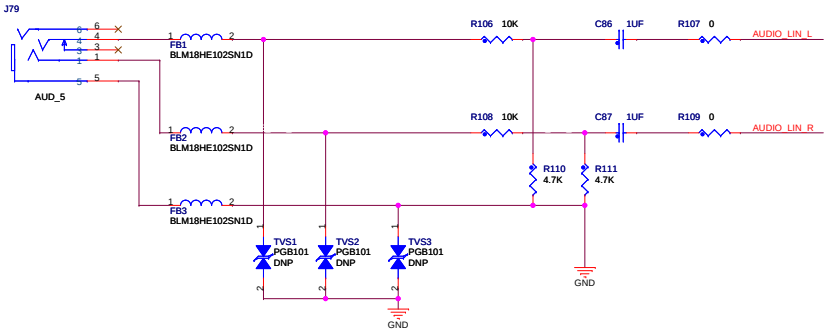


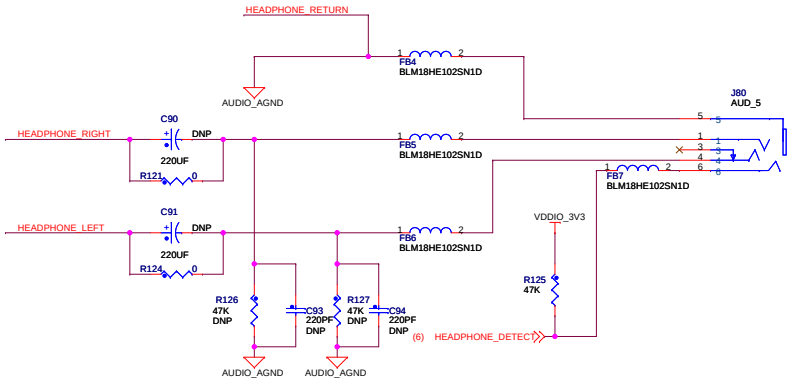
Audio CODEC



SPDIF output filter

Line-In Circuit





HeadPhone

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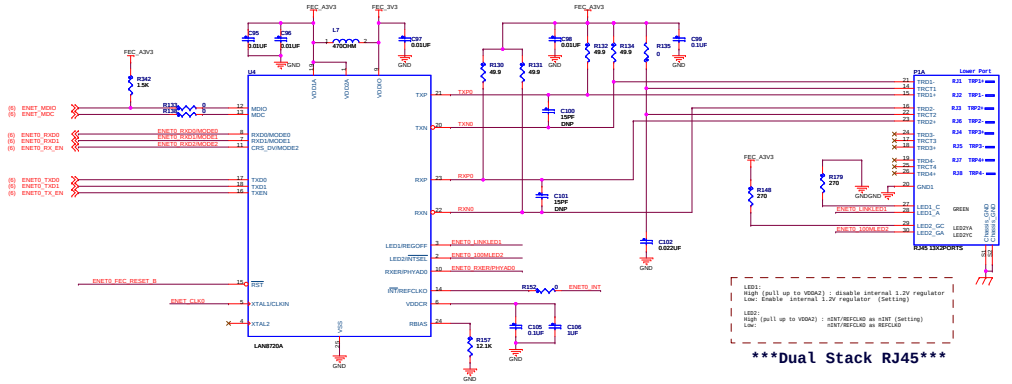

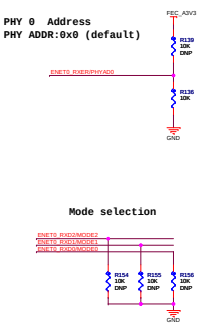

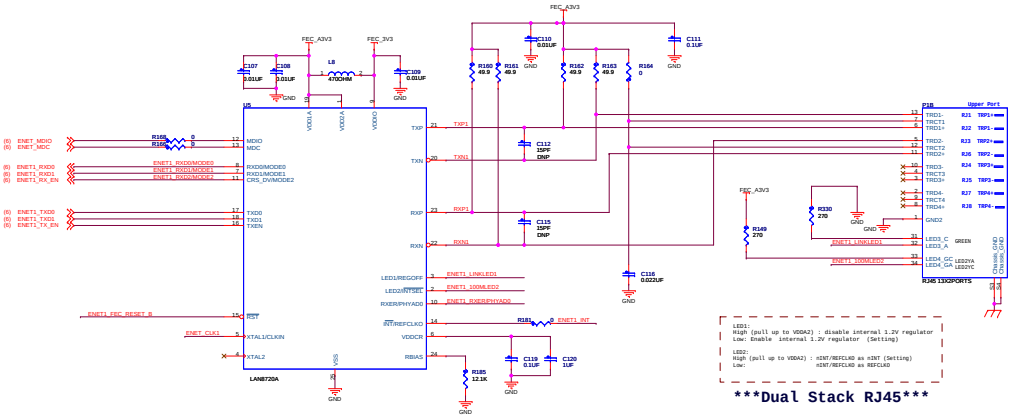

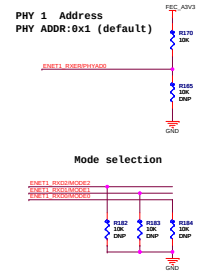

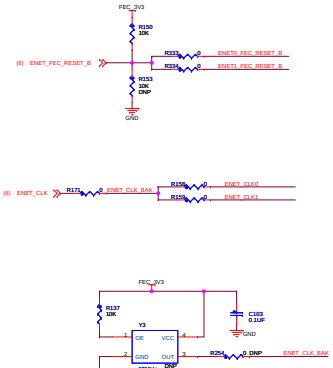

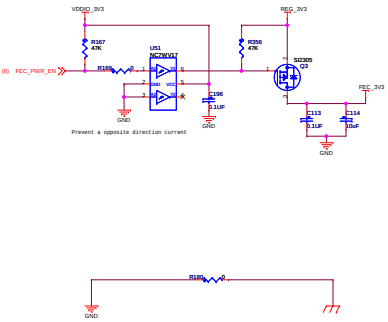

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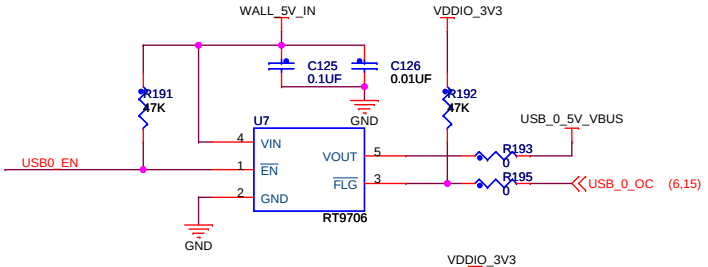
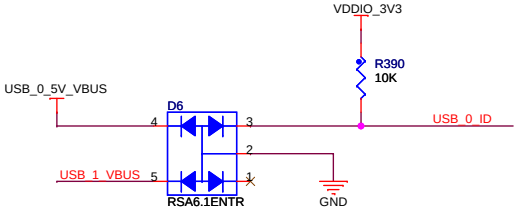
Power Switch





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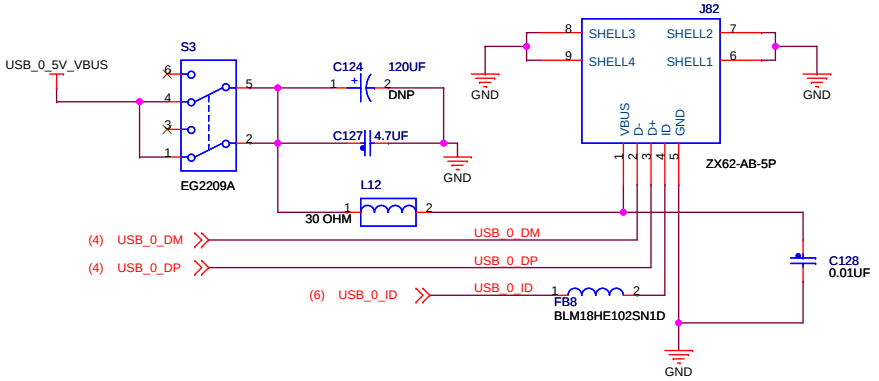
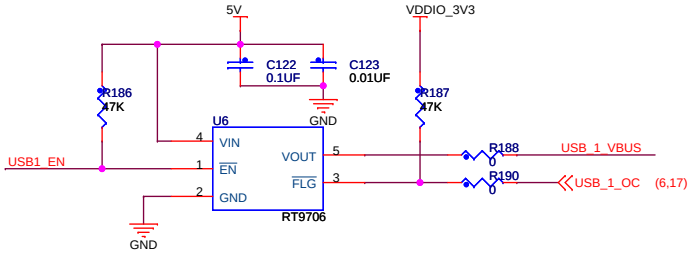
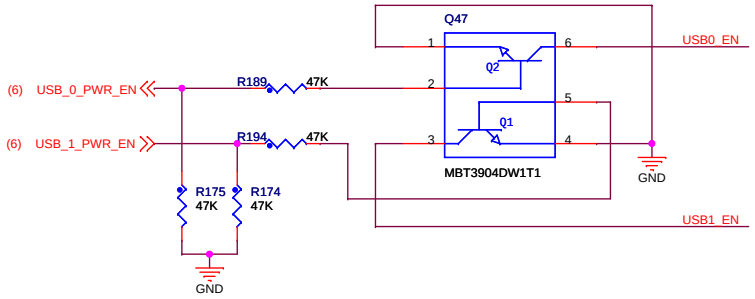
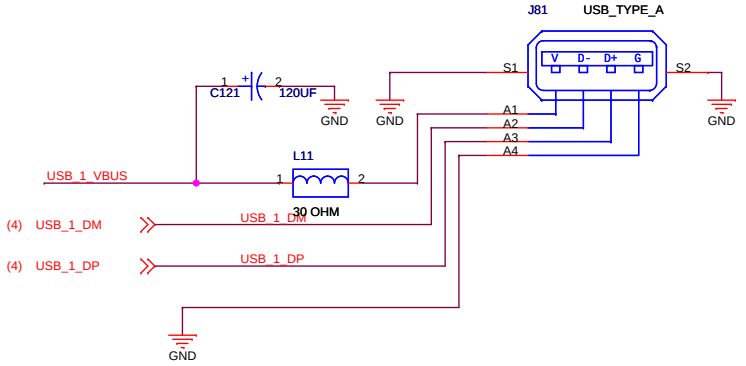


USB 0 HOST/DEVICE

Power Switch







USB 1 HOST

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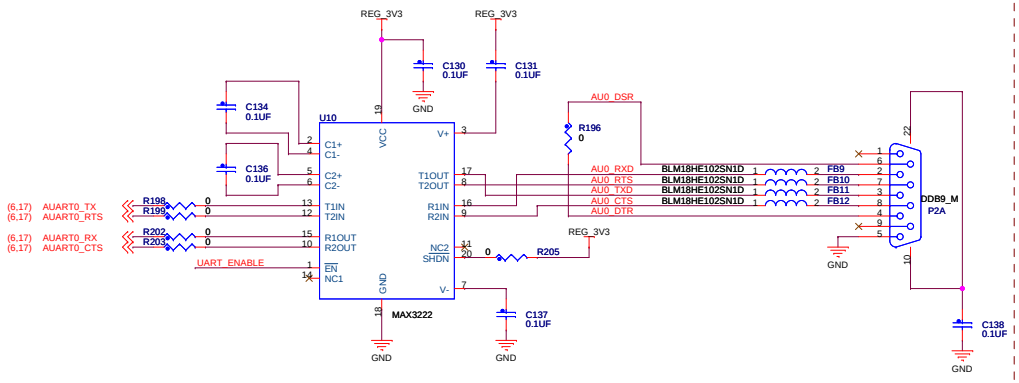

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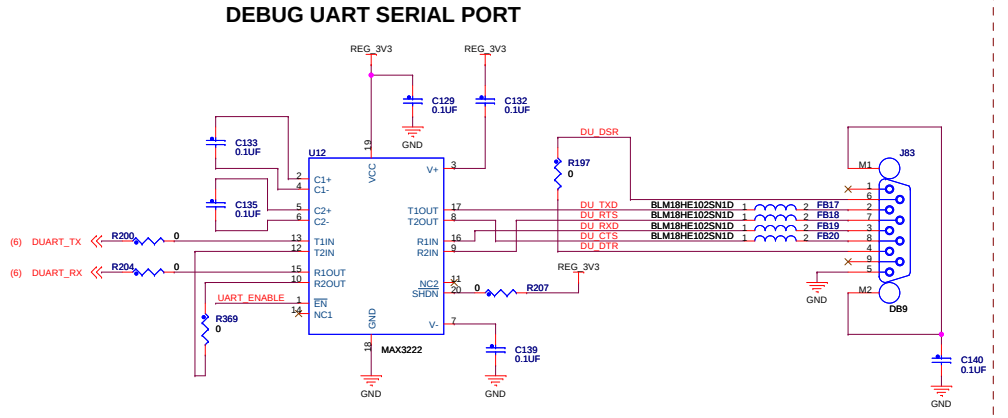
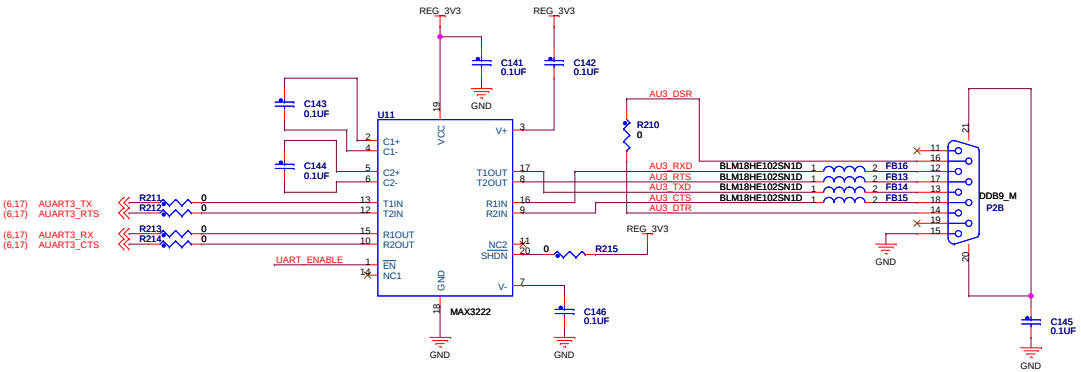


DEBUG UART SERIAL PORT (FEMALE)



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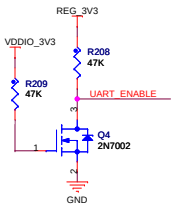

UART
(DCE-Female package)

DCE		
1	CD	O
2	TX	O
3	RX	I
4	DTR	I
5	GND	
6	DSR	O
7	RTS	I
8	CTS	O
9	RI	O

UART
(DTE-Male-package)

DTE		
1	CD	I
2	RX	I
3	TX	O
4	DTR	O
5	GND	
6	DSR	I
7	RTS	O
8	CTS	I
9	RI	I

Uart Enable

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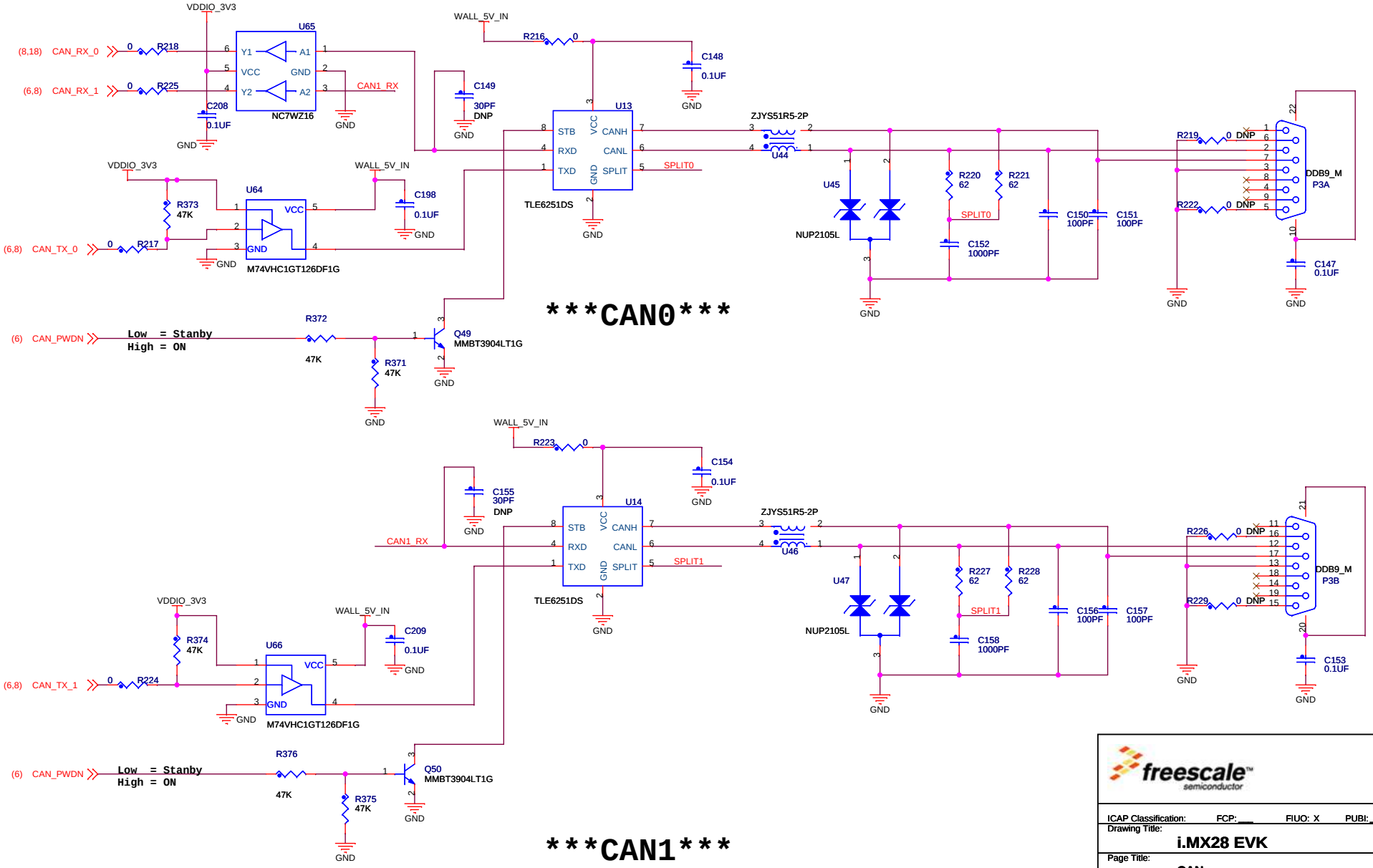
VDDIO_3V3
U65
(8,18) CAN_RX_0
R218
(6,8) CAN_RX_1
R225
C208
0.1UF
NC7WZ16
CAN1_RX
C149
30PF
DNP
WALL_5V_IN
R216
C148
0.1UF
U13
STB
RXD
TXD
VCC
GND
CANH
CANL
SPLIT
TLE6251DS
SPLIT0
ZJYS51R5-2P
U44
U45
NUP2105L
R220
62
R221
62
SPLIT0
C152
1000PF
C150
100PF
C151
100PF
R219
R222
0 DNP
DDB9_M
P3A
C147
0.1UF
U64
R373
47K
R217
(6,8) CAN_TX_0
M74VHC1GT126DF1G
C198
0.1UF
CAN0
(6) CAN_PWDN
Low = Stanby
High = ON
R372
47K
R371
47K
Q49
MMBT3904LT1G
R223
C154
0.1UF
C155
30PF
DNP
U14
U46
U47
R227
62
R228
62
SPLIT1
C158
1000PF
C156
100PF
C157
100PF
R226
R229
DDB9_M
P3B
C153
0.1UF
U66
R374
47K
R224
C209
0.1UF
R376
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CAN1
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semiconductor
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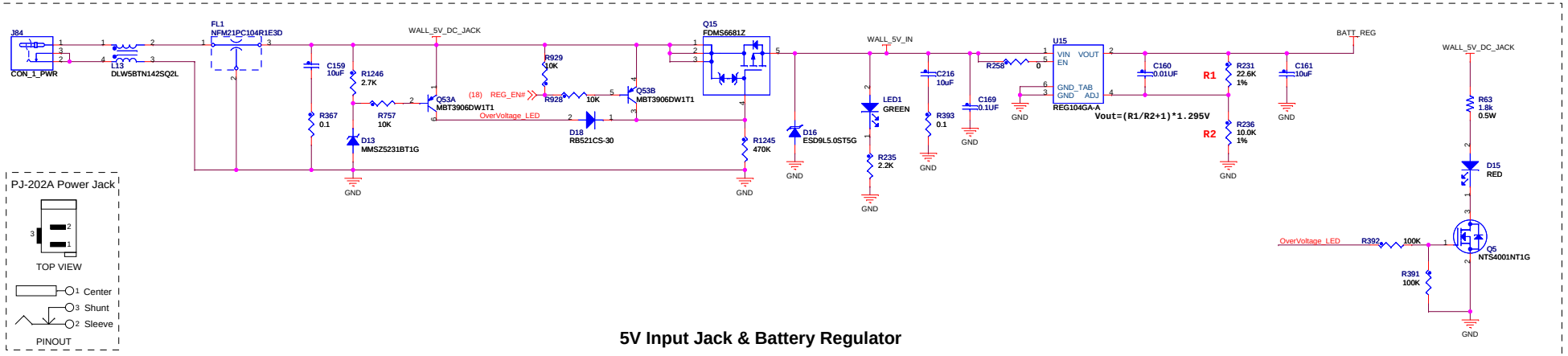

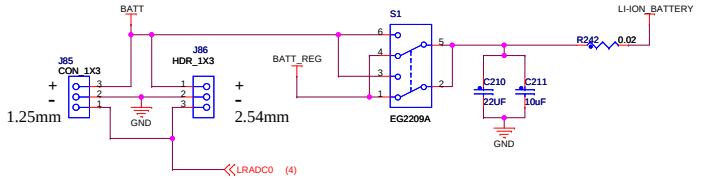

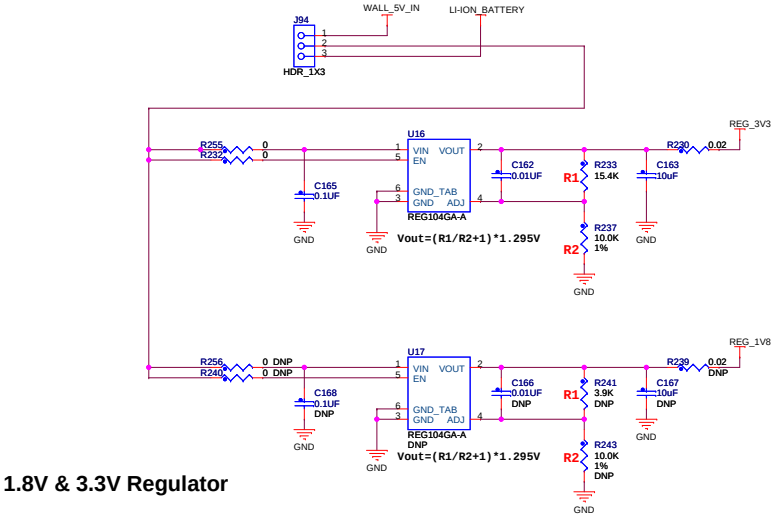

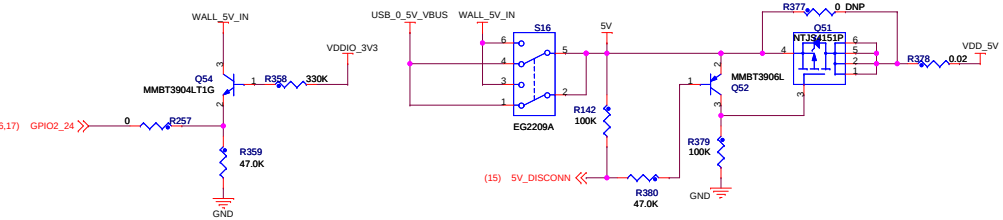

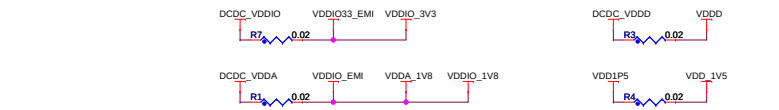

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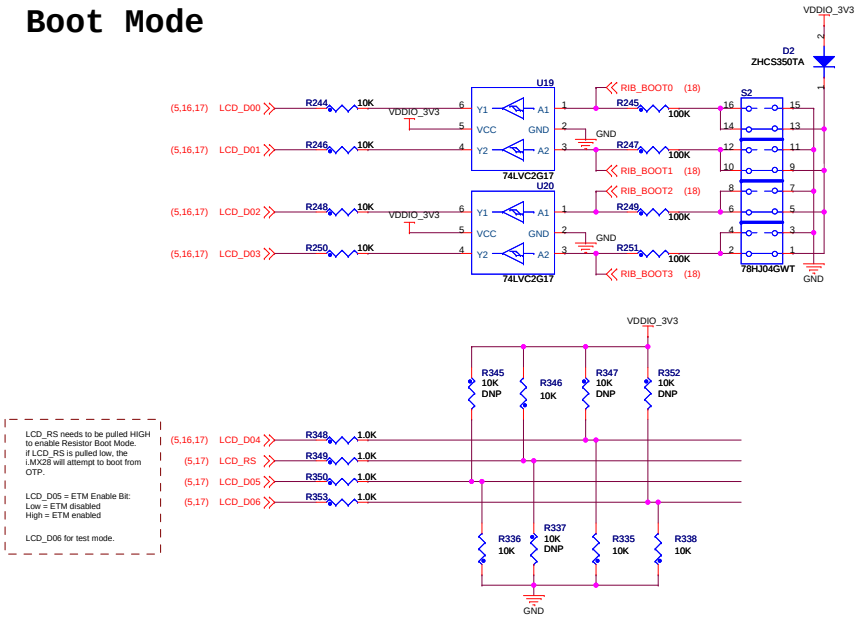
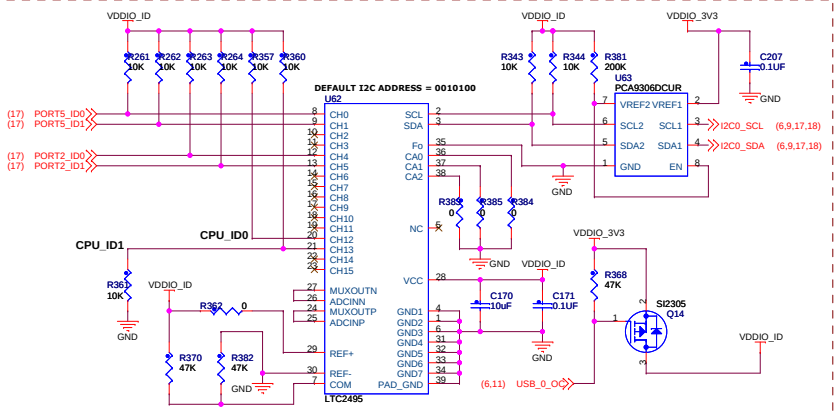
Table 40-3. Boot Mode Selection Map

ETM Enable/ LCD_ DATA[5]	VOLTAGE SELECTOR/ LCD_ DATA[4]	BM3/ LCD_ DATA[3]	BM2/ LCD_ DATA[2]	BM1/ LCD_ DATA[1]	BM0/ LCD_ DATA[0]	PORT	BOOT MODE
X	X	0	0	0	0	USB0	USB (unencrypted vs. encrypted is under OTP control)
X	0	0	0	0	1	I2C0	I2C0 master, 3.3 V
X	1	0	0	0	1	I2C0	I2C0 master, 1.8 V
X	0	0	0	1	0	SPI2	SPI master SSP2 boot from flash, 3.3 V
X	1	0	0	1	0	SPI2	SPI master SSP2 boot from flash, 1.8 V
X	0	0	0	1	1	SPI3	SPI master SSP3 boot from flash, 3.3 V
X	1	0	0	1	1	SPI3	SPI master SSP3 boot from flash, 1.8 V
X	0	0	1	0	0	GPMI	NAND, 3.3 V
X	1	0	1	0	0	GPMI	NAND, 1.8 V
X	0	0	1	0	1		Reserved
X	0	0	1	1	0		Reserved
X	0	0	1	1	1		Reserved
X	0	1	0	0	0	SPI3	SPI master SSP2 boot from EEPROM, 3.3 V
X	1	1	0	0	0	SPI3	SPI master SSP2 boot from EEPROM, 1.8 V
X	0	1	0	0	1	SSP0	SD/MMC master on SSP0, 3.3 V
X	1	1	0	0	1	SSP0	SD/MMC master on SSP0 1.8 V
X	0	1	0	1	0	SSP1	SD/MMC master on SSP1, 3.3 V
X	1	1	0	1	0	SSP1	SD/MMC master on SSP1, 1.8 V
X	0	1	0	1	1		Reserved
X	0	1	1	0	0		Reserved
X	0	1	1	0	1		Reserved
X	0	1	1	1	0		Reserved
X	0	1	1	1	1		Manufacturing Test Mode

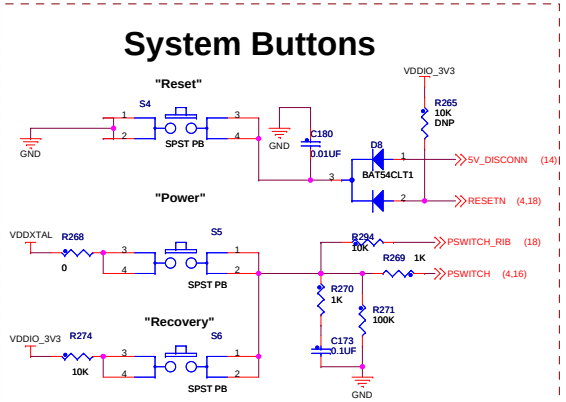
Boot Mode



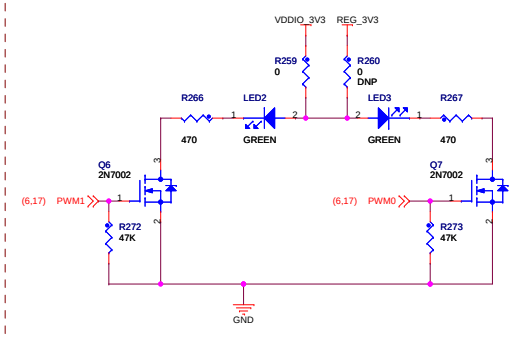
HARDWARE IDENTIFICATION (4-Channels)

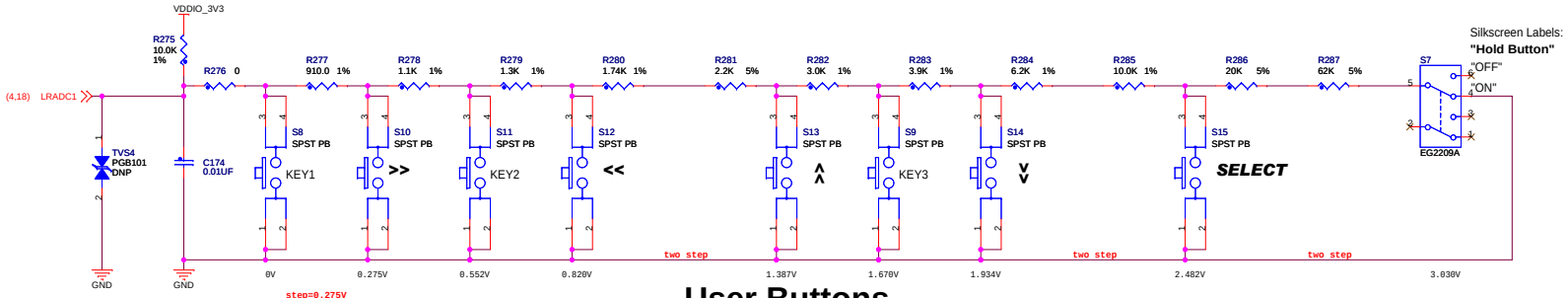


System Buttons

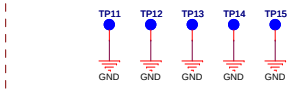


Indication LEDs





User Buttons



Test Point (4 corner and 1 middle)

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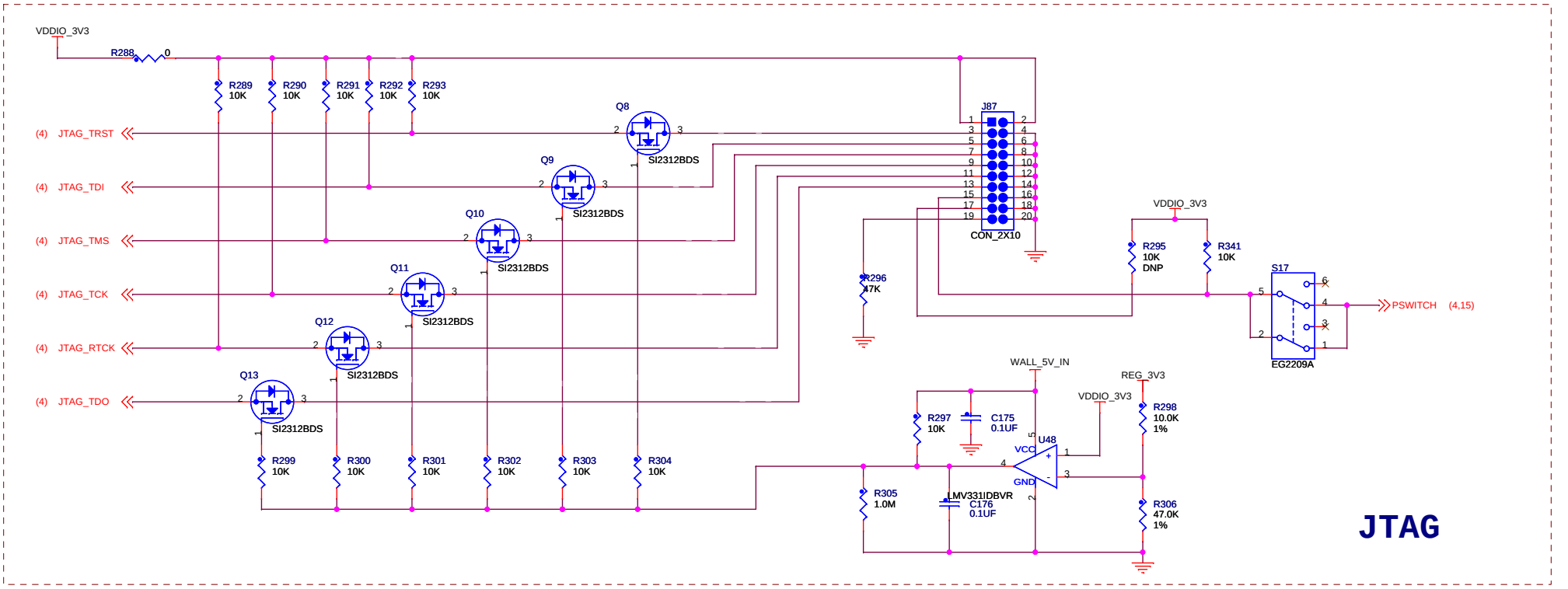

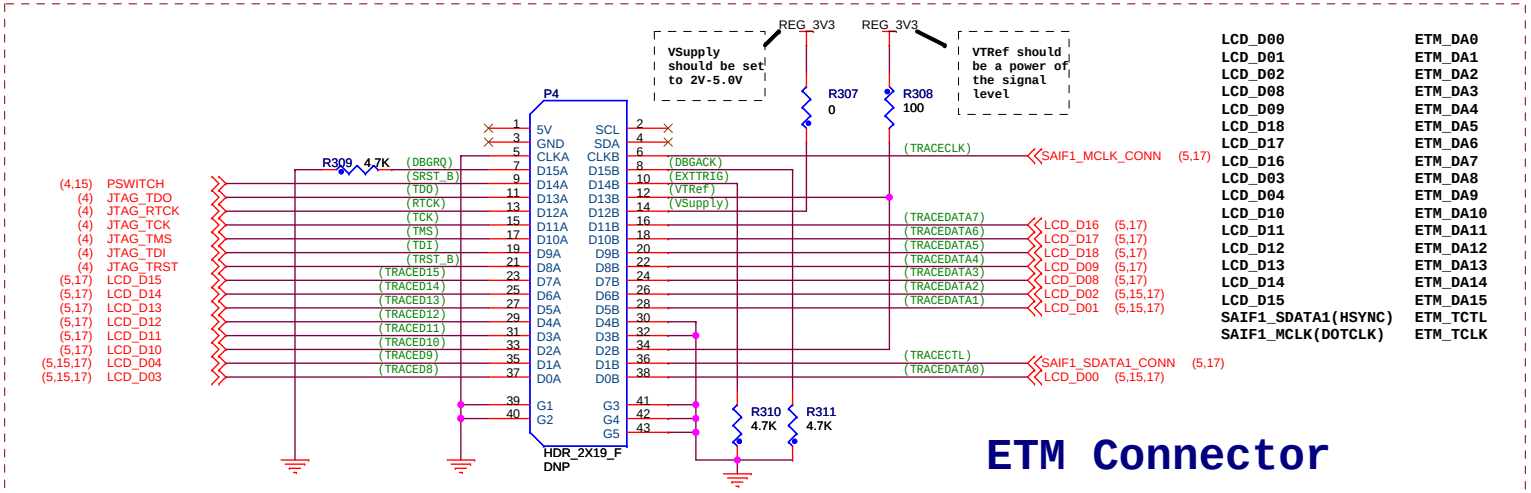

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Page Title: **JTAG&ETM**

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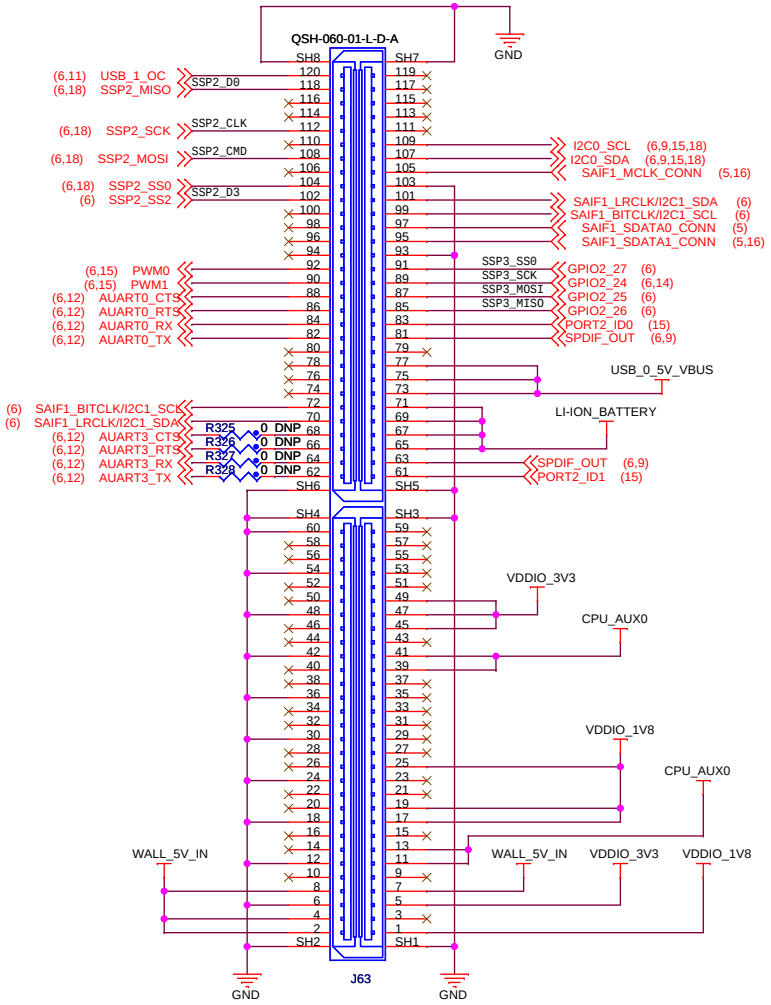
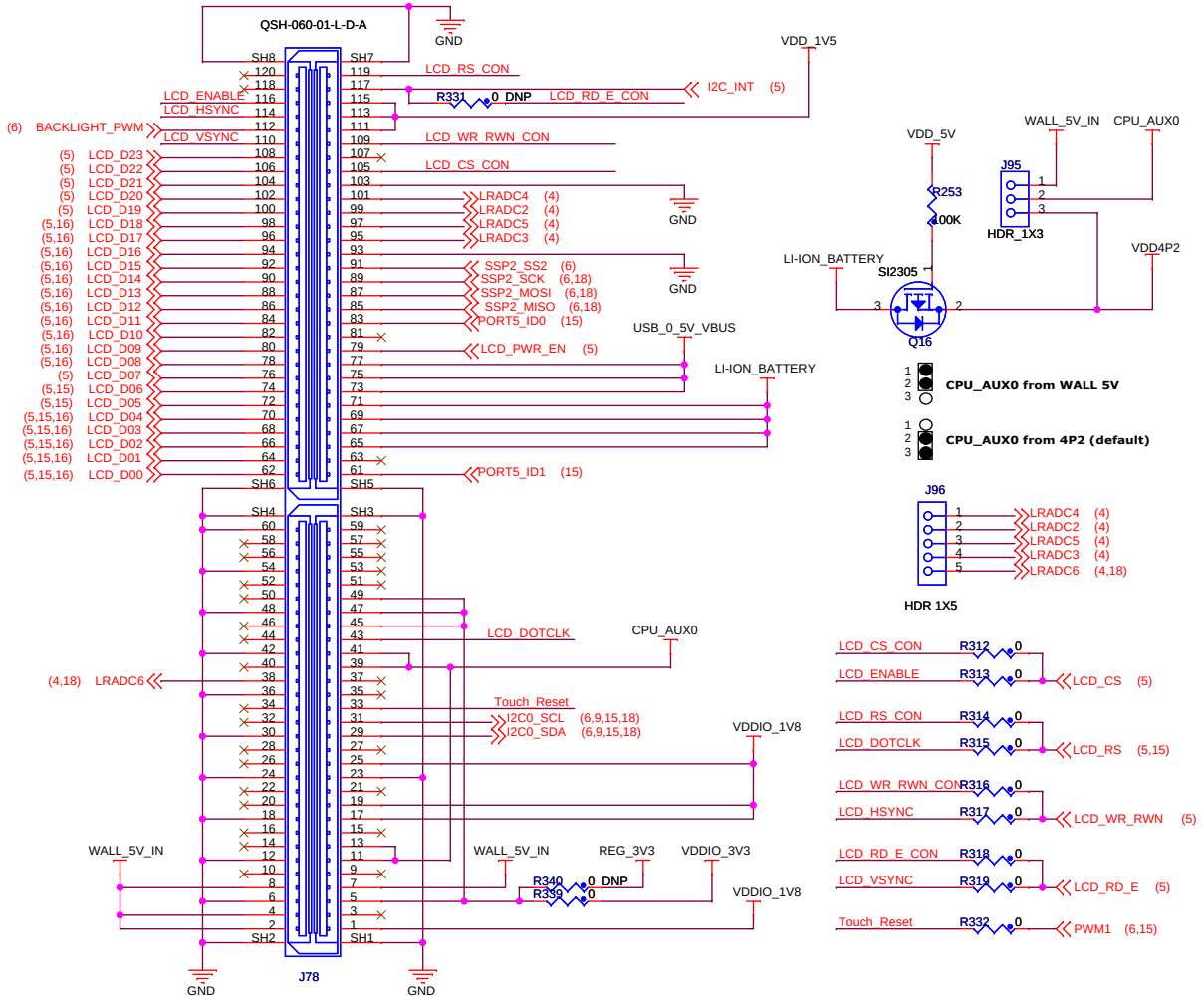


EXPANSION PORT



LCD PORT

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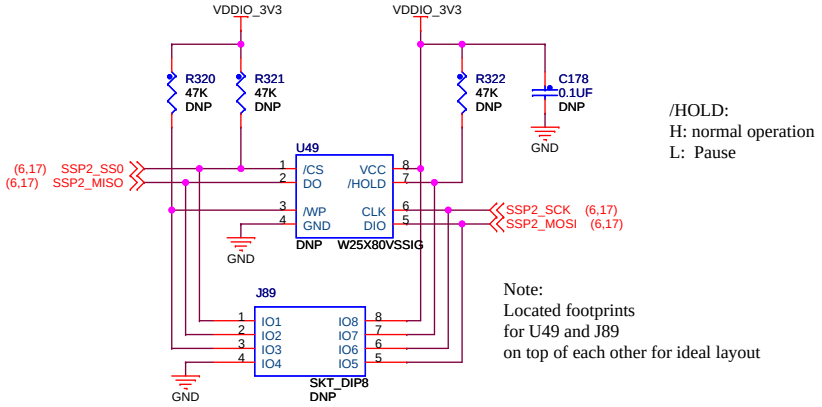
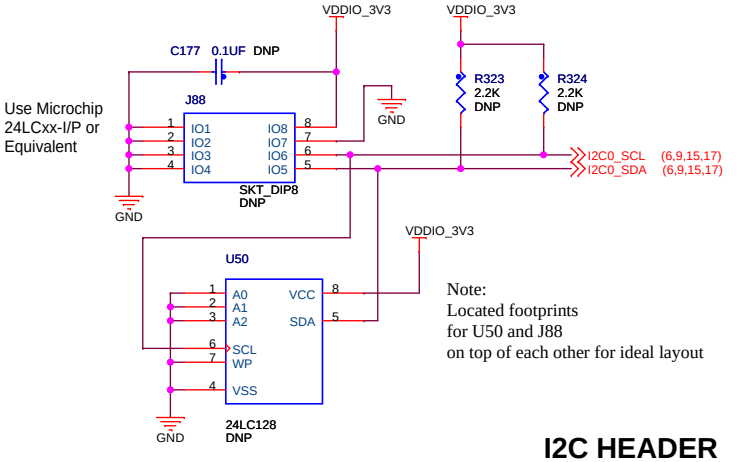


/HOLD:
H: normal operation
L: Pause

Note:
Located footprints
for U49 and J89
on top of each other for ideal layout

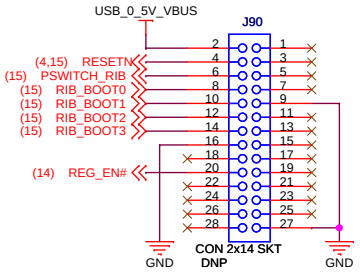
SPI Flash& Header

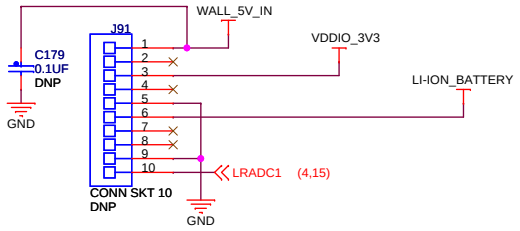


Use Microchip
24LCxx-I/P or
Equivalent

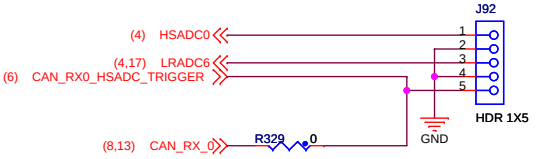
Note:
Located footprints
for U50 and J88
on top of each other for ideal layout

I2C HEADER





RIB REV. D BOARD HEADER



ADC HEADER

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