

IMX6 has on-chip pulldown. This may not be needed.

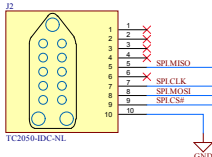
Design Checklist

2.6 JTAG signal termination

The following table is a JTAG termination chart (see recommendations in Table 2-5).

Table 2-19. JTAG interface summary

JTAG signal	I/O type	On-chip termination	External termination
JTAG_TCK	Input	47 k Ω pullup	Not required (can use 10 k Ω pullup)
JTAG_TMS	Input	47 k Ω pullup	Not required (can use 10 k Ω pullup)
JTAG_TDI	Input	47 k Ω pullup	Not required (can use 10 k Ω pullup)
JTAG_TDO	3-state output	Keeper	Do not use pull-up or pull-down
JTAG_TRST#	Input	47 k Ω pullup	Not required (can use 10 k Ω pullup)
JTAG_MCD	Input	100 k Ω pullup	Use 1 k Ω pulldown or tie to GND



Mark Programmer Pin
 Pin1 - SCL (I2C)
 Pin2 - GND
 Pin3 - SDA (I2C)
 Pin4 - NC (VDD)
 Pin5 - MOSI (SPI)
 Pin6 - MISO (SPI)
 Pin7 - SCL (I2C)
 Pin8 - SDA (I2C)
 Pin9 - SS (SPI)
 Pin10 - GND

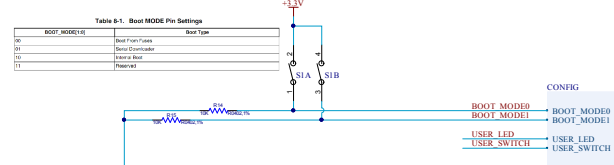
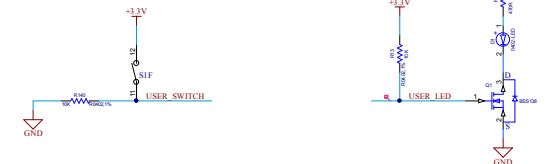
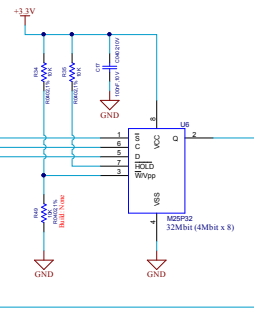
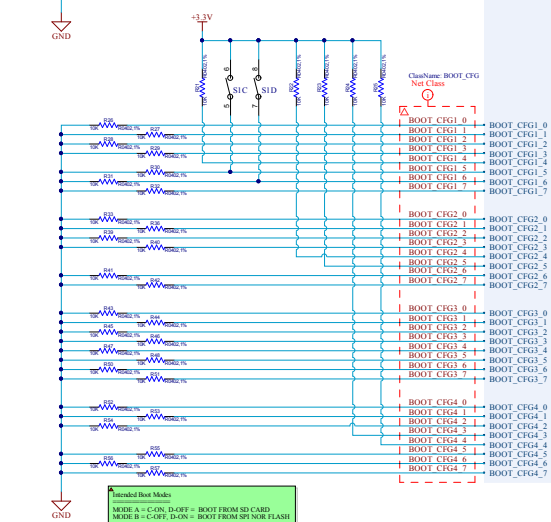


Table 8-1. Boot Mode Pin Settings

BOOT_MODE0	BOOT_MODE1	Boot Type
0	0	Boot From NAND
0	1	Boot From SPI
1	0	Internal Boot
1	1	Reserved



Reserved Boot Modes
 MODE A = C-ON, D-OFF = BOOT FROM SD CARD
 MODE B = C-OFF, D-ON = BOOT FROM SPI NOR FLASH

Boot mode	BT_CFG1	BT_CFG2	BT_CFG3	BT_CFG4
S1A S1B				
	7	6	5	4
NAND ON G0	x	x	0	0
NAND ON G1	0	0	0	0
NOR	0	0	0	0
SD_CPY	0	0	0	0
IMC_CPY	0	0	0	0
NFA_HDD	0	0	0	0
SPL_NGR	x	x	x	x