About i.MX 6Solo/DualLite Linux BSP

This document is intended to highlight the information using i.MX 6Solo/DualLite BSP. It consists of two parts:

- 3.0.15 kernel upgrade
- Add i.MX 6Solo/DualLite BSP support

Note: The information listed in this document is based on i.MX 6Solo/DualLite SS1 release.

3.0.15 kernel update

i.MX 6Solo/DualLite BSP is based on 3.0.15 kernel. The stable release of 3.0.15 kernel can be accessed from
http://git.kernel.org/?p=linux/kernel/git/stable/linux-stable.git;a=tag;h=6883cb303d2af0f3621f5687d1287dc2b0695524
Please refer to the following key changes to port from 2.6.38 kernel to 3.0.15 kernel:

CR Number	Description
ENGR00172374	This CR includes the key changes to upgrade to 3.0.15: - i.mx: CPUFREQ: not use cpufreq_debug_printk - pfuze: use pdata_size from mfd_cell struct - flexcan: use irq_set_irq_wake - remove platform _adjust_dma_zone function - GPIO: use chained_irq_enter/exit pair - fix the mlb modules build errors - Sound: Asoc: fix the snd_soc_resume resume crash
ENGR00172475	USB: Add wakeup entry for USB device
ENGR00173288	uSDHC: Add SD3.0 support
ENGR00173926	uSDHC: Support eMMC ddr mode
ENGR00174031	WiFi: Support AR6003 SDIO wifi on V3.0.x kernel

Add i.MX 6Solo/DualLite BSP support

Reference

Before reading BSP code, You should read the Application Note AN4397 to understand the differences of i.MX 6 serial family chips.

Changes

i.MX 6Solo/DualLite BSP is based on i.MX 6Dual/Quad BSP. To add i.MX 6Solo/DualLite BSP support, please refer to the following changes:

U-Boot:

CR Number	Description
ENGR00173966	This CR is to add the basic support of i.MX 6Solo/DualLite ARM2 CPU board which includes the support for DDR, IOMUX, FEC, and SDHC. Because i.MX6 Solo/DualLite shares the same board with i.MX6 Dual/Quad, the unique board file is used to support two chips. The different configurations **"CONFIG_MX6DL"** and "CONFIG_MX6Q" are used to distinguish i.MX 6Solo/DualLite and i.MX 6Dual/Quad. The system_rev for i.MX 6Solo/DualLite is **0x61000**, i.MX 6Dual/Quad is 0x63000.
ENGR00174155	The purpose of this CR is to make the default configuration of SS1 release as CPU@1GHz, DDR 400MHz@32bit, Single core. To support DDR 400MHz@64bit, the patch can be reverted by removing **CONFIG_DDR_32BIT** configuration. The main difference between 64bit and 32bit DDR configurations is located in the register MMDC_MDCTL and CS0_END. After changing the DDR from 64bit to 32bit, the memory size should be reduced from 2G to 1G.
ENGR00174407	The purpose of this CR is to add MFG tool support for i.MX 6Solo/DualLite ARM2 CPU board.

Kernel:

CR Number	Description
ENGR00173869	The purpose of this CR is to add MSL (Machine Specific Layer) support of i.MX 6Solo/DualLite chip. It includes - The changes for memory map, interrupt, GPIO, IOMUX, clock. - Reduce IRAM to 128K - Support one IPU - Remove SATA device, GC355 registration. - Apply cpu_is_mx6dl support into the drivers. To support one single kernel image for all i.MX6 boards, **cpu_is_mx6dl()** and cpu_is_mx6q() are used to distinguish i.MX 6Solo/DualLite and i.MX 6Dual/Quad dynamically. These functions are implemented by reading chip ID from ANATOP ID register. The layout for the register defines: Major Minor i.MX 6Dual/Quad 1.1: 6300 01 i.MX 6Dual/Quad 1.0: 6300 00 **i.MX 6Solo/DualLite 1.0: 6100 00**

ENGR00174152 ENGR00174425 ENGR00174649 ENGR00174896	The purpose of these CRs is used to change i.MX 6Solo/DualLite clock configurations: - Set ddr clock parent to pll2_mfd_400M - Set ipu1 clock to 270M - Set gpu3d_axi_clk@400MHz, gpu2d_axi_clk@400MHz, AXI_CLK@270MHz, VPU@270MHz
ENGR00174094	The purpose of this CR is to keep CPU voltages above 1V for all CPU frequencies
ENGR00173463	The purpose of this CR is to disable VPU IRAM usage because the IRAM of i.MX 6Solo/DualLite is mainly for VDOA and audio
ENGR00174309	The purpose of this CR is to enable GPU 2D and 3D by changing GPU clock source.
ENGR00174299	The purpose of this CR is to enable ePxP
ENGR00174106	The purpose of this CR is to enable EPDC
ENGR00174899	The purpose of this CR is to limit gc320's axi outstanding as 16 to make GPU runs stable at highest frequency.

imx-lib:

CR Number	Description
ENGR00173462 ENGR00174040	VPU: Integrate i.MX 6Solo/DualLite VPU firmware
ENGR00174611	ePxP: Enable ePxP library for i.MX6 platform.