6 Functional Block Requirements and Behaviors

6.1 Start-up

The PF0100 can be configured to start-up from either the internal OTP configuration, or with a hard-coded configuration built in to the device. The internal hard-coded configuration is enabled by connecting the VDDOTP pin to VCOREDIG through a 100 kohm resistor. The OTP configuration is enabled by connecting VDDOTP to GND.

For NP devices, selecting the OTP configuration causes the PF0100 to not start-up. However, the PF0100 can be controlled through the I^2C port for prototyping and programming. Once programmed, the NP device will startup with the customer programmed configuration.

6.1.1 Device Start-up Configuration

Table 10 shows the Default Configuration which can be accessed on all devices as described above, as well as the pre-programmed OTP configurations.

Table 10. Start-up Configuration

Registers	Default Configuration	Pre-programmed OTP Configuration				
	All Devices	F0	F1[23]	F2[23]	F3	F4
Default I^2C Address	0x08	0x08	0x08	0x08	0x08	0x08
VSNVS_VOLT	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V
SW1AB_VOLT	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V
SW1AB_SEQ	1	1	1	1	2	2
SW1C_VOLT	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V
SW1C_SEQ	1	2	1	1	2	2
SW2_VOLT	3.0 V	3.3 V	3.15 V	3.15 V	3.15 V	3.15 V
SW2_SEQ	2	5	2	2	1	1
SW3A_VOLT	1.5 V	1.5 V	1.2 V	1.5 V	1.2 V	1.5 V
SW3A_SEQ	3	3	4	4	4	4
SW3B_VOLT	1.5 V	1.5 V	1.2 V	1.5 V	1.2 V	1.5 V
SW3B_SEQ	3	3	4	4	4	4
SW4_VOLT	1.8 V	3.15 V	1.8 V	1.8 V	1.8 V	1.8 V
SW4_SEQ	3	6	3	3	3	3
SWBST_VOLT	-	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V
SWBST_SEQ	-	13	6	6	6	6
VREFDDR_SEQ	3	3	4	4	4	4
VGEN1_VOLT	-	1.5 V	1.2 V	1.2 V	1.2 V	1.2 V
VGEN1_SEQ	-	9	4	4	4	4
VGEN2_VOLT	1.5 V	1.5 V	-	-	-	-
VGEN2_SEQ	2	10	-	-	-	-
VGEN3_VOLT	-	2.5 V	-	-	-	-
VGEN3_SEQ	-	11	-	-	-	-

Table 10. Start-up Configuration

Registers	Default Configuration	Pre-programmed OTP Configuration				
	All Devices	**F0**	**F1[23]**	**F2[23]**	**F3**	**F4**
VGEN4_VOLT	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
VGEN4_SEQ	3	7	3	3	3	3
VGEN5_VOLT	2.5 V	2.8 V	2.5 V	2.5 V	2.5 V	2.5 V
VGEN5_SEQ	3	12	5	5	5	5
VGEN6_VOLT	2.8 V	3.3 V	-	-	-	-
VGEN6_SEQ	3	8	-	-	-	-
PU CONFIG, SEQ_CLK_SPEED	1.0 ms	2.0 ms	1.0 ms	1.0 ms	1.0 ms	1.0 ms
PU CONFIG, SWDVS_CLK	6.25 mV/µs	1.5625 mV/µs	12.5 mV/µs	12.5 mV/µs	12.5 mV/µs	12.5 mV/µs
PU CONFIG, PWRON	Level sensitive					
SW1AB CONFIG	SW1AB Single Phase, SW1C Independent Mode, 2.0 MHz					
SW1C CONFIG	2.0 MHz					
SW2 CONFIG	2.0 MHz					
SW3A CONFIG	SW3AB Single Phase, 2.0 MHz					
SW3B CONFIG	2.0 MHz					
SW4 CONFIG	No VTT, 2.0 MHz					
PG EN	RESETBMCU in Default Mode					

Notes
23. For designs using the i.MX 6-SoloLite, it is recommended to use the F3 OTP option instead of the F1 OTP option and F4 OTP option instead of the F2 OTP option