Windows Embedded CE 6.0

Reference Manual

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About This Book

This reference manual describes the requirements, implementation details, and testing for each module included in the Freescale software development kit (SDK) for Microsoft® Windows® CE 6.0.

Audience

This document is intended for device driver developers, application developers, and software test engineers who plan to use the product. This document is also intended for people who want to know more about Freescale's software development kit (SDK) for Microsoft Windows CE 6.0.

Suggested Reading

The Freescale manuals can be found at the Freescale Semiconductor, Inc. World Wide Web site listed on the back of the front cover of this document. These manuals can be downloaded directly from the Web site, or printed versions can be ordered. The Microsoft Platform Builder Help may be viewed from within the Platform Builder application.

- Microsoft Platform Builder for Windows Embedded CE 6.0 Help

Conventions

This document uses the following notational conventions:

- `Courier` indicates directory or file names and code examples.
- **Bold** indicates the menu options or buttons the user can select. Cascaded menu options are delimited with the > symbol.
- *Italic* indicates a reference to another document.

Definitions, Acronyms, and Abbreviations

Table i contains acronyms and abbreviations used in this document.

Table i. Acronyms and Abbreviated Terms

Term	Meaning
API	Application programming interface
BSP	Board support package
CSP	Chip support package
CSPI	Configurable serial peripheral interface
D3DM	Direct 3D Mobile
DHCP	Dynamic host configuration protocol
DPTC	Dynamic power and temperature control
DVFC	Dynamic voltage and frequency control
DVFS	Dynamic voltage and frequency scaling

Table i. Acronyms and Abbreviated Terms (continued)

Term	Meaning
EBOOT	Ethernet bootloader
EVB	Platform evaluation board
FAL	Flash abstraction layer
FIR	Fast infrared
FMD	Flash media driver
GDI	Graphics display interface
GPT	General purpose timer
I^2C	Inter-integrated circuit
IDE	Integrated development environment
IST	Interrupt service thread
IPU	Image processing unit
KITL	Kernel independent transport layer
LVDS	Low-voltage differential signaling
MAC	Media access control
MMC	Multimedia cards
OAL	OEM adaptation layer
OEM	Original equipment manufacturer
OS	Operating system
OTG	On-the-go
PMIC	Power management IC
PQOAL	Production quality OEM adaptation layer
PWM	Pulse-width modulator
SD	Secure digital cards
SDC	Synchronous display controller
SDHC	Secure digital host controller
SDIO	Secure digital I/O and combo cards
SDRAM	Synchronous dynamic random access memory
SDK	Software development kit
SIM	Subscriber identification module
SOC	System on a chip
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus

Chapter 1
Introduction

This Freescale board support package (BSP) is based on the Microsoft Windows® Embedded CE 6.0 operating system. This BSP supports the following Freescale platform(s):

- i.MX28 EVK Development System

This kit supports the Microsoft Windows Embedded CE 6.0 operating system, and requires the use of the Microsoft Platform Builder, which is an integrated development environment (IDE) for building customized embedded operating system designs. To view feature information, refer to the BSP Release Notes.

NOTE

Use this guide with the Microsoft Windows Platform Builder Help (or the identical *Platform Builder User Guide*).

- To view the Platform Builder Help, click **Help** from within the Platform Builder application.
- To view the online Windows Embedded CE 6.0 documentation, visit: http://msdn2.microsoft.com/en-us/library/bb159115.aspx

1.1 Getting Started

For instructions on installing this software release, building, downloading and running the OS image on the hardware board, refer to the appropriate User Guide.

1.2 Windows Embedded CE 6.0 Architecture

The Windows Embedded CE 6.0 architecture is a variation of the Windows operating system for minimalistic computers and embedded systems. The architecture of the operating system and sub-systems (for example, power management or DirectDraw) are described in several locations in the Help. Begin at the following location in Help:

Welcome to Windows Embedded CE 6.0 > Windows Embedded CE Architecture

Chapter 2
Audio Driver

The audio driver module provides audio playback and recording functions. For information about accessing an application with the audio driver using the methods and functions associated with the WaveOut or WaveIn functionality, see the Platform Builder Help at the following location:

Windows Embedded CE Features > Audio > Waveform Audio > Waveform Audio Application Development

2.1 Audio Driver Summary

Table 2-1 provides the source code location, library dependencies, and other BSP information.

Table 2-1. Audio Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Common Path	N/A
SOC Specific Path	..\PLATFORM\COMMON\SRC\SOC\<Target SOC>\WAVEDEV2
Platform Specific Path	..\PLATFORM\<*Target Platform*>\SRC\DRIVERS\WAVEDEV2\SGTL5000
Driver DLL	wavedev2_sgtl5000.dll
SDK Library	N/A
Catalog Item	Third Party > BSP > Freescale i.MX28-EVK:ARMV4I > Device Drivers > Audio > SGTL5000 Audio Driver
SYSGEN Dependency	SYSGEN_AUDIO
BSP Environment Variables	BSP_NOAUDIO= BSP_AUDIO_SGTL5000=1 BSP_I2CBUS1=1

NOTE

The selection and use of the Windows Media Player and the various software codecs is beyond the scope of the audio driver and is not discussed in this document. For information about these items, see the Platform Builder Help at the following location: **Windows Embedded CE Features > Audio**

2.2 Supported Functionality

The audio driver enables the system to provide the following software and hardware support:

1. Conforms to the audio driver architecture as defined for Windows Embedded CE 6.0 and all related operating systems
2. Double-buffered DMA operations to transfer audio data between memory and the hardware FIFO
3. Two power management modes: full on and full off
4. Full duplex playback and record
5. Minimizes power consumption at all times by using clock gating and by disabling all audio-related hardware components that are not actively being used
6. 8–96 KHz for both recording and playback
7. Mono and stereo 16-bit sample
8. Headphone detection

2.3 Hardware Operation

This section describes about the audio hardware operation.

2.3.1 Audio Hardware Design

This section describes the connection between the SoC audio peripherals and the external audio codec, the access interface of audio codec, and the audio input or output device connections.

2.3.1.1 i.MX28 EVK Audio Hardware Design

i.MX28 SoC uses 2 SAIF ports (Serial Audio Interface) for both audio playback and recording. The external stereo codec SGTL5000 is connected to SAIF0 and SAIF1 ports. External stereo codec SGTL5000 is configured to I2S mode, and SAIF0 is transmission port and SAIF1 is receiving port.

The i.MX28 uses the I^2C bus interface to access SGTL5000 control registers. The stereo codec SGTL5000 on i.MX28 EVK supports output to Headphone, input from Line In.

For operation and programming, refer to the chapters in the i.*MX28 Reference Manual* for the SAIF, DMA, and IOMUX components, and refer to the SGTL5000 *Datasheet* for Stereo Audio Codec SGTL5000.

2.3.2 Audio Playback

By default, the following hardware configuration options are enabled for the playback operation (based on the default audio driver configuration):

- The audio driver is configured to use SAIF0 and SAIF1 for I^2S mode and a sampling rate of 44.1 KHz
  - — Each audio data word is 16 bits long
  - — SAIF0 is transmitter for playback
  - — SAIF0 is configured to operate in master mode, and outputs MCLK/LRCLK/BITCLK

- The stereo codec is also configured for I^2S mode using a 44.1 KHz sample rate in slave mode, and get MCLK/LRCLK/BITCLK from SAIF0.
- The DMA channel supports 16-bit data transfers between the application memory buffers and the SAIF0 FIFO.
- Finally, the SAIF0 transmitter is enabled, which begins the transmission of the audio data stream.

The hardware repeatedly performs the following functions while audio playback is being performed:

- The SAIF0 issues a new DMA request when the transmitter FIFO level reaches the empty watermark level. The DMA controller then refills FIFO using data from the DMA buffers, until the DMA buffer is empty.
- An interrupt is generated when a DMA buffer is empty and this interrupt is handled by the audio driver. The audio driver refills the DMA buffer and returns it to the DMA controller for processing.
- Due to the double-buffering scheme, the DMA controller simply uses the other DMA buffer to continue refilling the SAIF0 transmitter FIFO while the previous DMA buffer is being refilled.

2.3.3 Audio Recording

The following hardware configuration steps are performed just prior to each recording operation (based upon the default audio driver configuration):

- SAIF1 is configured to receiver in slave mode to support recording. SAIF1 gets MCLK/LRCLK/BITCLK from SAIF0
- The DMA channel is fully configured to support 16-bit data transfers between the application memory buffers and the SAIF1 FIFO.
- The SAIF1 receiver is enabled and ready to receive data from the stereo codec.

The hardware repeatedly performs the following functions while audio recording is being performed:

- The SAIF1 issues a new DMA request whenever the receive FIFO level reaches the full watermark level. The DMA controller then transfers the data from the receiver FIFO to an input DMA buffer until the DMA buffer is full.
- The DMA controller generates an interrupt that is handled by the audio driver. The audio driver is responsible for copying the data from the full input DMA buffer into application-supplied buffers and then returning the empty input DMA buffer back to the DMA controller. Any data which cannot be transferred to an application-supplied buffer (for example, due to insufficient space) is simply discarded.
- Since a double-buffering scheme is being used, the DMA controller simply uses the other DMA buffer to continue recording the data from the SAIF1 receiver FIFO while the previous DMA buffer is being copied to application-supplied buffers.

2.3.4 Required SoC Peripherals

Table 2-2 shows the SoC hardware components required by the audio driver.

Table 2-2. Required SoC Peripherals

Component	Use
SAIF0	Playback
SAIF1	Record
APBX DMA	Manages the DMA channels that are used for playback and recording

2.3.5 Conflicts with SoC Peripherals

No conflicts.

2.3.6 Conflicts with Board Peripherals

The following section explains about the conflicts of the audio driver with board peripherals:

2.3.6.1 i.MX28 EVK Peripherals Conflicts

No conflicts.

2.3.7 Known Issues

The following section explains about the known issues in the audio driver:

2.3.7.1 i.MX28 Known Issues

If both the SGTL5000 stereo audio driver and the S/PDIF driver occurs, then the default audio device might be S/PDIF. The default audio device may be chosen by the AudioRouting application.

2.4 Software Operation

The audio driver follows the Microsoft-recommended architecture for audio drivers. For information about the architecture and operation, see the Platform Builder Help at the following location:

Developing a Device Driver > Windows CE Drivers > Audio Drivers > Audio Driver Development Concepts

2.4.1 Audio Playback

The software operation of the audio driver for playback is similar to the hardware configuration. Once the hardware components are configured, the audio driver only handles the output DMA buffer empty interrupts. This is done by the interrupt handler, which refills each of the output DMA buffers with new audio data that has been supplied by the application, and then returns the DMA buffer to the DMA controller.

2.4.2 Audio Recording

The operation of the audio driver for recording is similar to the hardware configuration. Once the hardware components are configured, then the audio driver handles the input DMA buffer full interrupts. This is done by the interrupt handler, which copies the contents of each input DMA buffer to an application-supplied buffer, and then returns the empty DMA buffer to the DMA controller. If the application-supplied buffer does not have enough space for all of the new data, discard any extra data. The application is signaled using a callback function when the application-supplied buffer is full.

2.4.3 Audio Driver Compile-Time Configuration Options

The audio driver can be configured for a wide variety of operating modes depending on the hardware and software requirements.

NOTE

Do not change the audio driver configuration settings without a detailed understanding of the platform hardware configuration and operating characteristics. Selecting invalid or incorrect configuration settings may result in the audio driver not loading or operating properly. Conversely, the audio driver performance and resource usage may be fine-tune by adjusting these configuration settings. For further information about the configuration options, see the corresponding source files.

2.4.3.1 i.MX28 Audio Driver Configuration Options

Table 2-3 gives the compile-time configuration options of the i.MX28 stereo audio driver.

Table 2-3. i.MX28 Audio Driver Configuration Options (oemsettings.h)

Configuration Setting Name	Description
INCHANNELS	Defines the number of input/recording channels that are available. Can be set to either 1 or 2. Default is 2.
OUTCHANNELS	Defines the number of output/playback channels that are available. Can be set to either 1 or 2. Default is 2.
BITSPERSAMPLE	The number of data bits per audio sample. This must match with the HWSAMPLE typedef and the AUDIO_SAMPLE_MAX/AUDIO_SAMPLE_MIN values. Default is 16.
HWSAMPLE	A typedef that defines the size of each audio data word. This must match the BITSPERSAMPLE and AUDIO_SAMPLE_MAX/AUDIO_SAMPLE_MIN values. Default is 16.
USE_MIX_SATURATE	Enable a check in the software mixer code to guard against saturation. Default is 1.
AUDIO_SAMPLE_MAX and AUDIO_SAMPLE_MIN	The valid range of each audio data word. Values that are outside of this range is clipped to the max/min value by the saturation protection code if USE_MIX_SATURATE is set to 1. Default is 32767 and -32768.
ENABLE_MIDI	If set to 1, MIDI code is included in the driver (~4 Kbytes).
USE_OS_MIXER	If set to 1, the driver does not do any internal mixing and relies on the OS mixer.

2.4.4 DMA Support

The audio driver uses the DMA controller to transfer digital audio data between the audio application and the audio FIFOs. This minimizes the processing required by the ARM core and can also reduce the power consumption during audio playback and recording operations. This section describes the audio driver DMA implementation issues and trade-offs, and the available compile-time DMA-related configuration options.

To use DMA transfers, the following items must be properly allocated, managed, and deallocated by the device driver:

- The DMA data buffers where the application data is kept
- The DMA buffer descriptors, which are used by the DMA hardware to manage the state of each DMA buffer

The DMA data buffers can be allocated from either the internal memory (which is provided by on-chip internal RAM) or external memory (which is provided by off-chip external DRAM).

Table 2-4 describes the issues and considerations for the type of memory to use for the DMA data buffers.

Table 2-4. DMA Memory Allocation Issues and Considerations

Memory Region	Memory Usage Issues and Considerations
Internal	• Allows the external memory to be placed in a low power mode while the DMA data buffers are being processed to reduce system power consumption (as long as nothing else on the system requires access to external memory) • Less power is required to access the internal RAM • The total size of the internal memory region is limited • The limited amount of internal memory may have to be shared by multiple device drivers • The entire internal memory region must be manually managed with predefined addressed ranges being reserved for each specific use
External	• The total size of the external memory is typically much greater than the size of the internal memory. This provides much greater flexibility in selecting the size of the DMA data buffers. • There is typically no need to worry about the possible impact and memory requirements of any other device driver. • Memory allocation is handled using the standard Windows Embedded CE 6.0 system calls • The external memory cannot be placed into a low power mode while the DMA is active

2.4.4.1 i.MX28 Audio DMA Buffer Use

The i.MX28 audio driver supports both playback and recording.Playback function always uses internal memory as DMA buffer, while recording function allocates DMA buffer from external memory.

Table 2-5 describes how to configure the build so that the audio driver allocates its DMA data buffers from either the internal or external memory. The DMA buffer descriptors can also be allocated either from internal or external memory.

Table 2-5. Configuration Options for Internal or External Memory DMA Data Buffer Allocation

Memory Region	Required Configuration Options
Internal	Set the BSP_AUDIO_DMA_BUF_ADDR macro in bsp_cfg.h to an address within the internal memory region. Set BSP_AUDIO_DMA_BUF_SIZE to the total size (in bytes) for all DMA data buffers that is allocated.
External	Make sure that the BSP_AUDIO_DMA_BUF_ADDR macro is commented out in bsp_cfg.h

2.4.5 Power Management

The primary method for limiting power consumption in the audio driver is to gate off all clocks to the SSI when those clocks are not needed, and to turn off all audio hardware components at the end of each audio stream. This is accomplished through the **DDKClockSetGatingMode** function call and the various PMIC audio APIs. In the BSP, the audio module can be disabled, and its clocks are turned off whenever there are no active audio I/O operations. The clock gating and the disabling of related audio hardware components is handled automatically within the audio module and requires no additional configuration or code changes.

The audio driver operates correctly when resuming after the power down mode.

2.4.5.1 PowerUp

This function resumes an audio I/O operation that was previously terminated by calling the PowerDown() API. It begins by restoring power and re-enabling all of the required audio hardware components. Then this function restarts the audio DMA transfers to complete the powerup process for the audio driver.

This function is intended to be called only by the Power Manager and must not block or depend on any hardware interrupts. Therefore, all required timed delays must be handled by using a polling loop instead of any of the normal **wait for an event to be signalled** functions. This functionality is currently handled by IOCTL_POWER_SET and the function is just a stub.

2.4.5.2 PowerDown

This function suspends all currently active audio I/O operations just before the entire system enters the low power state. This function is intended to be called only by the Power Manager and must not block or depend on any hardware interrupts. So, first thing this function must do is to signal all of the possible wait events that the normal audio driver thread may currently be waiting on. If this function does not signal all waiting events, the PowerDown thread may be blocked waiting for a critical section that is currently being held by the normal audio driver thread. This deadlocks the entire system and prevent it from properly entering the low power state.

When all waiting events are signalled, the normal audio thread is guaranteed (because of priority inversion) to run to the point where it releases the required critical section and allows the PowerDown thread to proceed without the possibility of deadlocking.

When the normal audio thread is not executing inside any critical section, the PowerDown thread can safely proceed to disable all active audio DMA operations and to power down the associated audio hardware components. Once this is done, the audio driver remains in a low power state until the PowerUp function is called by the Power Manager. This functionality is currently handled by IOCTL_POWER_SET and the function is just a stub.

2.4.5.3 IOCTL_POWER_SET

This Power Manager IOCTL is implemented for the audio driver. All system suspend and resume functions are handled by the IOCTL, which manages the PowerDown and PowerUp functionality. For all platforms, the following registry entry must be defined:

```
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\Audio]
        "IClass"="{A32942B7-920C-486b-B0E6-92A702A99B35}"    ; PMCLASS_GENERIC_DEVICE
```

This registry entry is required for proper power management functionality.

2.4.6 Audio Driver Registry Settings

At least one registry key must be properly defined so that the Device Manager loads the audio driver when the system is booted. Additional registry keys may also be defined and changed at runtime, to configure the operation of the audio driver.

2.4.6.1 i.MX28 Audio Driver Registry Settings

The following registry keys are required for the Device Manager to properly load the i.MX28 audio device driver during the device normal boot process. These registry settings should not be modified. If the settings are missing or incorrectly defined, then the audio driver may not be loaded and all audio functions are disabled.

```
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\Audio]
    "Prefix"="WAV"
    "Dll"="wavedev2_sgtl5000.dll"
    "Index"=dword:1
    "Order"=dword:4
    "Priority256"=dword:95
    "IClass"=multi_sz:"{A32942B7-920C-486b-B0E6-92A702A99B35}",
                      "{37168569-61C4-45fd-BD54-9442C7DBA46F}"

; Override wave API load order to follow audio driver
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\WAPIMAN]
   "Order"=dword:5
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\WAPIMAN_ACM]
   "Order"=dword:5
```

2.5 Unit Test

The audio driver is tested using the Waveform Audio Driver Test suite included with the Windows Embedded CE 6.0 Test Kit (CETK). The test suite includes automated and interactive tests used to test playback and recording functions.

2.5.1 Unit Test Hardware

Table 2-6 identifies the hardware needed to run the unit tests.

Table 2-6. Hardware Requirements

Requirement	Description
Stereo headphones or earphones	This is required to confirm that audio playback is working. The headphones or earphones should have a 3.5 mm jack
Mono microphoneLineIn cable	—used to connect LineIn port in board and PC

2.5.2 Unit Test Software

Table 2-7 lists the software required to run the unit tests.

Table 2-7. Software Requirements

Requirement	Description
Tux.exe	Tux test harness, which is needed for executing the test
Kato.dll	Kato logging engine, which is required for logging test data

Table 2-7. Software Requirements (continued)

Tooltalk.dll	Library required by Tux.exe and Kato.dll. Handles the transport between the target device and the development workstation
wavetest.dll	Test.dll file

2.5.3 Building the Audio Driver CETK Tests

The audio driver tests come pre-built as part of the CETK. No steps are required to build these tests. The wavetest.dll file is included with the CETK files in the following location:

```
[Drive]:\Program Files\Microsoft Platform Builder\6.00\cepb\wcetk\ddtk\armv4I
```

2.5.4 Running the Audio Driver CETK Tests

The command line for running the audio driver test is:

```
tux –o –d wavetest
```

Alternatively, use the CETK interface in the Platform Builder. If the full-duplex operation is not supported, the command line is:

```
tux -o -d wavetest -c "-e"
```

For detailed information about the audio driver tests, see the Platform Builder Help at the following location:

Windows Embedded CE Test Kit > **CETK Tests and Test Tools** > **CETK Tests** > **Audio Tests** > **Waveform Audio Driver Test**

2.6 System Level Audio Driver Tests

In addition to running the audio driver tests in the CETK, various system-level tests that involve the use of the audio driver can be performed. The following sections describe how to test the audio driver without using the CETK.

2.6.1 Checking for a Boot-Time Musical Tune

The normal Windows Embedded CE 6.0 boot procedure includes playing a short musical tune just before displaying the touch panel calibration screen. At this point, the audio driver should already have successfully loaded and the tune should be heard if a headset is attached to the stereo output jack.

2.6.2 Confirming Touchpanel Taps and Keypad Key Presses

The normal Windows Embedded CE 6.0 system configuration includes the ability to playback a short tapping sound when the stylus makes contact with the touchpanel. These taps should be heard when a headset is attached to the stereo output jack. A click should also be heard when a key on the keypad is pressed.

2.6.3 Playing Back Sample Audio and Video Files Using the Media Player

The Microsoft-supplied Media Player application can be used to load and play a variety of audio and video media files in a number of different formats. The only requirement is to include the software codecs in the OS image that may be needed to decode the media file. The Media Player includes controls for pausing, resuming, and stopping playback, and advancing playback to a specific point. Volume and muting controls are also provided.

2.6.4 Using the SDK Sample Audio Applications for Testing

The Windows Embedded CE 6.0 SDK that is included as part of the Platform Builder includes two audio-related sample applications. The `wavrec` sample application can be used to test the audio recording function while the `wavplay` sample application provides a command line-based method of playing back various media files. For additional information about these sample applications, see the Platform Builder Help at the following location:

Windows Embedded CE Features > Audio > Waveform Audio > Waveform Audio Samples

2.7 Audio Driver API Reference

For detailed reference information for the audio driver, see the Platform Builder Help at the following location:

Developing a Device Driver > Windows Embedded CE Drivers > Audio Drivers > Audio Driver Reference > Waveform Audio Driver Reference

2.8 Audio Driver Troubleshooting Guide

This section describes the techniques to identify and fix the most common problems involving the audio driver.

2.8.1 Checking Build-Time Configuration Options

Compile-time or link-time errors are probably occur due to incorrect or invalid configuration settings defined in `hwctxt.h` or `hwctxt.cpp`. See Section”i.MX28 Audio Driver Configuration Options for information about the device driver build configuration options. Follow the build procedure documented in the Release Notes to compile and link the audio driver. Confirm that the required Platform Builder catalog items are included in the OS design. See Table 2-1 for a list of the required and recommended audio driver-related catalog items.

2.8.2 Media Player Application Not Found

Make sure that the Media Player catalog item is included in the OS design. The Media Player application is not included in the final system image if the catalog item is not selected. For more information on this topic, see the Platform Builder Help at the following location:

Windows Embedded CE Features > Applications and Services > Windows Media Player for Windows Embedded CE

2.8.3 Media Player Fails to Load and Play an Audio File

This problem is typically caused by failing to include the appropriate software codec that is required to handle the audio file format.

Chapter 3
Backlight Driver

The backlight driver uses the hardware provided by the display module on the device, to control the backlight on the Liquid Crystal Display (LCD) panel. The backlight driver interfaces with the Windows CE Power Manager to provide timed control over the display backlight. A timeout interval controls the length of time that the backlight stays on. The backlight driver is power-manageable, and it meets the requirements of a power-manageable device by implementing the required power management I/O Controls (IOCTLs). The backlight driver uses its own defined timer to set the backlight power states.

3.1 Backlight Driver Summary

Table 3-1 provides a summary of source code location, library dependencies and other BSP information.

Table 3-1. Backlight Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Common Path	..\PLATFORM\COMMON\SRC\SOC\COMMON_FSL_V2_PDK1_9\BACKLIGHT
SOC Specific Path	N/A
Platform Specific Path	..\PLATFORM\<*Target Platform*>\SRC\DRIVERS\BACKLIKGHT
Driver DLL	backlight.dll
SDK Library	N\A
Catalog Item	Third Party > BSP > Freescale i.MX28 EVK PDK1_9: ARMV4I > Device Drivers > Backlight > Backlight PWM
SYSGEN Dependency	SYSGEN_BATTERY=1
BSP Environment Variables	BSP_BACKLIGHT=1

3.2 Supported Functionality

The backlight driver enables the 3-Stack System to provide the following support:

1. Conforms to the Device Manager streams interface
2. Supports 0–10 level adjustment
3. Supports power management mode: full on or full off

3.3 Hardware Operation

This section explains about the hardware operation

3.3.1 i.MX28-EVK Hardware Operation

The hardware consists of a PWM implemented by channel 2 of PWM controller.This PWM is dedicated to drive the backlight of LCD.It can be configured by adjusting the duty cycle in channel 2 of PWM controller.

3.4 Software Operation

The backlight driver is a stream interface driver and is accessed through the file system APIs. To use the backlight driver, a handle to the device must first be created using the **CreateFile** function. Subsequent commands to the device are issued using the **DeviceIoControl** function with IOCTL codes specifying the desired operation.

The control of the backlight operation requires a call to the **DeviceIoControl** function. The following are the possible choices available for the user:

- IOCTL_POWER_CAPABILITIES, register and inform the Power Manager of capabilities
- IOCTL_POWER_QUERY, where the new power state is returned
- IOCTL_POWER_SET, interface to the hardware that controls the backlight through the PDD layer
- IOCTL_POWER_GET, where the current power state is returned

3.4.1 Backlight Driver Registry Settings

This section explains about the backlight driver registry settings.

3.4.1.1 i.MX28-EVK Backlight Driver Registry Setting

The following registry keys are required to properly load backlight driver:

```
[HKEY_CURRENT_USER\ControlPanel\Backlight]
    "BattBacklightLevel"=dword:7F           ; Backlight level settings. 0x1E = Full On
    "ACBacklightLevel"=dword:7F             ; Backlight level settings. 0x1E = Full On
    "UseExt"=dword:0                        ; Disable timeout when on external power
    "UseBattery"=dword:0                    ; Disable timeout when on battery
    "AdvancedCPL"="AdvBacklight"            ; Enable Advanced Backlight control panel dialog
    "BatteryTimeout"=dword:1E               ; 30 Seconds
    "ACTimeout"=dword:3C                    ; 1 Minutes
```

3.4.2 Power Management

The backlight driver consumes power primarily through the operation of the LCD panel backlight. To facilitate the management of this module, the backlight driver implements the IOCTL code IOCTL_POWER_SET.

3.4.2.1 PowerUp

This function is not implemented for the backlight driver.

3.4.2.2 PowerDown

This function is not implemented for the backlight driver.

3.4.2.3 IOCTL_POWER_SET

The backlight driver implements the IOCTL_POWER_SET IOCTL API with support for the D0 (Turn On) and D4 (Set intensity to 0) power states. These states are handled in the following manner:

- D0—Backlight is enabled for LCD panel and the intensity can be adjusted through the PDD layer
- D4—Backlight intensity is set to 0 which is the lowest level of backlight

3.5 Unit Test

The backlight driver is tested by the application test. The following section explains about the hardware and software requirements for unit tests.

3.5.1 Unit Test Hardware

This section explains about the hardware required to run the backlight application test.

3.5.1.1 i.MX28-EVK Unit Test Hardware

Table 3-2 lists the required hardware to run the backlight application test.

Table 3-2. Hardware Requirements

Requirement	Description
SEIKO 43WVF1G-0 WVGA Panel	Display panel required for display of graphics data

3.5.2 Unit Test Software

Table 3-3 lists the required software to run the backlight application test.

Table 3-3. Software Requirements

Requirement	Description
backlight.dll	The backlight driver to implement the backlight functions
Advbacklight.dll	The file implements adding an Advanced button to the Backlight Control Panel application

3.5.3 Running the Backlight Application Test

Table 3-4 lists the backlight application test.

Table 3-4. Backlight Application Test

Test Case	Entry Criteria/Procedure/Expected Result
Backlight Level	Entry Criteria: N/A Procedure: 1. Go to Setting > Control Panel 2. Double click on the Display icon, then click on the Backlight tab 3. Click on the Advanced… button 4. Modify the backlight level setting for both battery and external power 5. Observe that the backlight level behaves according to the new setting Expected Result: N/A
Backlight Timeout	Entry Criteria: N/A Procedure: 1. Go to Setting > Control Panel 2. Double click on the Display icon, then click on the Backlight tab 3. Modify the backlight timeout setting for both battery and external power, and then click OK to apply the changes 4. Observe the time it takes for the backlight to go out, make sure it correspond with the new settings entered in step 3 Expected Result: N/A

3.6 Backlight API Reference

The API for the backlight driver conforms to the stream interface and exposes the standard functions. For more information, see Platform Builder Help at the following location:

Developing a Device Driver > Windows CE Embedded Drivers > Streams Interface Drivers

Chapter 4
Battery Driver

The battery driver module provides information about the battery level to the OS, and decides whether to execute the charging or discharging operation. It also reports battery capability and power supply state to the OS periodically by measuring the battery voltage. When charging, current-limit and voltage-limit is maintained to protect the charger and battery.

4.1 Battery Driver Summary

Table 4-1 provides a summary of source code location, library dependencies and other BSP information.

Table 4-1. Battery Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	N/A
SOC Common Path	N/A
SOC Specific Path	N/A
Platform Driver Path	..\PLATFORM\<*Target Platform*>\SRC\DRIVERS\BATTDRVR
Import Library	N/A
Driver DLL	battery.dll
Catalog Item	Third Party > BSP > Freescale i.MX28 EVK PDK1_9:ARMV4I > Device Drivers >Battery
SYSGEN Dependency	SYSGEN_BATTERY
BSP Environment Variables	BSP_NOBATTERY=

4.2 Supported Functionality

The battery driver enables the system to provide the following support:

1. Conforms to the battery driver interface
2. Supports two power management modes, full on and full off
3. Detects power source changes and reports current power source
4. Supports charging of Lion battery
5. Auto stop charging if the die temperature is too high

4.3 Hardware Operation

The battery driver is implemented with the power module of i.MX28. The power module contains on-chip analog to control charging function (including voltage monitor and current limiter). The LRADC channel 7 is used to get the level of voltage in the battery. This level is then used in determining the capacity level of the battery.

4.3.1 Conflicts with Other SoC Peripherals

No conflicts.

4.4 Software Operation

After initialization, the BatteryPDDGetStatus() function is called periodically to get the status of the battery. This function fills the structure SYSTEM_POWER_STATUS_EX2 and returns it to the system. The Power Properties window is updated based on the values in this structure.

4.4.1 Battery Driver Registry Settings

The following registry keys are required to properly load battery driver:

```
; These registry entries load the battery driver. The IClass value must match
; the BATTERY_DRIVER_CLASS definition in battery.h -- this is how the system
; knows which device is the battery driver. Note that we are using
; DEVFLAGS_NAKEDENTRIES with this driver. This tells the device manager
; to instantiate the device with the prefix named in the registry but to look
; for DLL entry points without the prefix. For example, it will look for Init
; instead of BAT_Init. This allows the prefix to be changed in the registry (if
; desired) without editing the driver code.
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\Battery]
   "Prefix"="BAT"
   "Dll"="battdrvr.dll"
   "Flags"=dword:8                      ; DEVFLAGS_NAKEDENTRIES
   "Order"=dword:3
   "MaxBatteryVoltage"=dword:1068       ; 4200mV
   "BatteryVoltageHighLevel"=dword:E74  ; 3700mV
   "BatteryVoltageLowLevel"=dword:C80   ; 3200mV
   "PollInterval"=dword:1F4           ; battery polling interval, in milliseonds(0.5 seconds)
   "IClass"="{DD176277-CD34-4980-91EE-67DBEF3D8913}"

[HKEY_LOCAL_MACHINE\System\Events]
    "SYSTEM/BatteryAPIsReady"="Battery Interface APIs"
```

4.4.2 Power Management

There is no additional power management implementation for battery driver.

4.5 Unit Test

The battery driver can be tested by switching on the system and monitoring the power properties window. When charging, the charge capacity of the battery can be seen increasing until it is charged to 100%.

NOTE

It is not allowed to plug in or remove out the battery after booting up the device.

4.5.1 Unit Test Hardware

The i.MX28-EVK board is required. For real battery mode, switch S1 to the up side and connect a real lion battery to J85 or J86; For fake battery mode, switch S1 to the down side.

4.6 Battery API Reference

The API for the battery driver conforms to the stream interface and exposes the standard functions. For more information, refer to the Platform Builder Help at the following location:

Developing a Device Driver > **Windows Embedded CE Drivers** > **Battery Drivers**

Chapter 5
Boot from Secure Digital/MultiMedia Card (SD/MMC)

Booting support from SD/MMC includes the following components:

- Boot Image
- Storage for OS binary image (NK)

Boot Image is stored in the SD/MMC card using a special tool, and NK is stored in the FAT partition. After the booting procedure, the user can select to boot the system from the SD/MMC card.

5.1 Boot from SD/MMC Summary

Table 5-1 provides a summary of source code location, library dependencies and other BSP information.

Table 5-1. Boot from SD/MMC Summary

Driver Attribute	Definition
Target Platform (TGTPLAT)	iMX28-EVK-PDK1_9
Target SOC	N/A
SOC Common Path	N/A
SOC Specific Path	N/A
Platform Specific Path	..\PLATFORM\<*Target Platform*>\SRC\BOOTLOADER ..\PLATFORM\COMMON\SRC\SOC\COMMON_FSL_V2\BOOT\FMD\SDMMC
Driver DLL	N/A
SDK Library	N/A
Catalog Item(s)	N/A
SYSGEN Dependency	N/A
BSP Environment Variable(s)	N/A

5.2 Supported Functionality

The Boot support from SD/MMC includes:

1. Supports boot from low or high capacity SD/MMC card
2. Supports storing OS images to SD/MMC flash
3. Supports loading OS image from SD/MMC flash to RAM
4. Supports file system on bootable SD/MMC card

5.3 Hardware Operation

This section explains about the hardware operation of the controller linked with SD/MMC.

5.3.1 Conflicts with Other Peripherals and Catalog Items

No conflicts.

5.4 Software Operation

On startup while booting from SD/MMC, the Boot ROM is responsible for initializing and bringing the SD/MMC memory to a proper working state. The Boot ROM executes the boot image and boot up the EBOOT, and then passes control to bootloader which in turn brings up the OS.

In the EBOOT, users can select the booting mode to **SDMMC Storage**. Then the EBOOT reads the NK from the FAT partition of the SD/MMC card, and boots up the system.

5.5 Card Flashing Tool

Flashing tool cfimager.exe is used to write the boot image to the SD/MMC. The tool is located in the directory `<%_WINCEROOT%>\SUPPORT_PDK1_9\TOOLS\COMMON\CFIMAGER`. Users can follow the instructions in the *readme.txt* file in that folder to write the boot image and boot up the system.

5.5.1 Write Image (EBOOT) to SD Card

Plug SD into Card Reader on PC, and run the following command. The *.sb files to flash are copied to `<%_WINCEROOT%>\SUPPORT_PDK1_9\TOOLS\iMX28-EVK\SDIMAGE`. The user can add that path before the filename.

```
cfimager -f eboot.sb -d <card reader drive, no colon>
```

After successful operation, users can copy nk.bin from release directory to <card reader drive>:\.

If users want to boot OS image (NK) without the bootloader (EBOOT), change the command to

```
cfimager -f nk.sb -d <card reader drive, no colon>
```

5.5.2 System Boot

Plug the flashed card into the board, ensure boot switch is set to the defined value and that the appropriate fuses are blown, then power on the board.

Chapter 6
Chip Support Package Driver Development Kit (CSPDDK)

The Chip Support Package Driver Development Kit (CSPDDK) provides an interface to access peripheral features and SOC configuration shared by the system. The CSPDDK executes as a device driver DLL and exports functions for the following SCC components:

- CLOCK
- GPIO
- IOMUX
- DMA (APBH DMA and APBX DMA)

6.1 CSPDDK Driver Summary

Table 6-1 provides a summary of source code location, library dependencies and other BSP information.

Table 6-1. CSPDDK Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Specific Path	..\PLATFORM\COMMON\SRC\SOC\<*Target SOC*>\CSPDDK
Platform Driver Path	..\PLATFORM\<*Target Platform*>\SRC\DRIVERS\CSPDDK
Driver DLL	cspddk.dll
SDK Library	N/A
Catalog Item	N/A
SYSGEN Dependency	N/A
BSP Environment Variables	BSP_NOCSPDDK=

6.2 Supported Functionality

The CSPDDK meets the following requirements:

1. Supports an interface that allows synchronized inter-process access to the following set of shared SoC resources:
   - IOMUX (DDK_IOMUX)
   - GPIO (DDK_GPIO)
   - DMA (DDK_APBHDMA and DDK_APBXDMA)
   - CLK (DDK_CLK)

2. Exposes exported functions that can be invoked without incurring a system call (for example, not a stream driver)

6.3 Hardware Operation

Refer to the hardware specification document for detailed operation and programming information.

6.3.1 Conflicts with Other Peripherals and Catalog Items

This section explains about the CSPDDK conflicts with other peripherals and catalog items.

6.3.1.1 Conflicts with SoC Peripherals

The following section explains about the CSPDDK conflicts with SoC peripherals.

6.3.1.1.1 iMX28 Peripheral Conflicts

Refer to the i.MX28 hardware specification document for possible conflicts.

6.3.1.2 Conflicts with Hardware Peripherals

No conflicts.

6.4 Software Operation

This section explains about the CSPDDK software operation.

6.4.1 Communicating with the CSPDDK

Similar to the CEDDK DLL, the CSPDDK DLL does not require any special initialization. All of the initialization required by the CSPDDK is performed when the DLL is loaded into the respective process space. Drivers required to utilize the CSPDDK simply need to link to the CSPDDK export library and invoke the exported functions.

6.4.2 Compile-Time Configuration Options

No options.

6.4.3 Registry Settings

There are no registry settings that need to be modified to use the CSPDDK driver. Since most drivers need to use CSPDDK functionality, the CSPDDK should be one of the first DLLs loaded by Device Manager.

6.4.4 Power Management

The CSPDDK exposes interfaces that allow drivers to self-manage power consumption by controlling clocking and pin configuration. The CSPDDK executes as a shared DLL and does not implement the

Power Manager driver IOCTLs or the PowerUp or PowerDown stream interface. However, the CSPDDK functions are invoked by other drivers during power state transits.

6.5 Unit Test

Due to the heavy use of the CSPDDK routines by other drivers on the system, currently there is no additional test case.

6.5.1 CSPDDK DLL System Clocking (DDK_CLK) Reference

The DDK_CLK interface allows device drivers to configure and query system clock settings.

6.5.1.1 DDK_CLK Enumerations

Table 6-2 lists all the programming elements in the DDK_CLK enumerations.

Table 6-2. DDK_CLK Enumerations

Programming Element	Description
DDK_CLOCK_SIGNAL	Clock signal name for querying/setting clock configuration
DDK_CLOCK_GATE_INDEX	Index for referencing the corresponding clock gating control bits within the CCM
DDK_CLOCK_GATE_MODE	Clock gating modes supported by CCM clock gating registers
DDK_CLOCK_BAUD_SOURCE	Input source for baud clock generation
DDK_DVFC_SETPOINT	Frequency/voltage setpoints supported by the DVFC driver

6.5.1.2 DDK_CLK Functions

The following functions are used to set DDK_CLK.

6.5.1.2.1 DDKClockSetGatingMode

This function sets the clock gating mode of the peripheral.

```
BOOL DDKClockSetGatingMode(
        DDK_CLOCK_GATE_INDEX index,
        DDK_CLOCK_GATE_MODE mode)
```

Parameters

index [in] Index for referencing the peripheral clock gating control bits

mode [in] Requested clock gating mode for the peripheral

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.1.2.2 DDKClockGetGatingMode

This function retrieves the clock gating mode of the peripheral.

```
BOOL DDKClockGetGatingMode(
        DDK_CLOCK_GATE_INDEX index,
        DDK_CLOCK_GATE_MODE *pMode)
```

Parameters

index	[in] Index for referencing the peripheral clock gating control bits
pMode	[out] Current clock gating mode for the peripheral
Return Values	Returns TRUE if successful, otherwise returns FALSE

6.5.1.2.3 DDKClockGetFreq

This function retrieves the clock frequency in Hz for the specified clock signal.

```
BOOL DDKClockGetFreq(
        DDK_CLOCK_SIGNAL sig,
        UINT32 *freq)
```

Parameters

sig	[in] Clock signal
freq	[out] Current frequency in Hz
Return Values	Returns TRUE if successful, otherwise returns FALSE

6.5.1.2.4 DDKClockSetFreq

This function sets the clock frequency in Hz for the specified clock signal.

```
BOOL DDKClockSetFreq(
        DDK_CLOCK_SIGNAL sig,
        UINT32 freq)
```

Parameters

sig	[in] Clock signal.
freq	[in] Requested frequency in Hz.
Return Values	Returns TRUE if successful, otherwise returns FALSE.

6.5.1.2.5 DDKClockConfigBaud

This function configures the input source clock and dividers for the specified CCM peripheral baud clock output.

```
BOOL DDKClockConfigBaud(
        DDK_CLOCK_SIGNAL sig,
        DDK_CLOCK_BAUD_SOURCE src,
        UINT32 preDiv,
        UINT32 postDiv)
```

Parameters

sig	[in] Clock signal to configure
src	[in] Selects the input clock source
preDiv	[in] Specifies the value programmed into the baud clock predivider
postDiv	[in] Specifies the value programmed into the baud clock postdivider
Return Values	Returns TRUE if successful, otherwise returns FALSE

6.5.1.2.6 DDKClockSetpointRequest

This function requests the DVFC driver to transition to a setpoint that meets or exceeds the voltage and clocking requirements of the setpoint being requested. This function optionally blocks until the setpoint request has been granted.

```
BOOL DDKClockSetpointRequest(
        DDK_DVFC_SETPOINT setpoint,
        BOOL bBlock)
```

Parameters

setpoint	[in] Specifies the setpoint to be requested
bBlock	[in] Set TRUE to block until the setpoint has been granted; set FALSE to return immediately after the request has been submitted
Return Values	Returns TRUE if successful, otherwise returns FALSE

6.5.1.2.7 DDKClockSetpointRelease

This function releases a setpoint previously requested using DDKClockSetpointRequest.

```
BOOL DDKClockSetpointRelease(
        DDK_DVFC_SETPOINT setpoint)
```

Parameters

setpoint	[in] Specifies the setpoint to be released
Return Values	Returns TRUE if successful, otherwise returns FALSE

6.5.1.2.8 DDKClockGetSharedConfig

This function obtains a reference to the global shared clock configuration data structure. This is intended to be used by the DVFC driver.

```
PDDK_CLK_CONFIG DDKClockGetSharedConfig(VOID)
```

Parameters	None
Return Values	Returns a pointer to the clock configuration data structure.

6.5.1.2.9 DDKClockLock

This function requests a lock of the global shared clock configuration data structure.

```
VOID DDKClockLock(VOID)
```

Parameters None

Return Values None

6.5.1.2.10 DDKClockUnLock

This function releases a lock of the global shared clock configuration data structure.

```
VOID DDKClockUnLock(VOID)
```

Parameters None

Return Values None

6.5.1.3 DDK_CLK Examples

The following are the example code for the DDK_CLK.

Example 6-1 shows the sample code for CSPDDK clock gating.

Example 6-1. CSPDDK Clock Gating

```
#include "csp.h"    // Includes CSPDDK definitions

// Enable I2C1 peripheral clock
DDKClockSetGatingMode(DDK_CLOCK_GATE_INDEX_I2C1, DDK_CLOCK_GATE_MODE_ENABLED_ALL);

// Disable I2C1 peripheral clock
DDKClockSetGatingMode(DDK_CLOCK_GATE_INDEX_I2C1, DDK_CLOCK_GATE_MODE_DISABLED);
```

Example 6-2 shows the sample code for CSPDDK clock rate query.

Example 6-2. CSPDDK Clock Rate Query

```
#include "csp.h"    // Includes CSPDDK definitions

UINT32 freq;

// Query the current bus clock
DDKClockGetFreq(DDK_CLOCK_SIGNAL_AHB, &freq);
```

6.5.2 CSPDDK DLL GPIO (DDK_GPIO) Reference

The DDK_GPIO interface allows device drivers to utilize the GPIO ports. Each GPIO port has a single interrupt request line that is shared for all port pins. In addition, configuration, status, and data registers are shared. The DDK_GPIO provides safe access to the shared GPIO resources.

6.5.2.1 DDK_GPIO Enumerations

Table 6-3 lists all the programming elements in the DDK_GPIO enumerations.

Table 6-3. DDK_GPIO Enumerations

Programming Element	Description
DDK_GPIO_BANK	Specifies the GPIO module instance
DDK_GPIO_CFG	Specifies the configuration of the GPIO pins

6.5.2.2 DDK_GPIO Functions

The following section explains about the DDK_GPIO functions.

6.5.2.2.1 DDKGpioConfig

This function configures the gpio_pin as input/output, sets the drive strength, voltage, and as interrupt selection (if applicable).

```
BOOL DDKGpioConfig(DDK_IOMUX_PIN gpio_pin,
                   DDK_GPIO_CFG gpio_cfg,
                   DDK_IOMUX_PAD_DRIVE drive,
                   DDK_IOMUX_PAD_VOLTAGE voltage,
                   BOOL bPull_Enable)
```

Parameters

gpio_pin [in] functional pin name

gpio_cfg [in] structure to configure the pin as input/output, interrupt selection.

drive [in] set the gpio_pin drivestrength.

voltage [in] set the gpio_pin voltage.

bPull_Enable [in] enable/disable the pullup for the gpio_pin.

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.2.2.2 DDKGpioEnableDataPin

This function sets the value in the register bit to drive on the gpio_pin.

```
BOOL DDKGpioEnableDataPin(DDK_IOMUX_PIN pin,UINT32 data)
```

Parameters

pin [in] functional pin name

data [in] data to be written to the pin.

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.2.2.3 DDKGpioWriteDataPin

This function sets the value in the register bit to drive on the gpio_pin.

```
BOOL DDKGpioWriteDataPin(DDK_IOMUX_PIN pin,UINT32 data)
```

Parameters

pin [in] functional pin name

data [in] data to be written to the pin.

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.2.2.4 DDKGpioReadDataPin

This function reads the GPIO port data from the specified pin.

```
BOOL DDKGpioReadDataPin(DDK_IOMUX_PIN pin, UINT32 *pData)
```

Parameters

pin [in] GPIO pin [0-31].

pData [out] points to buffer for data read. Data is shifted to LSB.

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.2.2.5 DDKGpioReadIntr

This function reads register for the interrupt status.

```
BOOL DDKGpioReadIntr(DDK_IOMUX_PIN pin, UINT32 *pData)
```

Parameters

pin [in] functional pin name

pData [out] pointer to the data read.

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.3 CSPDDK DLL IOMUX (DDK_IOMUX) Reference

The DDK_IOMUX interface allows device drivers to configure signal multiplexing and pad configuration. This control resides inside the IOMUX registers and is shared for the entire system. The DDK_IOMUX support allows drivers to dynamically update and query their signal multiplexing and pad configuration.

6.5.3.1 DDK_IOMUX Enumerations

Table 6-4 lists all the programming elements in the DDK_IOMUX enumerations.

Table 6-4. DDK_IOMUX Enumerations

Programming Element	Description
DDK_IOMUX_PIN	Specifies the functional pin name used to configure the IOMUX.
DDK_IOMUX_PIN_MUXMODE	Specifies the mux mode for a signal

Table 6-4. DDK_IOMUX Enumerations (continued)

Programming Element	Description
DDK_IOMUX_PAD_DRIVE	Specifies the drive strength for a pad; if no DRIVE bit for a PAD, the DDK_IOMUX_PAD_DRIVE_NULL should be set.
DDK_IOMUX_PAD_PULL	Specifies the pull-up/pull-down/keeper configuration for a pad
DDK_IOMUX_PAD_VOLTAGE	Specifies the driver voltage for a pad, either 1.8 V or 3.3 V

6.5.3.2 DDK_IOMUX Functions

This sections explains about the DDK_IOMUX functions.

6.5.3.2.1 DDKIomuxSetPinMux

This function sets the IOMUX mux for the specified IOMUX pin.

```
BOOL DDKIomuxSetPinMux(DDK_IOMUX_PIN pin, DDK_IOMUX_PIN_MUXMODE muxmode)
```

Parameters

pin [in] functional pin name used to configure IOMUX HW_PINCTRL_MUXSEL

muxmode [in] MUX_MODE configuration.

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.3.2.2 DDKIomuxGetPinMux

This function gets the IOMUX mux configuration for the specified IOMUX pin.

```
BOOL DDKIomuxGetPinMux(DDK_IOMUX_PIN pin, DDK_IOMUX_PIN_MUXMODE *pMuxmode)
```

Parameters

pin [in] functional pin name used to select the IOMUX output or input path that is returned.

pMuxmode [out] MUX_MODE configuration.

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.3.2.3 DDKIomuxSetPadConfig

This function sets the IOMUX pad configuration for the specified IOMUX pad.

```
BOOL DDKIomuxSetPadConfig(DDK_IOMUX_PIN pin,
                          DDK_IOMUX_PAD_DRIVE drive,
                          DDK_IOMUX_PAD_PULL pull,
                          DDK_IOMUX_PAD_VOLTAGE voltage)
```

Parameters

pad [in] functional pad name used to select the pad that is configured.

drive [in] drive strength configuration.

pull [in] pull-up, pull-down, or keeper configuration.

voltage [in] drive voltage configuration

Return Values Returns TRUE if successful, otherwise returns FALSE.

6.5.3.2.4 DDKIomuxEnablePullup

This function enables the IOMUX pad configuration for the specified IOMUX pad.

```
BOOL DDKIomuxEnablePullup(DDK_IOMUX_PIN pin, BOOL bEnable)
```

Parameters

pin [in] functional pin name used to select the IOMUX output or input path that is returned.

bEnable [in] enable or disable pullup

Return Values Returns TRUE if successful, otherwise returns FALSE.

6.5.3.2.5 DDKIomuxGetPadConfig

This function gets the IOMUX pad configuration for the specified IOMUX pad.

```
BOOL DDKIomuxGetPadConfig(DDK_IOMUX_PIN pin,
                          DDK_IOMUX_PAD_DRIVE   *pDrive,
                          DDK_IOMUX_PAD_PULL    *pPull,
                          DDK_IOMUX_PAD_VOLTAGE *pVoltage)
```

Parameters

pin [in] functional pin name used to select the IOMUX output or input path that is returned

pDrive [out] drive strength configuration

pPull [out] pull-up, pull-down, or keeper configuration

pVoltage [out] drive voltage configuration

Return Values Returns TRUE if successful, otherwise returns FALSE.

6.5.4 CSPDDK DLL DMA (DDK_DMA) Reference

The DDK_DMA interface allows device drivers to allocate, configure, and control shared DMA resources.

6.5.4.1 DDK_DMA Functions

This section explains about the DDK_DMA functions.

6.5.4.1.1 DDKApbhStartDma

This function loads the NEXTCOMMAND address and increments the semaphore to start the DMA operation for first command.

```
BOOL DDKApbhStartDma(UINT8 Channel,PVOID memAddrPA, UINT8 semaphore)
```

Parameters

Channel	[in] channel number
memAddrPA	[in] pointer of memory's physical address
semaphore	[in] DMA semaphore
Return Values	Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.2 DDKApbhStopDma

This function stops the DMA channel.

```
BOOL DDKApbhStopDma(UINT8 Channel)
```

Parameters

Channel	[in] channel number
Return Values	Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.3 DDKApbhDmaInitChan

This function initializes the requested DMA channel.

```
BOOL DDKApbhDmaInitChan(UINT8 Channel,BOOL bEnableIrq)
```

Parameters

Channel	[in] channel number
bEnableIrq	[in] enable or disable the irq
Return Values	Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.4 DDKApbhDmaChanCLKGATE

This function clears the interrupt for respective channel.

```
BOOL DDKApbhDmaChanCLKGATE(UINT8 Channel,BOOL bClockGate)
```

Parameters

Channel	[in] channel number
bClockGate	[in] gate or un-gate the channel
Return Values	Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.5 DDKApbhDmaClearCommandCmpltIrq

This function clears the interrupt for respective channel.

```
BOOL DDKApbhDmaClearCommandCmpltIrq(UINT8 Channel)
```

Parameters

Channel [in] channel number

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.6 DDKApbhDmaEnableCommandCmpltIrq

This function enables the interrupt for respective channel.

```
BOOL DDKApbhDmaEnableCommandCmpltIrq(UINT8 Channel,BOOL bEnable)
```

Parameters

Channel [in] channel number

bEnableIrq [in] enable or disable the interrupt for respective channel

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.7 DDKApbhDmaResetChan

This function resets the AHB to APBH bridge channel based on the argument channel.

```
BOOL DDKApbhDmaResetChan(UINT8 Channel,BOOL bReset)
```

Parameters

Channel [in] channel number

bReset [in] reset or un-reset the channel

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.8 DDKApbhDmaFreezeChan

This function freezes the AHB to APBH bridge channel based on the argument channel.

```
BOOL DDKApbhDmaFreezeChan(UINT8 Channel,BOOL bFreeze)
```

Parameters

Channel [in] channel number

bFreeze [in] freeze or un-freeze the channel

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.9 DDKApbhDmaGetPhore

This function gets the phore of respective channel.

```
UINT32 DDKApbhDmaGetPhore(UINT32 Channel)
```

Parameters

Channel [in] channel number

Return Values Returns the virtual channel index if successful, otherwise returns NULL**.**

6.5.4.1.10 DDKApbxStartDma

This function loads the NEXTCOMMAND address and increments the semaphore to start the DMA operation for first command.

```
BOOL DDKApbxStartDma(UINT8 Channel,PVOID memAddrPA, UINT8 semaphore)
```

Parameters

Channel [in] channel number

memAddrPA [in] pointer of memory's physical address

semaphore [in] DMA semaphore

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.11 DDKApbxGetNextCMDAR

This function gets the NEXTCOMMAND address.

```
UINT32 DDKApbxGetNextCMDAR(UINT8 Channel)
```

Parameters

Channel [in] channel number

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.12 DDKApbxStopDma

This function stops the DMA channel.

```
BOOL DDKApbxStopDma(UINT8 Channel)
```

Parameters

Channel [in] channel number

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.13 DDKApbxDmaInitChan

This function initializes the requested DMA channel.

```
BOOL DDKApbxDmaInitChan(UINT8 Channel,BOOL bEnableIrq)
```

Parameters

Channel [in] channel number

bEnableIrq [in] enable/disable the irq

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.14 DDKApbxDmaGetActiveIrq

This function gets the active irq status of DMA channel.

```
BOOL DDKApbxDmaGetActiveIrq(UINT8 Channel)
```

Parameters

Channel [in] channel number

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.15 DDKApbxDmaClearCommandCmpltIrq

This function clears the interrupt for respective channel.

```
BOOL DDKApbxDmaClearCommandCmpltIrq(UINT8 Channel)
```

Parameters

Channel [in] channel number

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.16 DDKApbxDmaClearErrorIrq

This function clears the error interrupt for respective channel.

```
BOOL DDKApbxDmaClearErrorIrq(UINT8 Channel)
```

Parameters

Channel [in] channel number

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.17 DDKApbxDmaEnableCommandCmpltIrq

This function enables the interrupt for respective channel.

```
BOOL DDKApbxDmaEnableCommandCmpltIrq(UINT8 Channel,BOOL bEnable)
```

Parameters

Channel [in] channel number

bEnableIrq [in] enable/disable the interrupt for respective channel

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.18 DDKApbxDmaEnableErrorIrq

This function enables the interrupt for respective channel.

```
BOOL DDKApbxDmaEnableErrorIrq(UINT8 Channel,BOOL bEnable)
```

Parameters

Channel [in] channel number

bEnableIrq [in] enable or disable the interrupt for respective channel

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.19 DDKApbxDmaResetChan

This function resets the AHB to APBX bridge channel based on the argument channel.

```
BOOL DDKApbxDmaResetChan(UINT8 Channel,BOOL bReset)
```

Parameters

Channel [in] channel number

bReset [in] reset or un-reset the channel

Return Values Returns TRUE if successful, otherwise returns FALSE

6.5.4.1.20 DDKApbxDmaFreezeChan

This function freezes the AHB to APBX bridge channel based on the argument channel.

```
BOOL DDKApbxDmaFreezeChan(UINT8 Channel,BOOL bFreeze)
```

Parameters

Channel [in] channel number

bFreeze [in] freeze or un-freeze the channel

Return Values Returns TRUE if successful, otherwise returns FALSE

Chapter 7
Configurable Serial Peripheral Interface (CSPI) Driver

The CSPI module provides master functionality of a standard CSPI bus.

NOTE

In this chapter, CSPI and SPI have the same meaning. For some SOCs platform, using CSPI, and for others, using SPI.

7.1 CSPI Driver Summary

Table 7-1 provides a summary of source code location, library dependencies, and other BSP information.

Table 7-1. CSPI Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Specific Path	..\PLATFORM\COMMON\SRC\SOC\<*Target SOC*>\SPI
Platform Driver Path	..\PLATFORM\<*Target Platform*>\DRIVERS\SPI
Import Library	spisdk.lib
Driver DLL	spi.dll
Catalog Item	Third Party > BSP > Freescale <*TGTPLAT*> > Device Drivers > SPI Bus
SYSGEN Dependency	N/A
BSP Environment Variables	BSP_SSP2_SPI = 1

7.2 Supported Functionality

The CSPI driver supports the following features:

1. Supports the CSPI master mode of operation
2. Supports CSPI configurable bus feature
3. Supports configurable access method of polling method
4. Supports stream interface
5. Supports two power management modes: full on and full off

7.2.1 Conflicts with Other Peripherals and Catalog Items

This section explains about the conflicts that the CSPI driver have with other peripherals and catalog items.

7.2.1.1 Conflicts with SoC Peripherals

No conflicts.

7.2.2 Conflicts with EVK Peripherals

No conflicts.

7.3 Software Operation

This section explains about the software operation for the CSPI module.

7.3.1 Registry Settings

The following registry keys are required to load the CSPI module.

```
;; SPI Bus Driver
;;
IF BSP_SSP2_SPI
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\SPI2]
   "Prefix"="SPI"
   "Dll"="spi.dll"
   "Index"=dword:2
ENDIF ;BSP_SSP2_SPI
```

7.3.2 Communicating with the CSPI

The CSPI is a stream interface driver, and is thus accessed through the file system APIs. To communicate using the CSPI, a handle to the device must first be created using the **CreateFile** function. Subsequent commands to the device are issued using the **DeviceIoControl** function with IOCTL codes specifying the desired operation. If preferred, the **DeviceIoControl** function calls can be replaced with macros that hide the **DeviceIoControl** call details. The following are the basic steps:

7.3.3 Creating a Handle to the CSPI

Call the **CreateFile** function to open a connection to the CSPI device. A CSPI port must be specified in this call. The format is **SPIX:**, with X being the number indicating the CSPI port. This number should not exceed the number of CSPI instances on the platform. If an CSPI port does not exist, **CreateFile** returns ERROR_FILE_NOT_FOUND.

To open a handle to the CSPI:

1. Insert a colon after the CSPI port for the first parameter, *lpFileName*
   For example, specify SPI1: as the CSPI port
2. Specify FILE_SHARE_READ | FILE_SHARE_WRITE in the *dwShareMode* parameter. Multiple handles to an CSPI port are supported by the driver.
3. Specify OPEN_EXISTING in the *dwCreationDisposition* parameter. This flag is required.
4. Specify FILE_FLAG_RANDOM_ACCESS in the *dwFlagsAndAttributes* parameter.

Example 7-1 is a sample code to open a CSPI port.

Example 7-1. Code to open CSPT port

```
// Open the serial port.
hSPI = CreateFile (L"SPI1:",                                  // name of device
                   GENERIC_READ | GENERIC_WRITE,              // access (read-write) mode
                   FILE_SHARE_READ | FILE_SHARE_WRITE,        // sharing mode
                   NULL,                                      // security attributes (ignored)
                   OPEN_EXISTING,                             // creation disposition
                   FILE_FLAG_RANDOM_ACCESS,                   // flags/attributes
                   NULL);                                     // template file (ignored)
```

7.3.4 Data Transfer Operations

The CSPI driver provides one command, SPIExchange, that facilitates performing both reads and writes through the CSPI bus. The basic unit of data transfer in the CSPI driver is the CSPI_XCH_PKT, which contains a buffer for reading and writing data, and a CSPI_BUSCONFIG datum that specifies the desired bus configuration and XCH method which is used during the SPI transmission. The following steps explain the process of performing write and read operations through the CSPI bus.

Before these actions can be taken, a handle to the CSPI port must already be opened. Each of these steps requires a call to the **DeviceIoControl** function. As parameters, the CSPI port handle, appropriate IOCTL code, and other input and output parameters are required.

To perform an CSPI transfer:

1. Create a CSPI_XCH_PKT object and initialize the fields of the packet as follows:
   a) Initialize a CSPI_BUSCONFIG datum to specify the bus parameters as SSPCTRL0, SSPCMD, SSPARG, BITCOUNT, bREAD, and specify the method parameters for use/not use DMA, use/not use POLLING, send/not send command.
   b) Set the *pBuf* field to the user buffer which sends and receives data.
   c) Set the *xchCnt* field, for the 1-8 bit XCH, the *xchCnt* = *bytes*, for the 9-16 bit XCH, the *xchCnt* = *words*, for the 17-32 bit XCH, the *xchCnt* = *dwords*.
2. Set the *hDevice* parameter to the previously acquired CSPI port handle.
3. Set the *dwIoControlCode* to the SPI_IOCTL_EXCHANGE IOCTL code.
4. Set the *lpInBuffer* to point to the CSPI_XCH_PKT object created in step 1. Set *nInBufferSize* to the size of that packet object.
5. Set *lpOutBuffer*, *lpBytesReturned*, and *lpOverlapped* to NULL. Set *nOutBufferSize* to 0.

Example 7-2 demonstrates how to perform a XCH transfer.

Example 7-2. Code for XCH transfer

```
CSPI_BUSCONFIG_T buscnfg =
{
    0x9000004,                      //configuration for SSP control register 0
    0,                              //command 0
    0,                              //command 1
    FALSE,                          //no DMA
    TRUE,                           //polling mode
```

```
    32,                                 //32 bits data
    FALSE,                              //write data
    0,                                  //no command is sent
};

DWORD Data[11];

CSPI_XCH_PKT_T xchPkt =
{
    &buscnfg,
    Data,
    1,                                  // XCH to target SPI device 1 times
    NULL,
    0
};
                                        // Transfer data via CSPI
DeviceIoControl(hCSPI,                  // file handle to the driver
     CSPI_IOCTL_EXCHANGE,               // I/O control code
                 (PBYTE) &xchPkt,       // in buffer
                 sizeof(xchPkt),        // in buffer size
                 NULL,                  // out buffer
                 0,                     // out buffer size
                 NULL,                  // number of bytes returned
                 NULL);                 // ignored (=NULL)
```

As a substitute for the **DeviceIoControl** call above, a SDK wrap function may be used to simplify the code. The following is the sample code:

```
CSPIExchange(hCSPI, &xchPkt);
```

7.3.5 Closing the Handle to the CSPI

Call the **CloseHandle** function to close a handle to the CSPI after an application finishes using it. **CloseHandle** has one parameter, which is the handle returned by the **CreateFile** function call that opened the CSPI port.

7.3.6 Power Management

The primary method for limiting power consumption in the CSPI module is to gate off the input clock to the module when the input CSPI clock is not needed. This is accomplished through the **DDKClockSetGatingMode** function call. In all of the BSP use cases, the CSPI controller acts as a master device. As a result, the CSPI clock can be turned off, whenever the module is not processing CSPI packets.

As described in the **Data Transfer Operations** section, the CSPI driver turns on the CSPI clocks and enables the CSPI module before processing an CSPI XCH, and then disables and turns off clocks to the CSPI module after the XCH has been done. This limits the time during which the CSPI module is consuming power to the time during which the CSPI is actively performing data transfers.

7.3.6.1 PowerUp

This function is not implemented for the CSPI driver. Power to the CSPI module is managed as CSPI transfer operations are processed. There are no additional power management steps needed for the CSPI.

7.3.6.2 PowerDown

This function is not implemented for the CSPI driver.

7.3.6.3 IOCTL_POWER_SET

This function is implemented for the CSPI driver. When D4 power mode is set, the driver switches its operating mode to polling mode that does not produce interrupt events to BSP system. When leaving the D4 power mode, the driver recovers its origin operating mode.

7.4 Unit Test

The CSPI driver does not use the CETK for unit testing, but uses the test program described in the following section for unit tests.

7.4.1 Building the Unit Tests

To build the CSPI tests, build an OS image for the desired configuration using these steps:

1. Within the Platform Builder, choose **Build OS** > **Open Release Directory**.
   A DOS prompt is displayed.
2. Change to the SPI Test directory: `\WINCE600\SUPPORT\TEST\SPITEST`
3. Enter **set WINCEREL=1** on the command prompt and press return.
   This copies the EXE to the flat release directory.
4. Input **build -c** to build SPI test.

After the build completes, the SPIAPP.EXE file is located in the $(_FLATRELEASEDIR) directory.

To run the application within VS2005 use the following steps:

1. Go to the Target menu option and select **Run Programs** option. This gives a list of applications that can be run on the OS.
2. Select **SPIAPP.EXE** from this list.
3. Click **Run** to run this application.

7.5 CSPI Driver API Reference

This section explains about the CSPI driver API reference.

7.5.1 CSPI Driver IOCTLs

This section consists of descriptions for the CSPI I/O control codes (IOCTLs). These IOCTLs are used in calls to **DeviceIoControl** to issue commands to the CSPI device. Only relevant parameters for the IOCTL have a description provided.

7.5.1.1 CSPI_IOCTL_EXCHANGE

This **DeviceIoControl** request performs the transfer of data to a target device. An CSPI_XCH_PKT object is required, which contains CSPI bus configuration parameters and data buffers. All of the required information should be stored in the CSPI_XCH_PKT passed in the *lpInBuffer* field.

Parameters

lpInBuffer	Pointer to an CSPI_XCH_PKT structure containing a pointer to bus configuration parameters and data buffers
nInBufferSize	Size in bytes of the CSPI_XCH_PKT

7.5.2 CSPI Driver SDK Wrapper

This section explains about the CSPI driver SDK wrapper.

7.5.2.1 CSPIOpenHandle

This function retrieves the CSPI device handle.

```
HANDLE CSPIOpenHandle(
        LPCWSTR lpDevName
);
```

Parameters

lpDevName	The CSPI device name for retrieving handle from CreateFile()
Return Values	Returns Handle for CSPI driver; returns INVALID_HANDLE_VALUE if failure

7.5.2.2 CSPICloseHandle

This function closes a handle of the CSPI stream driver.

```
BOOL CSPICloseHandle(
        HANDLE hDev
);
```

Parameters

hDev	The CSPI device handle retrieved from CreateFile()
Return Values	Returns TRUE or FALSE. If the result is TRUE, the operation is successful

7.5.2.3 CSPIExchange

This function performs XCH operations.

```
BOOL CSPITransfer(
        HANDLE hDev,
        PCSPI_XCH_PKT_T pCspiXchPkt
```

```
    );
```

Parameters

hDev	The CSPI device handle retrieved from CreateFile()
pCspiXchPkt	[in] Pointer to XCH packet with bus configuration parameters
Return Values	Returns TRUE or FALSE. If the result is TRUE, the operation is successful

7.5.3 CSPI Driver Structures

This section explains about the CSPI driver structures.

7.5.3.1 CSPI_BUSCONFIG_T

This structure contains the bus configuration information needed during CSPI performs XCH.

```
// CSPI bus configuration
typedef struct
{
    SSP_CTRL0 SspCtrl0;
    SSP_CMD0  SspCmd;
    SSP_CMD1  SspArg;
    BOOL      usedma;
    BOOL      usepolling;
    UINT8     bitcount;
    BOOL      bRead;
    BOOL      bCmd;
} CSPI_BUSCONFIG_T, *PCSPI_BUSCONFIG_T;
```

Table 7-2 shows the CSPI_BUSCONFIG_T structure members.

Table 7-2. CSPI_BUSCONFIG_T Structure Members

Member	Description
SspCtrl0	Configuration for SSP control register 0
SspCmd	Command 0 for SSP
SspArg	Command 1for SSP
usedma	If TRUE, uses DMA mode, not support DMA now
usepolling	If TRUE, uses polling mode, only support polling mode now
bitcount	Define bits used in a single XCH, range 1-32.
bRead	If TRUE, read data from CSPI
bCmd	If TRUE, send command 0 and command 1 to CSPI controller
usedma	If TRUE, uses DMA mode
usepolling	If TRUE, uses polling mode

7.5.3.2 CSPI_XCH_PKT_T

This structure contains an XCH buffer parameters to be used in data exchange to CSPI device.

```
// CSPI exchange packet
```

```
typedef struct
{
    PCSPI_BUSCONFIG_T pBusCnfg;
    LPVOID pBuf;
    UINT32 xchCnt;
    LPWSTR xchEvent;
    UINT32 xchEventLength;
} CSPI_XCH_PKT_T, *PCSPI_XCH_PKT_T;
```

Table 7-3 shows the CSPI_XCH_PKT_T structure members.

Table 7-3. CSPI_XCH_PKT_T Structure Members

Member	Description
pBusCnfg	A pointer to CSPI bus configuration object
pBuf	A pointer to data buffer
xchCnt	Amount of XCH operation to SPI device
xchEvent	Asynchronous access using the internal exchange queue
xchEventLength	Event name length including tailing Zero

Chapter 8
Display Driver for LCDIF and PXP

The Windows Embedded CE 6.0 BSP display driver is based on the Microsoft DirectDraw Graphics Primitive Engine (DDGPE) classes, and supports the Microsoft DirectDraw interface. This driver combines the functionality of a standard LCD display with DirectDraw support. The display driver interfaces with the LCD Interface (LCDIF) and Pixel Pipeline (PXP).

The display driver supports the following display type:

- SEIKO 43WVF1G-0 WVGA Panel

8.1 Display Driver Summary

Table 8-1 identifies the source code location, library dependencies and other BSP information for the display driver.

Table 8-1. Display Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Common Path	..\PLATFORM\COMMON\SRC\SOC\COMMON_FSL_V2\LCDIF ..\PLATFORM\COMMON\SRC\SOC\COMMON_FSL_V2\PXP
SOC Specific Path	..\PLATFORM\COMMON\SRC\SOC\<*Target SoC*>\LCDIF ..\PLATFORM\COMMON\SRC\SOC\<*Target SoC*>\PXP
Platform Specific Path	..\PLATFORM\<*Target Platform*>\SRC\DRIVERS\DISPLAY ..\PLATFORM\<*Target Platform*>\SRC\DRIVERS\PXP
Driver DLL	ddraw_mx28.dll
Import Library	ddgpe.lib, gpe.lib
Catalog Items	Third Party > BSP > Freescale <*Target Platform*>: ARMV4I > Device Drivers > Display > 43WVF1G(WVGA)
SYSGEN Dependency	SYSGEN_DDRAW=1
BSP Environment Variables	BSP_NODISPLAY=

8.2 Supported Functionality

The display driver enables the EVK board to provide the following software and hardware support:

1. RGB565 user interface
2. DirectDraw Hardware Abstraction Layer (DDHAL)

3. One overlay surface
4. Video overlays containing image data in any of the following FOURCC pixel formats: RGB565, YV12
5. Hardware-accelerated color space conversion in video overlays
6. Hardware-accelerated image resizing in video overlays
7. Overlay surface color key feature
8. Alpha blending with an overlay surface
9. Two power management modes: full on and full off (resume and suspend)
10. Screen rotation
11. Cropping of an overlay surface
12. Supports SEIKO 43WVF1G-0 WVGA Panel

NOTE

The following limitations apply to the display driver overlay support.

13. RGB image resize is not supported
14. Cropping is not supported while performing alpha blending operation
15. The width and height of the overlay surface must conform to an 8-pixel alignment restriction
16. The minimum width (or height if screen is rotated) of an overlay surface is 8 pixels
17. The minimum height (or width if screen is rotated) of an overlay surface is 8 pixels
18. When using the cropping feature, the x and y coordinate position must conform to 8-pixel alignment restriction

8.3 Hardware Operation

For operation and programming information, refer to the chapter on the Pixel Pipeline and LCD Interface in the Reference Manual.

8.3.1 Conflicts with Other Peripherals and Catalog Items

No conflicts.

8.4 Software Operation

This section explains about the software operation of the display driver.

8.4.1 Software Driver Components

Figure 8-1 shows the block diagram explaining the relationship between the software components in the display driver architecture.

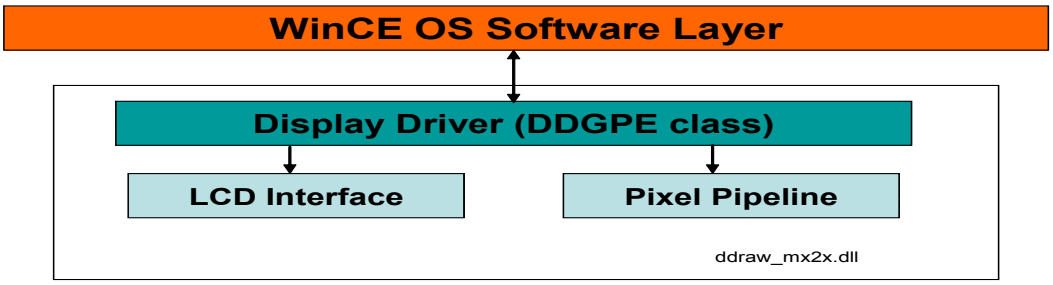

Figure 8-1. Software Driver Components Block Diagram

A list of the main elements of the display driver architecture is as follows:

- **Display Driver**—The high level DDGPE-based display driver. Contains implementations for DirectDraw APIs.
- **LCD Interface—**Set of functions provide access to LCDIF module for display control setting.
- **Pixel Pipeline Driver**—A stream interface driver that performs the following processing tasks: color space conversion, resizing, rotation, and combining.

8.4.1.1 Display Driver

The display driver is the top level interface between the display driver and the Windows CE OS or a calling application. This top level software component is composed of the DDLCDIF class, which is derived from the public DDGPE class and inherits the underlying GPE driver functionality. Graphics Device Interface (GDI) and DirectDraw APIs are implemented at this level.

8.4.1.2 LCD Interface

The LCDIF software component consists of a collection of functions that provide access to the LCDIF module registers. These functions are called from the display driver to implement the display control. The major tasks that this component performs include the following:

- Setting bus master and DMA operation modes for LCD.
- Configuring LCD data bus depending on the packet size.
- Programming timing and parameters to support a wide variety of displays.

8.4.1.3 Pixel Pipeline

The PXP driver provides a general resource that is capable of performing a set of processing tasks on a surface:

- Resizing
- Combining of video and graphics data

- Rotation
- Vertical and horizontal flipping
- Color Space Conversion (CSC)
- Cropping

The PXP driver is the primary means for performing resizing, rotation, CSC, cropping and combining on an overlay surface.

8.4.2 Communicating with the Display

Communication with the display driver is accomplished through Microsoft-defined APIs. A framework for accessing the display driver is provided through the Graphics Device Interface (GDI) and DirectDraw.

8.4.2.1 Using the GDI

The GDI provides basic controls for the display of text and graphics. For more information, see the Help in the following location:

Windows Embedded CE Features > Shell, GWES and User Interface > Graphics, Windowing and Events (GWES) > GWES Application Development > Graphics Device Interface (GDI)

8.4.2.2 Using DirectDraw

The DirectDraw API provides support for hardware-accelerated 2-D graphics, offering fast access to display hardware while retaining compatibility with the GDI. For information about the DirectDraw API, see the DirectDraw Help or the MSDN documentation library in the following location:

Windows Embedded CE Features > Graphics > DirectDraw

The following DirectDraw features are supported in the display driver by the PXP hardware:

- Page flipping with one backbuffer.
- Overlay surfaces using RGB or YV12 pixel format.
- Overlaying using a color key for the overlay surface for RGB colors.
- Stretching of overlay surfaces.

The PXP hardware module is used within the display driver to accelerate the following operations:

- Color space conversion of YUV overlay data to RGB. This conversion may be required in order to combine the overlay data with RGB graphics plane data before being displayed.
- Resizing of the overlay surface.
- Rotation of the overlay surface (used when the screen orientation is rotated).

8.4.2.3 Using Display Driver Escape Codes

In some cases, applications might need to communicate directly with a display driver. To make this possible, an escape code mechanism is provided as a part of the display driver.

For a detailed description of standard display driver escape codes, refer to the CE Help in the following location:

Developing a Device Driver > Windows Embedded CE Drivers > Display Drivers > Display Driver Development Concepts > Display Driver Escape Codes

8.4.3 Configuring the Display

The display configuration is based on the **GUID** registry key, which is described in Section 8.4.3.3, "Display Registry Settings." The **GUID** registry key indicates the display panel that is being used. The only one supported display panel is the SEIKO 43WVF1G-0 WVGA Panel.

8.4.3.1 Rotation Support

The DirectDraw display driver supports screen rotation.

NOTE

Due to lack of support for the co-existence of GDI screen rotation and DirectDraw, a DirectDraw display driver with rotation support may yield more failures in the GDI or DIRECTDRAW CETK test suite. It is recommended to run these CETK tests under 0 rotation degree. See the Windows CE Help, stating that GDI screen rotation cannot be used with DirectDraw.

8.4.3.2 Display Driver Blit Acceleration

On-chip Data Co-Processor (DCP) may be accessed through the display driver to accelerate a very limited subset of the GDI graphical blit operations. The subsequent sections provide details on the features offered by the DCP, and how to configure the BSP to enable acceleration through DCP.

8.4.3.2.1 DCP Graphics Acceleration

DCP graphics acceleration may be enabled by setting the platform environment variable BSP_DISPLAY_DCP=1. This may be achieved by navigating to the project properties, and adding the environment variable in the Configuration Properties->Environment window.

8.4.3.2.2 Supported Acceleration Features

1. Solid color fills.
2. ROP operation BLACKNESS.
3. ROP operation WHITENESS.
4. ROP operation SRCCOPY.

8.4.3.2.3 Hardware Restrictions

- DCP cannot support any rotation and resize case.
- DCP cannot support any alpha operation.

- DCP can only support 16BPP and 32BPP.
- While pixel format is 16BPP, DCP can only support destination surface whose width is a multiple of 2 in Solid color fills, BLACKNESS and WHITENESS ROP operation case.
- Source surface stride must be equal to source rectangle width for the ROP operation SRCCOPY case DCP supports.
- While using DCP for ROP operation SRCCOPY acceleration, source surface pixel format must be equal to destination surface pixel format.

8.4.3.2.4 Acceleration performance

Compared to software operation, performance benefit can only be gained while using DCP to process big block blit operations. In general, while block size is larger than 51200 bytes in Solid color fills, BLACKNESS and WHITENESS operation, DCP has better performance than software. For SRCCOPY case, the threshold could be 115200 bytes.

8.4.3.3 Display Registry Settings

A set of registry keys is included in the OS image, depending on the display panel catalog item included in the OS design.

8.4.3.3.1 i.MX28 Registry Settings

If the SEIKO 43WVF1G-0 WVGA panel is selected, the following registry keys are included:

```
[HKEY_LOCAL_MACHINE\System\GDI\Drivers]
"GUID"="{83A0FF68-78BB-4DF5-8DEB-077961EE75BC}";
"Bpp"=dword:10                              ; RGB565
"VideoMemSize"=dword:600000                 ; 6MB
"Alignment"=dword:8                         ;
```

The **Alignment** registry key indicates boundary restrictions and size restrictions of the source and destination rectangles used to display overlay surfaces according to PXP module hardware limitations. Both types of restrictions are expressed in terms of pixels (not bytes) and can apply to the source and destination rectangles.

For i.MX28, the **Alignment** registry key can be set to 0x8 or 0x10.

8.4.4 Power Management

The display driver implements the power management I/O Control (IOCTL) codes, such as IOCTL_POWER_CAPABILITIES, IOCTL_POWER_QUERY, IOCTL_POWER_GET and IOCTL_POWER_SET.

8.4.4.1 PowerUp

This function is implemented in the PXP driver. It enables clock gating with the PXP module and resets the PXP module to its default state. If an PXP operation is previously terminated by calling the `PowerDown()` API, the `PowerUp()` function restores the PXP module registers and restarts the PXP operation.

8.4.4.2 PowerDown

This function is implemented in the PXP driver. If the `PowerDown()` function is called while PXP operations are going on, it stores current PXP module registers setting temporarily. Then it disables clock gating with the PXP module and holds the PXP module in its reset (lower power) state.

8.4.4.3 IOCTL_POWER_SET

The display driver implements the IOCTL_POWER_SET IOCTL API with support for the D0 (Full On) and D4 (Off) power states. These states are handled in the following manner:

- D0—The LCDIF module is enabled. The display panel is enabled. Clock gating is enabled for clocks to the LCDIF.
- D4—The LCDIF module is disabled. The display panel is disabled. Clock gating is disabled for clocks to the LCDIF.

8.5 Unit Test

The display driver is subject to two test suites provided with the Windows CE Test Kit (CETK): the GDI Test and the DirectDraw Test. Additionally, the video playback is verified using the Windows Media Player application.

The GDI Test is designed to test a graphics device interface. This test verifies that basic shapes, including rectangles, triangles, circles, and ellipses, are drawn correctly. The test also examines the color palette of the display, verifies that the display is correctly divided into multiple regions, and tests whether a device context can be properly created, stored, retrieved, and destroyed.

The DirectDraw Test analyzes basic DirectDraw functionality including block image transfers (blits), scaling, color keying, color filling, flipping, and overlaying.

Windows Media Player may be used to play back WMV video files and visually verify correct operation of video overlays, accelerated color space conversion, and accelerated image resizing.

8.5.1 Unit Test Hardware

The SEIKO 43WVF1G-0 WVGA panel is needed to run the GDI and DirectDraw tests. The panel displays the graphics data.

8.5.2 Unit Test Software

This section explains about the software required for different tests.

8.5.2.1 GDI Tests

Table 8-2 lists the software required to run the GDI tests.

Table 8-2. GDI Software Requirements

Requirement	Description
Tux.exe	Tux test harness, which is needed for executing the test
Kato.dll	Kato logging engine, which is required for logging test data
Tooltalk.dll	Library required by Tux.exe and Kato.dll. Handles the transport between the target device and the development workstation
Gdiapi.dll	Main test.dll file
Ddi_test.dll	Graphics Primitive Engine (GPE)–based display driver that the GDI API uses to verify the success of each test case. If Ddi_test.dll is unavailable, run the test with manual verification

8.5.2.2 DirectDraw Tests

Table 8-3 lists the software required to run the DirectDraw tests.

Table 8-3. DirectDraw Software Requirements

Requirement	Description
Tux.exe	Tux test harness, which is needed for executing the test
Kato.dll	Kato logging engine, which is required for logging test data
Tooltalk.dll	Library required by Tux.exe and Kato.dll. Handles the transport between the target device and the development workstation
DDrawTK.dll	Test.dll file

8.5.2.3 Windows Media Player Tests

Table 8-4 lists the software required to perform WMV playback with Windows Media Player.

Table 8-4. Windows Media Player Software Requirements

Requirement	Description
Ceplayer.exe	Windows Media Player sample application
*.wmv sample video files	Sample windows media files

8.5.3 Building the Unit Tests

The GDI and DirectDraw tests come pre-built as part of the CETK. Ensure that the latest CETK suite is installed. No steps are required to build these tests. For information about the tests, see the Help at the following location:

Windows Embedded CE Test Kit > Running the CETK

For Windows Media Player testing, there are no build steps required. The Windows Media Player catalog item must be added to the OS image to ensure that `ceplayer.exe` is included in the image. Additionally, sample WMV files must be included in the image to demonstrate playback.

8.5.4 Running the Unit Tests

This section explains how to run different types of tests.

8.5.4.1 Running the GDI Tests

The command for running the GDI tests is:

```
tux –o –d gdiapi.dll -c "/NoResize"
```

For information about the GDI tests and command line options, see the Platform Builder Help topic:

Windows Embedded CE Test Kit > CETK Tests and Test Tools > CETK Tests > Display Tests > Graphics Device Interface Test

8.5.4.2 Running the DirectDraw Tests

The command for running the DirectDraw tests is:

```
tux –o –d ddrawtk
```

NOTE

The display driver fails the following DirectDraw CETK test cases: 1240, 1340. The failure occurs because the hardware can not support RGB image resize, and the failing tests perform RGB pixel format overlay surfaces resize that violate this restriction.

8.5.4.3 Running the Windows Media Player tests

The command for starting playback of a WMV test video clip in Windows Media Player is:

```
ceplayer [wmv test file]
```

For example, `ceplayer motocross_208x160_30fps.wmv`

If audio support is not included in the current BSP, the message **Audio hardware is missing or disabled** appears when the WMV file is being loaded. Click **OK** to continue to WMV playback.

To confirm the correct operation of this test, observe the application and verify whether the video clip have a clear image, normal coloring, and correct image sizing.

8.6 Display Driver API Reference

For information about the display driver APIs, see CE Help. No additional custom API information is required for the features currently supported in the display driver.

For reference information on basic display driver functions, methods, and structures, see the CE Help at the following location:

Developing a Device Driver > Windows Embedded CE Drivers > Display Drivers > Display Driver Reference

For reference information on DirectDraw functions, callbacks, and structures, see the CE Help at the following location:

Windows Embedded CE Features > Graphics > DirectDraw

Chapter 9
Dynamic Voltage and Frequency Control (DVFC) Driver

The BSP includes the DVFC driver that provides combined support for DVFS (Dynamic Voltage Frequency Scaling). The DVFC driver plays an important role in the reduction of active power consumption by dynamically adjusting the voltage and frequency settings of the system. The DVFC driver responds to DVFC hardware logic or load tracking software that is monitoring CPU loading and process/temperature performance of the silicon.

9.1 DVFC Driver Summary

Table 9-1 provides a summary of source code location, library dependencies, and other BSP information.

Table 9-1. DVFC Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Common Path	..\PLATFORM\COMMON\SRC\SOC\COMMON_FSL_V2PDK1_9\DVFC
SOC Specific Path	N/A
Platform Specific Path	..\PLATFORM\<*Target Platform*>\SRC\DRIVERS\DVFC
Driver DLL	dvfc.dll
SDK Library	N/A
Catalog Item	Third Party > BSP > Freescale <*Target Platform*>: ARMV4I > Device Drivers > DVFC driver
SYSGEN Dependency	N/A
BSP Environment Variables	BSP_DVFC = 1

9.2 Supported Functionality

The DVFC driver enables the hardware platform to provide the following software and hardware support:

1. Executes as a device driver and provides synchronized support of the DVFS power management feature.
2. Exposes stream interface for initialization and power management.
3. Supports D0 and D4 driver power states and support control of frequency or voltage setpoint based on Power Manager device power states.
4. Supports peripheral setpoint requests initiated by CSPDDK clock management code.

9.2.1 i.MX28 Supported Functionality

1. Supports DVFS for CPU, AHB and DDR frequency change.
2. Supports reactive CPU load tracking to control setpoint based on system performance requirements. Current release uses software load tracking algorithm.
3. Provides voltage control using PMU.

9.3 Hardware Operation

This section describes about the DVFC hardware operation.

9.3.1 Conflicts with Other Peripherals and Catalog Items

No conflicts.

9.3.2 i.MX28 EVK Configuration

The DVFC driver is dependent on the PMU interface to adjust voltage.

9.4 Software Operation

This section describes about the registry settings.

9.4.1 i.MX28 Registry Settings

The following registry keys are required to load the i.MX28 DVFC module.

```
;-------------------------------------------------------------------------------
; DVFC Driver
;
IF BSP_DVFC
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\DVFC]
   "Prefix" = "DVF"
   "Index" = dword:1
   "Dll"="dvfc.dll"
   "IClass"="{A32942B7-920C-486b-B0E6-92A702A99B35}"    ; PMCLASS_GENERIC_DEVICE
ENDIF ;BSP_DVFC
```

9.4.2 Loading and Initialization

The DVFC driver is automatically loaded to kernel space by the Device Manager as a stream driver. As part of the loading procedure of stream drivers, the device manager invokes the corresponding stream initialization function exported by the DVFC driver. The initialization sequence includes a call to platform-specific code `(BSPDvfcInit)` to allow the OEM to configure and tune the DVFC driver operation.

9.4.3 Operation

The DVFC driver is the central point in the BSP for controlling voltage and frequency scaling. The DVFC communicates with the PMIC and CCM to coordinate the DVFS. The DVFC driver responds to setpoint

requests from DDK_CLK (by driver calling **DDKClockSetGatingMode**) and Power Manager (by **IOCTL_POWER_SET**). A shared global data structure (**DDK_CLK_CONFIG**) is used to keep track of reference counts for each setpoint. The DVFC relies on synchronization with the DDK_CLK component to determine when it is safe to transition to a new setpoint. DVFC integration with the Power Manager allows drivers and applications direct control of the setpoint by using the **SetDevicePower** API.

9.4.3.1 i.MX28 Voltage or Frequency Setpoints

The i.MX28 DVFC driver supports mutually exclusive voltage and frequency setpoints for the CPU power domains. Table 9-2 provides the voltage/frequency characteristics for these setpoints.

Table 9-2. i.MX28 DVFC Setpoints

Setpoint Name	CPU/AHB/DDR Frequency [MHz]	VDDD Voltage
DDK_DVFC_SETPOINT_HIGH	454/151/200	1.575 V
DDK_DVFC_SETPOINT_MEDIUM	297/148/200	1.150 V
DDK_DVFC_SETPOINT_LOW	261/130/166	1.100 V

The setpoint attributes are controlled by the definitions in the platform-specific DVFS header file (found in `\PLATFORM\<Target Platform>\SRC\INC\dvfs.h`). The DVFC driver uses these definitions to populate a global setpoint array (g_SetPointConfig) that is referenced during setpoint transitions.

9.4.3.2 i.MX28 Setpoint Mapping

N/A

9.4.4 DDK Interface

The DVFC driver allows other drivers or applications to control some aspects of the DVFS operation. Due to the tight coupling with the system clock configuration, this interface is exposed within CSPDDK clocking support. See the CSPDDK documentation for the following functions:

- DDKClockSetpointRequest, Section 6.5.1.2.6, “DDKClockSetpointRequest.”
- DDKClockSetpointRelease, Section 6.5.1.2.7, “DDKClockSetpointRelease.”

9.4.5 Power Management

The DVFC is an integral part of the power management supported by the BSP. However, as the DVFC runs as a driver on the system, it also supports the Power Manager device driver interface. This allows the DVFC driver to be notified of when the system is suspending or resuming and configure the processor performance accordingly.

9.4.5.1 PowerUp

This stream interface function is not implemented for the DVFC driver.

9.4.5.2 PowerDown

This stream interface function is not implemented for the DVFC driver.

9.4.5.3 IOCTL_POWER_CAPABILITIES

The DVFC driver advertises that D0–D4 device power states are supported.

9.4.5.4 IOCTL_POWER_SET

The DVFC driver supports requests to enter D0–D4 device power state.

9.4.5.5 IOCTL_POWER_GET

The DVFC driver reports the current device power state (D0, D1, D2 or D4).

9.5 Unit Test

This section explains about the unit testing.

9.5.1 i.MX28 Unit Testing

A stress test application for the DVFC driver is provided for unit testing. This stress test uses the Power Manager interface (**SetDevicePower**) to randomly request setpoints for the CPU and peripheral DVFS domains. Follow these steps to run this unit test.

1. Open <*Target Platform*>-Mobility workspace and add the DVFC driver catalog item. Build OS image.

   NOTE

   Note that modifications to the default workspace may cause additional drivers to be included and may prevent the system from transitioning through all possible DVFS setpoints.

2. Build DVFC stress test located in \SUPPORT\TEST\APP\PWRMGMT. The resulting application pwrmgmt.exe is generated in the flat release directory.
3. Boot the OS image and launch application code such as media player that can perform continuous playback. WMA audio playback is a good use case since audio playback can be performed across all supported setpoints.
4. Launch the stress test application. From the CE shell, the stress test can be launched with the following command line:

   ```
   s \release\pwrmgmt.exe
   ```

Board modifications are required to observe voltage setpoints and are not covered in this document. Debug messages to indicate setpoint transitions can be enabled using the DVFC_VERBOSE macro found in `\PLATFORM\<Target Platform>\SRC\DRIVERS\DVFC\dvfc.c`

Chapter 10
Ethernet MAC Controller (ENET) Driver

The Ethernet MAC driver is used for connectivity with an IEEE 802.3 Ethernet using the on-chip Ethernet MAC Controller. The driver provides support to communicate with the Ethernet at 10/100 Mbps, using a MII or RMII compatible interface and an external transceiver . The Ethernet MAC driver is NDIS 4.0 compliant miniport driver.

10.1 Ethernet MAC Driver Summary

Table 10-1 provides a summary of source code location, library dependencies and other BSP information.

Table 10-1. ENET Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	N/A
SOC Common Path	..\PLATFORM\COMMON\SRC\SOC\COMMON_FSL_V2\ENET
SOC Specific Path	N/A
Platform Specific Path	..\PLATFORM\<*Target Platform*>\SRC\DRIVERS\ENET
Driver DLL	enet.dll
SDK Library	N/A
Catalog Item	Third Party > BSP > Freescale <*Target Platform*>:ARMV4I > Device Drivers > ENET
SYSGEN Dependency	SYSGEN_NDIS=1 SYSGEN_TCPIP=1 SYSGEN_WINSOCK=1
BSP Environment Variables	BSP_ENET1= 1 BSP_ENET2= 1

10.2 Supported Functionality

The ENET driver enables the hardware platform to provide the following software and hardware support:

1. Compliant with the NDIS 4.0 miniport driver
2. 10/100 Mbps network
3. MII PHY or RMII PHY
4. IEEE 1588 function demo

10.3 Hardware Operations

The Ethernet MAC Controller connects with the external transceivers using standard Media Independent Interface (MII) connection. All the registers in the external transceivers can be accessed by the MII compatible management frames. The interrupt signal from the external transceiver is connected to the processor through the Peripheral Bus Controller (PBC). Refer to the Peripheral Bus Controller document for detailed operation and programming information. The attached transceiver for the Ethernet MAC Controller can detect the speed of the ethernet network automatically by the auto-negotiation process. The software accesses the status register of attached transceiver to determine the speed of the ethernet network (10 Mbps or 100 Mbps).

The Ethernet MAC Controller connects with the external transceiver using standard RMII (Reduced Media Independent Interface) connection. All the registers in the external transceiver (LAN8720) can be accessed by the RMII compatible management frames. The attached transceiver for the Fast Ethernet Controller can detect the speed of the ethernet network automatically by the auto-negotiation process. The software accesses the status register of attached transceiver to determine the speed of the ethernet network (10 Mbps or 100 Mbps).

The programmable 10/100 Ethernet MAC with IEEE 1588 support integrates a standard IEEE 802.3 Ethernet MAC with a time stamping module to support Ethernet applications requiring precise timing references for incoming and outgoing frames to implement a distributed time synchronization protocol-such as the IEEE 1588.

10.3.1 Conflicts with Other Peripherals and Catalog Items

This section lists the conflicts with other peripherals and catalog items.

10.3.1.1 Conflicts with SoC Peripherals

No conflicts.

10.3.1.2 Conflicts with i.MX28 EVK Peripherals

No conflicts.

10.4 Software Operations

The Ethernet MAC driver follows the Microsoft-recommended architecture for NDIS miniport drivers. The details can be found in the Platform Builder Help at the following location:

Developing a Device Driver > **Windows Embedded CE Drivers** > **Network Drivers** > **Network Driver Development Concepts** > **Miniports, Intermediate Drivers, and Protocol Drivers**.

10.4.1 ENET Driver Registry Settings

The following register keys are required to properly load the Ethernet MAC driver and to configure the TCP/IP for Ethernet interface. To enable dynamic IP address assignment using DHCP, the variable EnableDHCP should be set to 1.

```
IF BSP_ENET1
[HKEY_LOCAL_MACHINE\Comm\1ENET]
   "DisplayName"="ENET Ethernet Driver"
   "Group"="NDIS"
   "ImagePath"="enet.dll"
    "Index"=dword:0

[HKEY_LOCAL_MACHINE\Comm\1ENET\Linkage]
   "Route"=multi_sz:"ENET1"

[HKEY_LOCAL_MACHINE\Comm\ENET1]
   "DisplayName"="ENET Ethernet Driver"
   "Group"="NDIS"
   "ImagePath"="enet.dll"

[HKEY_LOCAL_MACHINE\Comm\ENET1\Parms]
   "BusNumber"=dword:0
   "BusType"=dword:0
   ; DuplexMode: 0:AutoDetect; 1:HalfDuplex; 2:FullDuplex.
   "DuplexMode"=dword:0
   ; The Ethernet Physical Address. For example,
   ; Ethernet Address 00:24:20:10:bf:03 is MACAddress1=0024,
   ; MACAddress2=2010,and MACAddress3=bf03.
   "MACAddress1"=dword:1213
   "MACAddress2"=dword:1728
   "MACAddress3"=dword:3120

[HKEY_LOCAL_MACHINE\Comm\ENET1\Parms\TcpIp]
   ; This should be MULTI_SZ
   "DefaultGateway"=""
   ; This should be SZ... If null it means use LAN, else WAN and Interface.
   "LLInterface"=""
   ; Use zero for broadcast address? (or 255.255.255.255)
   "UseZeroBroadcast"=dword:0
   ; Thus should be MULTI_SZ, the IP address list
   "IpAddress"="0.0.0.0"
   ; This should be MULTI_SZ, the subnet masks for the above IP addresses
   "Subnetmask"="0.0.0.0"
   "EnableDHCP"=dword:1

[HKEY_LOCAL_MACHINE\Comm\TcpIp\Parms]

   ;Set to True to keep the device from entering idle mode if there's network adapter
    ;;"NoIdleIfAdapter"=dword:1
    ;Set to True to keep the device from entering idle mode while communicating/loop back
    "NoIdleIfConnected"=dword:1

[HKEY_LOCAL_MACHINE\Comm\Tcpip\Linkage]
   ; This should be MULTI_SZ
   ; This is the list of llip drivers to load
   "Bind"=multi_sz:"ENET1"
ENDIF ;  BSP_ENET1
IF BSP_ENET2
[HKEY_LOCAL_MACHINE\Comm\2ENET]
   "DisplayName"="ENET Ethernet Driver"
   "Group"="NDIS"
```

```
   "ImagePath"="enet.dll"
   "Index"=dword:1

[HKEY_LOCAL_MACHINE\Comm\2ENET\Linkage]
   "Route"=multi_sz:"ENET2"

[HKEY_LOCAL_MACHINE\Comm\ENET2]
   "DisplayName"="ENET Ethernet Driver"
   "Group"="NDIS"
   "ImagePath"="enet.dll"

[HKEY_LOCAL_MACHINE\Comm\ENET2\Parms]
   "BusNumber"=dword:0
   "BusType"=dword:0
   ; DuplexMode: 0:AutoDetect; 1:HalfDuplex; 2:FullDuplex.
   "DuplexMode"=dword:0
   ; The Ethernet Physical Address. For example,
   ; Ethernet Address 00:24:20:10:bf:03 is MACAddress1=0024,
   ; MACAddress2=2010,and MACAddress3=bf03.
   "MACAddress1"=dword:1213
   "MACAddress2"=dword:1728
   "MACAddress3"=dword:4567

[HKEY_LOCAL_MACHINE\Comm\ENET2\Parms\TcpIp]
   ; This should be MULTI_SZ
   "DefaultGateway"=""
   ; This should be SZ... If null it means use LAN, else WAN and Interface.
   "LLInterface"=""
   ; Use zero for broadcast address? (or 255.255.255.255)
   "UseZeroBroadcast"=dword:0
   ; Thus should be MULTI_SZ, the IP address list
   "IpAddress"="0.0.0.0"
   ; This should be MULTI_SZ, the subnet masks for the above IP addresses
   "Subnetmask"="0.0.0.0"
   "EnableDHCP"=dword:1

[HKEY_LOCAL_MACHINE\Comm\TcpIp\Parms]
   ;Set to True to keep the device from entering idle mode if there's network adapter
    ;;"NoIdleIfAdapter"=dword:1
    ;Set to True to keep the device from entering idle mode while communicating/loop back
     "NoIdleIfConnected"=dword:1

[HKEY_LOCAL_MACHINE\Comm\Tcpip\Linkage]
   ; This should be MULTI_SZ
   ; This is the list of llip drivers to load
   "Bind"=multi_sz:"ENET2"

ENDIF ;  BSP_ENET2
```

10.4.2 IEEE 1588 Features

This section explains the IEEE 1588 interrelated OIDS functions.

10.4.2.1 OID_GET_XMIT_TIMER

This function is the timestamp of the transmited packet with specific PTP sequence ID and returns the timestamp(second and nonsecond) .

10.4.2.2 OID_GET_RCV_TIMER

This function is the timestamp of the received packet with specific PTP sequence ID and returns the timestamp(sencond and nonsecond) .

10.4.2.3 OID_UPDATE_NEW_TIMER

This function updates the new PTP timer (second and nonsecond) for 1588 demo.

10.4.2.4 IEEE1588 Software Features

Ethernet IEEE1588 demo application support the following PTPV2 frame message:

- Sync Message
- Follow-Up Message
- Delay-Request Message
- Delay-Response Message

Figure 10-1 shows the IEEE 1588 Timer Sync flow chart.

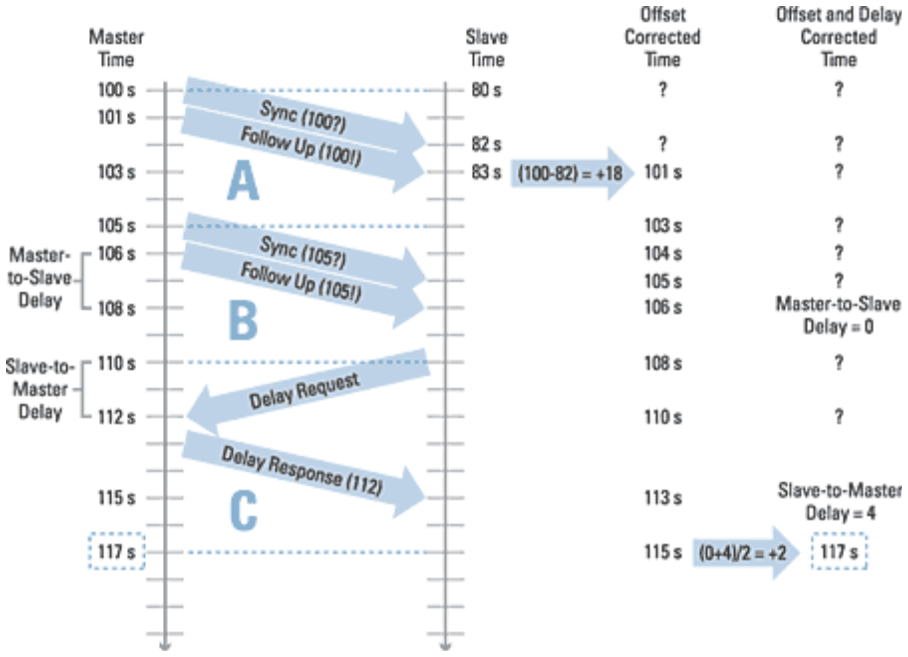

Figure 10-1. IEEE 1588 Timer Sync Flow Chart

10.5 Unit Tests

The Ethernet MAC driver is tested using the following:

- Network utilities/operations
  - Ping to and from the tested device
  - FTP transfers (file put and get) with tested device as FTP server
  - Internet browsing with Pocket Internet Explorer on the tested device
- Winsock CETK test cases
  - Winsock 2.0 Test (v4/v6)
  - Winsock Performance Test with tested device as client.

10.5.1 Unit Test Hardware

Table 10-2 lists the required hardware to run the unit tests.

Table 10-2. Hardware Requirements

Requirement	Description
HW Platform System	—
PC/machine	Counterpart for network operation
An Ethernet or a cross Ethernet cable	To and from an Ethernet

10.5.2 Unit Test Software

Table 10-3 lists the required software to run the unit tests.

Table 10-3. Software Requirements

Requirement	Description
Tux.exe	Tux test harness, which is needed for executing the test
Kato.dll	Kato logging engine, which is required for logging test data
Tooltalk.dll	Library required by Tux.exe and Kato.dll. Handles the transport between the target device and the development workstation
Ws2bvt.dll	Test .dll file for Winsock 2.0 Test (v4/v6)
Perflog.dll	Module that contains functions that monitor and log performance for Winsock Performance Test
Perf_winsock2.dll	Test .dll file for Winsock Performance Test
Perf_winsockd2.exe	Test .exe file (server program) for Winsock Performance Test
Ndt.dll	Protocol driver for One-card network card miniport driver test
Ndt_1c.dll	Test .dll for One-card network card miniport driver test
Ndt_2c.dll	Test .dll for Two-card network card miniport driver test
Ndp.dll	MS_NDP protocol driver for NDIS performance test

Table 10-3. Software Requirements (continued)

Perf_ndis.dll	Test .dll file NDIS performance test
master.exe	IEEE1588 master application demo exe file.
slave.exe	IEEE1588 slave application demo exe file.

10.5.3 Building the Unit Tests

This section explains how to build various unit tests.

10.5.3.1 Network Utilities Related Tests

- To include the ping utilities, the SYSGEN_NETUTILS = 1 needs to be set. Under **Catalog** > **Core OS** > **CEBASE** > **Communication Services and Networking** > **Networking General** > **Network Utilities**, IpConfig, Ping, and Route should be included in the OS design.
- To include FTP, SYSGEN_FTPD = 1 needs to be set. **Catalog** > **Core OS** > **CEBASE** > **Communication Services and Networking** > **Servers** > **FTP Server** should be included in the OS design.
- The following registry entry needs to be added to reg to allow get and put of files using the anonymous FTP login:

```
[HKEY_LOCAL_MACHINE\COMM\FTPD]
"AllowAnonymousUpload" = dword:1
```

10.5.3.2 Winsock 2.0 Test (v4/v6)

The Winsock 2.0 Test (v4/v6) comes pre-built as part of the CETK. No steps are required to build these tests. The `Ws2bvt.dll` file can be found alongside the other required CETK files in the following location:

```
[Drive]:\Program Files\Microsoft Platform Builder\6.00\cepb\wcetk\ddtk\armv4I
```

10.5.3.3 IEEE1588 Demo Applications

To build the IEEE1588 tests, build an OS image for the desired configuration using these steps:

1. Within the Platform Builder, choose **Build OS** > **Open Release Directory**.
   A DOS prompt is displayed.
2. Change to the 1588 Tests directory: `\WINCE600\SUPPORT\TEST\1588`
3. Enter **set WINCEREL=1** on the command prompt and press return.
   This copies the file to the flat release directory.
4. Input **build -c** to build the 1588 test.

After the build completes, the Master.exe and Slave.exe file is located in the $(_FLATRELEASEDIR) directory.

10.5.3.4 Winsock Performance Test

The Winsock Performance Test comes pre-built as part of the CETK. No steps are required to build these tests. The `Perf_winsock2.dll` and `Perf_winsockd2.exe` files can be found alongside the other required CETK files in the following location:

`Perf_winsock2.dll` in:

```
[Drive]:\Program Files\Microsoft Platform Builder\6.00\cepb\wcetk\ddtk\armv4I
```

`Perf_winsockd2.exe` in:

```
[Drive]:\Program Files\Microsoft Platform Builder\6.00\cepb\wcetk\ddtk\desktop
```

10.5.3.5 One-Card Network Card Miniport Driver Test

The One-card network card miniport driver test comes pre-built as part of the CETK. No steps are required to build these tests. The `ndt.dll` and `ndt_1c.dll` files can be found alongside the other required CETK files in the following location:

```
[Drive]:\Program Files\Microsoft Platform Builder\6.00\cepb\wcetk\ddtk\armv4I
```

10.5.3.6 Two-Card Network Card Miniport Driver Test

The Two-card network card miniport driver test comes pre-built as part of the CETK. No steps are required to build these tests. The `ndt.dll` and `ndt_2c.dll` files can be found alongside the other required CETK files in the following location:

```
[Drive]:\Program Files\Microsoft Platform Builder\6.00\cepb\wcetk\ddtk\armv4I
```

10.5.3.7 NDIS Performance Test

The NDIS performance test comes pre-built as part of the CETK. No steps are required to build these tests. The `ndp.dll` and `perf_ndis.dll` files can be found alongside the other required CETK files in the following location:

```
[Drive]:\Program Files\Microsoft Platform Builder\6.00\cepb\wcetk\ddtk\armv4I
```

10.5.4 Running the Unit Tests

This section explains how to run various network related unit tests.

Network Utilities Related Tests

10.5.4.1 Ping Tests

The ping tests can be run as usual from the tested device as well as from the PC side.

10.5.4.2 Browsing

The network browsing tests can be done after setting the following on the device front panel:

DNS servers in the TCP/IP properties of Fast Ethernet network interface (Control Panel Network and Dial-up Connections) Proxy server, if used in the test network on the Pocket Internet explorer.

10.5.4.3 FTP Tests

For running FTP tests, the FTP service needs to be started on the tested device using the following command on the DOS prompt:

```
services start FTP0:
```

10.5.4.4 Winsock 2.0 Test (v4/v6)

The test can be executed by using

```
tux –o –d Ws2bvt.dl
```

in the command line on the tested device. For detailed information on the Winsock 2.0 Test (v4/v6) tests, see the Platform Builder Help:

Windows Embedded CE Test Kit > **CETK Test and Test Tools** > **CETK Tests** > **Ethernet Tests** > **Tests Winsock 2.0 Test(v4/v6).**

10.5.4.5 Winsock Performance Test

Start the server on the PC by typing

```
Perf_winsockd2 - install
```

at the command line. Then client side test executes on the second device by using

```
tux –o –d Perf_winsock2.dll –c "-s 10.193.101.41"
```

in the command line on the tested target device, where 10.193.101.41 denotes PC IP address and needs to be replaced appropriately. For detailed information on the Winsock Performance tests, see the Platform Builder Help:

Windows Embedded CE Test Kit > **CETK Test and Test Tools** > **CETK Tests** > **Performance Test** > **Wisock Performance Test**.

NOTE

Cases 1007 and 1008 fail. This is a known MSFT CETK issue.

10.5.4.6 One-Card Network Card Miniport Driver Test

This test can be done by including `ndt.dll` and `ndt_1c.dll` in the image, and starting the test by entering

```
tux –o –d ndt_1c.dll –c "-t ENET1"
tux –o –d ndt_1c.dll –c "-t ENET2"
```

on the command line on the tested target device. For detailed information on the Winsock Performance tests, see the Platform Builder Help:

Windows Embedded CE Test Kit > **CETK Test and Test Tools** > **CETK Tests** > **Ethernet Tests** > **One-card Network Card Miniport Driver Test**.

10.5.4.7 Two-Card Network Card Miniport Driver Test

This test can be done by including `ndt.dll` and `ndt_2c.dll` in the image, and starting the test by entering

```
tux -o -d ndt_2c -c "-t ENET1 -s ENET2"
```

on the command line on the tested target device. For detailed information on the Winsock Performance tests, see the Platform Builder Help:

Windows Embedded CE Test Kit > **CETK Test and Test Tools** > **CETK Tests** > **Ethernet Tests** > **Two-card Network Card Miniport Driver Test**.

10.5.4.8 NDIS Performance Test

This test can be done by including `ndp.dll` and `perf_ndis.dll` in the image, and starting the test by entering

```
tux –o –d perf_ndis.dll –c “ENET1”
tux –o –d perf_ndis.dll –c “ENET2”
```

on the command line on the tested target device. For detailed information on the Winsock Performance tests, see the Platform Builder Help:

Windows Embedded CE Test Kit > **CETK Test and Test Tools** > **CETK Tests** > **Performance Test** > **NDIS Performance Test**.

10.5.4.9 IEEE1588 Demo Test

On the master demo board, run the **master.exe** and on the slave board, run **slave.exe**.

10.6 Ethernet ENET Driver API Reference

The Fast Ethernet driver conforms to NDIS 4.0 specification by Microsoft for the miniport network drivers. For reference information on basic NDIS driver functions, methods, and structures, refer to the CE Help:

Developing a Device Driver > **Windows Embedded CE Drivers** > **Network Drivers** > **Network Driver Reference**.

Chapter 11
Inter-Integrated Circuit (I^2C) Driver

The Inter-Integrated Circuit (I^2C) module provides the functionality of a standard I^2C master. The I^2C module is designed to be compatible with the standard Phillips I^2C bus protocol.

11.1 I^2C Driver Summary

Table 11-1 provides a summary of source code location, library dependencies and other BSP information.

Table 11-1. I^2C Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Common Path	..\PLATFORM\COMMON\SRC\SOC\iMX28_FSL_V2_PDK1_9\I2C
SOC Specific Path	..\PLATFORM\COMMON\SRC\SOC\<*Target SOC*>\I2C
Platform Driver Path	..\PLATFORM*Target Platform*>\SRC\DRIVERS\I2C
Import Library	N/A
Driver DLL	i2csdk.dll i2c.dll
Catalog Item	Third Party > BSP > Freescale <TGTPLAT> > Device Drivers > I2CBus
SYSGEN Dependency	N/A
BSP Environment Variables	BSP_I2CBUS1=1 or BSP_I2CBUS2=1

11.2 Supported Functionality

The I^2C driver supports the following features:

1. I^2C communication protocol
2. I^2C master mode of operation
3. Stream interface

11.3 Hardware Operation

The i.MX28 I^2C block has its own dedicated DMA channel in the APBX controller. DMA is used exclusively to transfer data to and from the bus as PIO mode is not fully supported in hardware.

11.3.1 Conflicts with Other Peripherals and Catalog Items

The following section explains about the conflicts that the I^2C driver have with other peripherals and catalog items:

11.3.1.1 Conflicts with SoC Peripherals

No conflicts.

11.3.1.2 Conflicts with Board Peripherals

No conflicts.

11.4 Software Operation

Only master mode is implemented in the driver; slave functions are stubbed out. As mentioned above, PIO mode is not fully supported in hardware so only DMA mode is implemented in the driver. The driver allocates its own DMA buffers for the data transfer. The calling application is expected to setup the data buffer with the slave address (7-bit or 10-bit) as part of the data to be sent in the format required by the slave device.

The I^2C APIs should be used to perform any operation on or using the I^2C module. Any array of packets to be transferred to or from the I^2C bus finish to completion without preemption by another request to transfer data.

11.4.1 Registry Settings

This section explains about the registry settings for the I^2C driver.

The following is the registry key to load the I^2C.

11.4.1.1 i.MX28 Registry Settings

The following is the registry key to load the I^2C.

```
IF BSP_I2CBUS1
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\I2C1]
   "Prefix"="I2C"
   "Dll"="i2c.dll"
   "Index"=dword:1
   "Order"=dword:3
ENDIF ; BSP_I2CBUS1
IF BSP_I2CBUS2
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\I2C2]
   "Prefix"="I2C"
   "Dll"="i2c.dll"
   "Index"=dword:2
   "Order"=dword:3
ENDIF ; BSP_I2CBUS1
```

11.4.2 Communicating with the I^2C

The I^2C is a stream interface driver, and is thus accessed through the file system APIs. To communicate using the I^2C, a handle to the device must first be created using the **CreateFile** function. Subsequent commands to the device are issued using the **DeviceIoControl** function with IOCTL codes specifying the desired operation. The following are the basic steps. The I^2C driver is provided to hide all the IOCTL calls from the calling application.

11.4.3 Creating a Handle

Call the **CreateFile** function to open a connection to the I^2C device. An I^2C port must be specified in this call. If an I^2C port does not exist, **CreateFile** returns ERROR_FILE_NOT_FOUND.

To open a handle to the I^2C:

1. Insert a colon after the I^2C port for the first parameter, *lpFileName*. For example, specify `I2C1:`.
2. Specify FILE_SHARE_READ | FILE_SHARE_WRITE in the *dwShareMode* parameter. Multiple handles to an I^2C port are supported by the driver.
3. Specify OPEN_EXISTING in the *dwCreationDisposition* parameter. This flag is required.
4. Specify FILE_FLAG_RANDOM_ACCESS in the *dwFlagsAndAttributes* parameter.

Example 11-1shows how to open an I^2C port.

Example 11-1. Code to Open I^2C Port

```
// Open the I2C port.
hI2C = CreateFile (,                                    // name of device
                   GENERIC_READ | GENERIC_WRITE,        // access (read-write) mode
                   FILE_SHARE_READ | FILE_SHARE_WRITE,  // sharing mode
                   NULL,                                // security attributes (ignored)
                   OPEN_EXISTING,                       // creation disposition
                   FILE_FLAG_RANDOM_ACCESS,             // flags/attributes
                   NULL);                               // template file (ignored)
```

Before writing to or reading from an I^2C port, configure the port. When an application opens an I^2C port, it uses the default configuration settings, which might not be suitable for the device at the other end of the connection.

11.4.4 Configuring the I^2C

Configuring the I^2C port for communications involves two main operations:

- Setting the master mode
- Setting the I^2C clock rate

Before these actions can be taken, a handle to the I^2C port must already be opened. Each of these steps requires a call to the **DeviceIoControl** function. As parameters, the I^2C port handle, appropriate IOCTL code, and other input and output parameters are required. Use the helper APIs to correctly configure the port.

Example 11-2 shows the code to configure an I2C port:

Example 11-2. Code to Configure I2C Port

```
HANDLE hI2C = I2COpenHandle(_T("I2C1:"));

if (hI2C == INVALID_HANDLE_VALUE)
{
        ERRORMSG(1, (L"Unable to open handle to I2C block\r\n"));
        retVal = -1;
        goto exit;
}

if (!I2CSetMasterMode(hI2C))
{
        ERRORMSG(1, (L"Unable to set master mode\r\n"));
        retVal = -1;
        goto exit;
}

if (!I2CSet(hI2C, EEPROM_CLOCK_RATE))
{
        ERRORMSG(1, (L"Unable to set \r\n"));
        retVal = -1;
        goto exit;
}
```

11.4.5 Data Transfer Operations

The I2C driver provides one command, transfer, that facilitates performing both reads and writes through the I2C. The basic unit of data transfer in the I2C driver is the I2C_PACKET, which contains a buffer for reading or writing data and a flag that specifies whether the desired operation is a read or a write. An array of these packets makes up an I2C_TRANSFER_BLOCK object, which is required to perform a Transfer operation. The steps below detail the process of performing write and read operations through the I2C.

Before these actions can be taken, a handle to the I2C port must already be opened, and it should already be configured in the correct mode with the correct frequency.

To perform an I2C transfer:

1. Create an array of I2C_PACKET objects and initialize the fields of each packet as follows:
   a) Set the *byRW* field to I2C_RW_WRITE to specify that the I2C operation is a write, or I2C_RW_READ to specify that the I2C operation is a read.
   b) If *byRW* is set to I2C_RW_WRITE, create a buffer of bytes and fill it with the data to write to the slave device. Set the *pbyBuf* field to point to this buffer. If *byRW* is set to I2C_RW_READ, create a buffer of bytes to hold the data which is read from the slave device.
   c) Set the *wLen* field to the size, in bytes, of the read or write buffer. This indicates the number of bytes to write or read.
   d) Set the *lpiResult* field to point to an integer that holds the return value from the write operation.
2. Call the I2CTransfer SDK API to start the I2C transfer.

3. After calling the I2CTransfer function, check the *lpiResult* field if the function returned FALSE, to narrow down the type of error that occurred.

11.4.6 Closing the Handle

Call the **CloseHandle** function to close the handle to the I^2C after the transfer task is complete. **CloseHandle** has one parameter, which is the handle returned by the **CreateFile** function call that opened the I^2C port.

11.5 Unit Test

The following section explains about the hardware and software requirements for unit tests.

11.5.1 Unit Test Hardware

The unit tests are not supported for this release.

11.5.2 Unit Test Software

The unit tests are not supported for this release.

11.5.3 Building the Unit Tests

The unit tests are not supported for this release.

11.5.4 Running the Unit Tests

The unit tests are not supported for this release.

11.6 Hardware Limitations

The following is the hardware limitations:

PIO mode is not supported by the hardware; DMA mode is always used. Slave mode is not implemented.

11.7 I^2C Driver API Reference

This section explains about the reference to I^2C driver API.

11.7.1 I^2C Driver IOCTLS

This section contains descriptions of the I^2C I/O control codes (IOCTLs). These IOCTLs are used in calls to **DeviceIoControl** to issue commands to the I^2C device. Only relevant parameters for the IOCTL have a description provided.

11.7.1.1 I2C_IOCTL_GET_CLOCK_RATE

This **DeviceIoControl** request retrieves the clock rate

Parameters

lpOutBuffer Pointer to the divisor indexclock rate.

nOutBufferSize Size in bytes of the divisor indexclock rate

11.7.1.2 I2C_IOCTL_GET_SELF_ADDR

This **DeviceIoControl** request retrieves the address of the I^2C device. This macro is only meaningful if it is currently in Slave mode.

Parameters

lpOutBuffer Pointer to the current I^2C device address, valid range is [0x00–0x7F]

nOutBufferSize Size in bytes of the I^2C device address

11.7.1.3 I2C_IOCTL_IS_MASTER

This **DeviceIoControl** request determines whether the I^2C is currently in Master mode.

Parameters

lpOutBuffer Pointer to a BYTE that contains the return value from the Master mode inquiry: TRUE if currently in Master mode; FALSE if currently in Slave mode

nOutBufferSize Size in bytes of the return value, should be one byte

11.7.1.4 I2C_IOCTL_IS_SLAVE

This **DeviceIoControl** request determines whether the I^2C is currently in Slave mode.

Parameters

lpOutBuffer Pointer to a BYTE that contains the return value from the Slave mode inquiry: TRUE if currently in Slave mode; FALSE if currently in Master mode

nOutBufferSize Size in bytes of the return value, should be one byte

11.7.1.5 I2C_IOCTL_RESET

This **DeviceIoControl** request performs a hardware reset. The I^2C driver maintains all of the current information of the device, including all of the initialized addresses.

11.7.1.6 I2C_IOCTL_SET_CLOCK_RATE

This **DeviceIoControl** request initializes the I^2C device with the given clock rate.

Parameters

lpInBuffer Pointer to the clock rate divisor index.

nInBufferSize Size in bytes of the clock rate divisor index

11.7.1.7 I2C_IOCTL_SET_MASTER_MODE

This DeviceIoControl request sets the I^2C device to Master mode.

11.7.1.8 I2C_IOCTL_SET_SELF_ADDR

This DeviceIoControl request initializes the I^2C device with the given address.

Parameters

lpInBuffer	Pointer to the expected I^2C device address, valid range is [0x00–0x7F]
nInBufferSize	Size in bytes of the I^2C device address
Remarks	The device expects to respond when any master on the I^2C bus wishes to proceed with any transfer. This IOCTL has no effect if the I^2C device is in Master mode.

11.7.1.9 I2C_IOCTL_SET_SLAVE_MODE

This **DeviceIoControl** request sets the I^2C device to Slave mode.

11.7.1.10 I2C_IOCTL_TRANSFER

This **DeviceIoControl** request performs the transfer (read or write) of one or more packets of data to a target device. An I2C_TRANSFER_BLOCK object is expected, which contains an array of I2C_PACKET objects to be executed sequentially. All of the required information should be stored in the I2C_TRANSFER_BLOCK passed in the lpInBuffer field.

Parameters

lpInBuffer	Pointer to an I2C_TRANSFER_BLOCK structure containing a pointer to an array of I2C_PACKET objects specifying all of the information required to perform the requested Read and Write operations
nInBufferSize	Size in bytes of the I2C_TRANSFER_BLOCK

11.7.1.11 I2C_IOCTL_ENABLE_SLAVE

This **DeviceIoControl** request starts the I^2C device to work in slave mode.

11.7.1.12 I2C_IOCTL_DISABLE_SLAVE

This **DeviceIoControl** request stops the I^2C device to work in slave mode.

11.7.2 I^2C Driver SDK Encapsulation

This section explains about the functions that are involved in I^2C driver SDK encapsulation.

11.7.2.1 I2COpenHandle

This function retrieves the I^2C device handle.

```
HANDLE I2COpenHandle(
        LPCWSTR lpDevName);
```

Parameters

lpDevName The I^2C device name for retrieving handle from CreateFile()

Return Values Returns the handle for I^2C driver, returns INVALID_HANDLE_VALUE if failure

11.7.2.2 I2CCloseHandle

This function closes a handle of the I^2C stream driver.

```
BOOL I2CCloseHandle(
        HANDLE hDev);
```

Parameters

hDev The I^2C device handle retrieved from CreateFile()

Return Values Returns TRUE or FALSE; if the result is TRUE, the operation is successful

11.7.2.3 I2CSetSlaveMode

This function sets the I^2C device in slave mode. This function is for back compatibility. Use **I2CEnableSlave** instead.

```
BOOL I2CSetSlaveMode(
        HANDLE hDev);
```

Parameters

hDev I^2C device handle retrieved from CreateFile()

Return Values Returns TRUE or FALSE; if the result is TRUE, the operation is successful

11.7.2.4 I2CSetMasterMode

This function sets the I^2C device in master mode. This function is for back compatibility. The default setting of driver is master.

```
BOOL I2CSetMasterMode(
        HANDLE hDev);
```

Parameters

hDev I^2C device handle retrieved from CreateFile()

Return Values Returns TRUE or FALSE, if the result is TRUE, the operation is successful

11.7.2.5 I2CIsMaster

This function determines whether the I^2C is currently in Master mode. This function is for back compatibility.

```
BOOL I2CIsMaster(
        HANDLE hDev,
        PBOOL pbIsMaster);
```

Parameters

hDev	I^2C device handle retrieved from CreateFile()
pbIsMaster	TRUE if the I^2C device is in master mode
Return Values	Returns TRUE or FALSE, if the result is TRUE, the operation is successful

11.7.2.6 I2CIsSlave

This function determines whether the I^2C is currently in Slave mode.

```
BOOL I2CIsSlave(
        HANDLE hDev,
        PBOOL pbIsSlave);
```

Parameters

hDev	I^2C device handle retrieved from CreateFile()
pbIsSlave	TRUE if the I^2C device is in Slave mode
Return Values	Returns TRUE or FALSE. If the result is TRUE, the operation is successful

11.7.2.7 I2CGetClockRate

This function retrieves the clock rate.

```
BOOL I2CGetClockRate(
        HANDLE hDev,
        PWORD pwClkRate);
```

Parameters

hDev	I^2C device handle retrieved from CreateFile()
pwClkRate	Pointer of WORD variable that retrieves **Return Values**Returns TRUE or FALSE, if the result is TRUE, the operation is successful

11.7.2.8 I2CSetClockRate

This function initializes the I^2C device with the given clock rate.

```
BOOL I2CSetClockRate(
        HANDLE hDev,
        WORD wClkRate);
```

Parameters

hDev	I^2C device handle retrieved from CreateFile()
wClkRate	**Return Values**Returns TRUE or FALSE, if the result is TRUE, the operation is successful

11.7.2.9 I2CSetSelfAddr

This function initializes the I^2C device with the given address. The device is expected to respond when any master within the I^2C bus wish to proceed with any transfer.

```
BOOL I2CSetSelfAddr(
        HANDLE hDev,
```

```
        BYTE bySelfAddr);
```

Parameters

hDev	I2C device handle retrieved from CreateFile()
bySelfAddr	Expected I2C device address. The valid range of address is [0x00–0x7F]
Return Values	Returns TRUE or FALSE, if the result is TRUE, the operation is successful

11.7.2.10 I2CGetSelfAddr

This function retrieves the address of the I2C device.

```
BOOL I2CGetSelfAddr(
        HANDLE hDev,
        PBYTE pbySelfAddr);
```

Parameters

hDev	I2C device handle retrieved from CreateFile()
pbySelfAddr	Pointer to BYTE variable that retrieves I2C device address
Return Values	Returns TRUE or FALSE, if the result is TRUE, the operation is successful

11.7.2.11 I2CTransfer

This function performs one or more I2C read or write operations. **pI2CTransferBlock** contains a pointer to the first of an array of I2C packets to be processed by the I2C. All the required information for the I2C operations should be contained in the array elements of pI2CPackets.

```
BOOL I2CTransfer(
        HANDLE hDev,
        PI2C_TRANSFER_BLOCK pI2CTransferBlock);
```

Parameters

hDev	I2C device handle retrieved from CreateFile()
pI2CTransferBlock	
pI2CPackets	[in] Pointer to an array of packets to be transferred sequentially
iNumPackets	[in] Number of packets pointed to by pI2CPackets (the number of packets to be transferred)
Return Values	Returns TRUE or FALSE, if the result is TRUE, the operation is successful

11.7.2.12 I2CReset

This function performs a hardware reset. The I2C driver maintains all the current information of the device, which includes all the initialized addresses.

```
BOOL I2CReset(
        HANDLE hDev);
```

Parameters

hDev	I2C device handle retrieved from CreateFile()
Return Values	Returns TRUE or FALSE, if the result is TRUE, the operation is successful

11.7.2.13 I2CEnableSlave

This function enables a I^2C slave access from the bus.

```
BOOL I2CEnableSlave(
        HANDLE hDev);
```

Parameters

hDev I^2C device handle retrieved from CreateFile()

Return Values Returns TRUE or FALSE, if the result is TRUE, the operation is successful

11.7.2.14 I2CDisableSlave

This function disables I^2C slave access from the bus. Note that after the I^2C slave interface disabled, I^2C slave module can be turned off.

```
BOOL I2CDisableSlave(
        HANDLE hDev);
```

Parameters

hDev I^2C device handle retrieved from CreateFile()

Return Values Returns TRUE or FALSE, if the result is TRUE, the operation is successful

11.7.3 I^2C Driver Structures

This section explains about the I^2C driver structures.

11.7.3.1 I2C_PACKET

This structure contains the information needed to write or read data using an I^2C port.

```
typedef struct {
        BYTE byRW;
        PBYTE pbyBuf;
        WORD wLen;
        LPINT lpiResult;
} I2C_PACKET, *PI2C_PACKET;
```

Parameters

byRW Determines whether the packet is a read or a write packet. Set to I2C_RW_READ for reading and I2C_RW_WRITE for writing.

pbyBuf Pointer to a buffer of bytes. For a read operation, this is the buffer into which data is read. For a write operation, this buffer contains the data to write to the target device.

wLen If the operation is a read, wLen specifies the number of bytes to read into pbyBuf. If the operation is a write, wLen specifies the number of bytes to write from pbyBuf.

lpiResult Pointer to an int that contains the return code from the transfer operation

11.7.3.2 I2C_TRANSFER_BLOCK

This structure contains an array of packets to be transferred using an I^2C port.

```
typedef struct {
        I2C_PACKET *pI2CPackets;
        INT32 iNumPackets;
} I2C_TRANSFER_BLOCK, *PI2C_TRANSFER_BLOCK;
```

Parameters

pI2CPackets	Pointer to an array of I2C_PACKET objects
iNumPackets	Number of I2C_PACKET objects pointed to by pI2CPackets

Chapter 12
Keypad Driver

The keypad driver converts input from the sensor into keyboard events that the driver enters into the Graphics, Windowing, and Events Subsystem (GWES).

12.1 Keypad Driver Summary

Table 12-1 provides a summary of source code location, library dependencies and other BSP information.

Table 12-1. Keypad Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Common Path	..\PLATFORM\COMMON\SRC\SOC\COMMON_FSL_V2_PDK1_9\KEYBDVS
SOC Specific Path	N/A
Platform Specific Path	..\PLATFORM\\<*Target Platform*>\SRC\DRIVERS\KEYPAD
Driver DLL	keypad.dll
SDK Library	N/A
Catalog Item	Third Party > BSP > Freescale i.MX28 EVK: PDK1_9:ARMV4I > Device Drivers > KEYPAD> KEYPAD
SYSGEN Dependency	N/A
BSP Environment Variables	BSP_NOKEYPAD=

12.2 Supported Functionality

The Keypad driver enables the hardware platform to provide the following software and hardware support:

1. Conforms to the Microsoft Layout Manager Interface
2. Two power management modes, full on and full off

12.3 Hardware Operation

Refer to the chapter on the Low-Resolution ADC (LRADC) in the hardware specification document for detailed operation and programming information.

12.3.1 Conflicts with Other Peripherals and Catalog Items

No conflicts.

12.3.2 Keypad

The keypad driver interfaces with the Windows CE Keyboard Driver Architecture to provide key input support.

12.3.2.1 i.MX28 EVK Keypad Mapping

The 8-key keypad is located on the accessory card and the mapping is shown in Table 12-2.

Table 12-2. Keypad Mapping

Label	Key
KEY1	ESCAPE
KEY2	WIN
KEY3	MENU
LEFT	LEFT
UP	UP
DOWN	DOWN
RIGHT	RIGHT
SELECT	ENTER

12.4 Software Operation

The i.MX28 Keypad driver do not follow the Microsoft recommended architecture for keyboard drivers. Use a standard stream driver for keypad scan.

12.4.1 Keypad Scan Codes and Virtual Keys

Each key on the keypad has a unique scan code, which is added to a buffer whenever that key is pressed or released. These scan codes, which are hardware specific, are converted to intermediate PS/2 keyboard scan code values and then converted into virtual keys, which are hardware independent numbers that identify the key. If a key is pressed from the keyboard, the generated scan code is directly converted into virtual keys.

12.4.1.1 i.MX28 Scan Code Mapping table

Table 12-3 shows the scan code mapping.

Table 12-3. Scan Code Mapping

Key	Keypad Scan Code	Virtual Key
KEY1	0x0	VK_ESCAPE
RIGHT	0x13c	VK_RIGHT
KEY2	0x2aa	VK_RWIN
LEFT	0x3a0	VK_LEFT
UP	0x62b	VK_UP
DOWN	0x890	VK_DOWN
KEY3	0x770	VK_MENU
SELECT	0xb00	VK_ENTER

12.4.2 Power Management

The following power management functions are used by the keypad driver.

12.4.2.1 BSPKppPowerOn

This function is used to power up the keypad. This function configures the necessary settings in the registers to bring up the keypad.

12.4.2.2 BSPKppPowerOff

This function powers down the keypad.

12.4.2.3 IOCTL_POWER_CAPABILITIES

This function is not implemented for the keypad driver.

12.4.2.4 IOCTL_POWER_SET

This function is not implemented for the keypad driver.

12.4.2.5 IOCTL_POWER_GET

This function is not implemented for the keypad driver.

12.4.3 Keypad Registry Settings

The following registry keys are required to load the keypad device layout and input language.

```
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\KEYPADS]
   "Prefix"="KPD"
   "Dll"="keypad.dll"
   "Index"=dword:1
   "Order"=dword:6

[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\KeyPadS]
   "RepeatLantency"=dword:3e8
   "RepeatRate"=dword:a
   "ScanPeriod"=dword:14
   "Debounce"=dword:2
   "ValidKeys"=dword:b
   "LRADC_KeyPAD"=dword:0
   "LRADC_Reference"=dword:6
   "LRADC_SCHEDULER"=dword:0
   "Hysteresis"=dword:80
   "ReleaseVolatge"=dword:00000e4a

[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\KeyPadS\Key2]
   "KeyName"="HotKey0"
   "AppName"="explorer.exe"
   "Parameter"=""
   "Voltage"=dword:00000550
   "Flag"=dword:00000001
   "VirtualKey"=dword:0000ffff
```

12.5 Unit Test

As keypad has only 8 keys. It is not a full-key keypad and it cannot pass the Keyboard Test included in the Windows CE Test Kit (CETK). A specific manual test to verify the 8-key functionality is described in following sections.

12.5.1 Unit Test Hardware

- i.MX28 EVK board

12.5.2 Unit Test Software

The manual keypad test requires Microsoft WordPad which can be built into the image.

12.5.3 Building the Unit Tests

No additional steps are required to build the keypad tests.

12.5.4 Running the Unit Tests

The procedure of keyboard tests is as follows:

1. Input Enter to run the Internet Explorer application
2. Input Menu

3. Input Up Down Left and Right
4. Input Windows Key
5. Open the help document by click the question mark on Internet Explorer application
6. Input the ESC to quit from help document
7. Input Return to quit the Explorer application

NOTE

Befoe running this test, ensure that the WordPad items are included in the project (SYSGEN_PWORD).

Chapter 13
LR Analog-Digital Converter (LRADC) Driver

The Low-Resolution Analog-Digital Converter is a multipurpose module used to measure the voltage applied to dedicated input pins. Some of the input pins can be used to interface a resistive touchscreen, while other pins can be used for general purpose inputs . The LRADC controller is not used directly by the software.

13.1 LRADC Driver Summary

The LRADC driver can be used to measure the voltage of the General Purpose LRADC pins and to interface with a touchscreen interface,and battery interface. Thus, only one driver interface is used by the touchscreen driver. The LRADC driver interacts with the TSC to drive the LRADC. Table 13-1 provides a summary of source code location, library dependencies and other BSP information.

Table 13-1. LRADC Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Common Path	N/A
SOC Specific Path	..PLATFORM\COMMON\SRC\SOC\\<*Target SOC*>\LRADC
Platform Specific Path	..\PLATFORM\\<*Target Platform*>\SRC\DRIVERS\LRADC
Driver DLL	lradc.dll
SDK Library	lradcsdk_$(_SOCDIR).lib
Catalog Item	Third Party > BSP > Freescale <*Target Platform*>: ARMV4I > Device Drivers > LRADC > LRADC
SYSGEN Dependency	N/A
BSP Environment Variables	BSP_LRADC=1

13.2 Supported Functionality

The LRADC driver enables the i.MX28 EVK System to provide the following software support:

1. Configures the Touchscreen setting
2. Retrieves of the Touchscreen samples
3. Configures the general conversion setting
4. Retrieves the general purpose samples

13.3 Hardware Operation

Refer to the *Low-Resolution ADC and Touch-Screen Interface* chatpers in the *i.MX28 Applications Processor Reference Manual* for hardware operation details.

13.3.1 Conflicts with Other Peripherals and Catalog Items

As the LRADC inputs are not multiplexed with other functions, the LRADC module does not have conflict with other peripherals.

13.4 Software Operation

The LRADC device driver framework for Windows CE is a stream interface driver .A description of the stream interface driver may be found in the Windows CE Platform Builder documentation at **Developing a Device Driver −> Windows CE Drivers −>Stream Interface Drivers**.. The LRADC Stream Interface driver controls the LRADC hardware . The LRADC SDK lib provide APIs for WindowsCE drivers and applications. We access the LRADC only need use the LRADC SDK LIB.

13.4.1 ADC Registry Settings

The ADC Registry settings are as follows:

```
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\LRADC]
    "Dll" = "lradc.dll"
    "Prefix" = "LDC"
    "Index" = dword:1
    "Order" = dword:2
```

13.4.2 Interfacing with the LRADC Driver

This section describes how to interface the LRADC driver.

13.4.2.1 Stream Interface

The LRADC driver is a stream interface driver, so it is accessed through the file system APIs.

13.4.2.2 Using the SDK

The LRADC driver includes a wrapper library that simplifies its use. This library is the ADC SDK and is described in Section 13.7, “LRADC SDK API Reference.”

13.4.2.3 DMA Support

The LRADC driver currently does not support DMA.

13.5 Power Management

This section explains the power management functions.

13.5.1 LDC_PowerUp

This function is not implemented for the LRADC driver.

13.5.2 LDC_PowerDown

This function is not implemented for the LRADC driver.

13.5.3 IOCTL_POWER_CAPABILITES

The power management capabilities are advertised with the power manager through this IOCTL. The LRADC module supports only two power states: D0 and D4.

13.5.4 IOCTL_POWER_SET

This function is implemented for the LRADC driver. If the clocks are disabled during the suspend (for example if the touchscreen is not a wake-up source), then the clocks are re-enabled at this time in the D0 state. If the touchscreen is not a wake-up source, then the clocks are disabled at this time in the D4 state.

13.5.5 IOCTL_POWER_GET

This IOCTL returns the current device power state. By design, the Power Manager knows the device power state of all power-manageable devices. It does not generally issue an **IOCTL_POWER_GET** call to the device unless an application calls **GetDevicePower** with the POWER_FORCE flag set.

13.6 Unit Test

Due to the heavy use of the LRADC routines by other drivers on the system, there are no additional test cases.

13.7 LRADC SDK API Reference

This section explains the LRADC SDK functions.

13.7.1 LRADCOpenHandle

This function creates a handle to the LRADC stream driver.

```
HANDLE LRADCOpenHandle(
        LPCWSTR lpDevName
);
```

Parameters

LpDevName	[in] Name of the device,for example TEXT("LDC1:")
Return Values	Handle to LRADC driver which is set in this method
	NULL indicates failure

13.7.2 LRADCCloseHandle

This function is used to close a handle to the LRADC stream driver.

```
void LRADCCloseHandle(
        HANDLE hLRADC
);
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle

Return Values None

13.7.3 LRADCConfigureChannel

This function configures a channel with the given settings.

```
BOOL LRADCConfigureChannel(
        HANDLE hLRADC,
        LRADC_CHANNEL eChannel,
        BOOL bEnableDivideByTwo,
        BOOL bEnableAccum,
        UINT8 u8NumSamples
);
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle
eChannel	[in] Identifier of the channel to configure
bEnableDivideByTwo	[in] TRUE to caused the A/D converter to use its analog divide by two circuit
bEnableAccum	[in] TRUE to add successive samples to the 18bit accumulator
u8NumSamples	[in] Number of samples that must be converted, between 1 and 16

Return Values TRUE on success and FALSE indicates a failure

13.7.4 LRADCEnableInterrupt

The function enable the Interrupt of the LRADC Channel.

```
BOOL LRADCEnableInterrupt(
        HANDLE hLRADC,
        LRADC_CHANNEL eChannel,
        BOOL bValue,
);
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle
eChannel	[in] Identifier of the channel to configure
bValue	[in] TRUE to enable ,FALSE to Disable

Return Values TRUE on success and FALSE indicates a failure

13.7.5 LRADCClearInterruptFlag

The function Clears the interrupt flag of a specified LRADC channel.

```
BOOL LRADCEnableInterrupt(
        HANDLE hLRADC,
        LRADC_CHANNEL eChannel,
);
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle
eChannel	[in] Identifier of the channel to configure
Return Values	TRUE on success and FALSE indicates a failure

13.7.6 LRADCSetDelayTrigger

The function Sets the ADC conversion sample time of the LRADC Channel.

```
BOOL LRADCEnableInterrupt(
        HANDLE hLRADC,
        LRADC_DELAYTRIGGER DelayTrigger,
        UINT32 TriggerLradcs,
        UINT32 DelayTriggers,
        UINT32 LoopCount,
        UINT32 DelayCount,
);
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle
DelayTrigger	[in] Identifier of LRADC delay Triggers
TriggerLradcs	[in] The delay controller to trigger the corresponding LRADC channel
DelayTriggers	[in] The delay controller to trigger the corresponding delay channel
LoopCount	[in] The number of times this delay counter
DelayCount	[in] Delaycount of the delay channel
Return Values	TRUE on success and FALSE indicates a failure

13.7.7 LRADCCLearDelayChannel

The function clears the ADC conversion sample time of the LRADC Channel.

```
BOOL LRADCCLearDelayChannel(
        HANDLE hLRADC,
        LRADC_CHANNEL eChannel,
);
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle
eChannel	[in] Identifier of the channel to clear
Return Values	TRUE on success and FALSE indicates a failure

13.7.8 LRADCSetDelayTriggerKick

The function set the delay trigger kick of the LRADC Channel.

```
BOOL LRADCEnableInterrupt(
        HANDLE hLRADC,
        LRADC_DELAYTRIGGER DelayTrigger,
        BOOL bValue,
);
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle
DelayTrigger	[in] Identifier of LRADC delay Triggers
bValue	[in] TRUE to enable ,FALSE for Disable
Return Values	TRUE on success and FALSE indicates a failure

13.7.9 LRADCGetAccumValue

The function gets the conversion value of a specified LRADC channel.

```
UINT16 LRADCGetAccumValue(
        HANDLE hLRADC,
        LRADC_CHANNEL Channel,
);
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle
eChannel	[in] Identifier of the channel to configure
Return Values	Accumulator value of the channel

13.7.10 LRADCEnableBatteryMeasurement

The function enables the Interrupt of the LRADC Channel.

```
BOOL LRADCEnableBatteryMeasurement(
        HANDLE hLRADC,
        LRADC_DELAYTRIGGER eTrigger,
        UINT32 TriggerLradcs,
        LRADC_BATTERYMODE eBatteryMode,
);
```

Parameters

hLRADC	[in] Handle to configure retrieved from LRADCOpenHandle
eTrigger	[in] Identifier of LRADC delay Triggers
riggerLradcs	[in] Specifies the smapling interval for the Battery value updation
eBatteryMode	[in] Specifies the Battery mode setup
Return Values	Return 0 If the operation is successful otherwise returns error value failure

13.7.11 LRADCEnableDieMeasurement

The function enables the LRADC channel for die temperature measurement.

```
BOOL LRADCEnableDieMeasurement(
        HANDLE hLRADC,
        );
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle

Return Values Return die temperature.

13.7.12 LRADCClearAccum

The function Clears the Accum Value of the specified LRADC channel.

```
BOOL LRADCEnableInterrupt(
        HANDLE hLRADC,
        LRADC_CHANNEL Channel,
);
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle
eChannel	[in] Identifier of the channel to configure

Return Values TRUE on success and FALSE indicates a failure

13.7.13 LRADCEnableTouchDetect

The function sets or clears the TOUCH_DETECT_ENABLE in HW_LRADC_CTRL0 Register.

```
BOOL LRADCEnableTouchDetect(
        HANDLE hLRADC,
        BOOL bValue,
);
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle
bValue	[in] TRUE for set ,FALSE for clear

Return Values TRUE on success and FALSE indicates a failure

13.7.14 LRADCGetTouchDetect

The function reads the TOUCH_DETECT_RAW bit of HW_LRADC_STATUS register.

```
BOOL LRADCGetTouchDetect(
        HANDLE hLRADC,
);
```

Parameters

hLRADC	[in] The LRADC device handle retrieved from LRADCOpenHandle

Return Values TRUE on success and FALSE indicates a failure

13.7.15 LRADCEnableTouchDetectInterrupt

The function sets or clears the TOUCH_DETECT_IRQ_EN in HW_LRADC_CTRL1 Register.

```
BOOL LRADCEnableTouchDetectInterrupt(
        HANDLE hLRADC,
        BOOL bValue,
);
```

Parameters

hLRADC [in] The LRADC device handle retrieved from LRADCOpenHandle

bValue [in] TRUE to enable ,FALSE for Disable

Return Values TRUE on success and FALSE indicates a failure

13.7.16 LRADCSetAnalogPowerUp

The function sets or clears the ADC analog power up.

```
BOOL LRADCEnableInterrupt(
        HANDLE hLRADC,
        BOOL bValue,
);
```

Parameters

hLRADC [in] The LRADC device handle retrieved from LRADCOpenHandle

bValue [in] TRUE to enable ,FALSE for Clear

Return Values TRUE on success and FALSE indicates a failure

13.7.17 LRADCClearTouchDetect

The function clears the touch detect status.

```
BOOL LRADCClearTouchDetect(
        HANDLE hLRADC,
);
```

Parameters

hLRADC [in] The LRADC device handle retrieved from LRADCOpenHandle

Return Values TRUE on success and FALSE indicates a failure

13.7.18 LRADCEnableTouchDetectXDrive

The function enables or disables the X Channels in HW_LRADC_CTRL0 Register.

```
BOOL LRADCEnableTouchDetectXDrive(
        HANDLE hLRADC,
        BOOL bValue,
);
```

Parameters

hLRADC [in] The LRADC device handle retrieved from LRADCOpenHandle

bValue [in] TRUE to enable ,FALSE for Disable

Return Values TRUE on success and FALSE indicates a failure

13.7.19 LRADCEnableTouchDetectYDrive

The function enables or disables the Y Channels in HW_LRADC_CTRL0 Register.

```
BOOL LRADCEnableTouchDetectYDrive(
        HANDLE hLRADC,
        BOOL bValue,
);
```

Parameters

hLRADC [in] The LRADC device handle retrieved from LRADCOpenHandle

bValue [in] TRUE to enable ,FALSE for Disable

Return Values TRUE on success and FALSE indicates a failure

Chapter 14
NAND Redundant Boot

Redundant boot supported from NAND includes the following components:

- Boot Image checking tool
- Boot Image updating tool

The Boot Image checking tool is used for checking the boot streams integrity every time when system boots up. The Boot Image updating tool is used for updating image. If the update fails, then the checking tool can easily restore the image when the system boots up the next time. These tools cannot run simultaneously to prevent boot stream corruption.

14.1 NAND Redundant Boot Summary

Table 14-1 provides a summary of source code location, library dependencies and other BSP information.

Table 14-1. NAND Redundant Boot Summary

Driver Attribute	Definition
Target Platform (TGTPLAT)	iMX28-EVK-PDK1_9
Target SOC	N/A
SOC Common Path	N/A
SOC Specific Path	N/A
Platform Specific Path	..\PLATFORM\<*Target Platform*>\SRC\COMMON\NANDBOOTBURNER ..\PLATFORM\<*Target Platform*>\SRC\APP\UpdateSB
Driver DLL	N/A
SDK Library	N/A
Catalog Item(s)	N/A
SYSGEN Dependency	N/A
BSP Environment Variable(s)	N/A

14.2 Supported Functionality

The NAND Redundant Boot enables the system to provide the following software and hardware support:

1. Supports updating image from certain location on the device.
2. Supports restoring backup image when the update fails.
3. Supports updating backup image when user confirms the updated image works well.

14.3 Hardware Operation

This section explains about the hardware operations.

14.3.1 Conflicts with Other Peripherals and Catalog Items

No conflict.

14.4 Software Operation

Figure 14-1 shows the Boot Image updating tool's work flow.

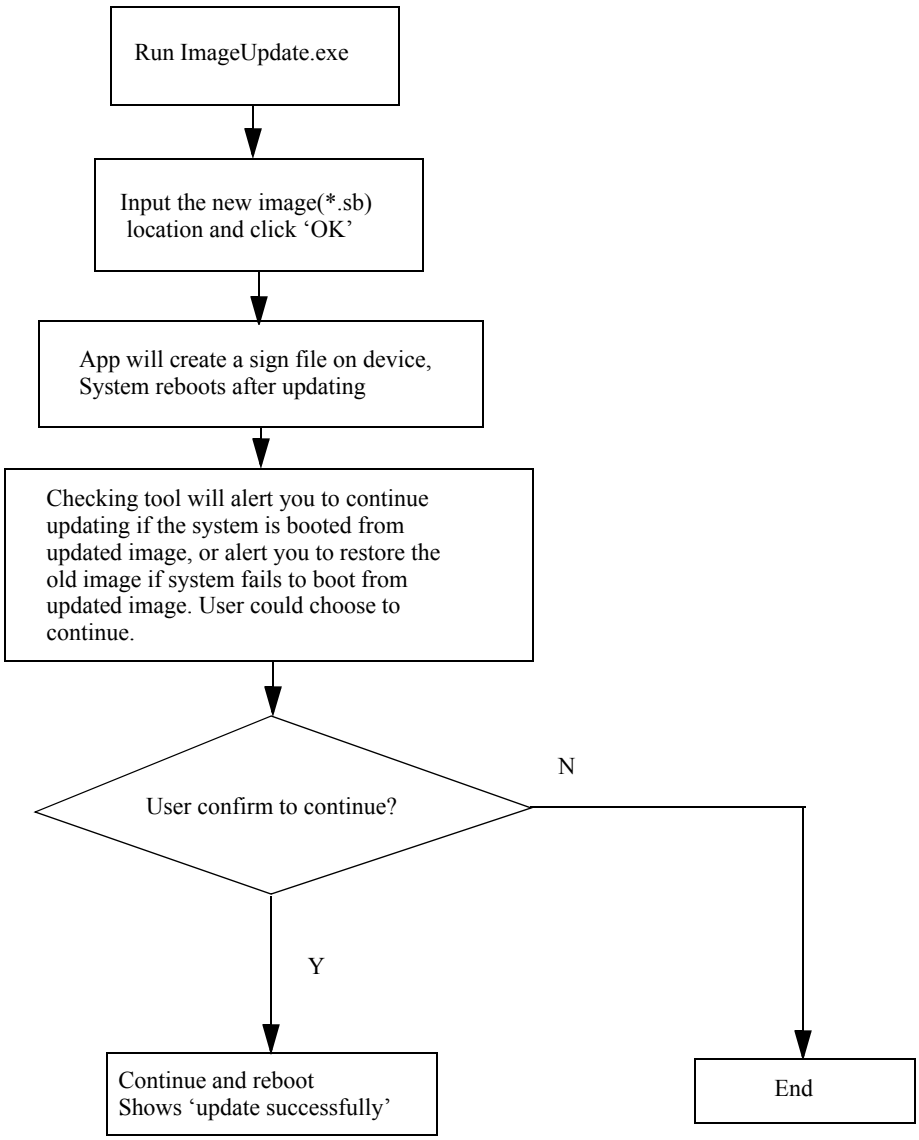

Figure 14-1. Image Updating Work Flow

Figure 14-2 shows the Boot Image checking tool's work flow.

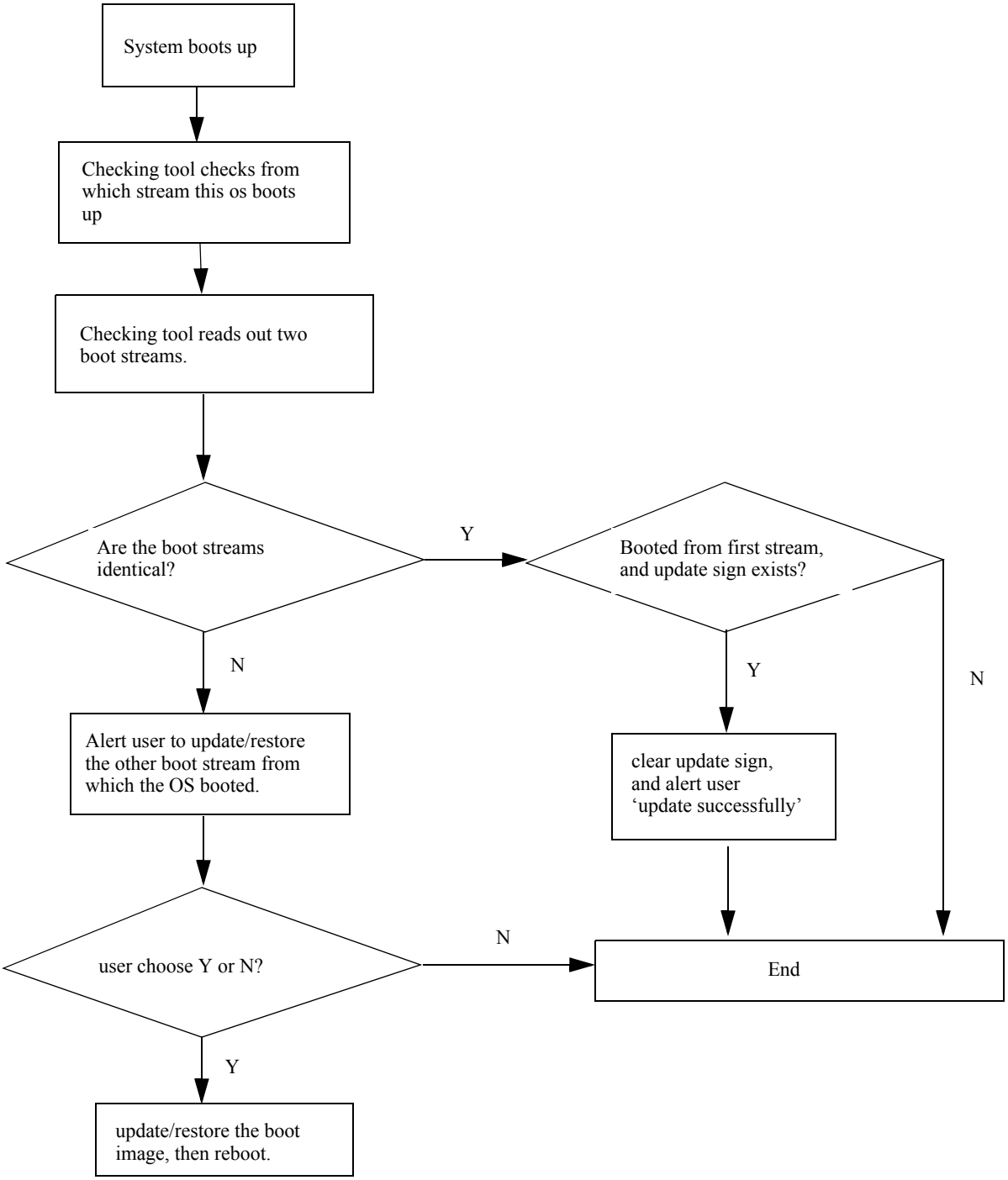

Figure 14-2. Image Checking Work Flow

14.5 Unit Test

The following section describes the testing update and restore functionality:

14.5.1 Testing Update Functionality

Perform the following steps to test the update functionality:

1. Run ImageUpdate.exe
2. Select the new image(*.sb)
3. Click **OK**.The image is updated and system reboots after update.
4. Ensure that this startup is from new image.
5. A continue update message appears asking the user to confirm the update.
6. Click **YES** to continue. The Image is updated and the system reboots.
7. After this startup, a **update successfully** message appears.

14.5.2 Testing Restore Functionality

Use the following steps to test the restore functionality:

1. Run ImageUpdate.exe
2. Select the new image(*.sb)
3. Click **OK**. The image is updated and the system reboots.
4. Ensure that this startup is from new image.
5. A message is displayed asking the user to continue updating.
6. Click **NO.**
7. Power OFF the device and power ON.
8. After this startup, a message is displayed asking the user to recover.
9. Click **YES** to continue. The image is recovered and the system reboots.
10. Ensure that this startup is from the old image.

Chapter 15
Power Management Unit Driver

15.1 PMU Summary

This chapter describes the API provided by Freescale, which allows complete access to the functionality of the PMU. This document is intended for device driver and application developers who need to understand and gain access to the functionality provided by the PMU.

Table 15-1 provides a summary of source code location, library dependencies, and other BSP information.

Table 15-1. PMU Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Specific Path	..\PLATFORM\COMMON\SRC\SOC\<*Target SOC*>\PMU
Platform Driver Path	..\PLATFORM\<*Target Platform*>\SRC\DRIVERS\PMU
Driver DLL	pmupdk.dll
SDK Library	pmusdk.dll
Catalog Item	N/A
SYSGEN Dependency	N/A
BSP Environment Variables	BSP_NOPMU=

15.2 Supported Functionality

The PMU device driver framework for Windows CE is a stream interface driver and a SDK DLL. A description of the stream interface driver can be found in the Windows CE Platform Builder documentation at **Developing a Device Driver** > **Windows CE Drivers** > **Stream Interface Drivers.**

The Stream Interface driver provides an IOCTL interface for SDK DLLs. The SDK DLLs provide APIs for Windows CE drivers and applications.

The API covers the PMU functionality of the following areas:

1. Battery
2. Battery Charger
3. Regulators

15.3 Hardware Operation

Refer to the hardware specification document for detailed operation and programming information.

15.3.1 Conflicts with Other Peripherals and Catalog Items

This section explains the PMU conflicts with other peripherals and catalog items.

15.3.1.1 Conflicts with Other On-Chip Peripherals

This section lists the conflicts with other On-Chip peripherals.

15.3.1.1.1 iMX28 Peripheral Conflicts

No conflicts.

15.3.1.1.2 Conflicts with Hardware Peripherals

No conflicts.

15.4 Software Operation

This section explains the software operation.

15.4.1 Communicating with the PMU

Similar to the CEDDK DLL, the PMU DLL does not require any special initialization. All the initialization required by the PMU is performed when the DLL is loaded into the respective process space. Drivers that should utilize the PMU simply need to link to the PMUSDK export library and invoke the exported functions.

15.4.2 Compile-Time Configuration Options

No options.

15.4.3 Registry Settings

There are no registry settings that have to be modified to use the PMU driver.

```
;-------------------------------------------------------------------------
; PMU PDK Driver
;
IF BSP_NOPMU !
; @XIPREGION IF PACKAGE_OEMDRIVERS
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\PMI]
   "Prefix"="PMI"
   "Dll"="pmupdk.dll"
   "Index"=dword:1
   "Order"=dword:3
   "IClass"="{A32942B7-920C-486b-B0E6-92A702A99B35}"    ; PMCLASS_GENERIC_DEVICE
```

```
; @XIPREGION ENDIF PACKAGE_OEMDRIVERS
ENDIF BSP_NOPMU!
```

15.4.4 Power Management

The PMU does not implement the Power Manager driver IOCTLs or the PowerUp or PowerDown stream interface. However, the PMU dirver uses the power button to set the system into (or out of) the suspend mode

15.5 Unit Test

No software is necessary for this test.

15.6 PMU Driver API Reference

The PMU interface allows device drivers to configure and control linear regulators, battery monitor and charger.

15.6.1 PmuInitBatteryMonitor

This function initializes the battery monitor for the battery module.

```
BOOL PmuInitBatteryMonitor(void)
```

Parameters

None.

Return Values Returns TRUE if successful otherwise returns FALSE

15.6.2 PmuGetBatteryVoltage

This function returns the current Battery voltage.

```
BOOL PmuGetBatteryVoltage(UINT32 *pBattVol)
```

Parameters

pBattVol [Out] battery voltage.

Return Values Returns TRUE if successful otherwise returns FALSE.

15.6.3 PmuSetCharger

This function is used to set the charger.

```
BOOL PmuSetCharger(DWORD current)
```

Parameters

current [in] The current value of charger

Return Values Returns TRUE if successful otherwise returns FALSE

15.6.4 PmuStopCharger

This function is used to stop the charger.

```
VOID PmuStopCharger()
```

Parameters None

Return Values Returns TRUE if successful otherwise returns FALSE

15.6.5 PmuGetBatteryChargingStatus

This routine returns the Battery charging status.

```
BOOL PmuGetBatteryChargingStatus(BOOL *bChargStas )
```

Parameters

bChargStas [Out] Changing states

Return Values Returns TRUE if successful otherwise returns FALSE

15.6.6 PmuSetVddd

This function sets the VDDD value and VDDD brownout level .

```
BOOL PmuSetVddd(UINT32 NewTargetmV,  UINT32 NewBrownoutmV )
```

Parameters

NewTargetmV [in] Vddd voltage in millivolts.

NewBrownoutmV [in] Vddd brownout in millivolts.

Return Values Returns TRUE if successful otherwise returns FALSE

15.6.7 PmuGetVddd

This function gets Vddd value.

```
BOOL PmuGetVddd(UINT32 *VdddmV)
```

Parameters

vdddmV [Out] Vddd voltage in millivolts.

Return Values Returns TRUE if successful otherwise returns FALSE

15.6.8 PmuGetVdddBrownont

This function returns the present values of the VDDD brownout in millivolts.

```
BOOL PmuGetVdddBrownont(UINT32 *VdddBo)
```

Parameters

vdddBo [Out] Vddd Brownout voltage in millivolts.

Return Values Returns TRUE if successful otherwise returns FALSE

15.6.9 PmuSetFets

This function sets the Fets mode.

```
BOOL PmuSetFets(PMU_POWER_FETSSET bFetsMode)
```

Parameters

bFetsMode [in] Fets mode.

Return Values Returns TRUE if successful otherwise returns FALSE

15.6.10 PmuPowerGetSupplyMode

This routine checks if the supply mode is 5V/Battery.

```
BOOL PmuPowerGetSupplyMode(PMU_POWER_SUPPLY_MODE *PowerMode)
```

Parameters

bPowerMode [Out] Supply mode 5V/Battery

Return Values Returns TRUE if successful otherwise returns FALSE

Chapter 16
Secure Digital Host Controller (SDHC) Driver

The SDHC module supports MMC, SD cards, and Secure Digital I/O. The SDHC driver provides the interface between the Microsoft SD Bus driver and the SSP hardware.

16.1 SDHC Driver Summary

Table 16-1 provides a summary of source code location, library dependencies and other BSP information.

Table 16-1. eSDHC Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Common Path	N/A
SOC Specific Path	..\PLATFORM\COMMON\SRC\SOC\<*Target SOC*>\SDHC
Platform Specific Path	..\PLATFORM\<*Target Platform*>\SRC\DRIVERS\SDHC
Driver DLL	sdhc.dll
SDK Library	sdhc_<*Target SOC*>.lib, sdcardlib.lib, sdhclib.lib, sdbus.lib
Catalog Item	Third Party > BSP > Freescale <*Target Platform*>: ARMV4I > Device Drivers > SD Controller > SSP1 SDHC Third Party > BSP > Freescale <*Target Platform*>: ARMV4I > Device Drivers > SD Controller > SSP2 SDHC
SYSGEN Dependency	SYSGEN_SD_MEMORY=1
BSP Environment Variables	N/A

16.2 Supported Functionality

The SDHC driver enables the EVK System to provide the following software and hardware support:

1. Supports the Synchronous Serial Ports(SSP) Controller
2. Designed and implemented as close as possible to Standard Host Controller Driver in CE 6.0 R2
3. Compliant with the SDBUS2 driver provided in CE 6.0 R2
4. Supports Fast Path
5. Supports DMA mode of data transfers
6. Supports SD, SD High Capacity (up to spec v2.1), MMC (up to spec v4.3), and SDIO cards (up to spec v2.0). High capacity MMC cards are not supported because SDBUS2 in CE 6.0 R2 does not support these cards

7. One host supports only one card to be connected to it
8. DLL supports multiple instances of the SSP controller
9. Supports the configuration of the block sizes from 1 – 4096 bytes in single and multi-block modes
10. Supports insertion and removal of card, even when system is suspended; when the system resumes, the card (if present) is remounted
11. Supports the write protect switch on SD cards
12. Supports MMC cards in 1-bit mode and SD/SDIO cards in 4-bit modes due to limitation in SDBUS2 in CE 6.0 R2.

16.3 Hardware Operation

Refer to the i.MX28 *Multimedia Applications Processor Reference Manual* for detailed operation and programming information on SSP.

16.3.1 Conflicts with Other Peripherals and Catalog Options

This section explains SDHC driver conflicts with other peripherals and catalog options.

16.3.1.1 Conflicts with SoC Peripherals

SSP2 conflicts with Nand Flash Controller (NFC).

16.3.1.2 Conflicts with Other EVK Peripherals

No conflicts.

16.4 Software Operation

The SDHC driver follows the Microsoft recommended architecture (standard host controller driver) for Secure Digital Host Controller drivers, whenever possible. The details of this architecture and its operation can be found in the Platform Builder Help under the heading **Secure Digital Card Driver Development Concepts**, or in the online documentation at the following URL:
http://msdn2.microsoft.com/en-us/library/aa925967.aspx

16.4.1 Required Catalog Items

The required catalog items are as follows:

16.4.1.1 SD and MMC Support

Catalog > Device Drivers > SDIO > SD Memory

Additionally, as the eSDHC driver supports high capacity cards, it is necessary to define IMGSDBUS2 variable in the workspace. By default, both the SYSGEN_SD_MEMORY and IMGSDBUS2 are set in the BSP workspace.

16.4.2 SDHC Registry Settings

This section explains the SDHC registry settings.

16.4.2.1 i.MX28 SDHC Registry Settings

The following registry keys are required to load the SDHC driver:

```
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\SDHC1]
    "Order"=dword:19
    "Dll"="sdhc.dll"
    "Prefix"="SHC"
    "Index"=dword:1
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\SDHC2]
    "Order"=dword:19
    "Dll"="sdhc.dll"
    "Prefix"="SHC"
    "Index"=dword:2

[HKEY_LOCAL_MACHINE\System\StorageManager\Profiles\MMC]
    "Name"="MMC Card"
    "Folder"="MMCMemory"

[HKEY_LOCAL_MACHINE\System\StorageManager\Profiles\SDMemory]
    "Name"="SD Memory Card"
    "Folder"="SDMemory"
```

16.4.3 DMA Support

DMA mode is supported by the SDHC driver. The driver uses the APBH DMA, which has a special SSP1 and SSP2 DMA channel.

16.4.4 Power Management

The SHC_powerUp and SHC_PowerDown APIs are the entry points for suspend/resume functionality.

16.5 Unit Test

The eSDHC driver is tested using the following tests included as part of the Windows CE 6.0 Test Kit (CETK).

- File System Driver Test
- Storage Device Block Driver Read/Write Test
- Storage Device Block Driver API Test
- Storage Device Block Driver Performance Test
- Partition Driver Test

16.5.1 Unit Test Hardware

Table 16-2 lists the required hardware to run the unit tests.

Table 16-2. Hardware Requirements

Requirement	Description
SD Cards	SanDisk (128MB, 512MB, Extreme III SDHC 4GB) ATP (SDHC 4GB) A-DATA Turbo (SDHC 4GB) Kingston (MiniSD 512MB, MicroSD 1GB)
MMC Cards	PQI (128 Mbytes) Kingmax (RS-MMC: 512MB, 1GB) Transcend (MMCPlus: 1 Gbytes, 4 Gbytes)

16.5.2 Unit Test Software

Table 16-3 lists the required software to run the unit tests.

Table 16-3. Software Requirements

Requirement	Description
tux.exe	Tux test harness, which is needed for executing the test
kato.dll	Kato logging engine, which is required for logging test data
tooltalk.dll	Library required by Tux.exe and Kato.dll. Handles the transport between the target device and the development workstation
fsdtst.dll	File System Driver Test.dll file
rwtest.dll	Storage Device Block Driver Read/Write Test.dll file
disktest.dll	Storage Device Block Driver API Test.dll file
disktest_perf.dll	Storage Device Block Driver Performance Test
msparttest.dll	Partition Driver Test.dll file

16.5.3 Building the Unit Tests

All the above mentioned tests come prebuilt as part of the CETK. No steps are required to build these tests. These test files can be found alongside the other required CETK files in the following location:

```
[Drive]:\Program Files\Microsoft Platform Builder\6.00\cepb\wcetk\ddtk\armv4I
```

16.5.4 Running the Unit Tests

The following tests and test procedures are available. Refer to the relevant sub sections under **CETK Tests** in the Platform Builder Help for detailed information on the below tests. Alternatively, online documentation can be referred at the following link:
http://msdn2.microsoft.com/en-us/library/aa934353.aspx

16.5.4.1 File System Driver Test

The following command is used to run the tests on an SD card:

```
tux –o –d fsdtst –c "-p SDMemory –z"
```

For MMC cards, use the following command:

```
tux –o –d fsdtst –c "-p MMC –z"
```

NOTE

This tests all inserted cards and the cards are to be formatted before running the test. For higher capacity cards, the test takes a longer time to complete, so it is recommended that the system power management (from control panel) be configured. This prevents the system from entering the suspend state during test execution.

16.5.4.2 Storage Device Block Driver Read/Write Tests

The following command line is used to run the tests:

```
tux –o –d rwtest –c "-z"
```

NOTE

This command tests only one card at a time.

16.5.4.3 Storage Device Block Driver API Tests

The following command line is used to run the tests:

```
tux –o –d disktest –c "-z"
```

NOTE

This command tests only one card at a time.

16.5.4.4 Storage Device Block Driver Performance Tests

The following command line is used to run the tests:

```
tux –o –d disktest_perf –c "-z -disk DSK1:"
```

NOTE

This command tests only one card at a time.

16.5.4.5 Partition Driver Test

The following command line is used to run the tests:

```
tux –o –d msparttest –c "-z"
```

NOTE

The cards should be of size 256 Mbytes and higher. For higher capacity cards, the test takes longer time to complete, so it is recommended that the system power management (from control panel) be configured. This prevents the system from entering the suspend state during test execution.

16.5.5 System Testing

The following system tests are performed to verify the operation of the SD and MMC memory cards:

- Use the **Start** > **Settings** > **Control Panel** > **Storage Manager** to format and create partitions on the mounted memory cards.
- Establish ActiveSync connection over USB and transfer files to/from the memory cards.
- Write media files to memory storage. Use Windows Media Player to playback media files from memory storage.

16.6 Secure Digital Card Driver API Reference

Detailed reference information for the Secure Digital Card driver can be found in the Platform Builder Help under the heading *Secure Digital Card Driver Reference* or in the online documentation at the following link: http://msdn2.microsoft.com/en-us/library/aa912994.aspx

Chapter 17
Serial Driver

The serial driver interfaces the low level serial driver hardware to the Windows CE serial subsystem.

17.1 Serial Driver Summary

The serial port driver is implemented as a stream interface driver and supports all the standard I/O control codes and entry points. The serial port driver handles all the internal UARTs except UART1 which is used for debugging. In the BSP implementation, the hardware-specific code that corresponds to the serial port driver lower layer is implemented as the platform-dependent driver (PDD). This PDD is linked with Microsoft-provided public serial MDD library (com_mdd2.lib) to form the whole serial port driver. Table 17-1 provides a summary of source code location, library dependencies and other BSP information.

Table 17-1. Serial Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
SOC Common Path	..\PLATFORM\COMMON\SRC\SOC\COMMON_FSL_V2_PDK1_9\SERIALAPP
SOC Specific Path	N/A
Platform Specific Path	..\PLATFORM\\<*Target Platform*>\SRC\DRIVERS\SERIAL
Driver DLL	csp_serial.dll
SDK Library	N\A
Catalog Item	Third Party –> BSP –> Freescale <*Target Platform*>: ARMV4I –> Device Drivers > Serial –> UART2 Third Party –> BSP –> Freescale <*Target Platform*>: ARMV4I –> Device Drivers –> Serial –> UART5
SYSGEN Dependency	N/A
BSP Environment Variables	BSP_SERIAL_UART2 =1 BSP_SERIAL_UART5 =1

17.2 Supported Functionality

The serial port driver enables the hardware system to provide the following support:

1. Conforms to RS232 protocol standard
2. Supports RTS/CTS hardware flow control function
3. Supports parity check and optional stop bit
4. Supports power management mode full on/full off

5. Supports DMA transfer
6. Supports baud rate up to 3.25 Mbps

17.3 Hardware Operation

Refer to the *Multimedia Applications Processor Reference Manual* for detailed operation and programming information on UART.

17.3.1 Conflicts with Other Peripherals and Catalog Items

The following section explains serial driver conflicts with other peripherals and catalog items.

17.3.1.1 Conflicts with SoC Peripherals

All UART pins can be configured for alternate functionality (I^2C, CAN, ENET...) using the i.MX28 IOMUX. The configuration is specified by the BSP serial driver. Changing this configuration can result in a conflict and prevent proper operation of the UART.

17.3.1.2 Conflicts with Board Peripherals

No conflicts.

17.4 Software Operation

The serial driver follows the Microsoft recommended architecture for serial drivers. The details of this architecture and its operation can be found in the Platform Builder Help documentation at the following location:

Developing a Device Driver > **Windows CE Drivers** > **Serial Drivers** > **Serial Driver Development Concepts**.

17.4.1 Registry Settings

This section explains the registry settings used to load the serial driver.

17.4.1.1 i.MX28 Registry Settings

The following registry keys are required to load the serial driver:

```
IF BSP_SERIAL_UART2
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\COM2]
   "DeviceArrayIndex"=dword:0
   "IoBase"=dword:8006A000
   "IoLen"=dword:D4
   "Prefix"="COM"
   "Dll"="csp_serial.dll"
   "Index"=dword:2
   "Order"=dword:3
   "useDMA"=dword:1
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\COM2\Unimodem]
```

```
   "Tsp"="Unimodem.dll"
   "DeviceType"=dword:0
   "FriendlyName"="i.MX28 COM2 UNIMODEM"
   "DevConfig"=hex: 10,00, 00,00, 05,00,00,00, 10,01,00,00, 00,4B,00,00, 00,00, 08, 00, 00,
00,00,00,00
ENDIF ; BSP_SERIAL_UART2
IF BSP_SERIAL_UART5
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\COM5]
   "DeviceArrayIndex"=dword:0
   "IoBase"=dword:80070000
   "IoLen"=dword:D4
   "Prefix"="COM"
   "Dll"="csp_serial.dll"
   "Index"=dword:5
   "Order"=dword:3
   "useDMA"=dword:1
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\COM5\Unimodem]
   "Tsp"="Unimodem.dll"
   "DeviceType"=dword:0
   "FriendlyName"="i.MX28 COM5 UNIMODEM"
   "DevConfig"=hex: 10,00, 00,00, 05,00,00,00, 10,01,00,00, 00,4B,00,00, 00,00, 08, 00, 00,
00,00,00,00
ENDIF ; BSP_SERIAL_UART5
```

17.4.2 Power Management

The serial driver supports full on/full off power management mode through `PowerUp( )` and `PowerDown()` functions.

17.5 Unit Test

The serial driver is tested using the Serial Port Driver Test and Serial Communications Test included as part of the CETK. The Serial Port Test assesses if the driver supports configurable device parameters such as baud rate and data bits. The test also assesses additional functionality such as COM port events, escape functions, and time-outs.

17.5.1 Unit Test Hardware

The following hardware is used for the unit test:

- i.MX28 EVK board

17.5.2 Unit Test Software

Table 17-2 lists the required software to run the unit tests.

Table 17-2. Software Requirements

Requirement	Description
Tux.exe	Tux test harness, which is needed for executing the test
Kato.dll	Kato logging engine, which is required for logging test data
Tooltalk.dll	Library required by Tux.exe and Kato.dll. Handles the transport between the target device and the development workstation
SerDrvBvt.dll	Test.dll file for Serial Port Driver Test

17.5.3 Building the Unit Tests

The serial port driver tests come pre-built as part of the CETK. No steps are required to build these tests. The Pserial.dll file can be found alongside the other required CETK files in the following location:

```
[Drive]:\Program Files\Microsoft Platform Builder\6.00\cepb\wcetk\ddtk\armv4i
```

17.5.4 Running the Unit Tests

The Serial Port Driver Test executes the `tux -o -d serdrvbvt` command line on default execution.

For detailed information on the Serial Port Tests, see

Debugging and Testing > Tools for Debugging and Testing > Windows CE Test Kit > CETK Tests > Serial Port Driver Test > Serial Port Driver Test Cases in the Platform Builder Help.

The Serial Port Tests are designed to test that the serial port driver works properly and the API behaves correctly, and it should be pass all the test cases.

Table 17-3 describes the Serial Port driver test cases.

Table 17-3. Serial Port Driver Test Cases

Test Case	Description
1001	Configures the port and writes data to the port at all possible baud rates, data bits, parities, and stop bits. This test fails if it cannot send data on the port with a particular configuration.
1002	Tests the **SetCommEvent** and **GetCommEvent** functions. This test fails if the driver does not properly support the **SetCommEvent** or **GetCommEvent** functions.
1003	Tests the **EscapeCommFunction** function. This test fails if the driver does not support one of the Microsoft Win32 **EscapeCommFunction** functions.
1004	Tests the **WaitCommEvent** function on the EV_TXEMPTY event. The test creates a thread to send data and waits for the EV_TXEMPTY event to occur when the thread finishes sending data. This test fails if the **WaitCommEvent** function behaves improperly or if the EV_TXEMPTY event does not signal appropriately.
1005	Tests the **SetCommBreak** and **ClearCommBreak** functions. This test fails if the driver does not properly support the **SetCommBreak** or **ClearCommBreak** functions.

Table 17-3. Serial Port Driver Test Cases (continued)

Test Case	Description
1006	Makes the **WaitCommEvent** function return a value when the handle for the current COM port is cleared. This test fails if the **WaitCommEvent** function behaves improperly.
1007	Makes the **WaitCommEvent** function return a value when the handle for the current COM port is closed. This test fails if the **WaitCommEvent** function behaves improperly.
1008	Tests the **SetCommTimeouts** function and verifies that the **ReadFile** function properly times out when no data is received. This test fails if the COM timeouts do not function correctly.
1009	Verifies that previous Device Control Block (DCB) settings are preserved when the **SetCommState** function call fails with DCB settings that are not valid. This test fails if the serial port driver does not keep previous DCB settings when DCB settings that are not valid are passed to the driver.

17.6 Serial Driver API Reference

The detailed reference information for the serial driver may be found in the Platform Builder Help at the following location:

Developing a Device Driver > Windows CE Drivers > Serial Port Drivers > Serial Port Driver Reference

17.6.1 Serial PDD Functions

Table 17-4 shows a mapping of Serial PDD functions to the functions used in the serial driver.

Table 17-4. Serial PDD Functions

PDD Function Pointer	Serial Driver Function
HWInit	SerSerialInit
HWPostInit	SerPostInit
HWDeinit	SerDeinit
HWOpen	SerOpen
HWClose	SerClose
HWGetIntrType	SL_GetIntrType
HWRxIntrHandler	SL_RxIntrHandler
HWTxIntrHandler	SL_TxIntrHandler
HWModemIntrHandler	SL_ModemIntrHandler
HWLineIntrHandler	SL_LineIntrHandler
HWGetRxBufferSize	SL_GetRxBufferSize
HWPowerOff	SerPowerOff
HWPowerOn	SerPowerOn
HWClearDTR	SL_ClearDTR

Table 17-4. Serial PDD Functions (continued)

PDD Function Pointer	Serial Driver Function
HWSetDTR	SL_SetDTR
HWClearRTS	SL_ClearRTS
HWSetRTS	SL_SetRTS
HWEnableIR	SerEnableIR
HWDisableIR	SerDisableIR
HWClearBreak	SL_ClearBreak
HWSetBreak	SL_SetBreak
HWXmitComChar	SL_XmitComChar
HWGetStatus	SL_GetStatus
HWReset	SL_Reset
HWGetModemStatus	SL_GetModemStatus
HWGetCommProperties	SerGetCommProperties
HWPurgeComm	SL_PurgeComm
HWSetDCB	SL_SetDCB
HWSetCommTimeouts	SL_SetCommTimeouts

17.6.2 Serial Driver Structures

This section explains the serial driver structures.

17.6.2.1 UART_INFO

This structure contains information about the UART Module.

```
typedef struct {
    volatile PCSP_UART_REG    pUartReg;
    ULONG    sUSR1;
    ULONG    sUSR2;
    BOOL    bDSR;
    uartType_c    UartType;
    ULONG    ulDiscard;
    BOOL    UseIrDA;
    ULONG    HwAddr;
    EVENT_FUNC    EventCallback;
    PVOID    pMDDContext;
    DCB    dcb
    COMMTIMEOUTS    CommTimeouts;
    PLOOKUP_TBL    pBaudTable;
    ULONG    DroppedBytes;
    HANDLE    FlushDone;
    BOOL    CTSFlowOff;
    BOOL    DSRFlowOff;
    BOOL    AddTXIntr;
```

```
    COMSTAT    Status;
    ULONG    CommErrors;
    ULONG    ModemStatus;
    CRITICAL_SECTION    TransmitCritSec;
    CRITICAL_SECTION    RegCritSec
    ULONG    ChipID;
} UART_INFO, * PUART_INFO;
```

Parameters

pUartReg	Pointer to UART Hardware registers
sUSR1	This value contains the UART status register
sUSR2	This value contains the UART status register
bDSR	This boolean value keeps the DSR state
UartType	This value contains the type of UART like DCE or DTE
UlDiscard	This is used to discard the echo characters in IrDa Mode
UseIrDA	This boolean value determines the driver is in IR mode or not
HwAddr	This value contains the hardware address of the UART Module
EventCallback	This is a callback to the Model Device Driver
pMDDContext	This contains the context of the UART, which is the first parameter to the callback function
dcb	This value contains the copy of Device Control Block
CommTimeouts	This contains the copy of CommTimeouts structure used to get and set the time-out parameters for a communication device
pBaudTable	Pointer to baud rate table
DroppedBytes	This value contains the number of bytes dropped
FlushDone	Handle to the flush done event
CTSFlowOff	This boolean value is used to store the CTS flow control state
DSRFlowOff	This boolean value is used to Store the DSR flow control state
AddTXIntr	This boolean value is used to fake a Tx interrupt
Status	This value contains the comm status
CommErrors	This value contains Win32 comm error status
ModemStatus	This value shows the Win32 Modem status
TransmitCritSec	This value is used as Critical Section for UART registers
RegCritSec	This value is used as Critical Section for UART
ChipID	This value contains Chip identifier (CHIP_ID_16550 or CHIP_ID_16450)

17.6.2.2 SER_INFO

This is a private structure contains the information about the serial.

```
typedef struct __SER_INFO {
```

```
    UART_INFO    uart_info;
    BOOL    fIRMode;
    DWORD    dwDevIndex;
    DWORD    dwIOBase;
    DWORD    dwIOLen;
    PCSP_UART_REG pBaseAddress;
    UINT8    cOpenCount;
    COMMPROP    CommProp;
    PHWOBJ    pHWObj;
    BOOL        useDMA;
    DDK_DMA_REQ     SerialDmaReqTx;
    DDK_DMA_REQ     SerialDmaReqRx;
    PHYSICAL_ADDRESS SerialPhysTxDMABufferAddr;
    PHYSICAL_ADDRESS SerialPhysRxDMABufferAddr;
    PBYTE       pSerialVirtTxDMABufferAddr;
    PBYTE       pSerialVirtRxDMABufferAddr;
    UINT8       SerialDmaChanRx;
    UINT8       SerialDmaChanTx;
    UINT8       currRxDmaBufId;
    UINT8       currTxDmaBufId;
    UINT        dmaRxStartIdx;
    UINT        availRxByteCount;
    UINT32      awaitingTxDMACompBmp;
    UINT32      dmaTxBufFirstUseBmp;
    UINT16      rxDMABufSize;
    UINT16      txDMABufSize;
} SER_INFO, *PSER_INFO;
```

Parameters

uart_info	This structure contains information about UART
fIRMode	This boolean value determines the module is FIR or serial
dwDevIndex	This static value contains the device index value which is read from registry
dwIOBase	This static value contains the I/O Base address of UART module which is read from registry
dwIOLen	This static value contains the I/O length of UART Module which is read from registry
pBaseAddress	Pointer to the start address of the UART registers mapped
cOpenCount	Contains count of the concurrent open
CommProp	Pointer to CommProp structure
pHWObj	Pointer to PDDs HWObj structure
useDMA	This boolean flag indicates if SDMA is to be used for transfers through this UART
SerialDmaReqTx	SDMA request line for Tx
SerialDmaReqRx	SDMA request line for Rx
SerialPhysTxDMABufferAddr	Physical address of Tx SDMA address
SerialPhysRxDMABufferAddr	Physical address of Rx SDMA address

pSerialVirtTxDMABufferAddr	Virtual address of Tx SDMA address
pSerialVirtRxDMABufferAddr	Virtual address of Rx SDMA address.
SerialDmaChanRx	SDMA virtual channel indices for Rx
SerialDmaChanTx	SDMA virtual channel indices for Tx
currRxDmaBufId	Index of the buffer descriptor next expected to complete its SDMA in the Rx SDMA buffer descriptor chains
currTxDmaBufId	Index of the buffer descriptor next expected to complete its SDMA in the Tx SDMA buffer descriptor chains
dmaRxStartIdx	Keeps the start index of byte to be delivered to MDD for Read
availRxByteCount	This variable keeps the remaining bytes in the Rx SDMA buffer
awaitingTxDMACompBmp	Indicates if an SDMA request is in progress on Tx SDMA buffer descriptor
dmaTxBufFirstUseBmp	Indicator for first time use of a Tx SDMA buffer descriptor
rxDMABufSize	Receive DMA buffer size
txDMABufSize	Transfer DMA buffer size

Chapter 18
Switch Driver

The switch driver module provides connectivity with an 3 port Programmable Ethernet switch engine, which is compatible with 10/100 Mbps MAC-NET core. The driver is Network Driver Interface Specification (NDIS) 4.0 compliant miniport driver. This port provides interface to configure switch function such as VLAN, mirror, snooping, and so on.

18.1 Switch Driver Summary

Table 18-1 provides a summary of source code location, library dependencies, and other BSP information.

Table 18-1. Switch Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	N/A
SOC Common Path	N/A
SOC Specific Path	N/A
Platform Driver Path	..\PLATFORM*COMMON*\SRC\SOC\COMMON_FSL_V2\SWITCH
Import Library	N/A
Driver DLL	enetswi.dll
Catalog Item	Third Party > BSP > Freescale i.MX28 EVKPDK1_9:ARMV4I > Device Drivers >ENET Driver > ENET Switch Driver
SYSGEN Dependency	SYSGEN_NDIS=1 SYSGEN_TCPIP=1 SYSGEN_WINSOCK=1
BSP Environment Variables	BSP_ENETSWI=1

18.2 Supported Functionality

The switch driver enables the system to provide the following support:

1. Compliant with the NDIS 4.0 miniport driver
2. 10/100 Mbps network
3. MII PHY or RMII PHY
4. Filters and forward traffic at wire-speed on all ports
5. Implements hardware switching look-up mechanism providing a learning capacity of upto 2K MAC addresses.

6. Supports configurable VLAN switching when MAC address lookup should be omitted.
7. Programmable Multicast destination port mask to restrict frame duplication for individual multicast addresses.
8. Multicast and Broadcast resolution with VLAN domain filtering providing a strict separation of upto 32 VLANs.
9. IP Snooping with programmable protocol and port number registers.
10. Event and status signals, which can be used to monitor port activity, severe error conditions, or any user specific event.
11. Support for 1588 precise time stamping applications

18.3 Hardware Operation

The switch driver module provides connectivity with an 3 port Programmable Ethernet switch engine, which is compatible with 10/100 Mbps MAC-NET core. It provides registers to configure switch functions. Refer to switch chapter in i.MX28 *Reference Manual* for detailed hardware operation and programming information.

18.3.1 Conflicts with Other SoC Peripherals

No conflicts.

18.3.2 Conflicts with i.MX28 EVK Peripherals

Conflict with ENET1 and ENET2.

18.4 Software Operation

The basic driver is compliant with NDIS 4.0 miniport driver architecture. Refer to the Platform Builder Help for more details at:

Developing a Device Driver > Windows Embedded CE Drivers > Network Drivers > Network Driver Development Concepts > Miniports, Intermediate Drivers, and Protocol Drivers.

It also provide the interface and an application for switch function configuration. After initialization, the module provides basic 3 port switch basic function. For advanced features, use the application to set or clear the corresponding switch register to enable them such as input/output VLAN, port mirror, IP snooping, port snooping, and so on.

18.4.1 Switch Driver Registry Settings

The following registry keys are required to load switch driver:

```
IF BSP_ENETSWI
[HKEY_LOCAL_MACHINE\Comm\ENETSWI]
   "DisplayName"="ENET Switch Driver"
   "Group"="NDIS"
   "ImagePath"="enetswi.dll"
```

```
   "Index"=dword:0

[HKEY_LOCAL_MACHINE\Comm\ENETSWI\Linkage]
   "Route"=multi_sz:"ENETSWI1"

[HKEY_LOCAL_MACHINE\Comm\ENETSWI1]
   "DisplayName"="ENET Switch Driver"
   "Group"="NDIS"
   "ImagePath"="enetswi.dll"

[HKEY_LOCAL_MACHINE\Comm\ENETSWI1\Parms]
   "BusNumber"=dword:0
   "BusType"=dword:0
   ; DuplexMode: 0:AutoDetect; 1:HalfDuplex; 2:FullDuplex.
   "DuplexMode"=dword:0
   ; The Ethernet Physical Address. For example,
   ; Ethernet Address 00:24:20:10:bf:03 is MACAddress1=0024,
   ; MACAddress2=2010,and MACAddress3=bf03.
   "MACAddress1"=dword:1213
   "MACAddress2"=dword:1728
   "MACAddress3"=dword:3120

[HKEY_LOCAL_MACHINE\Comm\ENETSWI1\Parms\TcpIp]
   ; This should be MULTI_SZ
   "DefaultGateway"=""
   ; This should be SZ... If null it means use LAN, else WAN and Interface.
   "LLInterface"=""
   ; Use zero for broadcast address? (or 255.255.255.255)
   "UseZeroBroadcast"=dword:0
   ; Thus should be MULTI_SZ, the IP address list
   "IpAddress"="0.0.0.0"
   ; This should be MULTI_SZ, the subnet masks for the above IP addresses
   "Subnetmask"="0.0.0.0"
   "EnableDHCP"=dword:1

[HKEY_LOCAL_MACHINE\Comm\TcpIp\Parms]

   ;Set to True to keep the device from entering idle mode if there's network adapter
    ;;"NoIdleIfAdapter"=dword:1
    ;Set to True to keep the device from entering idle mode while communicating/loop back
    "NoIdleIfConnected"=dword:1

[HKEY_LOCAL_MACHINE\Comm\Tcpip\Linkage]
   ; This should be MULTI_SZ
   ; This is the list of llip drivers to load
   "Bind"=multi_sz:"ENETSWI1"
ENDIF ;  BSP_ENETSWI
```

18.5 Unit Test

The switch unit test mainly focuses on the switch feature, seperated into basic and advanced feature. Capture the frame in the network to verify the switch feature.

18.5.1 Unit Test Hardware

The i.MX28 EVK board requires 3 PCs, two for connection test, and one for frame sniffer.

NOTE

Sniffer PC's registry has to be modified for VLAN tag analysis, if Broadcom NetXtreme 57xx Gbit Controller NIC is used.

Execute the following steps to run the Unit Test Hardware:

1. Run the Registry Editor (regedt32).
2. Search for TxCoalescingTicks and ensure that it is the only instance.
3. Right click the instance number (for example, 0008) and add a new string value.
4. Enter PreserveVLANInfoInRxPacket and enter the value as 1.
5. Restart computer.

18.5.2 Unit Test Software

WireShark (Ethereal).

SwitchSetting.exe (for WinCE) tool for switch feature configuration. Refer to Section 18.7.1, "SwitchSetting Usage," for more information.

18.5.3 Basic Feature Unit Test

Switch module provides basic frame forward function. Connect 2 PCs to ENET port1 and ENET port2, set the IP address for both the PCs and the test board, so that they could connect with each other. Connect one port to the public network, test board and the other PC can access the public network.

18.5.4 Advanced Feature Unit Test

This section explains the advanced feature unit tests.

18.5.4.1 Port Enable/Disable

Port Enable Bits. Two bits per port. The transmit and receive direction for each port can be enabled independently. When the transmit direction is enabled, a frame can be forwarded to the port. When disabled, all frames that are forwarded to the port are discarded. When the receive direction is enabled, the port is selected and a frame is accepted if it indicates data availability. If the receive direction is disabled, the input is ignored and it is never selected for frame reception.

1. Connect two PCs to ENET port1 and ENET port2.
2. Set IP address for each PC such as 192.168.1.1 for PC1 and 192.168.1.2 for PC2.
3. Ensure that port1 and port2 are enabled.
4. Test the connection by pinging PC2 from PC1.
5. Disable port1 or port2, PC1 cannot connect with PC2.

6. Test other ports in the same way.

18.5.4.2 Verifying the VLAN Domain

Provide the VLAN verify bit and discard bit for each port. If the VLAN verify bit is set, frames carry VLAN tag through the port and they are checked. The VLAN resolution table (VLAN domain resolution entry) is searched for matching VLAN id. Frame can be forwarded only when both input and output ports are members of VLAN domain. When the discard bit is set, a frame is received with a VLAN ID that is unknown, or has no VLAN tag. The frame is discarded and is not forwarded.

1. Send frame from PC1, which carries the VLAN tag, a ping packet for instance. Run Wireshark on sniffer PC to confirm that.
2. Connect two PCs to ENET port1 and ENET port2.
3. Set the IP address for each PC, such as 192.168.1.1 for PC1 and 192.168.1.2 for PC2.
4. Enable port1 and port2 VLAN verify.
5. PC1 sends ping frame which carries VLAN tag to PC2. The VLAN resolution table (VLAN domain resolution entry) is searched for matching VLAN id. Frame is forwarded to ports within the VLAN domain and is discarded if the destination port is not a member of the VLAN domain. If port1 and port2 are members of the corresponding VLAN domain, PC1 could connect with PC2.
6. PC1 sends ping frame without VLAN tag to PC2, untagged frame would be forward.
7. Enable port1 and port2 discard bit, untagged frame would be discarded, and PC1 can not connect with PC2.
8. Test other ports in the same way.

Figure 18-1 shows the VLAN domain verification screen.

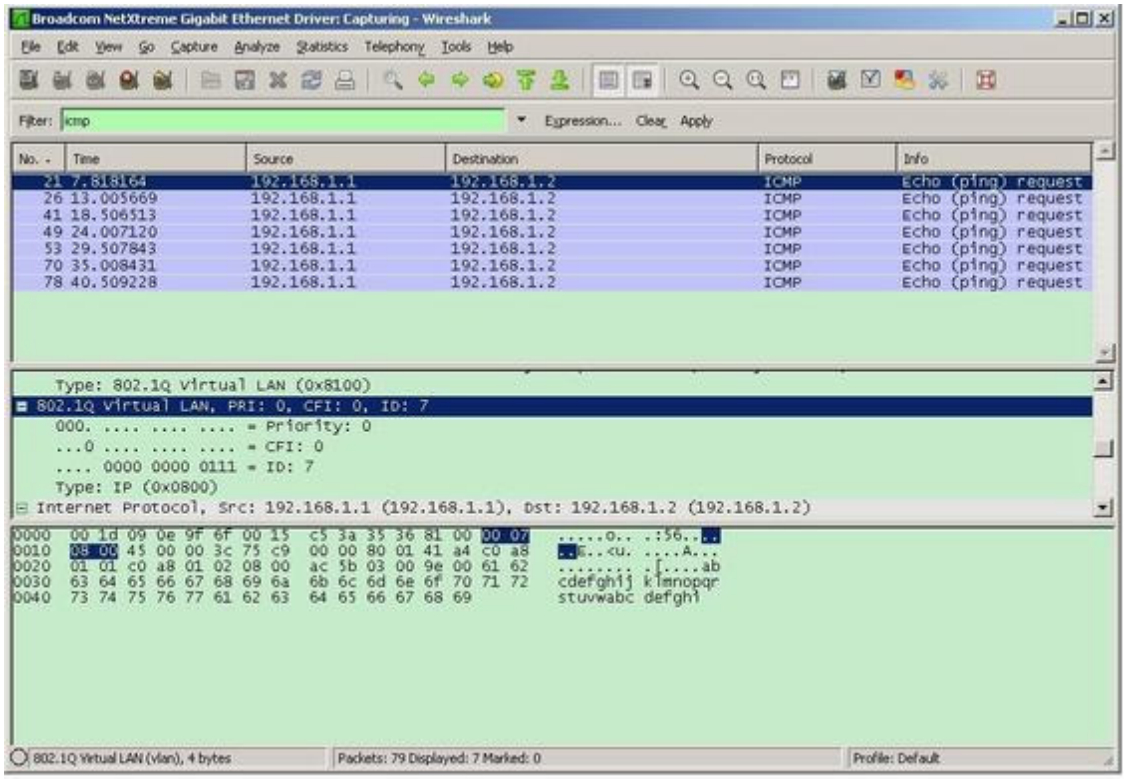

Figure 18-1. Verify VLAN Domain

18.5.4.3 Default Broadcast Resolution

1 bit per port. For broadcast/flooding resolution.

Execute the following steps to set the default broadcast resolution:

1. Connect one PC to ENET port1 and connect the sniffer PC to ENET port2.
2. Set the IP address for each PC, such as 192.168.1.1 for PC1 and 192.168.1.2 for sniffer PC.
3. Set port2 broadcast mask bit to 1.
4. Send ARP frame from PC1, the frame can be captured by sniffer PC.
5. Set port2 broadcast mask bit to 0.
6. Send ARP frame from PC1, the frame cannot be captured by sniffer PC.
7. Test other ports in the same way.

18.5.4.4 Default multicast resolution

1 bit per port. For broadcast/flooding resolution, instead of default broadcast resolution when the received frame carries a multicast address.

Execute the following steps to set the default multicast resolution:

1. Connect the sniffer PC to ENET port2 and connect ENET port1 to a public network.

2. Ensure that all multicast mask bit is set to 1.
3. Capture the multicast frame using the Sniffer PC such as STP frame that are forwarded by the switch.
4. Set the ENET port1 multicast mask bit to 0, sniffer PC cannot capture multicast frame.
5. Test ENET port2 in the same way.

Figure 18-2 shows the multicast resolution screen.

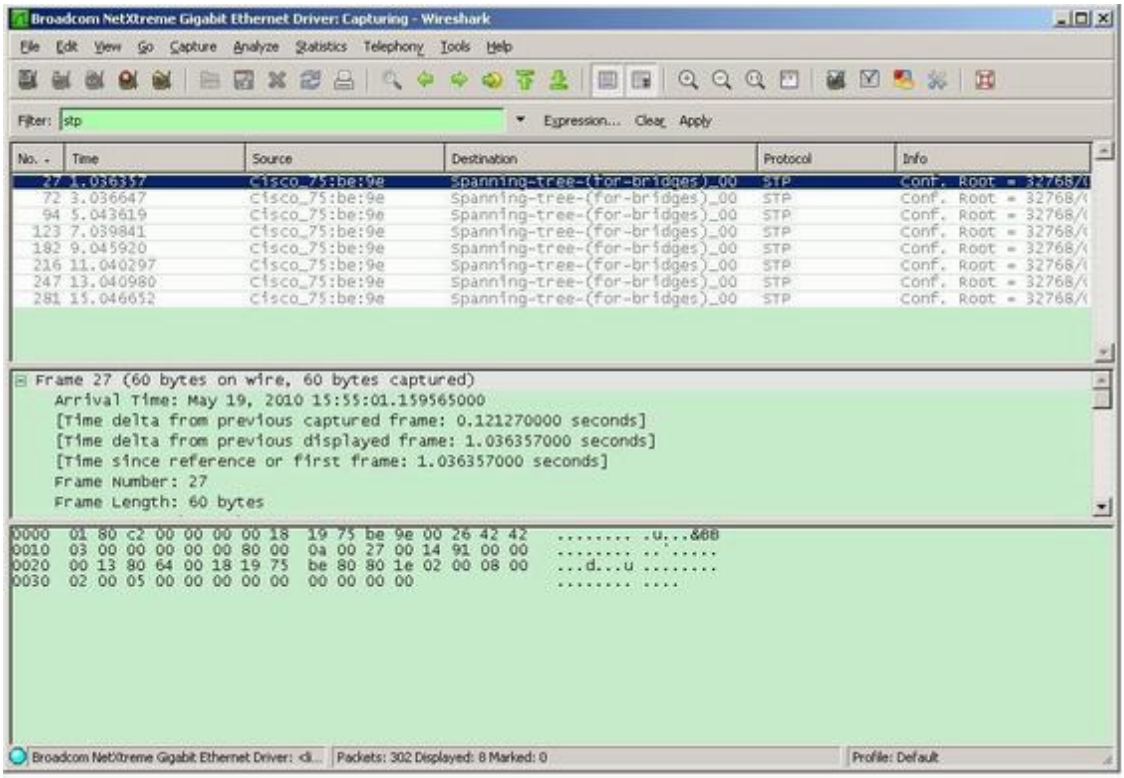

Figure 18-2. Multicast Resolution

18.5.4.5 Defining the port in Blocking State and Enable or Disable Learning

When blocking is enabled for a port, only Bridge Protocol data units are accepted on that input. Other frames are discarded.When learning is disabled for a port, only Bridge Protocol Data Unit frames are learned. Other frames are ignored for learning.

1. Connect the sniffer PC to ENET port2 and connect ENET port1 to a public network.
2. Confirm that all block enable bits are set to 0.
3. Sniffer PC captures all kinds of frames.
4. Set the ENET port1 block enable bit to 1.
5. The Sniffer PC can capture only BPDU frames (such as STP frame).
6. If learning bit set to 1, then the switch learns only from the BPDU frame.

Figure 18-3 shows the Input Blocking and Learning screen.

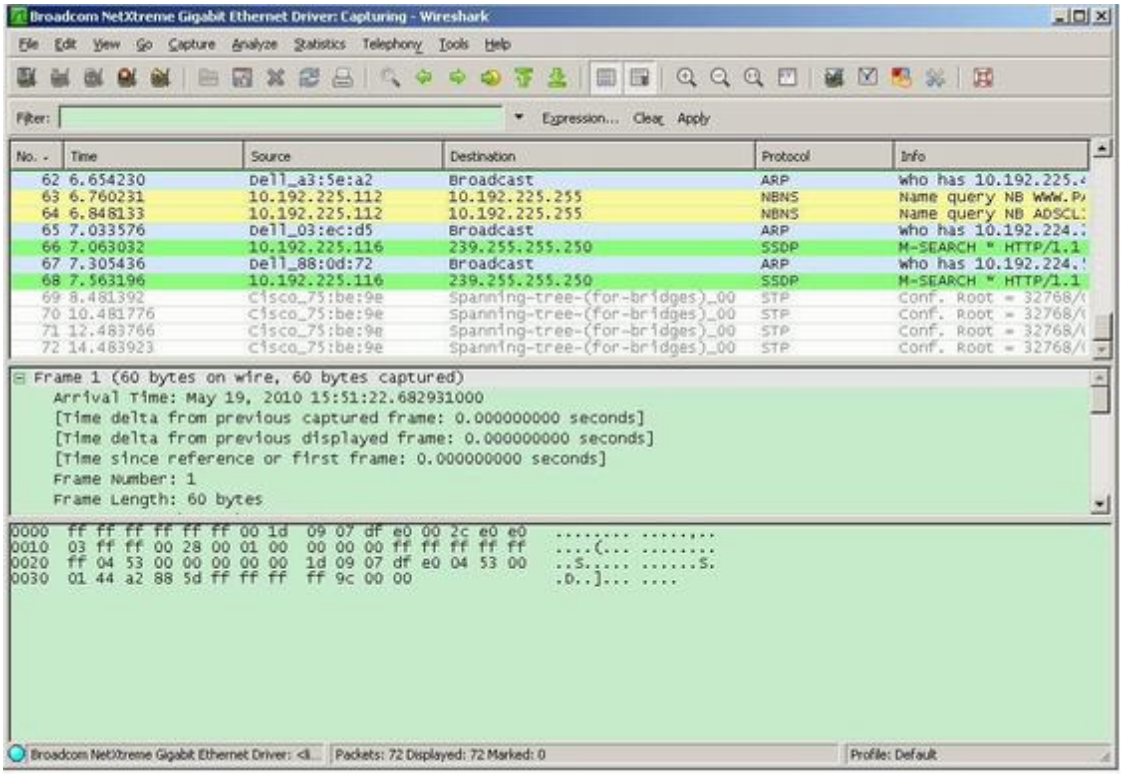

Figure 18-3. Input Blocking and Learning

18.5.4.6 Bridge Management Port Configuration

Port bit means the number of port that should act as a management port. Relevant to all functions that forward frames to the management port (i.e. BPDU processing, snooping).

NOTE

Management port must be set 0 in the switch configuration (Port 0 to DMA0 is the management port).

.If the Enable bit is set, then all BPDU frames are forwarded only to the management port. If cleared, the BPDU frames are forwarded as any other frame or discarded if the discard bit is set.

1. Connect the sniffer PC to ENET port2 and connect the ENET port1 to a public network.
2. Port bit must be set 0 in switch configuration.
3. If the discard bit is set, the BPDU frame is discarded and the sniffer PC cannot capture them.

18.5.4.7 Port Mirroring Configuration

Define mirror port and filtering conditions. Portx bit means the number of ports that should act as the mirror port and receive all mirrored frames. Mirror_enable to enable the mirror feature. Other bit to enable the corresponding filtering conditions.

1. Connect one PC to ENET port1 and connect the sniffer PC to ENET port2.
2. Set the IP address for each endpoint, such as 192.168.1.2 for sniffer PC, 192.168.1.1 for PC1 and 192.168.1.3 for DUT ENETSWI1.
3. Set portx bit and mirror_enable bit to 1 to set port1 as mirror port and enable mirror function.
4. If ing_map_enable bit is set, an ingress port bit is set in the ingress map (Port mirroring ingress port definitions) is mirrored.
5. If eg_map_enable bit is set, an output port bit is set in the egress map (Port mirroring egress port definitions) are mirrored.
6. If ing_sa_match bit is set, frames transmitted on an ingress port with source address matching with the value in register MIRROR_ISRC (Ingress source MAC address for mirroring) are mirrored.
7. If ing_da_match bit is set, frames transmitted on an ingress port with destination address matching with the value in the register MIRROR_IDST (Ingress destination MAC address for mirroring) are mirrored.
8. If eg_sa_match bit is set, frames transmitted on an egress port with source address matching with the value in the register MIRROR_ESRC (Egress source MAC address for mirroring) are mirrored.
9. If eg_da_match bit is set, frames transmitted on an egress port with destination address matching with the value in register MIRROR_EDST (Egress destination MAC address for mirroring) are mirrored.

Figure 18-4 shows the mirror configuration screen.

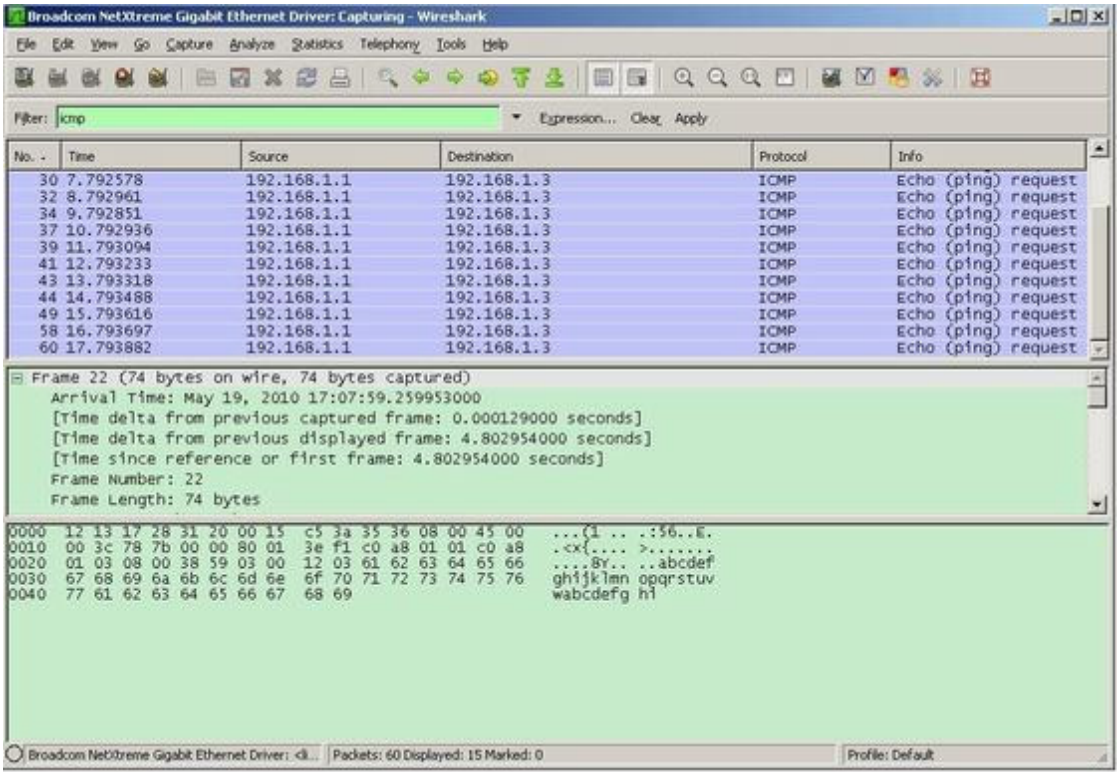

Figure 18-4. Mirror Configuration

18.5.4.8 Port Mirroring Egress Port Definitions

1 Bit per Port. If it is enabled, frames assigned to the port(s) are mirrored to the mirror port. Refer to Section 18.5.4.7, “Port Mirroring Configuration,” for more information.

18.5.4.9 Port mirroring ingress port definitions

Port mirroring ingress port definitions. 1 Bit per Port. If it is enabled, the frames from the port(s) are mirrored to the mirror port. Refer to Section 18.5.4.7, “Port Mirroring Configuration,” for more information.

18.5.4.10 Ingress Source MAC Address For Mirroring

Two registers, MIRROR_ISRC_0 and MIRROR_ISRC_1 are available. MIRROR_ISRC_0 contains first 4 bytes of MAC address. First byte of MAC address is 7:0, .. , 4th byte is 31:24. MIRROR_ISRC_1 contains last 2 bytes of MAC address. 5th byte in 7:0 and 6th byte in 15:8. Refer to Section 18.5.4.7, “Port Mirroring Configuration,” for more information.

18.5.4.11 Ingress Destination MAC Address for Mirroring

Two registers, MIRROR_IDST_0 and MIRROR_IDST_1 are available. Refer to Section 18.5.4.10, "Ingress Source MAC Address For Mirroring," and Section 18.5.4.7, "Port Mirroring Configuration," for more information.

18.5.4.12 Egress source MAC address for mirroring

Two registers, MIRROR_ESRC_0 and MIRROR_ESRC_1 are available. Refer to Section 18.5.4.10, "Ingress Source MAC Address For Mirroring," and Section 18.5.4.7, "Port Mirroring Configuration," for more information.

18.5.4.13 Egress destination MAC address for mirroring

Two registers, MIRROR_EDST_0 and MIRROR_EDST_1 are available. Refer to Section 18.5.4.10, "Ingress Source MAC Address For Mirroring," and Section 18.5.4.7, "Port Mirroring Configuration," for more information.

18.5.4.14 Count Value for Mirroring

Every Nth frame is forwarded to the mirror port if it is enabled. A value of 0 or 1 means every frame. Valid values are 0..255.

NOTE

If the egress filtering port map is active, then each forwarded frame is considered. Otherwise, frames are counted only if the mirroring decision indicates that the frame should be mirrored.

If the value is set to a valid value N (0–255), every Nth frame is forward to the mirror port. A value 0 and 1 means every frame.

18.5.4.15 Port snooping (8 Entries)

Eight independent entries are available.When the Enable bit is set, the entry contains a valid data and the function is active. If a match with the TCP/UDP destination port value occurs, the frame is processed as defined by the mode setting.

1. Set Enable bit to enable the function.
2. Define the forwarding mode as follows:
   - 00 - forward frames to designated management port
   - 01 - copy to management port and forward normally
   - 10 - discard frame. Management port defined in MGMT_CONFIG (Bridge management port configuration).
3. If compare_dest bit is set, TCP or UDP destination port numbers in the frame are compared with the value set in the Destination_port bit register.

4. If the compare_source bit is set, TCP or UDP source port number in the frame is compared with the value set in register (Destination_port bit).
5. Destination_port is the bit mentioned above. It contains 16-bit port number to compare within TCP or UDP header of a frame. Figure 18-5 shows the port snooping.

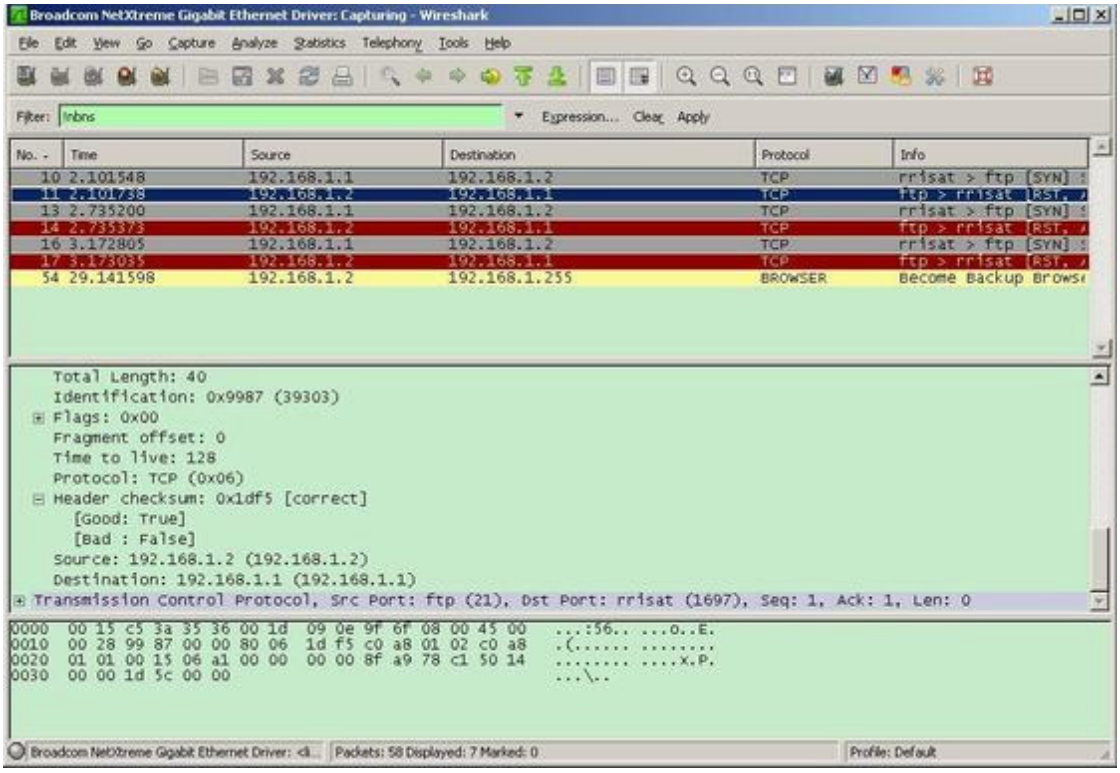

Figure 18-5. Port Snooping

18.5.4.16 IP snooping (8 Entries)

8 independent entries are available.When the Enable bit is set, the entry contains a valid data and the function is active. If a match with the protocol value occurs, then the frame is processed as defined by the mode setting.

1. Set the Enable bit to enable the function.
2. Define forwarding mode when an IP frame is received and the protocol field matches the protocol value (protocol bit) as follows:
   - 00 forward frames to designated management port
   - 01 copy to management port and forward normally
   - 10 discard frame. Management port defined in MGMT_CONFIG (Bridge management port configuration).
3. If the Protocol bit is the bit mentioned above. It contains an 8-bit protocol value to match with the incoming frame's IP header protocol field.

Figure 18-5 shows the IP snooping.

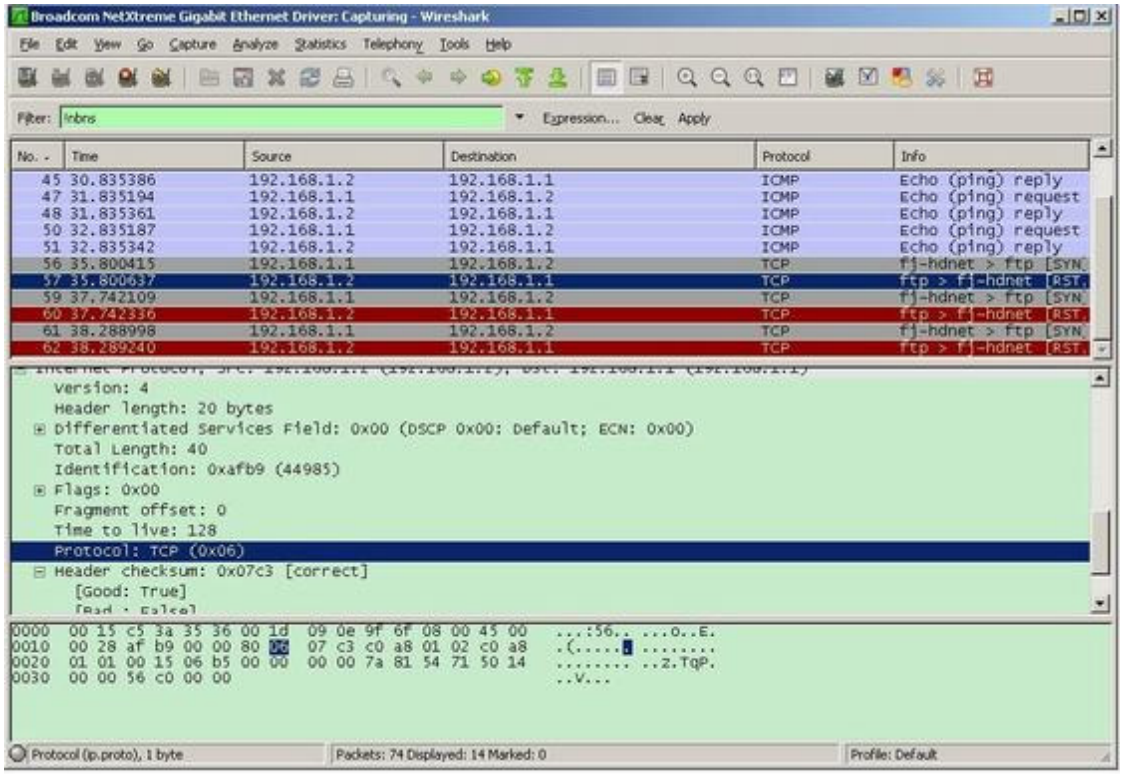

Figure 18-6. IP Snooping

18.5.4.17 VLAN Priority Resolution Map (P0–P2)

It implements a 3-bit to 3-bit VLAN priority mapping capability. The current frame's 3-bit VLAN priority field is used as an index and the corresponding priority is taken from the respective position of the register giving the final classification for the frame.

18.5.4.18 IPV4 and IPV6 Priority Resolution Table

Address bit is used to specify the address of the entry. If IPv4 select bit is set, then the IPv4 table is accessed. If cleared, then the IPV6 table is accessed. Priority port n means the priority information to write into the addressed table entry. These 2 bits represent the output priority selected when the frame is received on port n. 00=priority 0 (forwarded to output queue 0), 01=priority 1 (output queue 1), 10=priority 2 (output queue 2), 1=priority 3 (output queue 3). When reading from the register, the bits show the value from the addressed table entry (address from last write operation).

18.5.4.19 Priority Resolution Configuration (P0–P2)

Enable VLAN priority resolution for the received frames on port n. If set, the VLAN tag field of a frame is inspected and priority is resolved based on the setting in the VLAN_PRIORITYn for the port on which the frame is received.Enable IP priority resolution for frame received on port n. If set, the IP DiffServ/COS field is used and priority is resolved based on the IP_PRIORITYn setting for the port. Enable MAC based

priority resolution for the frame received on port n. If set, then the priority information available in the MAC address table is used.The default priority of a frame received on port n, if none of the priority resolutions could define a priority of the frame.

18.5.4.20 VLAN Domain Resolution Entry (32 Entries)

VLAN domain resolution entry is from 0–31. Bits 2..0: One bit per port that is member of the VLAN identified with the 12-bit VLAN ID of the entry. Bits 14..3: 12-bit VLAN identifier. Refer to the Section 18.5.4.2, "Verifying the VLAN Domain," for verifying the VLAN domain resolution.

18.6 Switch API Reference

The basic switch driver is compliant with the NDIS 4.0 miniport network drivers specification by Microsoft. Refer to the CE help for information on basic NDIS driver functions, methods and structures at:

Developing a Device Driver > Windows Embedded CE Drivers > Network Drivers > Network Driver Reference.

18.7 Appendix

18.7.1 SwitchSetting Usage

Usage:

Query value: switchsetting <-REGISTER_NAME> <-query> <-BIT_NAME>

Set value: switchsetting <-REGISTER_NAME> <-set> <-BIT_NAME> <VALUE>

Port Enable/Disable:

switchsetting -PORTENA -query

switchsetting -PORTENA -set -ENA_TRANSMIT_0 0 -ENA_TRANSMIT_1 0 -ENA_TRANSMIT_2 0 -ENA_RECEIVE_0 0 -ENA_RECEIVE_1 0 -ENA_RECEIVE_2 0

Verify VLAN Domain:

switchsetting -VLANVERIFY -query

switchsetting -VLANVERIFY -set -VLAN_VERIFY_0 0 -VLAN_VERIFY_1 0 -VLAN_VERIFY_2 0 -DISCARD_P0 0 -DISCARD_P1 0 -DISCARD_P2 0

VLAN Domain Resolution Entry:

switchsetting -VLANRESTABLE -query -ENTRY 0

switchsetting -VLANRESTABLE -set -ENTRY 0 -PORT_0 0 -PORT_1 0 -PORT_2 0 -VLAN_ID 0

NOTE

Valid entry values are 0–31.

Default Broadcast Resolution:

switchsetting -BCASTDEFAULTMASK -query

switchsetting -BCASTDEFAULTMASK -set -BCAST_DEFAULT_MASK_0 0 -BCAST_DEFAULT_MASK_1 0 -BCAST_DEFAULT_MASK_2 0

Default Multicast Resolution:

switchsetting -MCASTDEFAULTMASK -query

switchsetting -MCASTDEFAULTMASK -set -MCAST_DEFAULT_MASK_0 0 -MCAST_DEFAULT_MASK_1 0 -MCAST_DEFAULT_MASK_2 0

Define Port in Blocking State and Enable or Disable Learning:

switchsetting -INPUTLEARNBLOCK -query

switchsetting -INPUTLEARNBLOCK -set -BLOCKING_ENA_P0 0 -BLOCKING_ENA_P1 0 -BLOCKING_ENA_P2 0 -LEARNING_DIS_P0 0 -LEARNING_DIS_P1 0 -LEARNING_DIS_P2 0

Bridge Management Port Configuration:

switchsetting -MGMTCONFIG -query

switchsetting -MGMTCONFIG -set -PORT 0 -MESSAGE_TRANSMITTED 0 -ENABLE 0 -DISCARD 0 -PRIORITY 0 -PORTMASK 0

Port Mirroring Control:

switchsetting -MIRRORCONTROL -query

switchsetting -MIRRORCONTROL -set -PORTx 0 -MIRROR_ENABLE 0 -ING_MAP_ENABLE 0 -EG_MAP_ENABLE 0 -ING_SA_MATCH 0 -ING_DA_MATCH 0 -EG_SA_MATCH 0 -EG_DA_MATCH 0

Port Mirroring Configuration:

switchsetting -MIRRORCONFIG -query

switchsetting -MIRRORCONFIG -set -ING_MAP 0 -EG_MAP 0 -ISRC_0 0 -ISRC_1 0 -IDST_0 0 -IDST_1 0 -ESRC_0 0 -ESRC_1 0 -EDST_0 0 -EDST_1 0 -CNT 0

NOTE

MIRRORCONFIG command sets all the mirror configurations.

The following arguments are registers names:

- Register ING_MAP bits 0–2 are mapped to port 0–2,
- if ING_MAP is set to 1, then port0 is mirrored.
- If set to 2, port1 is mirrored.
- If set to 3, both port0 and port1 are mirrored and so on. EG_MAP is the same.

Port Snooping:

switchsetting -PORTSNOOP -query -ENTRY 0

switchsetting -PORTSNOOP -set -ENTRY 0 -ENABLE 0 -MODE 0 -COMPARE_DEST 0 -COMPARE_SOURCE 0 -DESTINATION_PORT 0

NOTE

Valid entry values are 0–7.

IP Snooping:

switchsetting -IPSNOOP -query -ENTRY 0

switchsetting -IPSNOOP -set -ENTRY 0 -ENABLE 0 -MODE 0 -PROTOCOL 0

NOTE

Valid entry values are 0–7.

VLAN Priority Resolution Map:

switchsetting -VLANPRIORITY -query -PORT 0

switchsetting -VLANPRIORITY -set -PORT 0 -P0 0 -P1 0 -P2 0 -P3 0 -P4 0 -P5 0 -P6 0 -P7 0

NOTE

Valid port values are 0–2.

IPV4 and IPV6 Priority Resolution Table:

switchsetting -IPPRIORITY -query

switchsetting -IPPRIORITY -set -ADDRESS 0 -IPV4_SELECT 0 -PRIORITY_PORT0 0 -PRIORITY_PORT1 0 -PRIORITY_PORT2 0 -READ 0

Priority Resolution Configuration:

switchsetting -PRIORITYCFG -query -PORT 0

switchsetting -PRIORITYCFG -set -PORT 0 -VLAN_EN 0 -IP_EN 0 -MAC_EN 0 -DEFAULT_PRIORITY 0

NOTE

Valid port values are 0–2.

Chapter 19
Touch Panel Driver

The touch screen interface provides all the circuitry required for a 4-wire resistive touch screen. The touch screen X plate is connected to TSX1 and TSX2 and the Y plate is connected to TSY1 and TSY2. A local supply ADREF serves as reference.

19.1 Touch Panel Driver Summary

Table 19-1 provides a summary of source code location, library dependencies, and other BSP information.

Table 19-1. Touch Panel Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	N/A
SOC Common Path	..\PLATFORM\COMMON\SRC\SOC\COMMON_FSL_V2_PDK1_9\TOUCHVS
SOC Specific Path	N/A
Platform Specific Path	..\PLATFORM\\<*Target Platform*>\SRC\DRIVERS\TOUCH
Driver DLL	touch.dll
SDK Library	N/A
Catalog Item	Third Party > BSP > Freescale i.MX28 EVK PDK1_9:ARMV4I > Device Drivers > TOUCH > Touchscreen
SYSGEN Dependency	SYSGEN_TOUCH = 1
BSP Environment Variables	BSP_LRADC = 1

19.2 Supported Functionality

The touch panel should conform to the standards as explained in the documentation below:

Developing a Device Driver > Windows Embedded CE Drivers > Touch Screen Drivers

19.3 Hardware Operations

The hardware consists of low resolution analog-to-digital converters and touch screen interface. The touch screen controller configures the LRADC driver required to measurement the X and Y values of the touchscreen.

19.4 .Software Operations

The touch screen driver reads user input from the touch screen hardware and converts the input to touch events. The touch screen events are then sent to the Graphics, Windowing, and Events Subsystem (GWES). The driver also converts un-calibrated coordinates to calibrated coordinates. Calibrated coordinates compensate for any hardware anomalies, such as skew or nonlinear sequences.

For the touch screen driver to work properly, it has to submit points while the user's finger or stylus is touching the touch screen. When the user's finger or stylus is removed from the screen, the driver must submit at least one final event indicating that the user's finger or stylus tip is removed. The calibrated coordinates must be reported to the nearest one-quarter of a pixel.

The following steps detail the basic algorithm that are used to sample and calibrate the screen with the touch screen driver:

1. Call the `TouchPanelEnable` function to start the screen sampling.
2. Call the `TouchPanelGetDeviceCaps` function to request the number of sampling points.

For every calibration point, perform the following steps:

1. Call `TouchPanelGetDeviceCaps` function to get a calibration coordinate. A crosshair appears on the screen, touching the cross hair starts the calibration
2. Call the `TouchPanelReadCalibrationPoint` function to get the calibration data.
3. Call the `TouchPanelSetCalibration` function to calculate the calibration coefficients.

19.4.1 Touch Driver Registry Settings

```
IF BSP_NOTOUCH !
IF BSP_LRADC_TOUCH
[HKEY_LOCAL_MACHINE\HARDWARE\DEVICEMAP\TOUCH]
    "DriverName"="touch.dll"
    "MaxCalError"=dword:7
IF BSP_PRECAL
    "CalibrationData"="539,520 280,259 280,778 793,781 794,259"

    ; Welcome.exe: Disable tutorial and calibration pages because we already
    ; have the necessary calibration data.
    ; Touch calibration (0x02), Stylus (0x04), Popup menu (0x08),
    ; Timezone (0x10), Complete (0x20)
[HKEY_LOCAL_MACHINE\Software\Microsoft\Welcome]
    "Disable"=dword:FFFFFFFF
ENDIF ; BSP_PRECAL

; For double-tap default setting
[HKEY_CURRENT_USER\ControlPanel\Pen]
    "DblTapDist"=dword:18
    "DblTapTime"=dword:637

; For launching the TouchPanel calibration application on boot.
[HKEY_LOCAL_MACHINE\init]
"Launch80"="touchc.exe"
"Depend80"=hex:14,00,1e,00 ; Wait for standard initialization
                           ; modules to load first (GWES.dll and
                           ; Device.exe).
```

```
ENDIF ; BSP_LRADC_TOUCH
ENDIF ; BSP_NOTOUCH !
```

19.5 Unit Tests

This section explains the unit tests.

19.5.1 Unit Test Hardware

Table 19-2 lists the hardware required to run the unit tests.

Table 19-2. Hardware Requirements

Requirement	Description
LCD panel	Display panel required for displaying graphics data.

19.5.2 Unit Test Software

Table 19-3 lists the software required to run the unit tests.

Table 19-3. Software Requirements

Requirement	Description
Tux.exe	Tux test harness, which is needed for executing the test
Kato.dll	Kato logging engine, which is required for logging test data
Ktux.dll	Ktux.dll which is required to run in kernel mode
Touchtest.dll	The Test.dll File
Touch.dll	Touch Panel Driver

NOTE

The touch driver works after the CETK Touch Panel Test. This is a known MSFT CETK issue. In the MSFT online help it is mentioned that when the test is complete, the OS does not regain control of the touch panel. The touch panel should be reset to restore normal operation. Refer to **CETK Tests and Test Tools > CETK Tests > Touch Panel Tests**

Cases 8011, 9001–9003 fail. The touch panel shows several lines when a circle or a arc is drawn. This is also a known MSFT CETK issue. All these points are captured.

Case 8011 cannot draw in the right part of screen after a 90° rotation. ethca.exe works after rotation and the CETK works when the case runs again.

19.5.3 Running the Touch Panel Tests

The touch panel test cases can be run by entering the following:

```
tux -o -n -d touchtest.dll -x <Test case id>
```

The test case IDs are described in the documentation at:

Windows Embedded CE Test Kit > CETK Tests and Test Tools >CETK Tests > Touch Panel Tests > Touch Panel Test

19.6 Touch Panel API Reference

The complete API reference is available in the documentation at:

Developing a Device Driver > Windows Embedded CE Drivers > Touch Screen Drivers > Touch Screen Driver Reference

Chapter 20
Universal Serial Bus (USB) On The Go (OTG) Driver

A USB OTG driver provides High Speed USB 2.0 host and peripheral support for the USB OTG port of the i.MX chip. The OTG driver automatically performs a host or peripheral functionality at any given time, depending on the type of USB cable plugged in. There are 3 components to achieve this functionality: USB host driver, USB peripheral driver, and USB OTG driver. The OTG driver maintains a state machine to decide whether a host driver or peripheral driver to be in charge. The OTG driver is also called as **Pin Detection Driver**, as the OTG functionality logic depends on the kind of USB cable plugged in.

Many class drivers are supported in WinCE. The host driver can be configured to work with mass storage, HID, printer, and RNDIS peripherals. The peripheral driver can be configured to provide mass storage, serial, or RNDIS functionality. The peripheral class supports are mutually exclusive, so that only one configuration can be selected as active configuration. The host functionality support do not have such limitation, and hence can recognize what kind of peripheral is plugged in and pick the right class driver to provide functionality.

Besides full OTG functionality, pure host driver and pure client driver options are also provided. These 2 options configure the BSP to work in a host-only or peripheral-only mode. In this case, pin detection driver is not active and no mode change happens between the host and the peripheral.

20.1 USB OTG Driver Summary

This section explains about the OTG port peripheral driver, host driver, and OTG driver.

20.1.1 OTG Peripheral Driver Summary

Table 20-1 lists the attributes of the OTG peripheral driver.

Table 20-1. OTG Peripheral Driver Summary

Driver Attribute	Definition
Target Platform	iMX28-EVK-PDK1_9
Target SOC	MX28_FSL_V2_PDK1_9
Common SOC	COMMON_FSL_V2
CSP Driver Path	..\SOC\<*Target SOC*>\USBD ..\SOC\<*Common Soc*>\ms\USBFN
CSP Static Library	usb_usbfn_<*Target SOC*>_PDK1_9.lib usb_usbfn_os_<*Target SOC*>_PDK1_9.lib usb_ufnmddbase_<*Common Soc*>_PDK1_9.lib
Platform Driver Path	\PLATFORM\<*Target Platform*>\SRC\DRIVERS\USBD

Table 20-1. OTG Peripheral Driver Summary (continued)

Driver Attribute	Definition
Import Library	NA
Driver DLL	usbfn.dll
Catalog Item	Third Party > BSP > Freescale <*Target Platform*>: ARMV4I > Device Drivers > USB Devices > USB High Speed OTG Device > High Speed OTG Port Pure Client Function
SYSGEN Dependency	SYSGEN_USBFN=1
BSP Environment Variable	BSP_NOUSB= BSP_USB_HSOTG_CLIENT=1

USB peripheral class drivers are required to provide corresponding functionality. These class drivers are implemented as WinCE public driver. These class drivers (described in Section 20.5.7, "Peripheral Class Drivers") can be selected through drag and drop from catalog items.

20.1.2 OTG Host Driver Summary

Table 20-2 lists the attributes of the host driver.

Table 20-2. OTG Host Driver Summary

Driver Attribute	Definition
Target Platform (TGTPLAT)	iMX28-EVK-PDK1_9
Target SOC (TGTSOC)	MX28_FSL_V2_PDK1_9
Common SOC	COMMON_FSL_V2_PDK1_9
CSP Driver Path	..\SOC\<*Common SOC*>\ms\USBH\EHCI ..\SOC\<*Common SOC*>\ms\USBH\EHCIPDD ..\SOC\<*Common SOC*>\ms\USBH\USB2COM
CSP Static Library	usbh_ehcdmdd_<*Common SOC*>.lib usbh_ehcdpdd_<*Common SOC*>.lib usbh_usb2com_<*Common SOC*>.lib
Platform Driver Path	\PLATFORM\<*Target Platform*>\SRC\DRIVERS\USBH\HSOTG
Import Library	NA
Driver DLL	hcd_hsotg.dll
Catalog Item	Third Party > BSP > Freescale <*Target Platform*>: ARMV4I > Device Drivers > USB Devices > USB High Speed OTG Device To support only host mode, choose .. > High Speed OTG Port Pure Host Function.
SYSGEN Dependency	SYSGEN_USB=1
BSP Environment Variable	BSP_NOUSB= BSP_USB_HSOTG_HOST=1

USB host class drivers are required to provide corresponding functionality. As peripheral class drivers, the host class drivers are also implemented as WinCE public driver. Refer to Section 20.5.8, "Host Class Drivers," for more information.

20.1.3 OTG (Pin-Detection) Driver Summary

Table 20-3 lists the attributes of the OTG driver.

Table 20-3. OTG Driver Summary

Driver Attribute	Definition
Target Platform (TGTPLAT)	iMX28-EVK-PDK1_9
Target SOC (TGTSOC)	MX28_FSL_V2_PDK1_9
Common SOC	COMMON_FSL_V2_PDK1_9
CSP Driver Path	..\SOC\<Common Soc>\MS\USBOTG\MDD
CSP Static Library	usbotgcm_<*Common SOC*>.lib
Platform Driver Path	PLATFORM\<*Target Platform*>\SRC\DRIVERS\USBOTG
Import Library	NA
Driver DLL	fsl_usbotg.dll
Catalog Item	Third Party > BSPs > Freescale <*Target Platform*>: ARMV4I > Device Drivers > USB Devices > USB High Speed OTG Device > High Speed OTG Port Full OTG Function
SYSGEN Dependency	SYSGEN_USBFN=1
BSP Environment Variable	BSP_NOUSB= BSP_USB_HSOTG_CLIENT=1 BSP_USB_HSOTG_HOST=1 BSP_USBOTG=1

20.2 USB Host1 Driver Summary

Table 20-4 lists the attributes of the host driver.

Table 20-4. Host1 Host Driver Summary

Driver Attribute	Definition
Target Platform (TGTPLAT)	iMX28-EVK-PDK1_9
Target SOC (TGTSOC)	MX28_FSL_V2_PDK1_9
Common SOC	COMMON_FSL_V2_PDK1_9
CSP Driver Path	..\SOC\<*Common SOC*>\ms\USBH\EHCI ..\SOC\<*Common SOC*>\ms\USBH\EHCIPDD ..\SOC\<*Common SOC*>\ms\USBH\USB2COM
CSP Static Library	usbh_ehcdmdd_<*Common SOC*>.lib usbh_ehcdpdd_<*Common SOC*>.lib usbh_usb2com_<*Common SOC*>.lib
Platform Driver Path	\PLATFORM\<*Target Platform*>\SRC\DRIVERS\USBH\HSH1
Import Library	NA
Driver DLL	hcd_hsh1.dll

Table 20-4. Host1 Host Driver Summary (continued)

Catalog Item	Third Party > BSP > Freescale <*Target Platform*>: ARMV4I > Device Drivers > USB Devices > USB High Speed OTG Device To support only host mode, choose .. > High Speed OTG Port Pure Host Function.
SYSGEN Dependency	SYSGEN_USB=1
BSP Environment Variable	BSP_NOUSB= BSP_USB_HSH1=1

USB host class drivers are required to provide corresponding functionality. As peripheral class drivers, the host class drivers are also implemented as WinCE public driver. Refer to Section 20.5.8, "Host Class Drivers," for more information.

20.3 Supported Functionality

The OTG driver provides the following software and hardware support:

1. The High Speed OTG or Host driver supports USB specification 2.0.
2. When a cable is not connected or a mini-B cable is connected (in either of these cases, the ID pin is pull up), OTG driver selects the peripheral driver to be in charge. On attaching a mini-A cable (in this case, the ID pin is pull down), OTG driver selects the host driver to be in charge.
3. The peripheral driver can support mass storage, RNDIS, serial, and basic personal healthcare classes. Only one class support is active.
4. The host driver can support mass storage, HID, and Printer classes.
5. When nothing is attached to the OTG port, the driver configures the USB module to be in a low power state.
6. When the system is suspended with no attachment to the OTG or Host port, it does not create a wake condition upon attachment of the port to a host or attachment of a device with mini-A plug.
7. When the system is suspended while the OTG or Host port is connected to a host or to a device with a mini-A plug, the system remains suspended when the OTG port connection is unplugged.
8. When the system resumes after suspend, any attached devices are enumerated and their class drivers are loaded appropriately.

20.4 Hardware Operation

An EHCI compliant High-Speed OTG Controller and an USB 2.0 UTMI PHY are integrated on i.MX233 Chip. It provide a full on-chip USB OTG solution.

20.4.1 Conflicts with Other Peripherals and Catalog Items

This section explains USB OTG conflicts with other peripherals and catalog items.

20.4.1.1 Conflicts with SoC Peripherals

No conflicts.

20.4.1.2 Conflicts with Board Peripherals

No conflicts.

20.5 Software Operation

This section explains about the software operation of the drivers.

20.5.1 USB Host Controller Driver

This driver enables the USB host functionality for the OTG port and H1 port. It is a part of the standard Windows USB software architecture.

Figure 20-1 shows the Windows USB driver architecture.

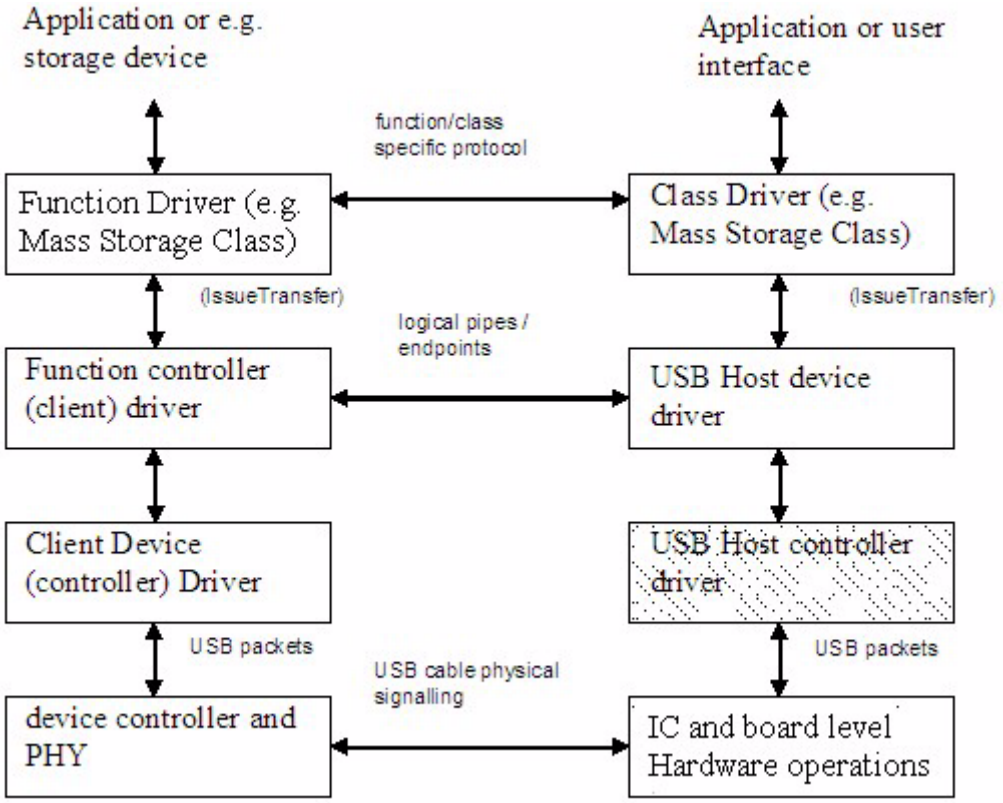

Figure 20-1. Windows USB Driver Architecture

The details about the Windows CE USB driver architecture and usage is available in the Platform Builder Help documentation in the following location:

Developing a Device Driver > Windows Embedded CE Drivers > USB Host Drivers

and

Developing a Device Driver > Windows Embedded CE Drivers > USB Host Drivers > USB Host Controller Drivers > USB Host Controller Driver Development Concepts

When the OTG driver is included, the OTG host driver is activated when an USB Mini-A plug is connected to the Mini USB OTG socket. When pure host mode is selected, the host driver is always in control with respect to the relevant USB controller. When an USB peripheral device is connected, the host driver enumerates it and activates the appropriate class driver.

The BSP supports the following USB class drivers:

- Mass Storage—Card Reader with SD or CF cards, USB HDD drive, thumb drive (disk-on-key). Some card reader firmware is not supported by the Microsoft standard Mass Storage class driver.
- HID—USB Keyboard and mouse
- RNDIS—Network Device Interface communication class

Hubs are also supported to extend the USB topology.

Refer to the Section 20.5.8, "Host Class Drivers," for more detailed description on the host class driver.

20.5.1.1 User Interface

As described above, users can access the USB host driver through class drivers. The details on the host client drivers are available in the Windows CE 6.0 Platform Builder Help documentation at the following location:

Developing a Device Driver > Windows Embedded CE Drivers > USB Host Drivers > USB Host Controller Drivers > USB Host Client Drivers.

The new class driver code is developed using the documentation. Refer to the host client driver interface functions (for example, IssueBulkTransfer) as documented in the Help topic:

Developing a Device Driver > Windows Embedded CE Drivers > USB Host Drivers > USB Host Controller Drivers > USB Host Client Drivers > Host Client Driver Reference.

20.5.1.2 Memory Configuration

The USB Host drivers (for all USB host ports) use DMA to perform all USB transfers. The physical memory for these transfer buffers is allocated as a pool during driver initialization. Unless physical addresses are specified in API accesses at the class-driver interface, the driver copies data between the user or class-provided data buffers and the DMA buffer from the driver's physical memory pool.

Host driver checks the registry key **PhysicalPageSize** for memory pool size. If it is not available or if the registry settings is less than 128 K, then the driver uses the default minimal buffer size, 128K, and apply it to the memory using the **HalAllocateCommonBuffer**.

20.5.1.3 Configured Power

USB host driver monitors the configured power for all devices attached to a USB host. The host driver verifies that each attached device does not exceed the configured current limit.

This power limit is implemented through the platform-specific function `BSPUsbhCheckConfigPower()` as described in Section 20.5.1.7.1, "BSPUsbhCheckConfigPower," and located in:

```
\PLATFORM\<Target Platform>\SRC\DRIVERS\USBH\Common\hwinit.c
```

This function is modified based on the platform hardware capabilities. Currently the current limit is set to 500 mA.

20.5.1.4 Registry Settings

This section explains the registry settings.

20.5.1.4.1 OTG Registry Settings

Refer to the Section 20.5.5, "USB OTG Registry Settings," for information about OTG registry settings.

20.5.1.4.2 HSH1 Registry Settings

The generated HSH1 registry settings are located in Table 20-5 lists the default values for the host driver settings.

Table 20-5. HSH1 Registry Default Values

Value	Type	Content	Description
Dll	sz	hcd_hsh1.dll	Driver dynamic link library
OTGSupport	dword	0	obsolete setting, must be set as 0
OTGGroup	sz	01	This unique string (example "00" to "99") is used to combine or correlate instances of the host, function, and transceiver driver within one USB OTG instance.
HcdCapability	dword	4	HCD_SUSPEND_ON_REQUEST. Note: HCD_SUSPEND_RESUME is always assumed.
PhysicalPageSize	dword	NA	This value represents the number of bytes allocated for the physical memory pool of the host driver, and defaults to 128 kB. From this buffer, 75% is allocated for transfer descriptors and the remaining buffer is available for allocation to simultaneous transfers. In most cases, only one transfer is active at any time (for example, in the Mass Storage Class). A good value is at least 3x as large as the largest data buffer transferred using IssueTransfer(). The BSP donot provide this setting and the driver uses the default 128 kB size.

20.5.1.5 PHY level USB Test

The USB 2.0 specification defines PHY-level test modes for all the USB host ports (refer to the USB 2.0 specifications chapter in the *USB Reference Manual*). Temporarily this feature is not enabled in the driver.

20.5.1.6 Unit Test

Different peripherals such as thumb disk, keyboard, and hub are used to test the host driver functionality. Manual tests include connecting the peripheral, confirming the connection during plug in, during unplug and during subsequent plug in of device, data transfer verification (for mass storage peripherals) and other expected functionality such as keyboard, mouse, and so on.

To verify the RNDIS class device, a CEPC containing Netchip 2280 USB function is attached and used to access a remote file server on the CEPC. To verify the low-level transport for bulk, interrupt, and

isochronous transfers, the CETK Host test kit is performed. This requires a CEPC configured with Netchip 2280 USB function and loopback driver.

20.5.1.6.1 USB Host Controller Driver Test

Documentation for the Windows CE 6.0 CETK USB Host tests is available in the Platform Builder Windows CE product documentation in the following location:

Debugging and Testing > Windows CE Test Kit > CE Test Kit

20.5.1.6.2 Building the Test Image

The following steps are used to build the test image:

1. Checkout the RTM to test or install the MSI provided
2. Add the following components from the catalog:
   - Freescale <Target Platform>: ARMV4I > Device Drivers > USB Devices > USB High Speed OTG Device > High Speed Port Pure Host Function.
   - Core OS > Windows CE devices > Core OS Services > USB HOST Support; and all the subcomponents of this catalog item (SubComponents such as USB Storage Class Driver.)
   - Core OS > Windows CE devices > File Systems And Data store > Storage Manager; (Sub Components: FAT File System, Partition Driver, Storage Manager control panel applet)
   - Device Drivers > USB Function > USB Function Clients > Serial.

20.5.1.6.3 Abstract

This test suite can be used to test USB host controller drivers that provides the same interface as Window CE USB host controller driver does. Refer to Section 20.5.1.1, “User Interface,” for more information. Also, it can be used to verify if a certain USB host controller (a stand alone card or an onboard logic) can operate with Windows CE.

Figure 20-2 shows the test setup and scenario.

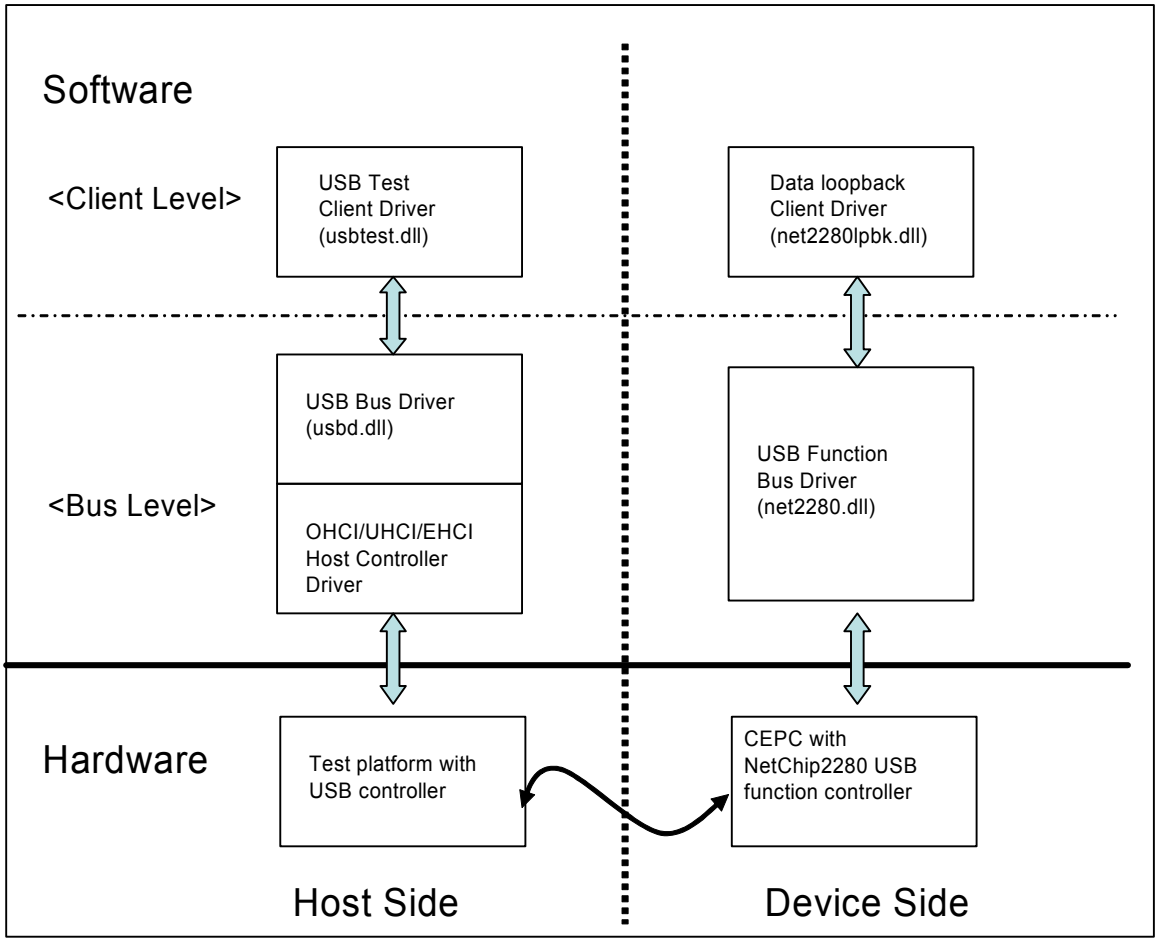

Figure 20-2. Test Setup

This test suite acts as a client driver above the USB bus driver (usbd.dll). It is loaded when test device is connected to the host through the USB cable. The test device is a CEPC with a NetChip2280 USB function controller card in it. After this CEPC is booted up and net2280lpbk.dll is loaded, the CEPC acts as a generic USB data loopback device. USB test suite (the test client driver on the host side) can then stream data or issue device requests to or from this data loopback device. This way, the USB host controller and its corresponding host controller drivers are used.

NetChip2280 USB function PCI controller card is a USB2.0 compatible USB function device. It can be used to test both USB2.0 and USB1.1 host controllers (EHCI, OHCI, or UHCI) and corresponding drivers.

Netchip2280 controller has 6 end points besides endpoint 0. The data loopback driver (net2280lpback.dll) configures these endpoints as 3 pairs: one bulk IN or OUT pair, one Interrupt IN or OUT pair, and one Isochronous IN or OUT pair. The data loopback tests are done by sending data from host side to device side through OUT pipe, and receive it back through IN pipe, and then verifies the data.

20.5.1.6.4 Unit Test Hardware

The following are the unit test hardware requirements:

- Test platform
- Host Controller Card (if not onboard logic)
- CEPC
- Netchip2280 Card
- USB cable

20.5.1.6.5 Unit Test Software

The following are the host side requirements:

- Tux.exe
- Ddlx.dll
- Usbtest.dll
- Tooltalk.dll
- Kato.dll
- USB component (usbd.dll, EHCI, OHCI or UHCI host controller driver(s)) must be included in the run time image.

The following are the device side requirements:

- Lufldrv.exe
- Net2280lpbk.dll
- NetChip2280 USB function support (net2280.dll) must be included in the CEPC run time image.

20.5.1.6.6 Running the Test

The test procedure is as follows:

1. Download runtime image to CEPC with Netchip2280 card on it.
2. After system boot up, run command `s lufldrv`, tester should verify if net2280lpbk.dll is loaded
3. Download runtime image to test platform with USB host controller in it
4. After system boot up, ensure that there is no connection between host side and device through USB cable. Then launch command `s tux -o -d ddlx -c "usbtest" "-xYYYY"`, where `"YYYY"` is the test case(s) to be run
5. The test indicates that there should be no connection between host and device side. Then after 7 seconds, the test needs to connect 2 sides with USB cable.
6. The test main body starts to run
7. If there are other tests to be run, do not disconnect the USB cable. Type the next test command, and the tests starts directly. If the USB connection was disconnected before the next test, the test needs to connect again.

20.5.1.6.7 Test Cases

Table 20-6 shows the test cases available in the test suite.

Table 20-6. USB Host Controller Driver Test Cases

Test Case ID	Test Description
1001-1315, 1501-1515	Data loopback tests: Concerning the transfer type, there are five categories: 1) Bulk pipe loopback tests (tests with ID end with 1, like xxx1) 2) Interrupt pipe loopback tests (tests with ID end with 2, xxx2) 3) Isochronous pipe loopback tests (tests with ID end with 3, xxx3) 4) All pipe transfer simultaneously (tests with ID end with 4, xxx4) 5) All three types transfers carry on simultaneously (tests with ID end with 5, xxx5) [1] There are five categories for how data is transferred: 1) Normal loopback tests (tests with ID start with 10, like 10) 2) loopback tests using physical memory (tests with ID start with 11, 11xx) 3) loopback tests using a part of allocated physical memory (tests with ID start with 12, 12xx) 4) Normal short transfer loopback tests (tests with ID start with 13, 13xx) 5) Stress short transfer loopback tests (tests with ID start with 15, 15xx) Also both synchronous and asynchronous transfer methods are exercised (test cases like xx1x using asynchronous transfer method, test cases like xx0x using synchronous method There are a total of 5 × 5 × 2 = 50 test cases
1401-1413	Additional data loopback tests. that mainly focus on testing APIs like GetTransferStatus(), AbortTransfer() and CloseTransfer()
2001-2013	Test related to Device requests
9001-9004	Special tests that test APIs such as SuspendDevice(), ResumeDevice() and DisableDevice()
9005	Test that stresses EP0 transfer (Vendor Transfer)

[1] This category of tests is designed for testing some other USB function devices which have more endpoints than host controller driver can handle. When using Netchip2280, it should be the same as category 4). Tester can just ignore this category.

By default, the data loopback device configures the endpoints with often-used packet sizes that are DWORD aligned, and neither too big nor too small. Passing all the listed tests above under this configuration is more than sufficient for a BVT-type test pass. However, testers can change the packet sizes (these values are hard-coded in the source code for net2280lpbk.dll) for each endpoint by themselves and run these test cases again for more comprehensive testing.

This test suite provides a way to change packet sizes of on NetChip2280 device dynamically. They are:

- Test case 3001 — Using some very small packet sizes in NetChip2280 device full speed configuration
- Test case 3002 — Using some very small packet sizes in NetChip2280 device high speed configuration
- Test case 3003 — Using some irregular packet sizes (like non DWORD-aligned size) in NetChip2280 device full speed configuration
- Test case 3004 — Using some irregular packet sizes (such as non DWORD-aligned size) in NetChip2280 device high speed configuration

- Test case 3005 (High Speed only) — Using some very large packet sizes (such as 2 × 1024 for Isochronous endpoints) in NetChip2280 device full speed configuration.

NOTE

Ideally, Netchip2280 cannot handle transfers using such large packet size as its onboard FIFO buffer is small.

What testers need to do is to run one of the test case above like running those normal tests, then after 15–20 seconds, automatically unload and load the `usbtest.dll` again through the Platform Builder. It means that the packets sizes on Netchip2280 side have already been changed. Then those normal tests can run. Use test case 3011 (for full speed config) and 3012 (for high speed) to restore the default packet sizes.

Another category test that is important for USB 2.0 host controllers and drivers is called the golden bridge tests, which means USB 2.0 host controller is connected with a full speed (USB 1.1) device. This is the only scenario that an USB 2.0 host controller performs split transfers.

NetChip2280 can be forced to be a full speed device. In the test setup stage, instead of running the `s lufldrv` to load loopback driver, it runs the `s lufldrv -f`. This forces the Netchip2280 to be configured as a full speed device.

Also testers can do some manual tests. The following are some examples:

- Plug in real USB devices, suspend system, and then resume; USB devices should still be there
- Plug in real USB devices, suspend system, unplug it, plug it in another device, then resume; system should enumerate that new device properly
- Run one of the data transfer tests, in the middle of transfer stage, suspend the system (host side), then resume; tests may fail, but system should not crash
- Run one of the data transfer tests, in the middle of transfer stage, disconnect the USB connection; tests should fail, but system should not crash

20.5.1.7 Platform-Specific API

This section explains about the platform-specific APIs.

20.5.1.7.1 BSPUsbhCheckConfigPower

This function is used to evaluate whether a device can be supported on the specified USB port.

Parameters

UCHAR bPort	[in] Unused. Each USB controller has only one port
DWORD dwCfgPower	[in] Power requirement (number of milliamps) requested by the device being evaluated for attachment support on this port
DWORD dwTotalPower	[in] current total power (number of milliamps) used by other previously attached devices on this port
Return Value	Return TRUE if device requesting dwCfgPower can be safely attached Return FALSE if device can not be attached

20.5.1.7.2 BSPUsbSetWakeUp

This function does what is necessary to enable or disable wakeup on the USB port. This function does not actually enable wake-up when a device is currently attached to the port.

Parameters

BOOL bEnable [in] TRUE to enable wakeup, FALSE to disable wakeup

20.5.1.7.3 BSPUsbCheckWakeUp

This function evaluates the wake-up condition for the relevant USB port, and clears the condition and interrupt.

Parameters None

Return Value Return TRUE when a wake-up condition was detected
Return FALSE when no wake-up condition was present

20.5.1.7.4 SetPHYPowerMgmt

This function is called by the USB driver when transitioning to or from the suspended state (for example, during system suspend). The function does what is necessary to place the transceiver hardware into a suspended (fSuspend = TRUE) or running (fSuspend = FALSE) state.

The standard implementation for i.MX System uses a ULPI-bus based ISP1504 transceiver for the HS OTG port, and this function configures the ULPI-bus for sleep state. If platform hardware uses other transceivers, this function must be modified appropriately.

Parameters

BOOL fSuspend [in] TRUE: system or controller is going to suspend mode. FALSE: resuming

20.5.2 USB Peripheral Driver

This driver enables the USB peripheral functionality for the i.MX device. When this driver is active and the i.MX System is connected to a USB host system (for example, high speed or full speed port of PC), it is enumerated according to the current active configuration settings, and the appropriate class driver is loaded on the PC.

System can be configured as one of the following USB functions by setting the appropriate environment variable during build (drag or drop from the catalog).

- Serial class - Serial ActiveSync
- Mass storage class - expose local storage (ATA hard disk, RAMDISK or other store) as USB drive
- RNDIS class - Remote Network Driver Interface Specification
- PHD class - basic Personal Healthcare Device Class support

When multiple class supports are selected, only one class acts as the active peripheral support. The default priority is: Serial Class > Mass Storage Class > RNDIS class > PHD class. Besides, we also provide tools to change current active class, refer to the Section 20.8.1, “Application for USB Peripheral Class Driver Switch.” for more information.

Refer to the Section 20.5.7, “Peripheral Class Drivers.” for detailed description on peripheral class driver.

20.5.2.1 User Interface

The USB client driver provides a standard Windows CE USB driver implementation. Refer to the Help documentation at the following location:

Developing a Device Driver > Windows Embedded CE Drivers > USB Function Drivers > USB Function Controller Drivers.

User can access the USB client driver through function drivers such as Mass Storage or RNDIS. Refer to the following location in the Windows CE 6.0 Platform Builder help topic:

Developing a Device Driver > Windows Embedded CE Drivers > USB Function Client Drivers.

To get information on the new function driver code, refer to the Function controller driver interface functions (for example, IssueTransfer) as documented in:

Developing a Device Driver > Windows Embedded CE Drivers > USB Function Controller Drivers > USB Function Controller Driver Reference.

20.5.2.2 Client Driver Configuration

Refer to the Section 20.5.4, “USB OTG Catalog Settings,” for information about the client driver configuration.

20.5.2.3 Registry Settings

Refer to the Section 20.5.5, “USB OTG Registry Settings,” for information about the registry settings.

20.5.2.4 PHY Test Mode

The USB 2.0 specification defines PHY-level test modes for USB device ports (refer to the USB 2.0 specifications chapter in the *USB Reference Manual*). This mechanism allows host to configure a device into test mode by commanding the device with a specific SET_FEATURE request. Once test mode is entered, the device cannot come out of the test mode. Do not enable this feature in BSP now.

20.5.2.5 Unit Test

There is no CETK test case for USB peripheral drivers. The USB Peripheral driver is tested manually for USB Serial function or USB Mass storage or RNDIS respectively. The test verifies basic USB peripheral functionality, including attach, detach, and data transfer. Separate images can be built and downloaded for each of the 3 peripheral function tests. Refer to the Section 20.5.1.6.2, “Building the Test Image,” for building the image. The peripheral class driver switch tool is also used to do these tests, refer to the Section 20.8.1, “Application for USB Peripheral Class Driver Switch,” for more information.

20.5.2.5.1 Unit Test Hardware

Table 20-7 lists the required hardware to run the unit tests.

Table 20-7. Hardware Requirements

Requirement	Description
Host system	A PC with proper driver and software installed
USB cable having Mini or Micro USB OTG plug A at one end and Mini or Micro USB OTG plug B on the other side	For connecting the PC and peripheral
ATA, NAND, Thumb disk, SD Card or MMC card mounted on CE system	Required as a storage device when the board is configured as mass storage class

20.5.2.5.2 Unit Test Software

Table 20-8 shows the software requirements for the USB Function controller driver test.

Table 20-8. Software Requirements

Requirement	Description
ActiveSync 4.1 and above	Host side software that is required to be available for testing the Serial class functionality

20.5.2.5.3 Running the USB Function Controller Driver Tests

Table 20-9 lists USB Function controller driver tests:

Table 20-9. USB Function Controller Driver Tests

Test Cases	Entry Criteria, Procedure and Expected Results
Board configured as USB Serial class and connected to a host system after the board boots up completely	Entry Criteria: Make sure there is no cable connected and the board is turned on and wait until the board boots-up completely Procedure: 1. Connect the mini or micro USB OTG plug B to the mini or micro USB OTG socket 2. Observe that the ActiveSync on the host side gets connected and is synchronized 3. Copy files from Host system to the Mobile Device. Files are copied 4. Copy files from the Mobile Device to the Host system. Files gets copied 5. Unplug the mini USB OTG plug B from the i.MX mini USB OTG socket to unload the Serial class driver Expected Result: ActiveSync should get synchronized and copying of files should happen between the Host and the System
Board configured as USB Mass storage client, with DSKx mounted, and connected to PC after the board boots up completely	Entry Criteria: Make sure there is no cable connected and the board is turned on and wait until the board boots-up completely Procedure: 1. Connect the mini or micro USB OTG plug B to the USB OTG socket 2. Observe that a new disk in My Computer having as Removable Disk appearing in it 3. Copy files from Host system to the new disk drive. Files are copied 4. Copy files from the new disk drive to the Host system. Files gets copied 5. Unplug the mini USB OTG plug B from the mini USB OTG socket to unload the mass storage class driver Expected Result: Files copied into mass storage client device match those copied out (when compared on Windows XP PC using file compare utility). Note that files are not visible from within the System until the system has been reset. The file system should not be used inside the System when it is being accessed through USB as a mass storage client.
Board configured as USB RNDIS client and connected to a host system after the board boots up completely. Browsing the Internet	Entry Criteria: Make sure there is no cable connected and the board is turned ON and wait until the board boots-up completely. Enusre that the NIC's local area connection is not having any IP address Procedure: 1. Connect the mini USB OTG plug B to the mini USB OTG socket 2. Observe that a new Local area connection in the Network and Dial up connections appears on the Windows XP machine. Bridge the NIC's local area connection and the RNDIS's local area connection 3. Configure the bridge by giving IP address, Subnetmask, Default gateway, DNS 4. On the System, a new Local area connection can be found in the Network and dial up connections. Configure the local area connection by giving IP address, Subnetmask, Default gateway, DNS 5. In the Internet explorer on the System, configure the Lan settings as per the local area settings Expected Result: Browsing the Internet should be possible

20.5.2.6 Platform-Specific API

This section explains about the platform-specific functions.

20.5.2.6.1 InitializeMux

This function is called to initialize the IOMUX connection within i.MX, from USB controller to the appropriate device pins for the transceiver. This function is implemented for the Pure Client situation.

Parameters

int Speed	[in] Unused
Return Value	Return TRUE if device requesting dwCfgPower can be safely attached

20.5.2.6.2 HardwarePullupDP

This function is called by the USB client driver when D+ must be pulled-up, in preparation for connection to a USB host. The standard code configures for ISP1504 or ISP1301 transceiver. It is possible to modify this routine to conditionally soft-disable USB connection.

Parameters

*CSP_USB_REGS *pRegs*	[in] pointer to the registers for the USB controller
Return Value	Return TRUE if D+ signal was pulled-up

20.5.3 USB OTG Driver (Pin-Detection Driver)

This driver is responsible for detecting the type of USB connector plugged into the USB OTG socket of the i.MX System. It loads the USB host driver or USB peripheral driver and let it in charge.

20.5.3.1 User Interface

There is no user interface to the transceiver driver. This driver merely manages the USB host or peripheral drivers, which provide the appropriate programming API.

20.5.3.2 OTG Driver Configuration

See the Section 20.5.4, “USB OTG Catalog Settings” for information on the OTG driver configuration.

20.5.3.3 Registry Settings

See the Section 20.5.5, “USB OTG Registry Settings” for information on the registry settings.

20.5.3.4 Unit Test

There is no CETK test case for USB OTG driver. It is tested using the mini or micro USB OTG plug A and mini or micro USB OTG plug B. The test is done by manually plugging in different cables to the OTG socket on the System and verifies if the appropriate driver is activated.

20.5.3.4.1 Unit Test Hardware

Table 20-10 lists the required hardware to run the unit tests.

Table 20-10. Hardware Requirements

Requirement	Description
Full OTG configuration selected in BSP	Make sure the OTG driver is running
PC (with appropriate driver and software installed) Peripherals such as thumb disk, USB keyboard, and hub	To test if control reaches the Host controller driver
mini or micro A to A receptacle cable mini or micro B to A cable	For connecting system with PC and peripherals. System acts as peripheral and host accordingly

20.5.3.4.2 Running the OTG Test

Table 20-11 lists OTG tests.

Table 20-11. OTG Tests

Test Cases	Entry Criteria, Procedure and Expected Results
Idle case when the cable is not plugged in	Entry Criteria: Ensure there is no cable connected and the board is turned ON, wait until the board boots-up completely Procedure: When the board is powered and completely booted-up, the board should be idle. Expected Result: Device boots up and is stable
Switch to peripheral	Entry Criteria: Ensure there is no mini USB OTG plug connected and the board is turned ON and wait until the board boots-up completely Procedure: When the board is powered and completely booted-up, connect the system to PC with the mini or micro B to A cable. Verify if PC recognizes it correctly. Expected Result: PC recognize the board (as peripheral) correctly (Activesync is active, or removable disk is visible, or network adaptor is recognized).
Switch to host	Entry Criteria: Unplug board from PC (in previous step) Procedure: 1. Disconnect the system with PC and connect a mini or micro A to A receptacle to the OTG socket. 2. Connect the USB peripheral device (such as a thumb disk) to the A receptacle. 3. The connected peripheral gets enumerated and starts functioning. For example, if an USB thumb disk is connected, a new disk is accessible on the CE system. Expected Result: Peripheral should start functioning on the CE system.
Switch between host and peripheral	Repeat the last 2 steps Expected Result: System always functions OK as both host and peripheral.

20.5.3.5 Platform-Specific API

NA.

20.5.4 USB OTG Catalog Settings

The driver is selected into the BSP build by dragging and dropping the appropriate catalog item for USB HS OTG.. There are 3 catalog items in **Freescale i.MX233 EVK: ARMV4I** > **Device Drivers** > **USB Devices** > **USB High Speed OTG** related to USBOTG functionality:

(a) **High Speed OTG Port Full OTG Function**

(b) **High Speed OTG Port Pure Client Function**

(c) **High Speed OTG Port Pure Host Function**

The selection of (a) implicitly selects (b) and (c), without selecting (a), (b) and (c) separately. So there are 3 possible configurations available for BSP users:

(1) All 3 catalogs are explicitly or implicitly selected, corresponding to both host and peripheral support plus OTG pin detection.

(2) Only **High Speed OTG Port Pure Client Function** is selected, corresponding to peripheral-only support.

(3) Only **High Speed OTG Port Pure Host Function** is selected, corresponding to host-only support.

20.5.5 USB OTG Registry Settings

3 possible configurations available in Section 20.5.4, “USB OTG Catalog Settings,” forms 3 corresponding registry structure.

20.5.5.1 Registry Structure

- With configuration 1, for full OTG configuration, the generated registry has the following structure:

```
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\UsbOtg]
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\UsbOtg\USBFN]
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\UsbOtg\Hcd]
```

- With configuration 2, for full peripheral-only configuration, the generated registry has the following structure:

```
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\UFN]
```

- With configuration 3, for full host-only configuration, the generated registry has the following structure:

```
[HKEY_LOCAL_MACHINE\Drivers\BuiltIn\HCD_HSOTG]
```

The contents in **BuiltIn\USBOtg\UsbFN** are similar to those in **BuiltIn\UFN** and the contents in **BuiltIn\UsbOtg\Hcd** are similar to those in **BuiltIn\HCD_HSOTG**. Most of the settings are common between the both. The differences are as follows:

In configuration 1, only **UsbOtg** key is located under **BuiltIn** key, which means the OTG driver is automatically loaded by the OS. In this case, the OTG driver decides to load the peripheral driver and the host driver.

In configuration 2 and 3, **UFN** or **HCD_HSOTG** is put directly under **BuiltIn** key. So the peripheral driver or host driver is loaded automatically by the OS.

20.5.5.2 Registry Key Settings

This section explains about the registry key settings.

20.5.5.2.1 OTG Driver Settings

Table 20-12 lists the USB OTG transceiver registry settings.

Table 20-12. USB OTG Transceiver Registry Settings

Value	Type	Content	Description
Dll	sz	fsl_usbotg.dll	Driver dynamic link library
IsrDll	sz	giisr.dll	ISR Chain Handler
DynamicClientLoad	dword	3	The value is set to 0x3, indicating both host driver and peripheral driver are loaded dynamically by the OTG driver.

20.5.5.2.2 Peripheral Driver Settings

Table 20-13 lists the USB OTG client registry settings.

Table 20-13. USB OTG Client Registry Settings

Value	Type	Content	Description
Dll	sz	usbfn.dll	Driver dynamic link library
OTGSupport	dword	0	obsolete setting, must be set as 0
Priority256	dword	64	The reference peripheral driver IST priority
OTGGroup	sz	1	This unique string (for example, 00 to 99) is used to combine or correlate instances of the host, function, and transceiver driver within one USB OTG instance

20.5.5.2.3 Host Driver Settings

Table 20-14 lists the default values for the host driver settings.

Table 20-14. OTG Host Default Values

Value	Type	Content	Description
Dll	sz	hcd_hsotg.dll	Driver dynamic link library
OTGSupport	dword	0	obsolete setting, must be set as 0
OTGGroup	sz	01	This unique string (for example, 00 to 99) is used to combine or correlate instances of the host, function, and transceiver driver within one USB OTG instance.

Table 20-14. OTG Host Default Values (continued)

Value	Type	Content	Description
HcdCapability	dword	4	HCD_SUSPEND_ON_REQUEST. **Note:** HCD_SUSPEND_RESUME is always assumed.
PhysicalPageSize	dword	NA	This value represents the number of bytes allocated for the physical memory pool of the OTG host driver, and defaults to 128 Kbyte. From this buffer, 75% is allocated for transfer descriptors and the remaining buffer is available for allocation to simultaneous transfers. In most cases, only one transfer is active at any time (for example, in the Mass Storage Class). A good value is at least 3x as large as the largest data buffer transferred using `IssueTransfer()`. The BSP does not provide this setting and the driver uses the default 128 Kbyte size.

20.5.6 Power Management

The USB OTG driver enters the low power mode in the following cases:

- No bus activity for a specified period of time
- System enters the suspend state

Similar procedures are followed to let the USB module to enter or exit low power mode in either of the 2 cases. The following section explains about the description on the general power management procedures.

20.5.6.1 Power Down Procedure

To set the USB module to low power mode, both PHY and controller should be set to low power mode respectively.

20.5.6.1.1 Set PHY to Low Power Mode

The following function is called to set the PHY to low power mode:

```
BSPUsbPhyEnterLowPowerMode(pUsbRegs, TRUE)
```

This function is defined in

`..\platform\<`*Target Platform*`>\src\drivers\usbcommon\usbutils.c`

The following procedure is used for setting the PHY to low power mode.

- enable the wakeup interrupt source which can be activated without USB clock
- close power to all PHY sub module

20.5.6.1.2 Close USB Controller Clock

The following function is called to close the USB controller clock:

```
BSPUSBClockSwitch(FALSE)
```

This function is defined in

`..\platform\<`*Target Platform*`>\src\drivers\usbcommon\usbclock.c`

It gates the IC clock to USB Controller module.

20.5.6.2 Power Up Procedure

The USB module is powered up by reversing the procedures that are used to exit the low power mode.

20.5.6.2.1 Open USB Controller Clock

The following function is called to open the USB controller clock:

```
BSPUSBClockSwitch(TRUE)
```

It ungates the IC clock to the USB Controller module.

20.5.6.2.2 Put PHY Out of Low Power Mode

The following function is called to retrieve the PHY from low power mode:

```
BSPUsbPhyEnterLowPowerMode(pUsbRegs, FALSE)
```

The following procedures are implemented to set the PHY out of low power mode.

- disable the wakeup interrupt source which can be activated without the USB clock.
- open power to all PHY sub module

20.5.6.3 Processing Methodology

This section explains how to integrate the power down and power up procedure into the USB OTG driver. As the USB OTG driver includes the OTG driver, the host driver and the peripheral driver, the processing methodology for all 3 drivers is discussed in this section.

20.5.6.3.1 Host Driver Methodology

1) Auto low power

The host driver IST waits for the USB IRQ for a specified interval of time. The interval is defined as a macro **USB_IDLE_TIMEOUT**, which is set to 3000 ms in the BSP. If there are no USB IRQ during this period, there is nothing to be connected, so the driver follows the procedure as described in Section 20.5.6.1, “Power Down Procedure,” to set the USB module to low power mode.

When the module is in low power mode, the driver is sensitive to the USB interrupt. Once such an interrupt is caught, the driver follows the procedure described in Section 20.5.6.2, “Power Up Procedure,” to set the USB module out of low power mode and function normally.

The implementation is found in

`CHW::UsbInterruptThread`, which is located in

`SOC\<Common SOC>\ms\USBH\EHCI\chw.cpp`

2) Low power mode with system suspend

When the system enters the suspend mode, the USB module enters the low power mode. The power down procedures described in Section 20.5.6.1, “Power Down Procedure,” are also implemented in host driver

`CHW::PowerMgmtCallback`, which is located in

`SOC\<Common SOC>\ms\USBH\EHCI\chw.cpp`

This function is called by the OS automatically during system suspend.

When the system exits suspend mode, the USB module also exits the low power mode. The power up procedures described in Section 20.5.6.2, "Power Up Procedure," are also implemented in

`CHW::PowerMgmtCallback`

This function is called by the OS automatically during system resume.

20.5.6.3.2 Peripheral Driver Methodology

1) Auto low power

The peripheral driver IST waits for the USB IRQ for a specified interval of time. The interval is defined as a macro **IDLE_TIMEOUT**, which is set to 3000 ms in the BSP. If there are no USB IRQ during this period, there is nothing to be connected, so the driver follows the procedure as described in Section 20.5.6.1, "Power Down Procedure," to set the USB module to low power mode.

When the module is in low power mode, the driver is sensitive to USB interrupt. Once such an interrupt is occurs, the driver follows the procedure described in Section 20.5.6.2, "Power Up Procedure," to set the USB module out of low power mode and function normally.

The implementation can be found in

`InterruptHandle`, which is located in

`SOC\<Common SOC>\ms\USBD\COMMON\pdd.c`

2) Low power mode with system suspend

When the system enters suspend mode, the USB module also enters the low power mode. The power down procedures described in Section 20.5.6.1, "Power Down Procedure," are implemented in peripheral driver in

`UfnPdd_PowerDown`

Which is located in

`SOC\<Common SOC>\ms\USBD\COMMON\pdd.c`

This function is called by the OS automatically during system suspend.

When the system exits suspend mode, the USB module also exits low power mode. The power up procedures described in Section 20.5.6.2, "Power Up Procedure," are implemented in

`UfnPdd_PowerUp`

Which is also located in

`SOC\<Common SOC>\ms\USBD\COMMON\pdd.c`

20.5.6.3.3 OTG Driver Methodology

At any time after system is boot up, either host driver or peripheral driver is in charge of the USB module. When the USB module needs to enter or exit low power mode, all the tasks are done by the in-charge driver. So there is no need for the OTG Driver to provide redundant processing.

20.5.6.4 USB Wakeup

For some system design, it is preferred that an USB action by peripheral (such as plug, unplug and so on.) wakes up the whole system for the host driver after the system goes into the suspend mode. It is not implemented in i.MX233.

20.5.7 Peripheral Class Drivers

The function drivers can be configured using the Windows CE 6.0 Platform Builder catalog and are located at:

Device Drivers > USB Function > USB Function Clients

Besides that, basic Personal Health Care Class (PHCC) support and Communication Device Class (CDC) Abstract Control Mode (ACM) support are included in the BSP, the catalog is

Third Party > BSP > Freescale <Target Platform>: ARMV4I > Device Drivers > USB Devices > USB Functional Class Driver > Personal HealthCare Class Support

or

Third Party > BSP > Freescale <Target Platform>: ARMV4I > Device Drivers > USB Devices > USB Functional Class Driver > Communication Device Class Support

The default function driver is launched, when the USB device port is attached to a host. This default function driver is selected by the registry key (the last instance of this value in reginit.ini applies):

```
[HKEY_LOCAL_MACHINE\Drivers\USB\FunctionDrivers]
   "DefaultClientDriver"=- ; erase previous default
[HKEY_LOCAL_MACHINE\Drivers\USB\FunctionDrivers]
   "DefaultClientDriver"="Mass_Storage_Class"
```

or

```
   "DefaultClientDriver"="RNDIS"
```

or

```
   "DefaultClientDriver"="Serial_Class"
```

or

```
   "DefaultClientDriver"="Personal_HealthCare_Class"
```

or

```
   "DefaultClientDriver"="CDC"
```

20.5.7.1 Mass Storage Function

Table 20-15 lists the mass storage functions.

Table 20-15. Mass Storage Function

Driver Attribute	Definition
CSP Driver Path	..\SOC\<*Common SOC*>\ms\USBFN\CLASS

Table 20-15. Mass Storage Function (continued)

CSP Static Library	NA
Platform Driver Path	NA
Import Library	USBMSFN_LIB_<*Common SOC*>.lib UFNCLIENTLIB.LIB
Driver DLL	usbmsfn.dll
Catalog Item	Device Drivers > USB Function > USB Function Clients > Mass Storage
SYSGEN Dependency	SYSGEN_USBFN_STORAGE

The Mass Storage function exposes a local data store as a USB peripheral storage device. The device used can be specified in registry. In platfrom.reg, the following template is provided:

```
PUBLIC\Common\OAK\Files\common.reg
"DeviceName"=- ;
; "DeviceName"="ATA HARD DISK"
; "DeviceName"="SDMEMORY CARD"
; "DeviceName"="MMC CARD"
; "DeviceName"="USB HARD DISK"
; "DeviceName"="NAND FLASH"
```

Any item from this list can be specified to act as the mass storage medium. Do not comment the corresponding line and rebuild the BSP to make that item active.

If none of the items are specified explicitly, a precoded priority is used to determine what active drive acts as a mass storage medium. The priority is described as the following:

```
ATA HARD DISK > SDMEMORY CARD (MMC CARD) > USB HARD DISK > NAND FLASH
```

The platform.reg can also override other USBMSFN related default settings. This allows customizing the following values which must be properly configured for a commercial device:

```
[HKEY_LOCAL_MACHINE\Drivers\USB\FunctionDrivers\Mass_Storage_Class]
; idVendor must be changed. 045E belongs to Microsoft and is only to be used for
; prototype devices in your labs. Visit http://www.usb.org to obtain a vendor id.
   "idVendor"=dword:045E
   "Manufacturer"="Generic Manufacturer (PROTOTYPE--Remember to change idVendor)"
   "idProduct"=dword:FFFF
   "Product"="Generic Mass Storage (PROTOTYPE--Remember to change idVendor)"
   "bcdDevice"=dword:0
```

20.5.7.2 Serial Function

The primary use of serial function is ActiveSync. Table 20-16 lists the serial functions.

Table 20-16. Serial Function

Driver Attribute	Definition
CSP Driver Path	NA
PUBLIC driver path	PUBLIC\Common\OAK\Drivers\USBFN\CLASS\SERIAL
CSP Static Library	NA

Table 20-16. Serial Function (continued)

Platform Driver Path	NA
Export Library	serialusbfn.lib
Import Library	com_mdd2.lib serpddcm.lib ufnclientlib.lib
Driver DLL	SerialUsbFn.dll
Catalog Item	Device Drivers > USB Function > USB Function Clients > Serial Client
SYSGEN Dependency	SYSGEN_USBFN_SERIAL

NOTE

ActiveSync is tested using the connection to PC with the ActiveSync version 4.1 or above. Refer www.microsoft.com to download the latest ActiveSync software for the PC. In some cases, DEBUGCHK may be triggered during attachment to ActiveSync in DEBUG builds.

When SYSGEN_USBFN_SERIAL is defined, the default registry entry is automatically included from:

```
PUBLIC\Common\OAK\FILES\common.reg
```

For commercial products, this registry entry must be copied into platform.reg and modified to override the defaults. This allows customizing the following values that must be properly configured for a commercial device:

```
[HKEY_LOCAL_MACHINE\Drivers\USB\FunctionDrivers\Serial_Class]
; idVendor must be changed. 045E belongs to Microsoft and is only to be used for
; prototype devices in your labs. Visit http://www.usb.org to obtain a vendor id.
   "idVendor"=dword:045E
   "Manufacturer"="Generic Manufacturer (PROTOTYPE--Remember to change idVendor)"
   "idProduct"=dword:00ce
   "Product"="Generic Serial (PROTOTYPE--Remember to change idVendor)"
   "bcdDevice"=dword:0
```

20.5.7.3 RNDIS Function

The RNDIS function allows communication over the USB to supply it to the ethernet NDIS interface of protocol stack. Table 20-17 lists the RNDIS functions.

Table 20-17. RNDIS Function

Driver Attribute	Definition
CSP Driver Path	NA
CSP Static Library	NA
Platform Driver Path	NA
PUBLIC Driver Path	PUBLIC*\OAK\Drivers\USBFN\Class\RNDIS
Import Library	ndis.lib
Driver DLL	RNDISFN.DLL

Table 20-17. RNDIS Function (continued)

Catalog Item	Device Drivers > USB Function > USB Function Clients > RNDIS Client
SYSGEN Dependency	SYSGEN_USBFN_ETHERNET

RNDIS function is tested using the Freescale RNDIS class driver located at:

```
Support\RNDIS\ce6_rndis.inf
%WINDIR%\System32\drivers\usb8023x.sys
```

When SYSGEN_USBFN_ETHERNET is defined, the default registry entry is automatically included from:

```
PUBLIC\Common\OAK\FILES\common.reg
```

For commercial products, this registry entry must be copied into platform.reg and modified to override the defaults. This allows customizing the following values which must be properly configured for a commercial device:

```
[HKEY_LOCAL_MACHINE\Drivers\USB\FunctionDrivers\RNDIS]
; idVendor must be changed. 045E belongs to Microsoft and is only to be used for
; prototype devices in your labs. Visit http://www.usb.org to obtain a vendor id.
"idVendor"=dword:045E
"Manufacturer"="Generic Manufacturer (PROTOTYPE--Remember to change idVendor)"
"idProduct"=dword:0301
"Product"="Generic RNDIS (PROTOTYPE--Remember to change idVendor)"
"bcdDevice"=dword:0
```

20.5.7.4 PHDC Function

PHDC collects the personal health related data such as glucose meters and temperature measurements from portable devices, and then transmit the data to the center agent. For example, PC or health care center host. Table 20-18 lists the PHDC functions.

Table 20-18. PHDC Function

Driver Attribute	Definition
CSP Driver Path	..\SOC\<*Common SOC*>\UFNCLASS\CLASS\PHDC
PUBLIC driver path	NA
CSP Static Library	NA
Platform Driver Path	NA
Export Library	NA
Import Library	NA
Driver DLL	usbphdfn.dll
Catalog Item	Third Party > BSP > Freescale <Target Platform>: ARMV4I > Device Drivers > USB Devices > USB Functional Class Driver > Personal HealthCare Class Support
SYSGEN Dependency	NA
BSP Variable	BSP_USBFN_PHD_SUPPORT

As it is a non Microsoft provided class driver, the PHDC class driver currently support basic reliable personal health data transfer in the continua alliance framework. A peripheral side API is developed to transfer the multiple personal health measurement, including weight, glucose, blood pressure and temperature to a PC installed with proper PHDC host driver and application. Refer to the Section 20.8.2, "Application for Multispec PHDC Demo," for more details.

20.5.7.5 CDC Function

The Communications Device Class is a device level definition and is used by the host to properly identify a communication device that can present several different types of interfaces. Only the Abstract Control Mode, which is used for modem devices that are controlled through a serial command set is implemented.

Table 20-19 lists the CDC functions.

Table 20-19. CDC Function

Driver Attribute	Definition
CSP Driver Path	..\SOC\<*Common SOC*>\ms\USBFN\CLASS\CDC
PUBLIC driver path	NA
CSP Static Library	NA
Platform Driver Path	NA
Export Library	NA
Import Library	NA
Driver DLL	usbfncdc.dll
Catalog Item	Third Party > BSP > Freescale <Target Platform>: ARMV4I > Device Drivers > USB Devices > USB Functional Class Driver > Communication Device Class Support
SYSGEN Dependency	NA
BSP Variable	BSP_USBFN_CDC_SUPPORT

The following registry should be added into platform.reg.

```
[HKEY_LOCAL_MACHINE\Drivers\USB\FunctionDrivers\CDC]
   "Dll"="usbfncdc.dll"
   "DeviceName"="COM7:"
   "Prefix"="COM"
   "Index"=dword:7
   "FriendlyName"="CDClass"
   "DeviceArrayIndex"=dword:1
   "RxBufferSize"=dword:4000
   "idVendor"=dword:2504
   "Manufacturer"="Freescale"
   "idProduct"=dword:0300
   "Product"="Communication Device"
   "SerialNumber"="8022709035731"
   "Tsp"="Unimodem.dll"
   "bcdDevice"=dword:0002
```

The idVendor and the idProduct are specific for working with FSL CDC Host. A demo application uses USB as virtual com port through CDC class driver. Refer to the Section 20.8.3, "Application for CDC Demo," for more details.

20.5.8 Host Class Drivers

All host ports support the same class drivers, and this configuration is common to all host ports. Class drivers must also be configured for the USB host ports. Class driver configuration is common to all host ports; there is no port-specific configuration for any class driver.

Table 20-20 shows the standard Microsoft-supplied drivers, and these drivers can be dragged and dropped from the catalog.

Table 20-20. Class Drivers

Class Driver	Configuration Flag	Catalog Item
HID	SYSGEN_USB_HID	Core OS > Windows CE devices > Core OS Services > USB Host Support > USB Human Input Device (HID) Class Driver
Printer	SYSGEN_USB_PRINTER	.. > USB Printer Class Driver (and refer to the additional configuration in Section 20.7.2, "Dependencies of Drivers")
Keyboard	SYSGEN_USB_HID _KEYBOARD	.. > Keyboard HID Device (and refer to the additional configuration in Section 20.7.2, "Dependencies of Drivers")
Mouse	SYSGEN_USB_HID _MOUSE	.. > Mouse HID Device (and refer to the additional configuration in Section 20.7.2, "Dependencies of Drivers")
RNDIS	SYSGEN_ETH_USB_HOST	.. > USB Remote NDIS Class Driver
Storage	SYSGEN_USB_STORAGE	.. > USB (mass) Storage Class Driver

20.5.8.1 HID Mouse

For mouse support, the cursor requires to test or use the mouse.

Table 20-21 shows the HID mouse class drivers.

Table 20-21. HID Mouse Class Driver

Catalog Item	Configuration Flag	Catalog Item
HID	SYSGEN_CURSOR	Core OS > Shell and User Interface > User Interface > Customizable UI > Mouse

20.5.8.2 HID Keyboard

The System keyboard key mapping conflicts with the HID keyboard. So, when the USB keyboard is included, remove the System keyboard and include the appropriate stub keyboard and keyboard.dll file.

Table 20-22 lists the HID keyboard driver that has to be removed.

Table 20-22. HID Keyboard Driver for Removal

Remove Item	Remove Catalog Item
Keyboard	Third Party > Freescale <*Target Platform*>: ARMV4I > Device Drivers > Input Devices > Keyboard US or Keypad

Table 20-23 lists the stub keyboard driver that has to be included.

Table 20-23. ID Keyboard Driver for Inclusion

Catalog Item	Configuration Flag	Catalog Item
NOP Stub Keyboard	BSP_KEYBD_NOP	Device Drivers > Input Devices > Keyboard or Mouse > NOP (Stub) Keyboard or Mouse English

Include appropriate keyboard.dll. For example, define SYSGEN_KBD_US and add the following lines in the platform.bib (immediately before the FILES section):

```
IF BSP_KEYBD_NOP
    kbdmouse.dll    $(_FLATRELEASEDIR)\KbdnopUs.dll                    NK SH
ENDIF; BSP_KEYBD_NOP
```

20.6 Known Issues

N.A.

20.7 Basic Elements for Driver Development

This section provides details of the basic elements for driver development in the Platform System.

20.7.1 BSP Environment Variables

Table 20-24 summarizes the System environment variables.

Table 20-24. System Environment Variables Summary

Name	Definition
BSP_USBOTG	Set to enable Full OTG functionality (enable host-client switching) on the High Speed OTG port
BSP_USB_HSOTG_CLIENT	Set to include USB client functionality on High Speed OTG port
BSP_USB_HSOTG_HOST	Set to include USB host functionality on High Speed OTG port.

20.7.2 Dependencies of Drivers

Table 20-25 summarizes the Microsoft-defined environment variables used in the BSP.

Table 20-25. USB Driver

Name	Definition
SYSGEN_USBFN_SERIAL	Set to support serial class for USB Function controller
SYSGEN_USBFN_STORAGE	Set to support mass storage class for USB Function controller
SYSGEN_USBFN_ETHERNET	Set to support RNDIS class for USB Function controller
SYSGEN_CURSOR	Set to support mouse cursor
SYSGEN_FATFS	Set to support FAT16 file system
SYSGEN_PCL	Set to support PCL printing
SYSGEN_PRINTING	Set to support printer
SYSGEN_STOREMGR	Set to support storage manager
SYSGEN_UDFS	Set to support Universal Disc File System
SYSGEN_USB	Set to support USB driver
SYSGEN_USB_HID	Set to support Human Interface driver (HID) class
SYSGEN_USB_HID_CLIENTS	Set to support HID clients
SYSGEN_USB_HID_KEYBOARD	Set to support HID keyboards (keyboard stub and associated.dll are required)
SYSGEN_USB_HID_MOUSE	Set to support HID mouse
SYSGEN_USB_PRINTER	Set to support Printer (printer driver support, such as PCL (SYSGEN_PCL), may be required)
SYSGEN_USB_STORAGE	Set to support storage medium

20.8 USB Application Tools

This section describes about the application tools that are used for the USB.

20.8.1 Application for USB Peripheral Class Driver Switch

Only one USB peripheral drivers can be active out of many. When multiple class drivers are included in the image, it is convenient for switching. It is convenient for both the end users and test engineers. The following executable programs are added in ..\platform\<*Target Platform*>\files:

switchUsb2Msc.exe, switchUsb2Rndis.exe, switchUsb2Serial.exe, switchUsb2Phdc.exe.

These executable programs are selectively integrated into nk.bin during the generation of OS image. During WinCE start up, the programs can be found in `\WINDOWS` directory. On execution of these programs activate the mass storage, RNDIS, Serial, or PHDC peripheral drivers respectively.

20.8.2 Application for Multispec PHDC Demo

A peripheral side GUI is required to use the PHDC class driver. The application is used to select any data from the available personal health measurements and send the selected data to PC. The PHDC_Peripheral_App.exe is located in the directory ..\platform\<*Target Platform*>\files.

During WinCE start up, the file can be found in `\WINDOWS` directory.

On the host side, Continua Alliance CESL Reference Software is necessary to setup PHDC communication channel. Contact www.continuaalliance.org for more details.

When PC side is ready, run the PHDC_Peripheral_App.exe. It displays a GUI with the following button controls

- **Select Device Spec** Button — Used to select between the four different personal health data category.
- **Send Measurement** Button — Used to send current measurement data category to host.
- **Disconnect** Button — Used to test PHDC protocol level disconnect.

20.8.3 Application for CDC Demo

A peripheral side application uses USB as a virtual COM port to communicate with Host side (PC). This application replicates what it received from virtual COM port on the UART and sends them back to the Host.

Follow the steps below to setup CDC Host driver and configure HyperTerminal application:

1. Turn on the board and ensure that the USB client driver is CDC and then connect with PC. The Found New Hardware window appears as shown in Figure 20-3.

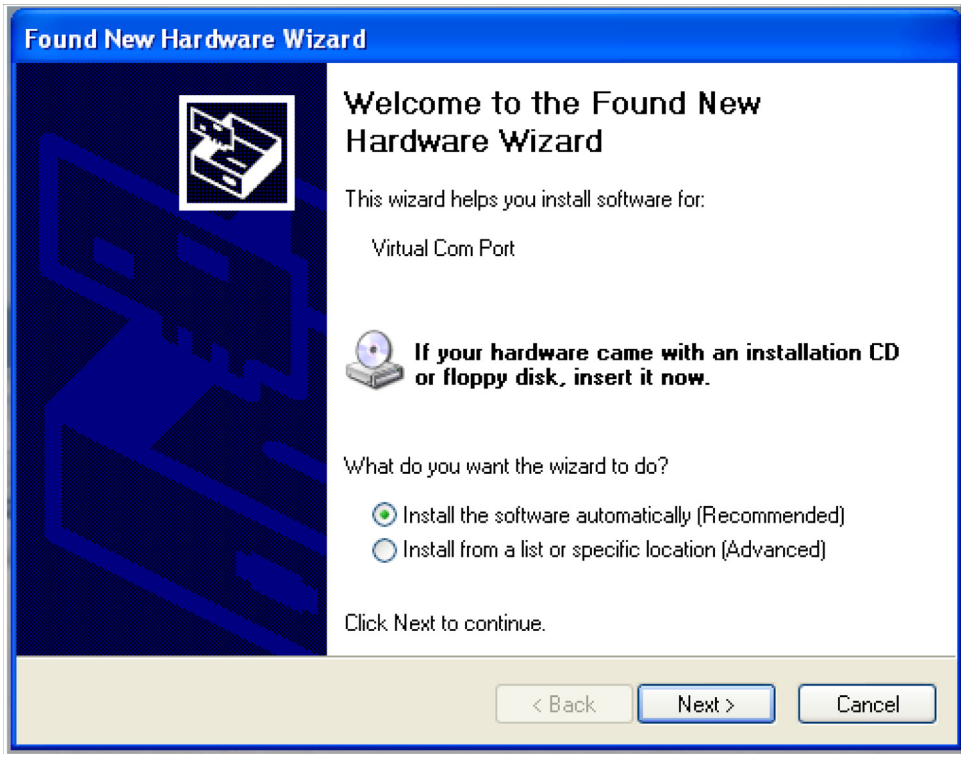

Figure 20-3. Found New Hardware Window

2. Select **Install from a list or specific location (Advanced)** option and click **Next**. The Search and installation options window appears as shown in Figure 20-4.

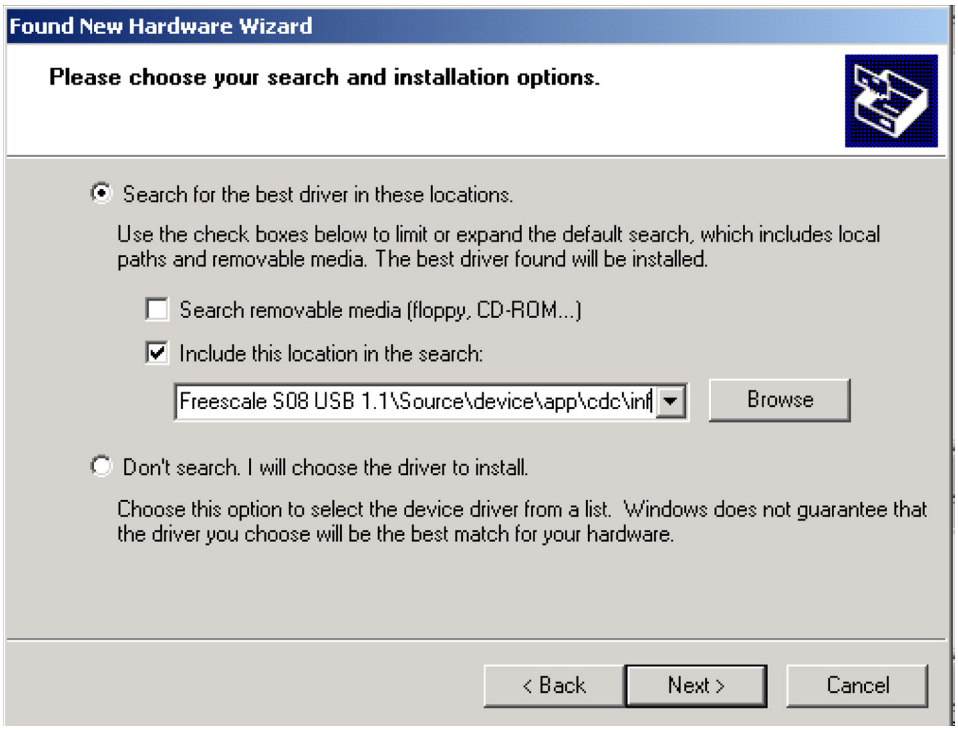

Figure 20-4. Search and Installation Option Window

Point the search path to the inf directory and click **Next**. The inf file is available in `WINCE600\SUPPORT\APP\USB_CDC_APP\INF`. The driver for the device is installed. To verify the installation, open the device manager. TheFSL Virtual COM Port device entries must be visible as shown in Figure 20-5.

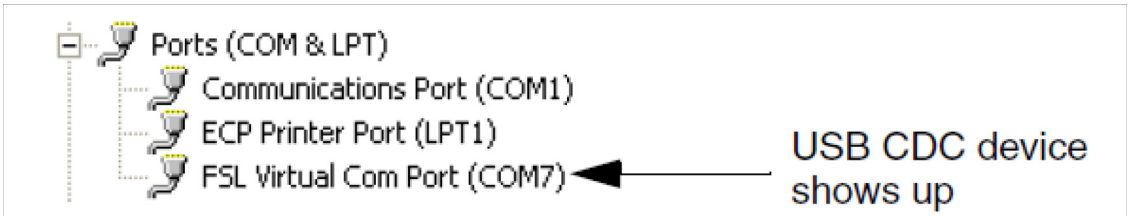

Figure 20-5. Virtual COM Port Device Entries

3. Open the HyperTerminal application as shown in Figure 20-6.

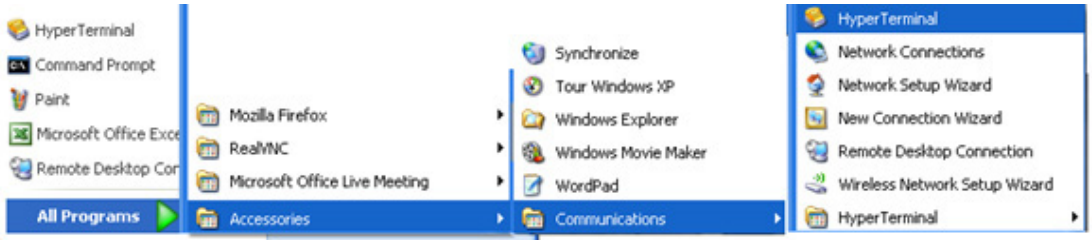

Figure 20-6. Hyper Terminal Application

4. Enter the name of the connection and click **OK**. as shown in Figure 20-7.

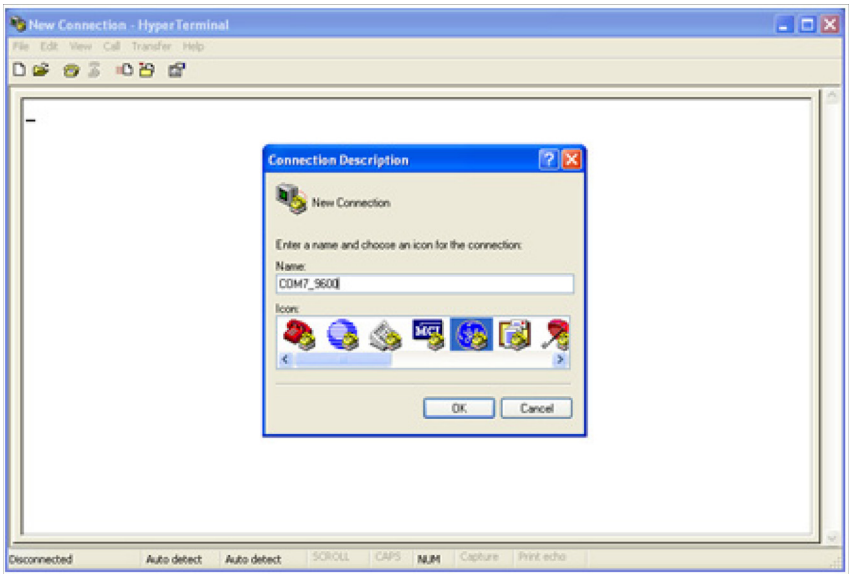

Figure 20-7. Connection Name

5. Select the COM port identical to the one that shows up on the device manager as shown in Figure 20-8.

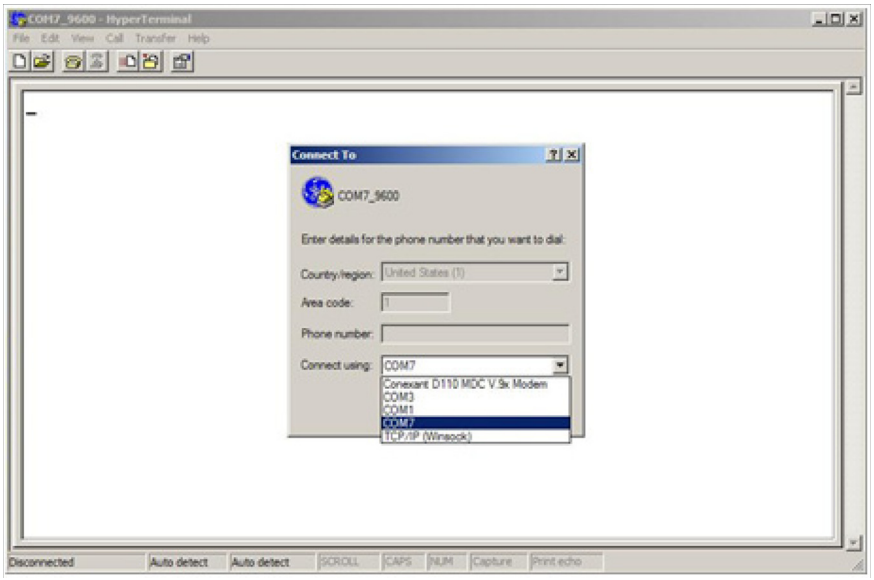

Figure 20-8. COM Port Selection

6. Configure the virtual COM port baud rate and other properties as shown in Figure 20-9.

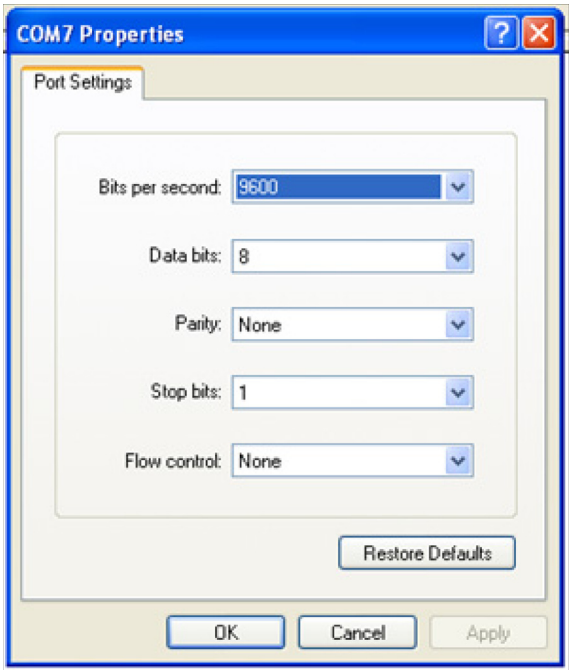

Figure 20-9. COM Port Properties

7. Configure the HyperTerminal. Click on the **OK** button to submit changes as shown in Figure 20-10.

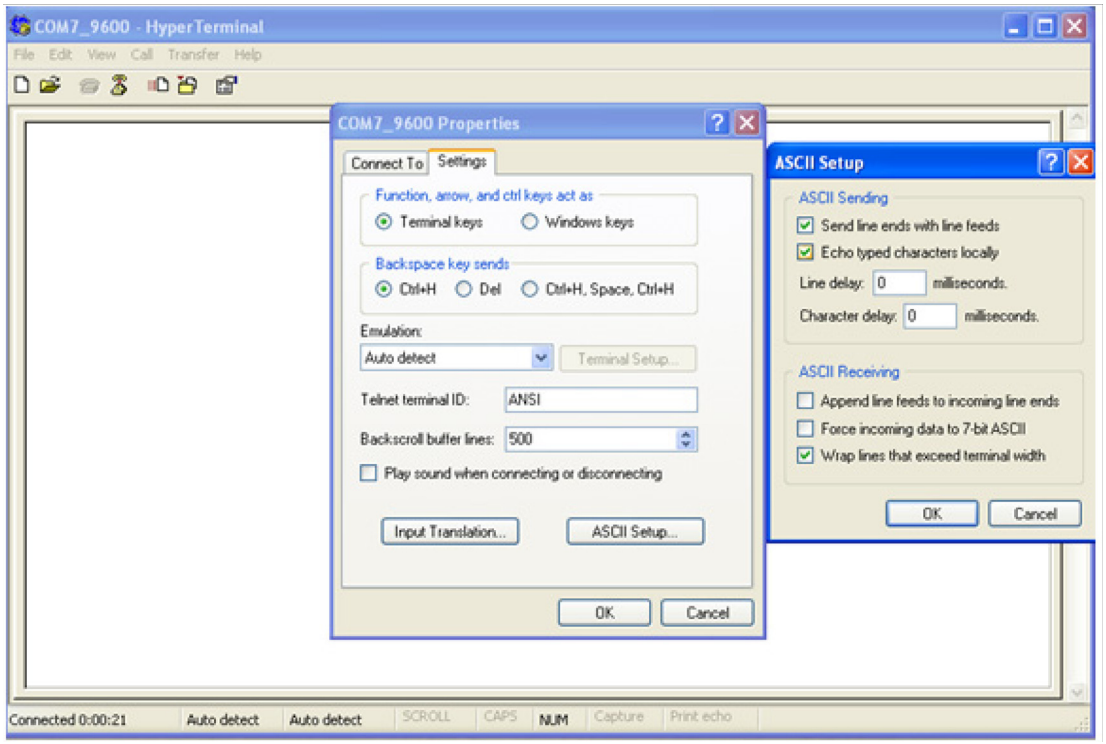

Figure 20-10. HyperTerminal Configuration

8. The HyperTerminal is configured. The values entered are replicated from the virtual COM port. Therefore, it appears as duplicate as shown in Figure 20-11.

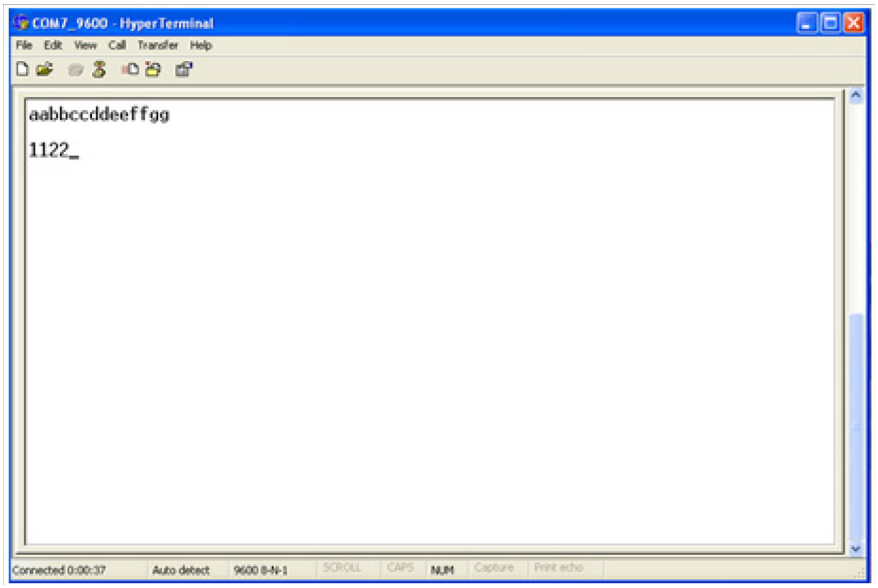

Figure 20-11. Duplicate Values