i.MX6Solo ESAI TDM slot issue (1/)

- Overview
  - The TX output data slot location could be misaligned when ESAI_TX(RX)_CLK frequency is higher than 20.8MHz.
- The customer's setting
  - The customer's system is as Figure-1.
  - They use i.MX6S ESAI for 96KHz TDM 8ch output.
    - In this condition, ESAI_TX_CLK and ESAI_RX_CLK should be 24.576MHz.
  - i.MX6S ESAI is used as clock slave and the clock is provided from external. HF_CLK is not provided.
  - TX data is generated internally and transferred using DMA.
  - This phenomenon can be seen also in the case that ESAI_TX_CLK and ESAI_RX_CLK are generated internally.
  - ESAI is used as 8slot TDM. (Figure-2)
  - Polarity settings for each clock: Rising Edge
    - They tried Falling Edge setting, but the phenomenon came to be worse.
  - Direction settings for each clocks: Input
  - Frame Sync Length(TCR-TFSL) setting: Word Length
  - Sync setting(SAICR-SYN): ASYNC
  - Internal clock settings for the clock to be sent to ESAI: Default (Figure-3, Figure-4-1, Figure-4-2)
    - ESAI clock can be up to 33MHz (132MHz/4)
  - Word Length and Slot Length setting(TSWS): Word Length:24bit, Slot Length:32bit(0x1F)
  - When the issue occurred, no error bit was found in status register(SAISR).
    - They confirmed no underrun nor overrun error was found in SAISR captured in interrupt service routine.
    - Please find another attached file for register dump. Please note the dump was captured after the software stoped and overrun/underrun error bit was set due to the software stop.

i.MX6Solo ESAI TDM slot issue(2/)

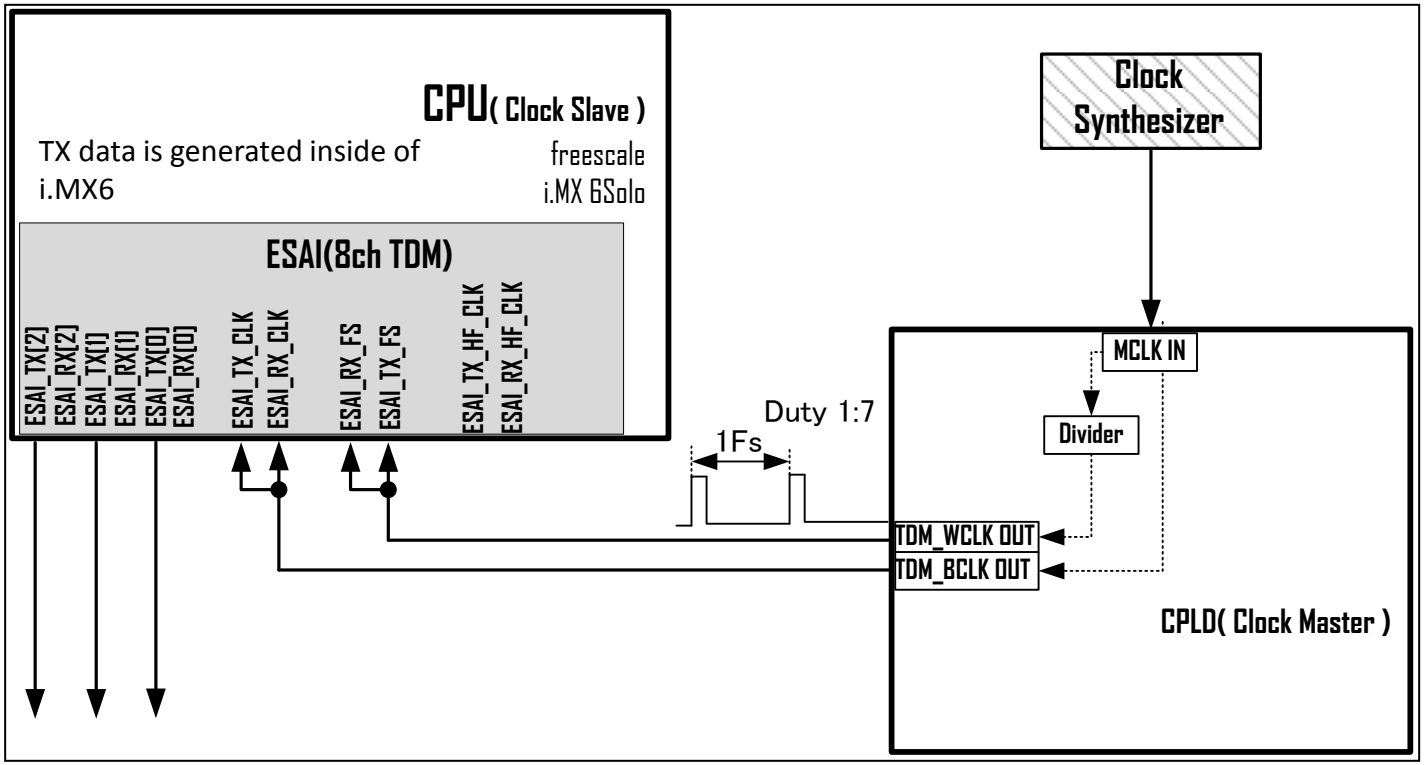


Figure-1

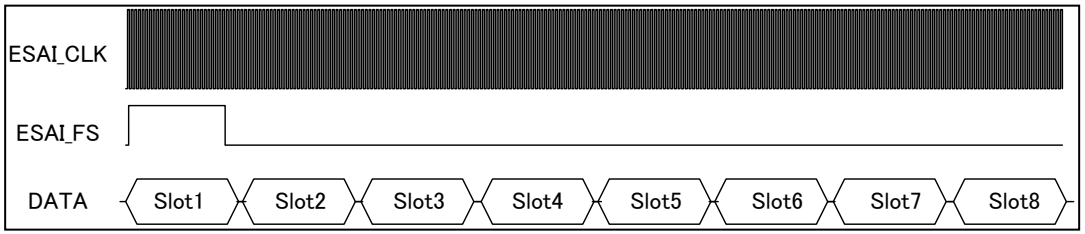
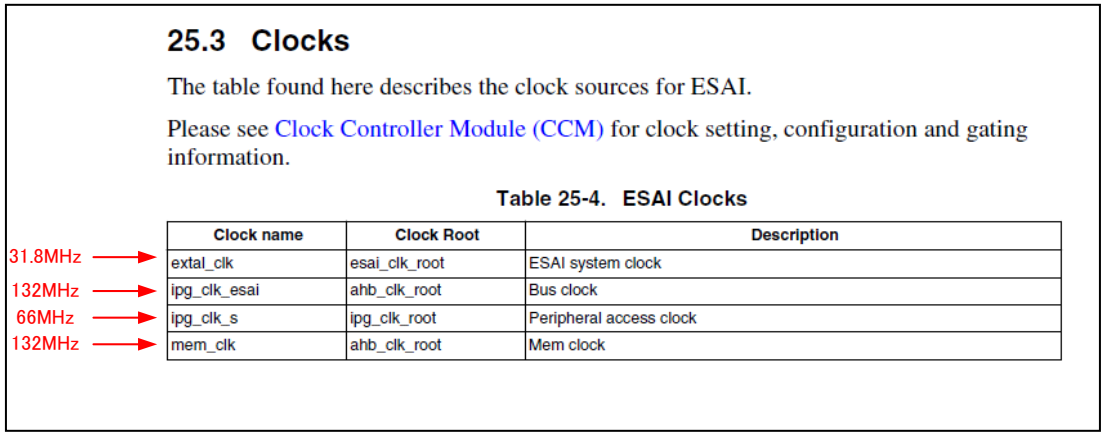


Figure-2 8 slots TDM data

i.MX6Solo ESAI TDM slot issue(3/)



25.3 Clocks

The table found here describes the clock sources for ESAI.

Please see Clock Controller Module (CCM) for clock setting, configuration and gating information.

Table 25-4. ESAI Clocks

	Clock name	Clock Root	Description
31.8MHz →	extal_clk	esai_clk_root	ESAI system clock
132MHz →	ipg_clk_esai	ahb_clk_root	Bus clock
66MHz →	ipg_clk_s	ipg_clk_root	Peripheral access clock
132MHz →	mem_clk	ahb_clk_root	Mem clock

Figure-3 ESAI clocks setting

i.MX6Solo ESAI TDM slot issue(4/)

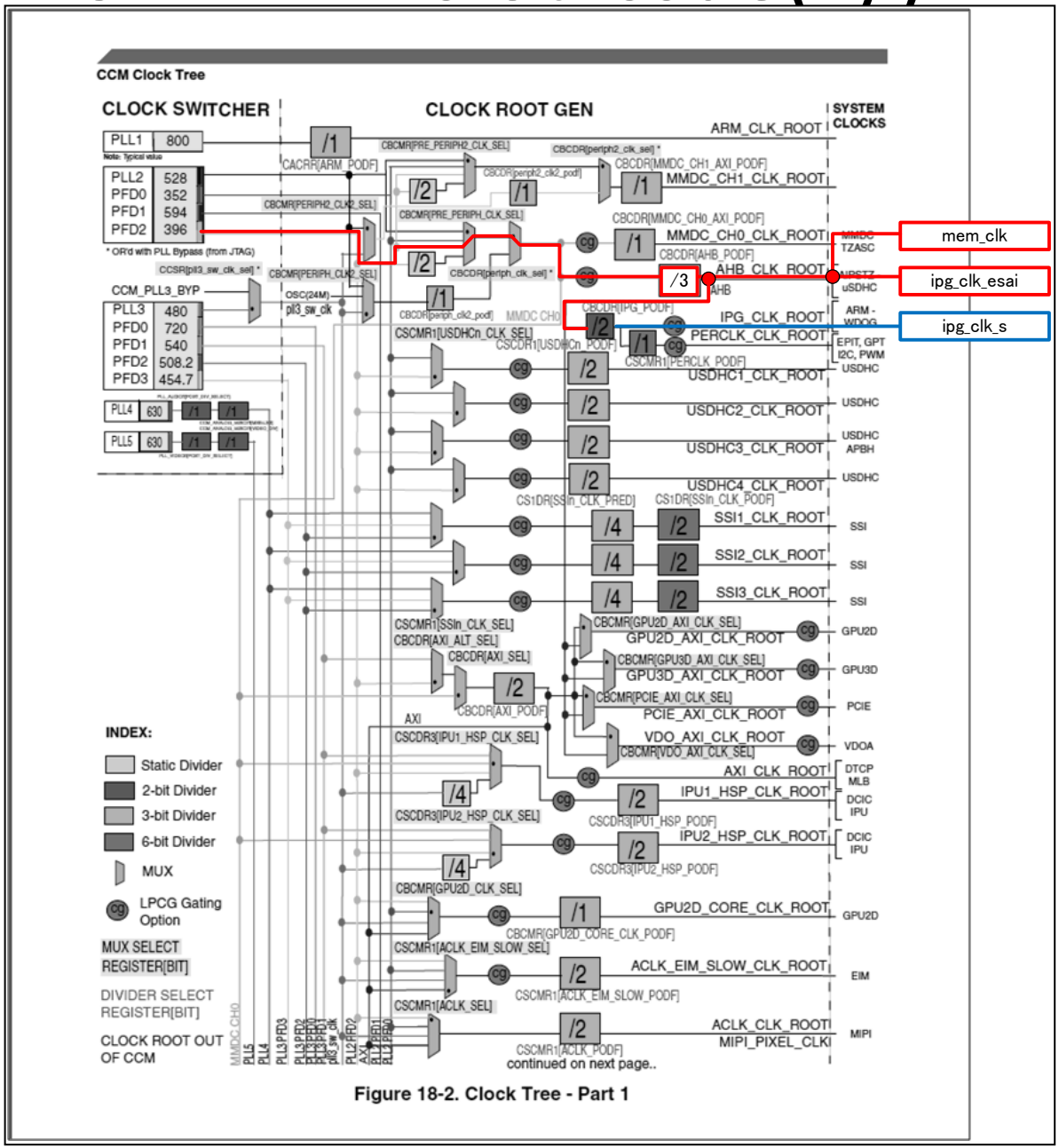


Figure 18-2. Clock Tree - Part 1

Figure-4-1 clock tree setting

i.MX6Solo ESAI TDM slot issue(5/)

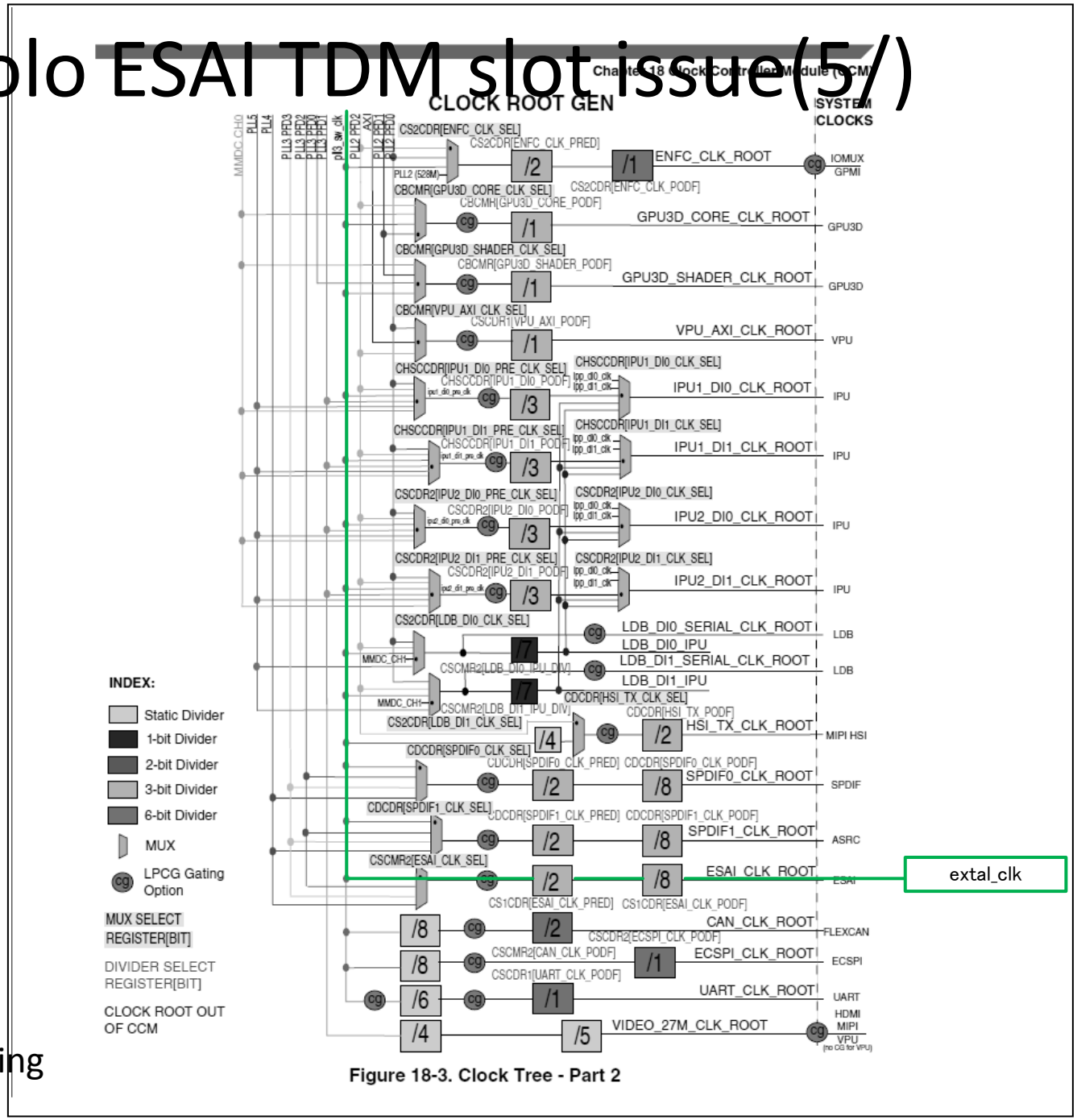


Figure 18-3. Clock Tree - Part 2

Figure-4-2 clock tree setting

i.MX6Solo ESAI TDM slot issue(6/)

- Phenomenon
  - For the test, the data of slot1 TX is set to 0xFFFFFF00 and the data of other slots are set to 0 inside of i.MX6S in order to monitor the waveform of the slot data easily.
  - In above situation, the TX output from i.MX6S should be as Figure-5.
  - The slot misalignment could be seen in the customer's lab. (Figure-6)
  - Figure-6 shows that the slot1 data location is misaligned.
  - The customer tested if the issue can occur with various ESAI_TX(RX)_CLK frequencies. As the result, they found that the issue could occur only when the frequency of ESAI_TX(RX)_CLK input is higher than 20.8MHz.
  - In the case of lower ESAI_TX(RX)_CLK frequency than 20.8MHz, the issue does not occur.
  - For the test, they tried with 198MHz of ahb_root_clk (CBCDR[AHB_PODF] divisor = 1/2). In this case, the issue did not occur even when the ESAI_TX(RX)_CLK is higher than 20.8MHz. From this test, the quality of ESAI_TX(RX)_CLK signal generated externally seems to be OK.

i.MX6Solo ESAI TDM slot issue(7/)

ESAI_TX

ESAI_FS

Figure-5 Expected behavior

Figure-6 slot location misalignment