Chapter 3
Interrupts and SDMA Events

3.1 Overview

The Interrupts and SDMA Events chapter provides information on the assignments of the interrupts of the ARM platform domain in ARM Platform Interrupts and of the DMA events in SDMA Event Mapping.

3.2 ARM Platform Interrupts

The TrustZone Aware Interrupt Controller (TZIC) collects up to 128 interrupt requests from all MCIMX53 sources and provides an interface to the core. Each interrupt can be configured as a normal or a secure interrupt. Software force registers and software priority masking are also supported. Table 3-1 details the ARM Cortex A8^{tm} Platform (ARM) interrupt sources.

Table 3-1. ARM Domain Interrupt Summary

IRQ	Interrupt Source	Interrupt Description
0	Reserved	Reserved
1	ESDHCV2-1	Enhanced SDHC Interrupt Request
2	ESDHCV2-2	Enhanced SDHC Interrupt Request
3	ESDHCV3-3	CE-ATA Interrupt Request based on ESDHCV3-3
4	ESDHCV2-4	Enhanced SDHC Interrupt Request
5	DAP	
6	SDMA	AND of all 48 interrupts from all the channels
7	IOMUXC	POWER FAIL interrupt. This is a power fail indicator interrupt from on board power management IC via GPIO_16 PAD on ALT2, PWRFAIL_INT signal.

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Table 3-1. ARM Domain Interrupt Summary (continued)

IRQ	Interrupt Source	Interrupt Description
8	EXTMC	NFC interrupt
9	VPU	VPU Interrupt Request
10	IPU	IPU Error Interrupt
11	IPU	IPU Sync Interrupt
12	GPU3D	GPU Interrupt Request
13	UART-4	UART-4 ORed interrupt
14	USB	USB Host 1
15	EXTMC	Consolidated EXTMC Interrupt
16	USB	USB Host 2
17	USB	USB Host 3
18	USB	USB OTG
19	SAHARA	SAHARA Interrupt for Host 0
20	SAHARA	SAHARA Intr for Host 1
21	SCC	Security Monitor High Priority Interrupt Request.
22	SCC	Secure (TrustZone) Interrupt Request.
23	SCC	Regular (Non-Secure) Interrupt Request.
24	SRTC	SRTC Consolidated Interrupt. Non TZ.
25	SRTC	SRTC Security Interrupt. TZ.
26	RTIC	RTIC (Trust Zone) Interrupt Request. Indicates that the RTIC has completed hashing the selected memory block(s) during single-hash/boot mode.
27	CSU	CSU Interrupt Request 1. Indicates to the processor that one or more alarm inputs were asserted
28	SATA	SATA interrupt request
29	SSI-1	SSI-1 Interrupt Request
30	SSI-2	SSI-2 Interrupt Request
31	UART-1	UART-1 ORed interrupt
32	UART-2	UART-2 ORed interrupt
33	UART-3	UART-3 ORed interrupt
34	IPTP	RTC (IEEE1588) interrupt request
35	IPTP	PTP (IEEE1588) interrupt request
36	ECSPI-1	ECSPI-1 interrupt request line to the core.
37	ECSPI-2	ECSPI-2 interrupt request line to the core.
38	CSPI	CSPI interrupt request line to the core.

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Table 3-1. ARM Domain Interrupt Summary (continued)

IRQ	Interrupt Source	Interrupt Description
39	GPT	OR of GPT Rollover interrupt line, Input Capture 1 & 2 lines, Output Compare 1, 2 &3 Interrupt lines
40	EPIT-1	EPIT-1 output compare interrupt
41	EPIT-2	EPIT-2 output compare interrupt
42	GPIO-1	Active HIGH Interrupt from INT7 from GPIO
43	GPIO-1	Active HIGH Interrupt from INT6 from GPIO
44	GPIO-1	Active HIGH Interrupt from INT5 from GPIO
45	GPIO-1	Active HIGH Interrupt from INT4 from GPIO
46	GPIO-1	Active HIGH Interrupt from INT3 from GPIO
47	GPIO-1	Active HIGH Interrupt from INT2 from GPIO
48	GPIO-1	Active HIGH Interrupt from INT1 from GPIO
49	GPIO-1	Active HIGH Interrupt from INT0 from GPIO
50	GPIO-1	Combined interrupt indication for GPIO-1 signal 0 throughout 15
51	GPIO-1	Combined interrupt indication for GPIO-1 signal 16 throughout 31
52	GPIO-2	Combined interrupt indication for GPIO-2 signal 0 throughout 15
53	GPIO-2	Combined interrupt indication for GPIO-2 signal 16 throughout 31
54	GPIO-3	Combined interrupt indication for GPIO-3 signal 0 throughout 15
55	GPIO-3	Combined interrupt indication for GPIO-3 signal 16 throughout 31
56	GPIO-4	Combined interrupt indication for GPIO-4 signal 0 throughout 15
57	GPIO-4	Combined interrupt indication for GPIO-4 signal 16 throughout 31
58	WDOG-1	Watchdog Timer reset
59	WDOG-2	TrustZone Watchdog Timer reset
60	KPP	Keypad Interrupt
61	PWM-1	Cumulative interrupt line. OR of Rollover Interrupt line, Compare Interrupt line and FIFO Waterlevel crossing interrupt line.
62	I2C-1	I2C-1 Interrupt
63	I2C-2	I2C-2 Interrupt
64	I2C-3	I2C-3 Interrupt
65	MLB	NOR of all interrupts, mlb_cint and mlb_sint

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Table 3-1. ARM Domain Interrupt Summary (continued)

IRQ	Interrupt Source	Interrupt Description
66	ASRC	ASRC Interrupt for core 1
67	SPDIF	SPDIF Tx interrupt OR SPDIF Rx interrupt
68	Reserved	Reserved
69	IIM	Interrupt request to the processor. Indicates to the processor that program or explicit sense cycle is completed successfully or in case of error. This signal is low-asserted.
70	PATA	Parallel ATA host controller interrupt request
71	CCM	CCM, Interrupt Request 1
72	CCM	CCM, Interrupt Request 2
73	GPC	GPC, Interrupt Request 1
74	GPC	GPC, Interrupt Request 2
75	SRC	SRC interrupt request
76	P_PLATFORM_NE_32K_256K	Neon Monitor Interrupt
77	P_PLATFORM_NE_32K_256K	Performance Unit Interrupt (nPMUIRQ). This is an interrupt generated by the ARMCORE and used for system profiling and debug. GPIO_16 PAD in ALT3 mode acts as nPMUIRQ signal (also named PMU_IRQ_B signal).
78	P_PLATFORM_NE_32K_256K	CTI IRQ
79	P_PLATFORM_NE_32K_256K	Debug Interrupt, from Cross-Trigger 1 Interface 1
80	P_PLATFORM_NE_32K_256K	Debug Interrupt, from Cross-Trigger 1 Interface 0
81	ESAI	ESAI interrupt
82	FLEXCAN-1	NOR of all interrupts; ipi_int_mbor, ipi_int_wakein, ipi_int_busoff and ipi_int_error.
83	FLEXCAN-2	NOR of all interrupts; ipi_int_mbor, ipi_int_wakein, ipi_int_busoff and ipi_int_error.
84	OPENVG	General Interrupt
85	OPENVG	Busy signal (for S/W power gating feasibility)
86	UART-5	UART-5 ORed interrupt
87	FEC	Fast Interrupt Request (OR of 13 interrupt sources)
88	OWIRE	1-Wire Interrupt Request
89	P_PLATFORM_NE_32K_256K	Debug Interrupt, from Cross-Trigger 1 Interface 2
90	SJC	
91	Reserved	Reserved
92	TVE	
93	FIRI	FIRI Intr (OR of all 4 interrupt sources)

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Table 3-1. ARM Domain Interrupt Summary (continued)

IRQ	Interrupt Source	Interrupt Description
94	PWM-2	Cumulative interrupt line. OR of Rollover Interrupt line, Compare Interrupt line and FIFO Waterlevel crossing interrupt line.
95	Reserved	Reserved for SLM
96	SSI-3	SSI-3 Interrupt Request
97	Reserved	
98	P_PLATFORM_NE_32K_256K	Debug Interrupt, from Cross-Trigger 1 Interface 3
99	Reserved	Was belong to SLM
100	VPU	Idle interrupt from VPU (for S/W power gating)
101	EXTMC	Indicates all pages have been transferred to NFC during an auto_prog operation
102	GPU3D	Idle interrupt from GPU (for S/W power gating)
103	GPIO-5	Combined interrupt indication for GPIO-5 signal 0 throughout 15
104	GPIO-5	Combined interrupt indication for GPIO-5 signal 16 throughout 31
105	GPIO-6	Combined interrupt indication for GPIO-6 signal 0 throughout 15
106	GPIO-6	Combined interrupt indication for GPIO-6 signal 16 throughout 31
107	GPIO-7	Combined interrupt indication for GPIO-7 signal 0 throughout 15
108	GPIO-7	Combined interrupt indication for GPIO-7 signal 16 throughout 31
109_128	Reserved	Reserved

3.3 SDMA Event Mapping

Table 3-2 shows the DMA request signals for peripherals in i.MX53.

Table 3-2. SDMA Event Mapping

Event Number	DMA Source	Description
0	VPU	VPU DMA request
1	GPC	Will be used for power management.
2	UART-4 PATA	UART-4RX muxed with PATA RX (selector IOMUXC GPR0 register bit [7]).

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Table 3-2. SDMA Event Mapping (continued)

Event Number	DMA Source	Description
3	UART-4 PATA	UART-4TX muxed with PATA TX (selector IOMUXC GPR0 register bit [8]).
4	PATA	PATA Transfer End
5	IPU	IPU DMA Event
6	ECSPI	DMA Rx request
7	ECSPI-1	DMA Tx request
8	ECSPI-2	DMA Rx request
9	ECSPI-2	DMA Tx request
10	I2C-3 ESDHCV3-3	I2C-3 muxed with ESDHCV3-3
11	ESDHCV2-4 CTI2	ESDHC4 muxed with CTI2 (SDMA_CTI) trigger_out[0] connected to SDMA event.
12	UART-2 FIRI	UART-2RX muxed with FIRI REQ[0] (selector IOMUXC GPR0 register bit [9]).
13	UART-2 FIRI	UART-2TX muxed with FIRI REQ[1] (selector IOMUXC GPR0 register bit [10]).
14	SPDIF IOMUXC	SPDIF RX DMA request Muxed with External DMA request #0 from PAD DISP0_DAT16 or GPIO_17 (using daisy chain selector). The event selector is in IOMUXC GPR0 register bit [4].
15	SPDIF	SPDIF TX DMA request
16	UART-5	Rx FIFO of UART-5
17	UART-5	Tx FIFO of UART-5
18	UART-1	Rx FIFO of UART-1
19	UART-1	Tx FIFO of UART-1
20	I2C-1 ESDHCV2-1	I2C-1 muxed with ESDHCV2-1
21	I2C-2 ESDHCV2-2	I2C-2 muxed with ESDHCV2-2
22	SSI-2	SSI-2 receive 2 DMA request
23	SSI-2	SSI-2 transmit 2 DMA request
24	SSI-2	SSI-2 receive 1 DMA request
25	SSI-2	SSI-2 transmit 1 DMA request
26	SSI-1	SSI-1 receive 2 DMA request
27	SSI-1	SSI-1 transmit 2 DMA request
28	SSI-1	SSI-1 receive 1 DMA request
29	SSI-1	SSI-1 transmit 1 DMA request
30	EXTMC	Asserts every time NFC finishes reading a page
31	EXTMC	Asserts at the beginning of auto-program sequence, and every time the NFC finishes transferring data from the RAM to the NAND (Meaning, the SDMA can write to the RAM the next page).

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Table 3-2. SDMA Event Mapping (continued)

Event Number	DMA Source	Description
32	ASRC	ASRC dma1 request (Pair A input Request)
33	ASRC	ASRC dma2 request (Pair B input Request)
34	ASRC	ASRC dma3 request (Pair C input Request)
35	ASRC	ASRC dma4 request (Pair A output Request)
36	ASRC	ASRC dma5 request (Pair B output Request)
37	ASRC	ASRC dma6 request (Pair C output Request)
38	CSPI EPIT-2	CSPI DMA Rx request Muxed with EPIT-2 DMA request
39	CSPI IOMUXC	CSPI DMA Tx request Muxed with External DMA request #1 from PAD DISP0_DAT17 or GPIO_18 (using daisy chain selector). The event selector is in IOMUXC GPR0 register bit [6].
40	ESAI	ESAI Rx FIFO DMA request
41	ESAI	ESAI Tx FIFO DMA request
42	UART-3	Rx FIFO of UART-3
43	UART-3	Tx FIFO of UART-3
44	SSI-3	SSI-3 receive 2 DMA request
45	SSI-3	SSI-3 transmit 2 DMA request
46	SSI-3	SSI-3 receive 1 DMA request
47	SSI-3	SSI-3 transmit 1 DMA request

As shown in the table, some of the events are shared through a multiplexer. The select of shared DMA event sources is controlled by DMAREQ_MUX_SELn fields of the IOMUXC.IOMUXC_GPRO Register.

For other shared connectivity peripherals that do not have dedicated DMA request signals, the ARM platform interrupt service routines have the option to program the SDMA to move data between the peripheral and memory.