NXP Semiconductors
User's Guide

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i.MX 8M Plus Hardware Developer’s Guide

Chapter 1
Overview

This document aims to help hardware engineers design and test the i.MX 8M Plus series processors. It provides examples on board layout and design checklists to ensure first-pass success, and solutions to avoid board bring-up problems.

Engineers should understand board layouts and board hardware terminology.

This guide is released with relevant device-specific hardware documentation, such as datasheets, reference manuals, and application notes. All these documents are available on www.nxp.com/imx8mplusevk.

1.1 Device supported

This document supports the i.MX 8M Plus (15 x 15 mm package).

1.2 Essential references

This guide is supplementary to the i.MX 8M Plus series chip reference manuals and data sheets. For reflow profile and thermal limits during soldering, see General Soldering Temperature Process Guidelines (document AN3300). These documents are available on www.nxp.com/i.MX8MPLUS.

1.3 Supplementary references

1.3.1 General information

The following documents introduces the Arm® processor architecture and computer architecture.

- For information about the Arm Cortex-A53 processor, see www.arm.com/products/processors/cortex-a/cortex-a53-processor.php
- For information about the Arm Cortex-M7 processor, see https://www.arm.com/products/processors/cortex-m/cortex-m7-processor.php
- Computer Architecture - A Quantitative Approach (Fourth Edition) - John L. Hennessy and David A. Patterson
- Computer Organization and Design - The Hardware/Software Interface (Second Edition) - David A. Patterson and John L. Hennessy

The following documentation introduces the high-speed board design:

- Right the First Time- A Practical Handbook on High Speed PCB and System Design - Volumes I & II - Lee W. Ritchey (Speeding Edge) - ISBN 0-9741936- 0-72
- Signal and Power Integrity Simplified (2nd Edition) - Eric Bogatin (Prentice Hall)- ISBN 0-13-703502-0
- High Speed Digital Design- A Handbook of Black Magic - Howard W. Johnson & Martin Graham (Prentice Hall) - ISBN 0-13-395724-1
- High Speed Signal Propagation- Advanced Black Magic - Howard W. Johnson & Martin Graham - (Prentice Hall) - ISBN 0-13-084408-X
- High Speed Digital System Design- A handbook of Interconnect Theory and Practice - Hall, Hall and McCall (Wiley Interscience 2000) - ISBN 0-36090-2
- Signal Integrity Issues and Printed Circuit Design - Doug Brooks (Prentice Hall) ISBN 0-13-141884-X
- PCB Design for Real-World EMI Control - Bruce R. Archambeault (Kluwer Academic Publishers Group) - ISBN 1-4020-7130-2
- Digital Design for Interference Specifications - A Practical Handbook for EMI Suppression -David L. Terrell & R. Kenneth Keenan (Newnes Publishing) - ISBN 0-7506-7282-X

- Electromagnetic Compatibility Engineering - Henry Ott (1st Edition - John Wiley and Sons) - ISBN 0-471-85068-3
- Introduction to Electromagnetic Compatibility - Clayton R. Paul (John Wiley and Sons) - ISBN 978-0-470-18930-6
- Grounding & Shielding Techniques - Ralph Morrison (5th Edition - John Wiley & Sons) - ISBN 0-471-24518-6
- EMC for Product Engineers - Tim Williams (Newnes Publishing) - ISBN 0-7506- 2466-3

1.4 Related documentation

Additional literature will be published in the future.

For the list of current documents, see i.MX8MPLUS and AN4579.

1.5 Conventions

Table 1 lists the notational conventions used in this document.

Table 1. Conventions used in the document

Conventions	Description
`Courier`	Used to indicate commands, command parameters, code examples, and file and directory names.
Italics	Used to indicates command or function parameters.
Bold	Function names are written in bold.
cleared/set	When a bit takes the value zero, it means to be cleared; when it takes a value of one, it means to be set.
mnemonics	Instruction mnemonics are shown in lowercase bold. Book titles in text are set in italics.
sig_name	Internal signals are written in all lowercase.
nnnn nnnnh	Denotes hexadecimal number
0b	Denotes binary number
rA, rB	Instruction syntax used to identify a source GPR
rD	Instruction syntax used to identify a destination GPR
REG[FIELD]	Abbreviations for registers are shown in uppercase. Specific bits, fields, or ranges appear in brackets. For example, MSR[LE] refers to the little-endian mode enable bit in the machine state register.
x	An italicized *x* indicates an alphanumeric variable.
n, m	An italicized *n* indicates a numeric variable.

In this document, notation for all logical, bit-wise, arithmetic, comparison, and assignment operations follow C Language conventions.

1.6 Acronyms and abbreviations

Table 2 defines the acronyms and abbreviations used in this document.

Table 2. Definitions and acronyms

Acronym	Definition
ARM	Advanced RISC Machines processor architecture
BGA	Ball Grid Array package
BOM	Bill of Materials
BSDL	Boundary Scan Description Language
CAN	Flexible Controller Area Network peripheral
CCM	Clock Controller Module
CSI	MIPI Camera Serial Interface
DDR	Dual Data Rate DRAM
DDR4	DDR4 DRAM
DDRC	DDR Controller
DFP	Downstream Facing Port (USB Type-C)
DRP	Dual Role Port (USB Type-C)
ECSPI	Enhanced Configurable SPI peripheral
EIM	External Interface Module
ENET	10/100/1000 Mbps Ethernet MAC peripheral
EPIT	Enhanced Periodic Interrupt Timer peripheral
ESR	Equivalent Series Resistance
GND	Ground
GPC	General Power Controller
GPIO	General Purpose Input/Output
I^2C	Inter-integrated Circuit interface
IBIS	Input output Buffer Information Specification
IOMUX	i.MX 8M Plus chip-level I/O multiplexing
JTAG	Joint Test Action Group
KPP	Keypad Port Peripheral

Table continues on the next page...

Table 2. Definitions and acronyms (continued)

Acronym	Definition
LDB	LVDS Display Bridge
LDO	Low Drop-Out regulator
LPCG	Low Power Clock Gating
LPDDR4	Low Power DDR4 DRAM
LVDS	Low-Voltage Differential Signaling
ODT	On-Die Termination
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCIe	PCI Express
PCISig	Peripheral Component Interconnect Special Interest Group
PDN	Power Distribution Network
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
PTH	Plated Through Hole PCB (that is, no microvias)
RGMII	Reduced Gigabit Media Independent Interface (Ethernet)
RMII	Reduced Media Independent Interface (Ethernet)
ROM	Read-Only Memory

Chapter 2
i.MX 8M Plus design checklist

This document provides a design checklist for the i.MX 8M Plus (15 x 15 mm package) processor. The design checklist tables recommend optimal design and provide explanations to help users understand better. All supplemental tables referenced by the checklist appear in sections following the design checklist tables.

2.1 Design checklist table

Table 3. LPDDR4 recommendations (i.MX 8M Plus)

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Connect the DRAM_ZN ball on the processor (ball R1) to a 240 Ω, 1% resistor to GND.	This is a reference used during DRAM output buffer driver calibration.
	2. The ZQ0 and ZQ1 balls on the LPDDR4 device should be connected through 240Ω, 1% resistors to the LPDDR4 VDD2 rail.	—
	3. Place a 10 kΩ, 5% resistor to ground on the DRAM reset signal.	This will ensure adherence to the JEDEC specification until the control is configured and starts driving the DDR.
	4. The ODT_CA balls on the LPDDR4 device should be connected directly to the LPDDR4 VDD2 rail.	LPDDR4 ODT on the i.MX 8M Plus is command-based, making processor ODT_CA output balls unnecessary.
	5. The architecture for each chip inside the DRAM package must be x 16.	The processor does not support byte mode specified in JESD209-4B.
	6. The processor ball MTEST (ball P2), should be left unconnected.	These are observability ports for manufacturing and are not used otherwise.
	7. The VREF pin on the processor (ball R2) can be left unconnected.	The VREF signal for LPDDR4 is generated internally by the processor.
	8. It is strongly suggested to use LPDDR4 if lower power consumption is required since DLL-off mode is not supported.	The LPDDR4 can operate at low frequency without DLL-off mode.

Table 4. DDR4 recommendations (i.MX 8M Plus)

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Connect the ZQ(DRAM_ZN) ball on the processor (ball R1) to individual 240 Ω, 1% resistors to GND.	This is a reference used during DRAM output buffer driver calibration.
	2. The ZQ ball on each DDR4 device should be connected through individual 240 Ω, 1% resistors to GND.	—

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Table 4. DDR4 recommendations (i.MX 8M Plus) (continued)

Check box	Recommendations	Explanation/Supplemental recommendations
	3. Place a 10 kΩ, 5% resistor to ground on the DRAM reset signal.	This will ensure adherence to the JEDEC specification until the control is configured and starts driving the DDR.
	4. The processor ball MTEST (ball P2), should be left unconnected.	These are observability ports for manufacturing and are not used otherwise.
	5. If boundary scan mode of the DDR4 DRAM device is to be used to test connectivity with the i.MX 8M Plus, TEN pin of the DRAM device should be routed to a test point and pulled to GND through a resistor. Otherwise it can be directly connected to GND. See Testing DDR4 connectivity using boundary scan for details about the limitations of the DRAM_RESET_N signal in the boundary scan mode.	TEN=HIGH makes the DDR4 DRAM device enter boundary scan mode(connectivity test mode). For normal operation, TEN must be LOW.
	6. DLL-off mode is not supported, which means DDR4 cannot run in low frequency, such as 100 MTS.	The power consumption for low power mode in DDR4 system will be higher compared with LPDDR4 system.

NOTE

Refer to i.MX 8M Plus data sheet for supported DDR chip selects and bus width configurations.

Table 5. I^2C recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Verify the target I^2C interface clock rates	The I^2C bus can only be operated as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I^2C port.
	2. Verify that there are no I^2C address conflicts on any of the I^2C buses utilized	There are multiple I^2C ports available on chip, so if a conflict exists, move one of the conflicting devices to a different I^2C bus. If it is impossible, use a I^2C bus switch (NXP part number PCA9646).
	3. Do not place more than one set of pull-up resistors on the I^2C lines.	This could result in excessive loading and potential incorrect operation. Choose the pull-up value commensurate with the bus speed being used.
	4. Ensure that the VCC rail powering the i.MX 8M Plus I^2C interface balls matches the supply voltage used for the pull-up resistors and the slave I^2C devices.	Prevent device damage or incorrect operation due to voltage mismatch.

Table 6. JTAG recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Do not use external pullup or pulldown resistors on JTAG_TDO.	JTAG_TDO is configured with an on-chip keeper circuit and the floating condition is actively eliminated.
	2. Follow the recommendations for external pull-up and pull-down resistors given in Table 15.	—
	3. For normal operation, JTAG_MOD (ball G20) should be pulled down using a 10KOhm resistor. To enter boundary-scan mode, this pin should be pulled up to NVCC_JTAG using a 2.2KOhm resistor. Please reference “COMPLIANCE_PATTERNS” in the chip BSDL file.	—

Table 7. Reset and ON/OFF recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. The POR_B input must be asserted at powered up and remain asserted until the last power rail for devices required for system boot are at their working voltage. This functionality is controlled by the PMIC (PCA9450CHN) on EVK.	POR_B is driven by the PMIC. If a reset button is used, it should be connected to the PMIC_RST_B pin of the PMIC instead of directly connected to POR_B pin of the CPU. When POR_B is asserted (low) on the i.MX 8M Plus, the output PMIC_ON_REQ remains asserted (high).
	2. For portable applications, the ONOFF pin may be connected to an ON/OFF SPST push-button switch to ground. An external pull-up resistor is required on this pin.	A brief connection to GND in OFF mode causes the internal power management state machine to change state to ON. In ON mode, a brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). The connection to GND for approximate 5 seconds or more causes a forced OFF.
	3. Connect GPIO1_IO02(WDOG_B, ball B6) to external PMIC or reset IC to repower the system except SNVS is strongly recommended.	i.MX8M Plus cannot be reset by internal reset source in idle mode, repower is preferred. Some peripherals like SD3.0, QSPI also need repower during system reset.
	4. GPIO1_IO02(WDOG_B, ball B6) is used as Cold Reset. If using a PMIC other than PCA9450, an external pull-up resistor (100 Kohm) might be required to support boundary-scan mode.	In boundary-scan mode, WDOG_B is floating. Without the external 100 Kohm pull up, WDOG_B might repeatedly reset the system when entering boundary-scan mode. The PCA9450 disables WDOG_B reset by default, so will not be impacted.

Table 8. PCIe recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Use an appropriate external PCIe reference clock generator.	The NXP EVK board design uses an IDT 9FGV0241 device. However, NXP does not recommend one supplier over another, and does not suggest that this is the only clock generator supplier. The device used should support all the specs (jitter, accuracy, etc.).
	2. The differential transmitters from the processor must be AC coupled. It is recommended to use a 0.1 μF cap on both the PCIE_TXP and PCIE_TXN outputs.	PCIe specification compliance requires AC coupling at each transmitter. The receiver must be DC coupled.
	3. The PCIEx_RESREF ball (ball F16) should be connected to the ground through a 8.2 K Ω, 1% resistor.	—

Table 9. USB recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Connect a 200 Ω, 1% resistor to the ground on the USBx_TXRTUNE ball (ball F10 and F12).	—
	2. Route all USB differential signals with 90 Ω differential impedance.	—
	3. ESD protection should be implemented at the connector pins. Choose a low capacitance device recommended for high-speed interfaces.	This will prevent potential damages to board components from ESD.
	4. USB1_DNU, USB2_DNU are not functional, recommend to use common GPIO if USB identification is needed.	—
	5. If USB connector is MicroAB or MicroB, USBx_VBUS must not connect directly to the 5 V VBUS voltage of connector; Instead, this pin must be isloated with an external 30 K 1% resistor.	—
	6. PCB trace length of the USB3.0 TX/RX signals should not exceed 6 inches in order for the eye diagram to meet compliance test requirement.	—

Table 10. FlexSPI recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Read strobe(DQS) pad should be floated or with a 10-18pF cap load to compensate SIO/SCK pins load for high speed running, if the memory device does not provide DQS.	There are three modes for the internal sample clock for FlexSPI read data: Dummy read strobe generated by FlexSPI controller and looped back

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Table 10. FlexSPI recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
		internally(FlexSPIn_MCR0[RXCLKSRC] = 0x0), can only reach 66Mhz operation frequency; Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad(FlexSPIn_MCR0[RXCLKSRC] = 0x1), can reach 133Mhz operation frequency. In this mode, this pin can be floated or put some cap loads on board level to compensate SIO/SCK pins load; Read strobe provided by memory device and input from DQS pad(FlexSPIn_MCR0[RXCLKSRC] = 0x3), can reach 133Mhz operation frequency.

Table 11. Oscillator/Crystal recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Connect a 24 MHz crystal and a 510K Ω resistor between 24M_XTALI and 24M_XTALO (balls G25 and G26).	This crystal should have ESR not greater than 60 Ω, and be rated for a drive level of at least 100 µW. Follow the manufacturer's recommendation for loading capacitance. Use short traces between the crystal and the processor, with a ground plane under the crystal, load capacitors, and associated traces.
	2. Connect a 32.768 KHz crystal and a 4.7M Ω feedback resistor (must install) between RTC_XTALI and RTC_XTALO (balls J25 and J26). Alternatively, an external 32.768 KHz clock can be fed into RTC_XTALI to provide the RTC clock for the i.MX 8M Plus. See item #3.	This crystal should have ESR not greater than 70 kΩ, and be rated for a drive level of at least 0.5 µW. Follow the manufacturer's recommendation for loading capacitance. Use short traces between the crystal and the processor, with a ground plane under the crystal, load capacitors, and associated traces.
	3. If using external 32.768 KHz clock rather than a crystal to provide the RTC clock, it should be connected to RTC_XTALI pin. The RTC_XTALO pin should be connected to NVCC_SNVS_1P8 through a 100Kohm resistor.	The voltage level of this driving clock should not exceed the voltage of the NVCC_SNVS_1P8 rail, or damage/malfunction may occur. The RTC signal should not be driven if the NVCC_SNVS_1P8 supply is OFF. For RTC V_{IL} and V_{IH} voltage levels, see the latest i.MX 8M Plus data sheet available at www.nxp.com/i.MX8MPLUS.

Table 12. i.MX 8M Plus power/decoupling recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Comply with the power-up sequence guidelines as described in the data sheet to guarantee reliable operations of the device.	Any deviation from these sequences may result in the following situations:

Table continues on the next page...

Table 12. i.MX 8M Plus power/decoupling recommendations (continued)

Check box	Recommendations	Explanation/Supplemental recommendations
		• Excessive current during power-up phase • Prevention of the device from booting • Irreversible damage to the processor (worst case)
	2. Maximum ripple voltage requirements	Common requirement for ripple noise peak-to-peak value should be less than 5% of the supply voltage nominal value.
	3. If using PCA9450CHN PMIC to provide power, make sure all the regulators have output L/C components properly connected, even if unused.	Leaving any regulator output open will lead to malfunction of the whole PMIC.
	4. Check PMIC switcher output currents and the switcher inductor current ratings are sufficient for the Maximum supply currents ratings per rail as specified within the data sheet.	When using an non-NXP PMIC, or scaling down a power rail, insure the PMIC and inductor will meet the maximum current demands of the system. Note: Currents will be higher at hotter SoC temperatures than at room temperature.
	5. Suggest using 3.3 V for NVCC_ECSPI_HDMI rather than 1.8 V.	It is easier to find 3.3 V to 5 V dedicated HDMI DDC level shifter on the market, like NXP PCA9507. No much choice for 1.8 V to 5 V dedicated HDMI DDC level shifter.

Table 13. Decoupling capacitors recommendations (i.MX 8M Plus)

Checkbox	Supply	0.22 μF	1 μF	4.7 μF	10 μF	Notes
	VDD_SOC, VDD_ARM_PLL_0P8, VDD_DRAM_PLL_0P8, VDD_HDMI_0P8, VDD_SAI_PLL_0P8 VDD_ANA1_0P8, VDD_MIPI_0P8, VDD_PCI_0P8, VDD_USB_0P8	—	16	—	4	These 9 power rails are combined on EVK
	NVCC_DRAM	—	7	—	2	—
	VDD_ARM	—	8	—	2	—
	VDD_SNVS_0P8_CAP	—	1	—	—	—
	NVCC_SNVS_1P8	—	1	—	—	—

Table continues on the next page...

Table 13. Decoupling capacitors recommendations (i.MX 8M Plus) (continued)

Checkbox	Supply	0.22 µF	1 µF	4.7 µF	10 µF	Notes
	VDD_24M_XTAL_1P8, VDD_EARC_1P8, VDD_ANA1_1P8, VDD_ANA2_1P8, VDD_ARM_PLL_1P8, VDD_AVPLL_1P8, VDD_DRAM_PLL_1P8, VDD_ANA0_1P8, VDD_HDMI_1P8, VDD_LVDS_1P8, VDD_MIPI_1P8, VDD_PCI_1P8, VDD_SAI_PLL_1P8, VDD_USB_1P8	—	9	—	1	These 14 power rails are combined on EVK
	NVCC_JTAG, NVCC_NAND, NVCC_SAI1_SAI5, NVCC_SAI2_SAI3_SPDIF, NVCC_GPIO, NVCC_I2C_UART, NVCC_ECSPI_HDMI, NVCC_ENET, NVCC_SD1, NVCC_CLK, PVCC_1P8	—	9	—	1	These 11 power rails are combined on EVK
	NVCC_SD2	1	—	—	—	—
	VDD_USB_3P3	1	—	—	—	—
	VDD_MIPI_1P2_CAP	—	—	1	—	—
	Capacitor part number used on EVK: • 0.22 µF --- LMK063BJ224MP-F • 1 µF --- 02016D105MAT2A • 4.7 µF --- C1005X5R0J475M050BC					

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Table 13. Decoupling capacitors recommendations (i.MX 8M Plus) (continued)

Checkbox	Supply	0.22 µF	1 µF	4.7 µF	10 µF	Notes
	• 10 µF --- CL05A106MQ5NUNC					

Table 14. PCB design recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. High-speed signal traces have reference plane in adjacent layer and are impedance-controlled.	Controlled impedance is the key factor to have good signal integrity. Note that the reference plane can only be GND or the signal's own I/O power. Do not use other nets as reference.
	2. High-speed signal traces never cross gap or slot in reference plane.	Crossing gap in reference plane will cause reflection and increase crosstalk.
	3. Place at least one GND stitching via within 50 mils of signal via when switching reference planes.	GND stitching via can help keep impedance continuous and reduce via crosstalk.
	4. Appropriate delay matching is done for parallel bus.	Signals within a bus should have delay time matched to maintain timing margin.
	5. The true and complementary signal of a differential pair must have delay matched to within 1ps.	The true and complementary signal within a differential pair should have delay time tightly matched.
	6. DDR interface passed SI simulation. Alternatively, directly copy the EVK DDR layout design.	Generally, SI simulation should be performed for DDR interface that runs at 4000 MT/s to ensure stable working. If this is not feasible, just copy the EVK DDR layout design as well as the board stack-up and materials.
	7. Place test point on key signals to ease debugging. When placing test point on high-speed signal traces, make sure its diameter is no more than 20mil and the test point be directly placed on the trace with no stub.	Test points can bring excessive capacitance and should be carefully handled on high-speed signal traces.
	8. Decoupling capacitors are placed as close to IC power pins as possible.	This is to reduce the inductance from decoupling capacitor to IC power pin, to improve decoupling effectiveness.

2.2 JTAG signal termination

Table 15 is a JTAG termination chart showing what terminations should be placed on PCB designs.

Table 15. Recommended JTAG board terminations

JTAG signal	I/O type	External termination	Comments
JTAG_TCK	Input	None	Internal pulled up to NVCC_JTAG, no external termination required

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Table 15. Recommended JTAG board terminations (continued)

JTAG signal	I/O type	External termination	Comments
JTAG_TMS	Input	None	Internal pulled up to NVCC_JTAG, no external termination required
JTAG_TDI	Input	None	Internal pulled up to NVCC_JTAG, no external termination required
JTAG_TDO	3-state output	None	—

2.3 Signal termination for Boundary-scan

Table 16 is a signal termination chart showing what terminations should be placed on board designs to support Boundary-scan.

Table 16. Recommended board terminations for Boundary-scan

Signal	I/O type	External termination	Comments
BOOT_MODE0	Input	Pull Up	BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD, POR_B must be at 111111 to enter Boundary-scan mode.
BOOT_MODE1	Input	Pull Up	
BOOT_MODE2	Input	Pull Up	
BOOT_MODE3	Input	Pull Up	
JTAG_MOD	Input	Pull Up	
POR_B	Input	Pull Up	
GPIO1_IO02 (WDOG_B)	Input	Pull Up	If using a PMIC other than PCA9450, external pull-up resistor (100 Kohm) is needed to support boundary-scan mode.

2.4 General recommendations

More than one software operating environment can run on the i.MX 8M Plus platforms concurrently. Peripherals on these SoCs are accessible to all software operating environments. Conflict occurs when more than one software operating environment reads or writes the state of the same peripheral. Therefore, software operating environments must be isolated from each other when accessing shared resources. For instance, if two operating environments read and write the same region of DRAM without coordinating their access, results are unpredictable. The same behavior is applicable for peripheral registers, especially for the IP modules which offer multiple logical channels. For example, GPIO, I2C, SPI, SAI, and DMA.

Therefore, any sharing of an IP module between Cortex-M and Cortex-A domains must be coordinated with the system software architecture because software operating environments must be isolated from each other when accessing shared resources in order to avoid safety/reliability issues.

Consider an example. Individual GPIO pins are aggregated into groups, each group is controlled by a single GPIO module. Each GPIO module is a distinct peripheral that must be protected from conflicting access by different software operating environments. For example, GPIO1 module be assigned as a shared peripheral for Linux on the Arm Cortex-A and RTOS on the Cortex-M. Cortex-A and Cortex-M should obtain a semaphore lock before access to any pin of GPIO1 module is allowed. If Cortex-A and Cortex-M attempt to access to GPIO1 module at the same time, which can result in lack of isolation leading to safety/reliability issues.

Another important note, resource allocation should assure any peripheral that has external signals pinned out and its IO resource can be synchronously controlled by Cortex-A or Cortex-M in the corresponding software operating environment.

Not allocating correctly can result in lack of isolation leading to safety/reliability issues that can only be overcome with complex software such as virtual drivers which indirectly, can affect the HW isolation of Software Domains and the peripheral performance. In this case, customer needs to implement customized software solutions like: RPMSG Client/server-style cooperative device drivers or Peripheral Exclusive Access using a Mutex solution implemented using SEMA42. Implementation on the i.MX 8M Plus is up to the customer’s Software Architecture.

Under those circumstances, the Peripheral Modules have to be allocated to Software Systems per module basis and not a per signal basis from board design phase.

Chapter 3
i.MX 8M Plus layout/routing recommendations

3.1 Introduction

This chapter describes how to assist design engineers with the layout of an i.MX 8M Plus-based system.

3.2 Basic design recommendations

When using the Allegro design tool, the schematic symbol & PCB footprint created by NXP is recommended. When not using the Allegro tool, use the Allegro footprint export feature (supported by many tools). If the export is not possible, create the footprint per the package dimensions outlined in the product data sheet.

Native Allegro layout and gerber files are available on www.nxp.com/imx8mplusevk.

3.2.1 Placing decoupling capacitors

Place small decoupling and larger bulk capacitors on the bottom side of the PCB.

The 0201 or 0402 decoupling and 0603 or larger bulk capacitors should be mounted as close as possible to the power vias. The distance should be less than 50 mils. Additional bulk capacitors can be placed near the edge of the BGA via array. Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure high-speed transient current required by the processor. See the i.MX 8M Plus EVK layouts for the recommended decoupling capacitor placement.

The following list describes how to choose correct decoupling scheme:

- Place the largest capacitance in the smallest package that budget and manufacturing can support.
- For high-speed bypassing, select the required capacitance with the smallest package (for example, 1.0 μF, or even 2.2 μF in a 0201 package size).
- Minimize trace length (inductance) to small caps.
- Series inductance cancels out capacitance.
- Tie caps to GND plane directly with a via.
- Place capacitors close to the power ball of the associated package from the schematic.
- A preferred BGA power decoupling design is available on the EVK board design available on www.nxp.com/imx8mplusevk. Customers should use the NXP design strategy for power and decoupling.

3.3 Stack-up and manufacturing recommendations

3.3.1 Stack-up recommendation (i.MX 8M Plus)

Due to the number of balls on the i.MX 8M Plus processor in the 15 mm x 15 mm package, a minimum 6-layer PCB stack-up is recommended. For the 6 layers on the PCB, at least 1 layer need to be dedicated to power on routing to meet the IR drop target of 2% for the i.MX 8M Plus CPU power rails.

The constraints for the trace width will depend on such factors as the board stack-up and associated dielectric and copper thickness, required impedance, and required current (for power traces). The stack-up also determines the constraints for routing and spacing. Consider the following requirements when designing the stack-up and selecting board material:

- Board stack-up is critical for high-speed signal quality.
- Preplanning impedance of critical traces is required.
- High-speed signals must have reference planes on adjacent layers.

- PCB material: the material used on EVK is TU768.

3.3.2 Manufacturing recommendation (i.MX 8M Plus)

Since the i.MX 8M Plus processor uses 0.5mm-pitch BGA package, the PCB technology must meet below requirement to fully fanout all the signals of the processor using PTH(plated through holes).

- Minimum trace width: 3.2mil
- Minimum trace to trace/pad spacing: 3.2mil
- Minimum via size: 8mil-diameter hole, 16mil-diameter pad
- Minimum via pad to pad spacing: 4mil

Figure 1 shows the reference routing of the i.MX 8M Plus, PTH is OK for the fanout, HDI is not needed.

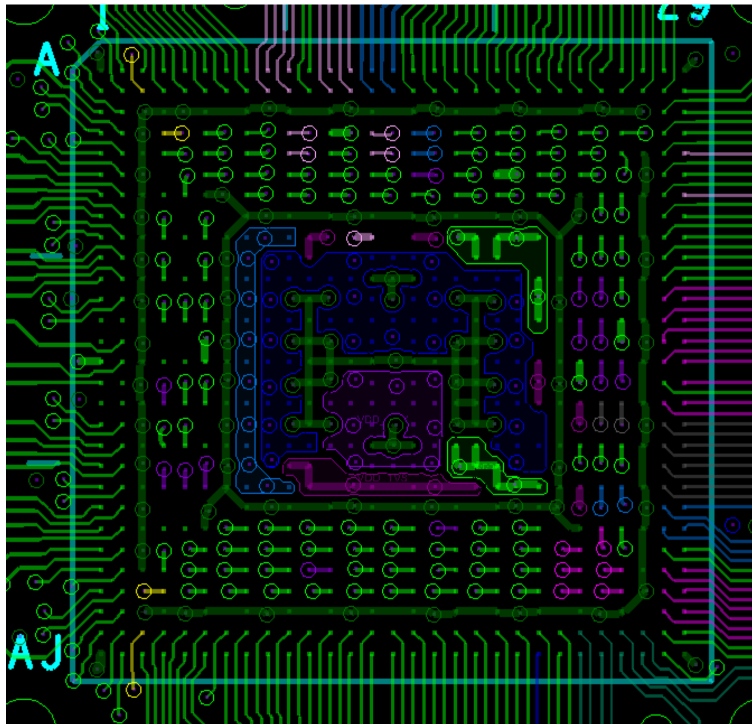

Figure 1. i.MX 8M Plus fanout routing on EVK

3.3.3 EVK PCB stack-up (i.MX 8M Plus)

Table 17 and Table 18 show stack-up of the EVK. CPU board uses 6-layer stack-up and the BB board uses 8-layer stack-up.

Table 17. 8MPLUSLPD4-CPU Board stack up information

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
1	Signal	0.33+Plating			1.15 mil
	Dielectric		1067 RC74%	3.49	2.5 mil
2	GND	1			

Table continues on the next page...

Table 17. 8MPLUSLPD4-CPU Board stack up information (continued)

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
	Dielectric		Core 0.075MM 1/1	3.97	2.95 mil
3	Signal	1			
	Dielectric		7628 RC49% 2116 RC54% 2116 RC54% 7628 RC49%	4.15 4.01 4.01 4.15	26.4 mil
4	Power	1			
	Dielectric		Core 0.075MM 1/1	3.97	2.95 mil
5	GND	1			
	Dielectric		1067 RC74%	3.49	2.5 mil
6	Signal	0.33+Plating			1.15 mil
Finished:	47.244(4.724/-4.724) mil			1.2(+0.12/-0.12) MM	
Designed:	45.5 mil			1.156 MM	
Material:	TU768				

Table 18. 8MPLUS-BB Board stack up information

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
1	Signal	0.5+Plating			1.31 mil
	Dielectric		1080 RC64%	3.75	2.96 mil
2	GND	1			
	Dielectric		Core 0.1MM 1/1	4.13	3.94 mil
3	Signal	1			
	Dielectric		7628 RC47% 2116 RC58%	4.2 3.91	12.88 mil
4	Power	1			
	Dielectric		Core 0.3MM 1/1	4.47	11.81 mil
5	Power	1			

Table continues on the next page...

Table 18. 8MPLUS-BB Board stack up information (continued)

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
	Dielectric		2116 RC58% 7628 RC47%	3.91 4.2	12.7 mil
6	Signal	1			
	Dielectric		Core 0.1MM 1/1	4.13	3.94 mil
7	GND	1			
	Dielectric		1080 RC64%	3.75	2.96 mil
8	Signal	0.5+Plating			1.31 mil
Finished:	62.992(+6.299/-6.299) mil			1.6(+0.16/-0.16) MM	
Designed:	61.01 mil			1.55 MM	
Material:	TU768				

3.4 DDR design recommendations

3.4.1 DDR connection information

The i.MX 8M Plus processor can be used with LPDDR4 or DDR4 memory. Since these memory types have different I/O signals, there are 38 generically-named functional balls, depending on the type of memory used. See Table 19 for the connectivity of these generic balls for LPDDR4 and DDR4. The schematic symbol created by NXP already replaced these generic names with DDR function.

Table 19. LPDDR4/DDR4 connectivity

Ball name	Ball #	LPDDR4 function	DDR4 function
DRAM_AC00	J6	CKE0_A	CKE0
DRAM_AC01	G5	CKE1_A	CKE1
DRAM_AC02	N6	CS0_A	CS0_n
DRAM_AC03	J4	CS1_A	C0
DRAM_AC04	M1	CK_t_A	BG0
DRAM_AC05	M2	CK_c_A	BG1
DRAM_AC06	G4	-	ACT_n
DRAM_AC07	J5	-	A9
DRAM_AC08	L6	CA0_A	A12

Table continues on the next page...

Table 19. LPDDR4/DDR4 connectivity (continued)

Ball name	Ball #	LPDDR4 function	DDR4 function
DRAM_AC09	L4	CA1_A	A11
DRAM_AC10	E4	CA2_A	A7
DRAM_AC11	D4	CA3_A	A8
DRAM_AC12	N4	CA4_A	A6
DRAM_AC13	N5	CA5_A	A5
DRAM_AC14	L5	-	A4
DRAM_AC15	R5	-	A3
DRAM_AC16	N1	-	CK_t_A
DRAM_AC17	N2	-	CK_c_A
DRAM_AC19	P2	MTEST	MTEST
DRAM_AC20	AA4	CKE0_B	CK_t_B
DRAM_AC21	AA5	CKE1_B	CK_c_B
DRAM_AC22	AA6	CS1_B	-
DRAM_AC23	U4	CS0_B	-
DRAM_AC24	V2	CK_t_B	A2
DRAM_AC25	V1	CK_c_B	A1
DRAM_AC26	P1	-	BA1
DRAM_AC27	R4	-	PARITY
DRAM_AC28	W4	CA0_B	A13
DRAM_AC29	W5	CA1_B	BA0
DRAM_AC30	AE4	CA2_B	A10 / AP
DRAM_AC31	AF4	CA3_B	A0
DRAM_AC32	U5	CA4_B	C2
DRAM_AC33	U6	CA5_B	CAS_n / A15
DRAM_AC34	U1	-	WE_n / A14

Table continues on the next page...

Table 19. LPDDR4/DDR4 connectivity (continued)

Ball name	Ball #	LPDDR4 function	DDR4 function
DRAM_AC35	U2	-	RAS_n / A16
DRAM_AC36	W6	-	ODT0
DRAM_AC37	AC4	-	ODT1
DRAM_AC38	AC5	-	CS1_n

3.4.2 LPDDR4-4000 design recommendations

The following list provides some generic guidelines that should be adhered to when implementing an i.MX 8M Plus design using LPDDR4.

1. It is expected that the layout engineer and design team already has experience and training with DDR designs at speeds of 2 GHz / 4000 MT/s.
2. Use only solid GND planes as reference planes for all the high-speed signal traces.
3. Keep edge to edge spacing of high-speed signal traces no less than 2 times the trace width to minimize trace crosstalk. Widen edge-to-edge spacing to 3x-4x where space is available in order to further minimize crosstalk.
4. At a speed of 4000 MT/s, signal vias can be a significant source of crosstalk. If not properly designed, it can introduce crosstalk larger than that from the trace. To minimize via crosstalk, make sure the total number of vias is no more than two on each point-to-point single-ended/differential trace. Place at least one ground stitching via within 50 mils of signal via when switching reference planes to provide continuous return path and reduce crosstalk. If it is not possible to place enough ground stitching vias due to space limitation, try to make the length that the signal actually travels on the via as short as possible, as illustrated in Figure 2. The i.MX 8M Plus is optimized to use layer 1 and layer 3 for all single-ended traces. The differential traces, CLK, DQS0,1,2,3 are often routed on the bottom layer. These require the stitching GND vias. The EVK reference design demonstrates this method.

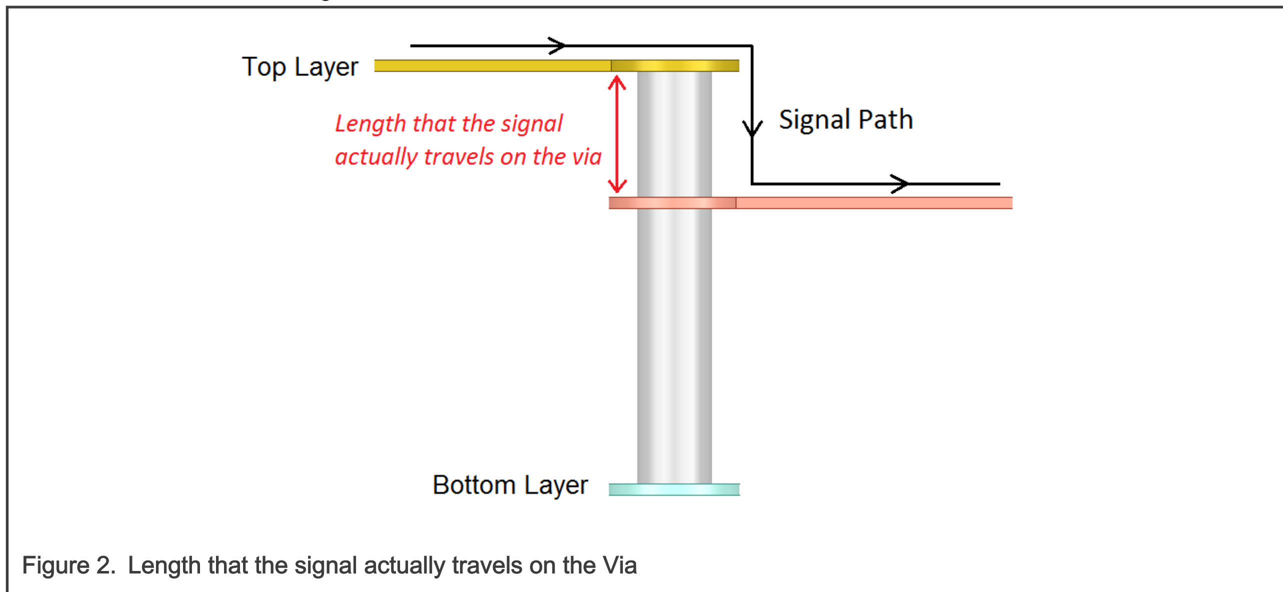

Figure 2. Length that the signal actually travels on the Via

5. CLK and DQS signal can be routed on different layer with DQ/CA signals to ease routing. When doing this, keep no less than 5 times trace width spacing from other signals.
6. Use time delay instead of length when performing the delay matching. The delay matching includes the PCB trace delay and the IC package delay. Incorporate the package pin delay into the CAD tool's constraint manager.

7. Include the delay of vias when performing delay matching. This can be realized in Allegro tool by enabling the **Z Axis Delay** in “Setup -> Constraints -> Modes”.
8. Byte swapping within each 16-bit channel is OK. Bit swapping within each slice/byte lane is OK.
9. Bit swapping of Command/Address (CA[5:0]) pins is **NOT** allowed.
10. i.MX 8M Plus does not drive ODT_CA signals. The ODT_CA balls on the LPDDR4 devices should be connected directly or through a resistor to the VDD2 supply.
11. In general, the 200-ball LPDDR4 package should be placed 200 mils from the i.MX 8M Plus.
12. Make sure to enable the DBI (data bus inversion) feature. This reduces power consumption and noise.

3.4.2.1 i.MX 8M Plus LPDDR4-4000 routing recommendations

LPDDR4-4000 needs to be routed with signal fly times matched shown in Table 20. The delay of the via transitions needs to be included in the overall calculation. This can be realized in Allegro tool by enabling the **Z Axis Delay** in “Setup - Constraints - Modes”.

An example of the delay match calculation has been shown for the i.MX 8M Plus EVK board design in Table 21 and Table 22. This analysis was done for the LPDDR4-4000 implementation using the i.MX 8M Plus. In Table 21 and Table 22, the **PCB Delay** column is obtained directly from the Allegro PCB file, and the **Pkg Delay** column is the package delay obtained from i.MX 8M Plus DDR package delay.

NXP strongly recommends that users simulate their LPDDR4 implementation before fabricating PCBs.

Table 20. i.MX 8M Plus LPDDR4-4000 routing recommendations

LPDDR4-4000				
LPDDR4 signal (each 16-bit channel)	Group	PCB + package prop delay		
		Min	Max	Considerations
CK_t/CK_c	Clock	Short as possible	200 ps	Match the true/complement signals within 1 ps.
CA5, CA4	Address/ Command/ Control	CK_t - 50 ps	CK_t + 50 ps	Match CA5, CA4 within 2 ps
CA3, CA2, CA1, CA0				Match CA3, CA2, CA1, CA0 within 2 ps
CKE1, CKE0, CS1, CS0				Match CKE1, CKE0, CS1, CS0 within 2 ps
DQS0_t/DQS0_c	Byte 0 - DQS	CK_t - 75 ps	CK_t + 75 ps	Match the true/complement signals of DQS within 1 ps.
DM0	Byte 0 - Data	DQS0_t -50 ps	DQS0_t +50 ps	
DQ[7:0]				
DQS1_t/DQS1_c	Byte 1 - DQS	CK_t - 75 ps	CK_t + 75 ps	
DM1	Byte 1 - Data	DQS1_t -50 ps	DQS1_t +50 ps	
DQ[15:8]				

Table 21. LPDDR4 delay matching example (CA/CTL signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
DRAM_CK_T_A	106.7	38.0	Vias are L1-> L6->L1
	144.7		Total Net Delay
DRAM_CK_C_A	107.5	37.8	Vias are L1-> L6->L1
	145.3		Total Net Delay
DRAM_CA0_A	153.5	40.8	Vias are L1-> L3->L1
	194.3		Total Net Delay
DRAM_CA1_A	160.3	33.5	Vias are L1-> L3->L1
	193.8		Total Net Delay
DRAM_CA2_A	132.6	61.7	Vias are L1-> L3->L1
	194.3		Total Net Delay
DRAM_CA3_A	122.9	71.6	Vias are L1-> L3->L1
	194.5		Total Net Delay
DRAM_CA4_A	145.3	28.3	Vias are L1-> L3->L1
	173.6		Total Net Delay
DRAM_CA5_A	125.9	47.4	Vias are L1-> L3->L1
	173.3		Total Net Delay
DRAM_nCS0_A	119.8	24.5	Vias are L1-> L3->L1
	144.3		Total Net Delay
DRAM_nCS1_A	96.2	48.9	Vias are L1-> L3->L1
	145.1		Total Net Delay
DRAM_CKE0_A	105.3	39.8	Vias are L1-> L3->L1
	145.1		Total Net Delay
DRAM_CKE1_A	102.8	43.1	Vias are L1-> L3->L1
	145.9		Total Net Delay

Table 22. LPDDR4 delay matching example (byte lane 1 signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
DRAM_SDQS1_T_A	85.1	39.5	Vias are L1-> L6->L1
	124.6		Total Net Delay
DRAM_SDQS1_C_A	85.1	40.3	Vias are L1-> L6->L1
	125.4		Total Net Delay
DRAM_DMI1_A	59.5	49.1	Routed on top layer, no via
	108.6		Total Net Delay
DRAM_DATA8_A	51.7	43.5	Routed on top layer, no via
	95.2		Total Net Delay
DRAM_DATA9_A	48.7	48.3	Routed on top layer, no via
	97.0		Total Net Delay
DRAM_DATA10_A	55.1	44.2	Routed on top layer, no via
	99.3		Total Net Delay
DRAM_DATA11_A	50.6	39.5	Routed on top layer, no via
	90.1		Total Net Delay
DRAM_DATA12_A	48.4	33.5	Routed on top layer, no via
	81.9		Total Net Delay
DRAM_DATA13_A	70.7	42.6	Routed on top layer, no via
	113.3		Total Net Delay
DRAM_DATA14_A	83.1	54.4	Routed on top layer, no via
	137.5		Total Net Delay
DRAM_DATA15_A	83.2	62.3	Routed on top layer, no via
	145.5		Total Net Delay

3.4.2.2 LPDDR4-4000 routing example (i.MX 8M Plus)

Figure 3 to Figure 5 show the placement and routing of the LPDDR4 signals on the i.MX 8M Plus EVK board. The CLK and DQS signals are routed on bottom layer to save routing space on top layer and layer 3. Chanel A data byte lane 1 and channel B data byte lane 0 signals are routed on top layer, and Chanel A data byte lane 0, channel B data byte lane 1 and CA/CTL signals are routed on layer 3. This is to minimize the distance the signal actually travels on the via to minimize via crosstalk.

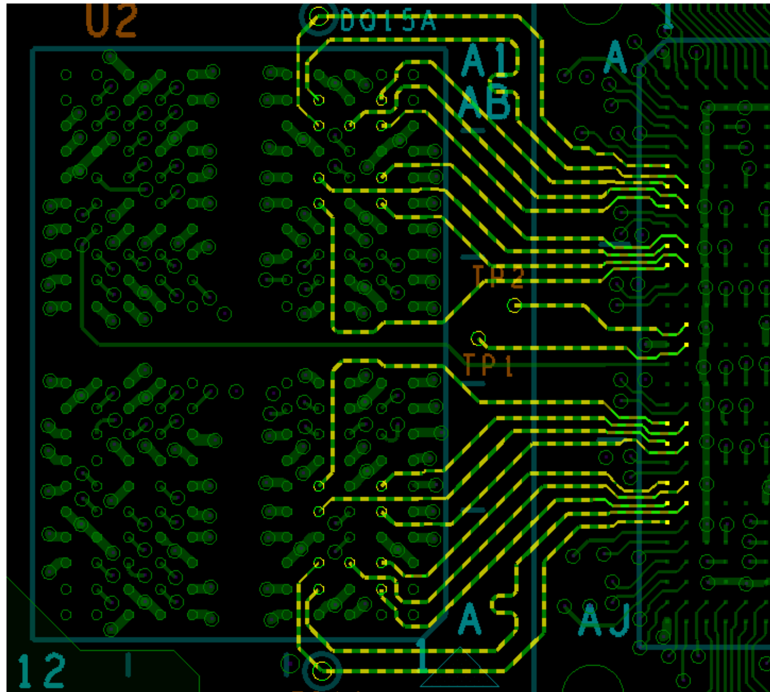

Figure 3. i.MX 8M Plus EVK board LPDDR4 routing (Top Layer)

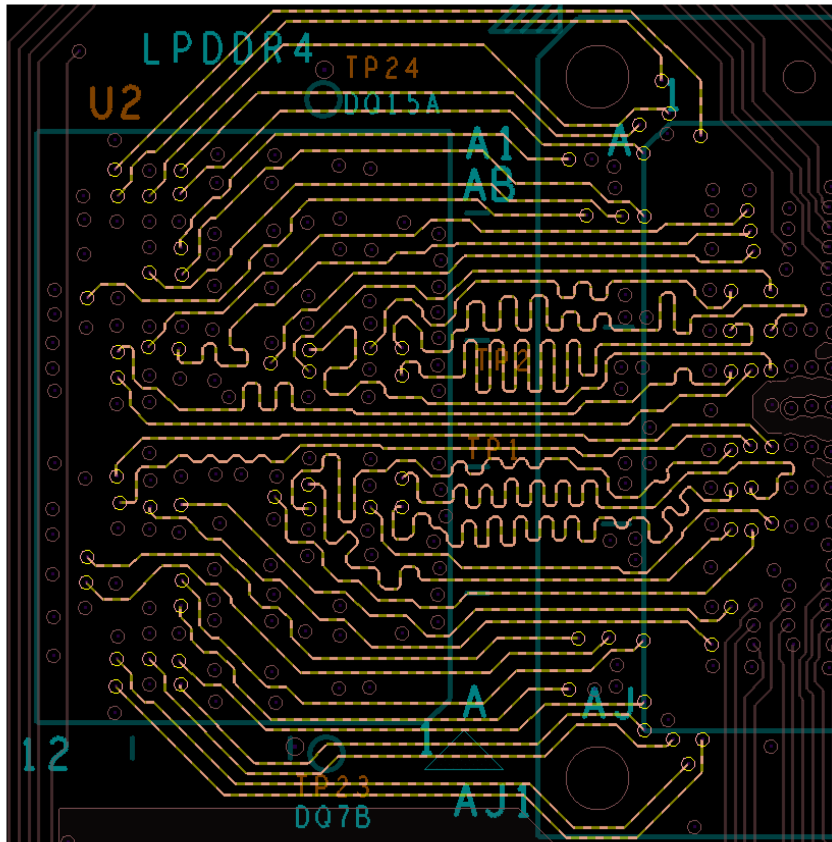

Figure 4. i.MX 8M Plus EVK board LPDDR4 routing (Layer 3)

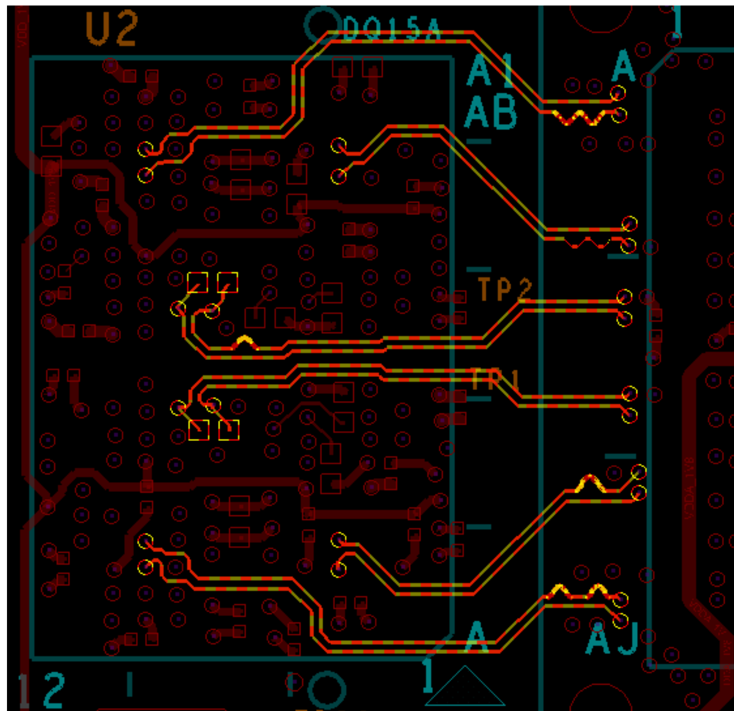

Figure 5. i.MX 8M Plus EVK board LPDDR4 routing (Bottom Layer)

3.4.3 i.MX 8M Plus DDR SI simulation guide

The simulation architecture includes the DDR controller (that is, the i.MX 8M Plus processor), the PCB and the DRAM device. The IBIS model for the i.MX 8M Plus processor is available from NXP. The DRAM device IBIS model must be obtained from the memory vendor.

This section describes how to check SI performance of the layout for a DDR design using the i.MX 8M Plus.

- Firstly, perform S-parameter extraction:
- It requires a 2.5D full-wave extraction tool, such as PowerSI from Cadence.
- Set the extraction bandwidth to 20 GHz.
- Port reference impedance: 50 Ω for signal ports, and 0.1 Ω for power ports.
- Coupled mode: Set the rise time to 20 ps and coupling coefficient to 1%.
- Secondly, perform time domain simulation:
- Stimulus pattern: 500-bit random code and different pattern for each signal within the same byte.
- Ideal power.
- Probe at the die.
- Simulation at slow corner (worst case).
- Eye waveform triggered by aligning with the timing reference (DQS/CLK).

When the simulation is done, find the simulated worst eye width and compare with following requirements to see if it can pass:

- For LPDDR4-4000
- DQ Write: Eye width @V_{REF} ±60mV should be over 187 ps.
- DQ Read: Eye width @V_{REF} ±70mV should be over 152 ps.

- Cmd/Addr/Ctrl: Eye width @V_{REF} ±72.5mV should be over 353 ps.

Figure 6 shows an example of simulated eye width of LPDDR4-4000 DQ write.

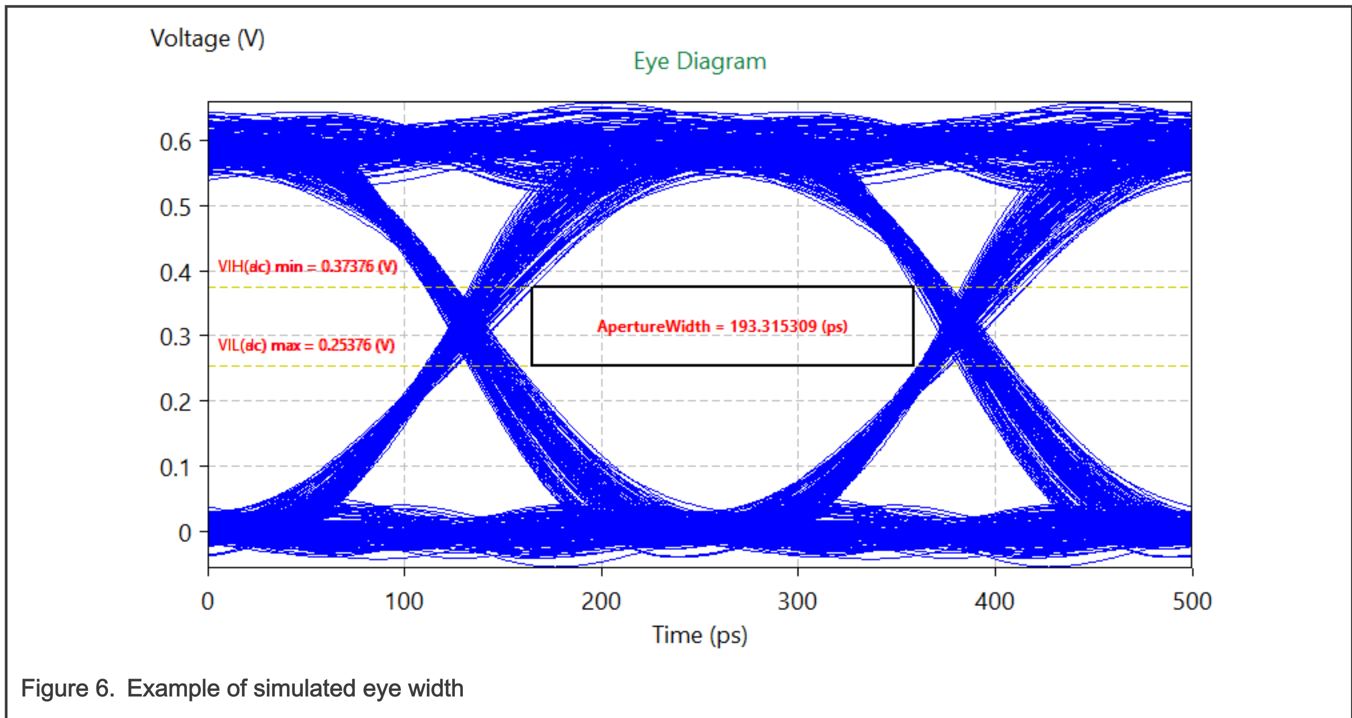

Figure 6. Example of simulated eye width

3.4.4 i.MX 8M Plus DDR package delay

When performing the required delay matching for LPDDR4/DDR4 routing, the substrate routing within the i.MX 8M Plus package need to be accounted for and included in the match calculation. Table 23 lists the propagation/fly time from the die I/O to the package ball.

Table 23. i.MX 8M Plus DDR package trace delays

Ball Name	Delay (ps)	Ball name	Delay (ps)
DRAM_AC00	39.8	DRAM_DM2	43.1
DRAM_AC01	43.1	DRAM_DM3	47.5
DRAM_AC02	24.5	DRAM_DQS0_N	50.9
DRAM_AC03	48.9	DRAM_DQS0_P	50.5
DRAM_AC04	38.0	DRAM_DQS1_N	40.3
DRAM_AC05	37.8	DRAM_DQS1_P	39.5
DRAM_AC06	54.1	DRAM_DQS2_N	38.4
DRAM_AC07	41.1	DRAM_DQS2_P	36.0
DRAM_AC08	40.8	DRAM_DQS3_N	48.8

Table continues on the next page...

Table 23. i.MX 8M Plus DDR package trace delays (continued)

Ball Name	Delay (ps)	Ball name	Delay (ps)
DRAM_AC09	33.5	DRAM_DQS3_P	48.2
DRAM_AC10	61.7	DRAM_DQ00	50.1
DRAM_AC11	71.6	DRAM_DQ01	56.5
DRAM_AC12	28.3	DRAM_DQ02	60.9
DRAM_AC13	47.4	DRAM_DQ03	47.9
DRAM_AC14	51.9	DRAM_DQ04	51.7
DRAM_AC15	35.9	DRAM_DQ05	56.2
DRAM_AC16	38.3	DRAM_DQ06	62.8
DRAM_AC17	38.3	DRAM_DQ07	62.4
DRAM_AC19	44.8	DRAM_DQ08	43.5
DRAM_AC20	44.2	DRAM_DQ09	48.3
DRAM_AC21	44.5	DRAM_DQ10	44.2
DRAM_AC22	62.3	DRAM_DQ11	39.5
DRAM_AC23	22.6	DRAM_DQ12	33.5
DRAM_AC24	33.5	DRAM_DQ13	42.6
DRAM_AC25	35.3	DRAM_DQ14	54.4
DRAM_AC26	53.7	DRAM_DQ15	62.3
DRAM_AC27	31.0	DRAM_DQ16	49.8
DRAM_AC28	27.4	DRAM_DQ17	50.9
DRAM_AC29	32.5	DRAM_DQ18	46.9
DRAM_AC30	55.3	DRAM_DQ19	43.2
DRAM_AC31	51.7	DRAM_DQ20	54.5
DRAM_AC32	25.0	DRAM_DQ21	54.2
DRAM_AC33	29.1	DRAM_DQ22	48.6
DRAM_AC34	41.7	DRAM_DQ23	44.5

Table continues on the next page...

Table 23. i.MX 8M Plus DDR package trace delays (continued)

Ball Name	Delay (ps)	Ball name	Delay (ps)
DRAM_AC35	45.1	DRAM_DQ24	58.6
DRAM_AC36	17.6	DRAM_DQ25	58.2
DRAM_AC37	42.1	DRAM_DQ26	45.6
DRAM_AC38	40.3	DRAM_DQ27	44.8
DRAM_ALERT_N	32.0	DRAM_DQ28	49.2
DRAM_RESET_N	32.4	DRAM_DQ29	54.7
DRAM_DM0	57.3	DRAM_DQ30	45.0
DRAM_DM1	49.1	DRAM_DQ31	53.8

3.4.5 JEDEC specification compliance

The i.MX 8M Plus processors are designed and tested to work with the JEDEC JESD209-4A–compliant LPDDR4 and JEDEC JESD79-3F-compliant DDR3L memories. Timing diagrams and tolerances required to work with these memories are specified in the respective documents and are not reprinted here.

Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. In this document, NXP cannot cover all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part variation. The PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, VIA placement, GND and supply planes layout, and DDR controller/PHY register settings all are factors affecting the performance of the memory system. Nevertheless, this hardware user's guide contains a large amount of valuable design information that NXP believes aid the design engineers in developing a DRAM memory system compliant with the JEDEC standards. NXP has validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors, and DDR trace routing between the processor and the selected DDR memory.

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as a closure to a customer-reported DDR issue. Customers bear the responsibility of properly designing the printed circuit board, correctly simulating and modeling the designed DDR system, and validating the system under all expected operating conditions (temperatures, voltages) before releasing their product to the market.

3.4.6 High-speed routing recommendations

For more information about general high-speed routing considerations, see High-Frequency Design Considerations (document AN12298)

3.4.7 Disclaimers

Nothing in this document relieves the design engineer/customer from ultimate responsibility in producing a proper functioning DRAM subsystem that meets JEDEC specifications.

It is expected that the design engineer already has a strong understanding of PCB design using high-speed components. This is not an all-encompassing training document that can be used by beginning designers to produce reliable PCB designs using modern processors.

Design engineers should use all available design guidelines provided by the manufacturers of other high-speed components used in the system. Should a conflict arise between this document and the guidelines from other manufactures, contact NXP for resolution (community.nxp.com).

NXP strongly recommends that one of the example layouts provided for the i.MX8 designs be copied exactly for the placement of the processor, DRAM device, decoupling capacitors underneath the processor, and the interconnecting traces/vias between these parts. This includes the board stack-up design and PCB dielectric materials chosen. These designs have been tested and validated at NXP and they are proven reliable. While NXP does not expect every customer to copy our designs, customers must expect that the amount of support that can be provided for assisting a new design cannot be as great as the support provided for designs already known to NXP.

NXP provides the processor IBIS models and timing models necessary for performing complete DRAM simulations of a design. NXP strongly recommends that the end users perform simulations of any new designs before the release of a PCB layout design for manufacturing.

Processor reference manuals and user's guides are continuously reviewed and revised to contain the most up-to-date information regarding the processor. In addition, erratas and engineering bulletins may be issued to document unintended processor behavior. The design engineers should consult the official NXP website for the latest versions of these documents as a part of the final checks of a PCB design before releasing the board to manufacturing.

When a fully assembled board is returned to the design engineer, it is the engineer's responsibility to perform a complete check of the board design to ensure that all subsystems are functioning correctly. See Thermal considerations for recommended board bring-up guidelines.

3.4.8 Reset architecture/routing

A reset button may be connected to PMIC_RST_B pin of the PMIC (PCA9450CHN) for development purposes. This allows all voltages to be put to their initial default power-on state when depressing the reset button.

Pressing the reset button causes the PMIC to trigger a cold reset event. This will cause all the power supplies except for the SNVS domain to be OFF. During this time, the POR_B driven by the PMIC will also keep asserted (low). This state will keep several hundred milliseconds to provide enough time for the power supplies to be completely powered down, and then the power supplies will start to ramp up again in defined sequence. When all the power supplies have reached their operating voltages, POR_B will be de-asserted, and the CPU may begin booting from reset.

NOTE

If the customer wants to pass test 1.1.4 and 1.1.5 of the MIPI-DSI compliance test on their board, he should ensure that the parasitic capacitance of each PCB trace of MIPI-DSI data signals to be no more than 10 pF. This is because the test requires connecting a 50 pF load board to the signal, and the capacitance load driving capability of the i.MX 8M Plus MIPI-DSI LP driver is 70 pF, also considering the i.MX 8M Plus chip itself can have up to 10 pF capacitance, so the final allowed maximum capacitance of the PCB trace will be 10 pF. For normal function, the customer only needs to ensure that the total capacitance load seen by the i.MX 8M Plus is no more than 60 pF.

3.5 Trace impedance recommendations

Table 24 is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/ trace widths.

Table 24. Trace impedance recommendations

Signal group	Impedance	PCB manufacturer tolerance (+/-)
All single-ended signals, unless specified	50 Ω Single-ended	10%
DDR DQS/CLK, PCIe TX/RX data pairs and reference clock	85 Ω Differential	10%

Table continues on the next page...

Table 24. Trace impedance recommendations (continued)

Signal group	Impedance	PCB manufacturer tolerance (+/-)
USB differential signals	90 Ω Differential	10%
Differential signals, including Ethernet, MIPI (CSI and DSI), HDMI, eARC, LVDS	100 Ω Differential	10%

3.6 Power connectivity/routing

Delivering clean, reliable power to the i.MX 8M Plus internal power rails is critical to a successful board design. The PCB PDN should be designed to accommodate the maximum output current from each voltage regulator into the i.MX 8M Plus supply balls. Table 25 lists the design goals for each high-current i.MX 8M Plus power rail.

Table 25. i.MX 8M Plus maximum current design levels

Supply input	i.MX 8M Plus Max current (mA)
VDD_ARM	2200
VDD_SOC	5000
NVCC_DRAM	1000

3.6.1 i.MX 8M Plus power distribution block diagram

There are companion PMICs that provide a low-cost and efficient solution for powering the i.MX 8M Plus processor, for example, NXP PCA9450CHN.

The PCA9450CHN features remote voltage sensing on BUCK1, BUCK2 and BUCK3, which means the output voltage sensing point can be on processor power pins to compensate for the IR drop of the power path from PMIC to processor. For more information on PMIC, see the following link: https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/power-manage-ic-pmic-for-i-mx-8m-mini-nano-plus:PCA9450. Note that this does not mean the IR drop of the power path can be arbitrarily large because resistance of the power path and capacitance of the decaps at processor power pins introduce phase lag and can lead to instability of the control loop. The 2% IR drop requirement should still be met.

To supply the 5A current of VDD_SOC, BUCK1 and BUCK3 are combined to operate in dual phase mode which can provide current up to 6A. In this mode, the R_SNSP3_CFG pin should be tied to GND.

The default output of BUCK6 is 1.1 V, which is for LPDDR4 NVCC_DRAM. You can modify the voltage to 1.2 V for DDR4 by programming PMIC in SPL code before the U-Boot or kernel image is loaded onto DDR. This function has been fully verified, so you can use the **ONE** PMIC part for all kinds of DDR memories.

Figure 7 shows a block diagram of the power tree of the NXP i.MX 8M Plus EVK board. It uses a single PCA9450CHN PMIC to power ON rails of the processor.

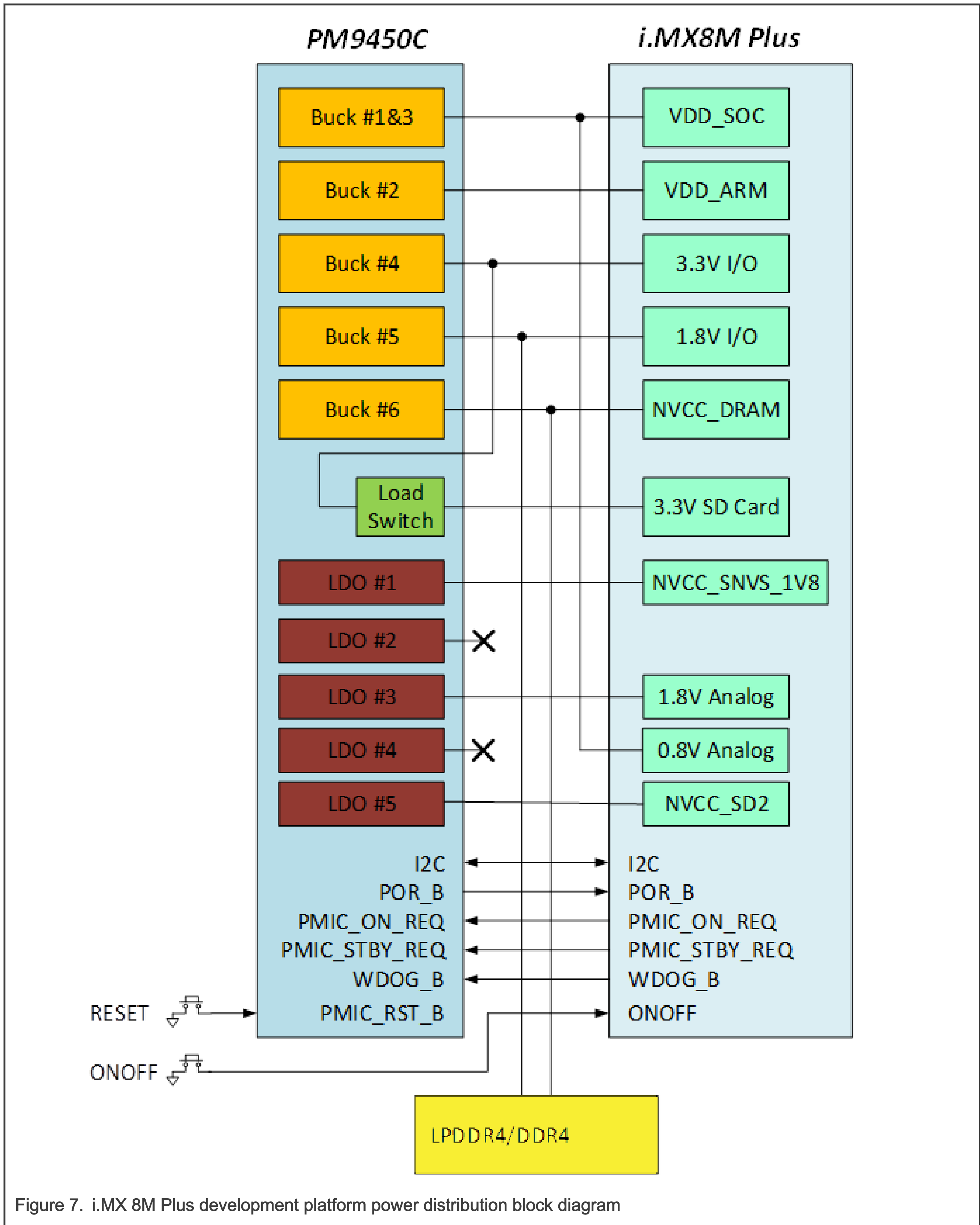

Figure 7. i.MX 8M Plus development platform power distribution block diagram

3.6.2 Power routing/distribution requirements

The designing for a good Power Delivery Network (PDN) is complicated. It includes:

1. Choose a good PCB stack-up (adequate Cu thicknesses, and layer assignments/utilization).
2. Optimize the placement and routing of the PDN. This includes good placement of the decoupling capacitors and connecting them to the power ground planes with as short and wide a trace as possible (as the increased inductance of a longer etch will degrade the effectivity of the capacitor). Use the number/placement of capacitors on the NXP development platforms.
3. Optimize DC IR drop. This involves using very wide traces/plane fills to route high-current power nets and ensure an adequate number of vias on power net layer transitions. Neck down of fill areas should be minimized and current density minimized. The maximum DC IR drop on a board should be 2% (preferably 1%) of the voltage rail (that is, on a 1.1V rail, the maximum voltage drop should be less than 0.022 V, preferably less than 0.011 V). See Table 26 for the DC IR drop requirement.
4. AC impedance check – the target impedance at different frequencies should be below specified values. See Table 27 for the impedance targets vs. frequency for specified power rail for the i.MX 8M Plus PCB design.

Table 26. i.MX 8M Plus DC IR drop requirements

Supply input	Nominal voltage (V)	Max current (mA)	IR drop target	Corresponding power path resistance requirement (mΩ)
VDD_ARM	0.85/0.95/1.0	2200	<2%	< 9.1
VDD_SOC	0.85/0.95	5000	<2%	< 3.8
NVCC_DRAM	1.1	1000	<2%	< 22

Table 27. i.MX 8M Plus PDN target impedance

Supply Input	< 20 MHz (mΩ)	20 - 100 MHz (mΩ)
VDD_ARM	20	90
VDD_SOC	8	38
NVCC_DRAM	15	68

3.7 USB connectivity

The i.MX 8M Plus provides two complete USB3.0 interfaces and the following configurations (or any subset) are supported:

- Dedicated host or device using Type-A connector or Type-B connector;
- Dual role using Type-C connector.

To implement a USB Type-C interface (UFP, DFP, or DRP), external hardware must be added to manage the two configuration channel IOs (CC1 and CC2) as well as monitor the plug orientation and switch the single USB3 SS interface.

See the NXP development platform schematic for an example USB Type-C implementation.

3.8 PCIE connectivity

The i.MX 8M Plus has one PCIE interface. There is a pair of pins with the name of PCIE _CLK_P/N. These pins are bi-directional which can either be used to feed 100 MHz reference clock to the PHY from external clock source, or to output an internal generated 100 MHz reference clock to PCIE connector or PCIE device.

On EVK, a PCIE clock generator chip (9FGV0241) is used to feed high-quality clock to both the PHY and connecter/device. If a PCIE clock generator is not available, use the internal clock of the chip. Note that the internal clock exhibits larger jitter than that from PCIE clock generator.

3.9 HDMI connectivity

The i.MX 8M Plus provides an HDMI transmitter capable of supporting an HDMI2.0 compatible output. Level shifters are required on HDMI_DDC_SCL, HDMI_DDC_SDA, HDMI_HPD, HDMI_CEC signals to shift the original 3.3V or 1.8V level to 5V required by HDMI interface.

3.10 Unused input/output terminations

3.10.1 i.MX 8M Plus unused input/output guidance

For the i.MX 8M Plus, the I/Os and power rails of an unused function can be terminated to reduce overall board power. Table 28 lists connectivity examples for unused functions except MIPI and USB. The use case for MIPI and USB is a little more complex so the connection recommendations for these two are listed in Table 29 and Table 30 respectively.

Table 28. i.MX 8M Plus unused function strapping recommendations

Function	Ball name	Recommendation if unused
LVDS	VDD_LVDS_1P8, LVDS1_CLK_P/N, LVDS1_Dx_P/N, LVDS2_CLK_P/N, LVDS2_Dx_P/N	Floating
PCIe	VDD_PCI_1P8, VDD_PCI_0P8, PCIE_TXN_P/N, PCIE_RXN_P/N, PCIE_REF_PAD_CLK_P/N, PCIE_RESREF	Floating
HDMI	VDD_HDMI_1P8, VDD_HDMI_0P8, HDMI_TXC_P/N, HDMI_TXx_P/N, HDMI_REXT	Floating
eARC	VDD_EARC_1P8	Tie to ground using a 10k resistor
	EARC_AUX, EARC_N_HPD, EARC_P_UTIL	Floating
Digital I/O supplies	NVCC_SAI2_SAI3_SPDIF, NVCC_ECSPI_HDMI, NVCC_ENET, NVCC_GPIO, NVCC_I2C_UART, NVCC_JTAG, NVCC_NAND, NVCC_SAI1_SAI5, NVCC_SD1, NVCC_SD2, NVCC_CLK	Floating if entire bank not used

Table 29. i.MX 8M Plus MIPI strapping recommendations

Use case	Ball name	Recommendation
All MIPI-CSI1 & MPI-CSI2 & MIPI-DSI used	VDD_MIPI_1P8, VDD_MIPI_0P8,	Supply
	VDD_MIPI_1P2_CAP/ MIPI_VREG1_CAP	Connect to outside cap
	MIPI_TEST_DNU	Floating
	MIPI_CSI1_CLK_P/N, MIPI_CSI1_Dx_P/N MIPI_CSI2_CLK_P/N, MIPI_CSI2_Dx_P/N	Function

Table continues on the next page...

Table 29. i.MX 8M Plus MIPI strapping recommendations (continued)

Use case	Ball name	Recommendation
	MIPI_DSI_CLK_P/N, MIPI_DSI_Dx_P/N	
Only MIPI-CSI1 & MPI-CSI2 used	VDD_MIPI_1P8, VDD_MIPI_0P8,	Supply
	MIPI_VREG1_CAP	Floating
	VDD_MIPI_1P2_CAP	Connect to outside cap
	MIPI_TEST_DNU	Floating
	MIPI_CSI1_CLK_P/N, MIPI_CSI1_Dx_P/N MIPI_CSI2_CLK_P/N, MIPI_CSI2_Dx_P/N	Function
	MIPI_DSI_CLK_P/N, MIPI_DSI_Dx_P/N	Floating
Only MIPI-CSI1 & MPI-DSI used	VDD_MIPI_1P8, VDD_MIPI_0P8,	Supply
	VDD_MIPI_1P2_CAP/ MIPI_VREG1_CAP	Connect to outside cap
	MIPI_TEST_DNU	Floating
	MIPI_CSI1_CLK_P/N, MIPI_CSI1_Dx_P/N	Function
	MIPI_CSI2_CLK_P/N, MIPI_CSI2_Dx_P/N	Tied to ground
	MIPI_DSI_CLK_P/N, MIPI_DSI_Dx_P/N	Function
Only MIPI-CSI2 & MPI-DSI used	VDD_MIPI_1P8, VDD_MIPI_0P8,	Supply
	VDD_MIPI_1P2_CAP/ MIPI_VREG1_CAP	Connect to outside cap
	MIPI_TEST_DNU	Floating
	MIPI_CSI1_CLK_P/N, MIPI_CSI1_Dx_P/N	Tied to ground
	MIPI_CSI2_CLK_P/N, MIPI_CSI2_Dx_P/N	Function
	MIPI_DSI_CLK_P/N, MIPI_DSI_Dx_P/N	Function
Only MIPI-DSI used	VDD_MIPI_1P8, VDD_MIPI_0P8,	Supply
	VDD_MIPI_1P2_CAP/ MIPI_VREG1_CAP	Connect to outside cap
	MIPI_TEST_DNU	Floating
	MIPI_CSI1_CLK_P/N, MIPI_CSI1_Dx_P/N	Tied to ground
	MIPI_CSI2_CLK_P/N, MIPI_CSI2_Dx_P/N	Tied to ground

Table continues on the next page...

Table 29. i.MX 8M Plus MIPI strapping recommendations (continued)

Use case	Ball name	Recommendation
All MIPI-CSI1/2 and DSI not used	VDD_MIPI_1P8, VDD_MIPI_0P8	Floating
	VDD_MIPI_1P2_CAP/ MIPI_VREG1_CAP	Floating
	MIPI_TEST_DNU	Floating
	MIPI_CSI1_CLK_P/N, MIPI_CSI1_Dx_P/N	Floating
	MIPI_CSI2_CLK_P/N, MIPI_CSI2_Dx_P/N	Floating
	MIPI_DSI_CLK_P/N, MIPI_DSI_Dx_P/N	Floating

Table 30. i.MX 8M Plus USB strapping recommendations

Use case	Ball name	Recommendation
Both USB1 & USB2 used	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Supply
	USB1_VBUS, USB1_D_P/N, USB1_TX_P/N, USB1_DNU, USB1_TXRTUNE, USB1_RX_P/N	Function
	USB2_VBUS, USB2_D_P/N, USB2_TX_P/N, USB2_DNU, USB2_TXRTUNE, USB2_RX_P/N	Function
Only USB1 used	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Supply
	USB1_VBUS, USB1_D_P/N, USB1_TX_P/N, USB1_DNU, USB1_TXRTUNE, USB1_RX_P/N	Function
	USB2_VBUS, USB2_D_P/N, USB2_TX_P/N, USB2_DNU, USB2_TXRTUNE, USB2_RX_P/N	Ground *RX_P/N, others floating
Only USB2 used	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Supply
	USB1_VBUS, USB1_D_P/N, USB1_TX_P/N, USB1_DNU, USB1_TXRTUNE, USB1_RX_P/N	Ground *RX_P/N, others floating
	USB2_VBUS, USB2_D_P/N, USB2_TX_P/N, USB2_DNU, USB2_TXRTUNE, USB2_RX_P/N	Function
Both USB1 and USB2 unused	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Floating
	USB1_VBUS, USB1_D_P/N, USB1_TX_P/N, USB1_DNU, USB1_TXRTUNE, USB1_RX_P/N	Ground *_RX_P/N, others floating
	USB2_VBUS, USB2_D_P/N, USB2_TX_P/N, USB2_DNU, USB2_TXRTUNE, USB2_RX_P/N	Ground *_RX_P/N, others floating

Chapter 4
Avoiding board bring-up problems

4.1 Introduction

This chapter describes how to avoid mistakes when bringing up a board for the first time. The recommendations below consist of basic techniques for detecting board issues and preventing/locating the three issues encountered: power, clocks, and reset.

4.2 Avoiding power pitfalls—current

Excessive current can damage the board. Use a current-limiting laboratory supply set to the expected main current draw (at most). Monitor the main supply current with an ammeter when powering up the board for the first time. You can use the supply's internal ammeter if there is. By monitoring the main supply current and controlling the current limit, any excessive current can be detected before permanent damage occurs.

Before the board test, you can ohm out the board power rails to the ground to verify that there are no short circuits. Then, you can power on the board and there will not be any damage to the board and/or components.

4.3 Avoiding power pitfalls—voltage

To avoid incorrect voltage rails, create a basic table called a voltage report prior to board bring up/testing. The table helps to validate that all the supplies are reaching the expected levels.

To create a voltage report, list the following:

- Board voltage sources
- Default power-up values for the board voltage sources
- Best location on the board to measure the voltage level of each supply

Determine the best measurement location for each power supply to avoid a large voltage drop (IR drop) on the board. The drop causes inaccurate voltage values. The following guidelines help produce the best voltage measurements:

- Measure closest to the load (in the case of the i.MX 8M Plus processor).
- Make two measurements: the first after initial board power-up and the second while running a heavy use-case that stresses the i.MX 8M Plus processor.

Ensure that the i.MX 8M Plus power supply meets the DC electrical specifications as listed in the chip-specific data sheet. See Table 31 for a sample voltage report table.

NOTE

This report table is for the i.MX 8M Plus EVK board. Sample voltage reports for customer PCBs will be different from this, depending on the Processor and Power Management IC (PMIC) used and the assignment of the PMIC power resources.

Table 31. Sample voltage report table

Source	Net name	Expected (V)	Measured (V)	Measure point	Comment
PCA9450CHN _BUCK2	VDD_ARM	0.85/0.95/1.0[1]	-	TP25	-
PCA9450CHN _BUCK1/3	VDD_SOC	0.85/0.95[2]	-	TP27	-

Table continues on the next page...

Table 31. Sample voltage report table (continued)

Source	Net name	Expected (V)	Measured (V)	Measure point	Comment
PCA9450CHN _LDO1	NVCC_SNVS_1V8	1.8	-	TP28	-
PCA9450CHN _LDO3	VDDA_1V8	1.8	-	TP30	-
PCA9450CHN _BUCK4	VDD_3V3	3.3	-	TP31	-
PCA9450CHN _BUCK5	VDD_1V8	1.8	-	TP33	-
PCA9450CHN _LDO5	NVCC_SD2	3.3/1.8	-	TP34	Can be either under SW control
PCA9450CHN _BUCK6	NVCC_DRAM_1V1	1.1/1.2[3]	-	TP35	-
MP8759GD	VSYS_5V	5.0	-	TP47	-
USB type-C connector	VBUS_IN	5.0	-	TP102	Main supply for board
Load switch from MP8759GD	VDD_5V	5.0	-	TP68	-
MP2147	VEXT_3V3	3.3	-	TP70	-
TPS70933DBVR	VLDO_3V3	3.3	-	TP23	-

1. The default output voltage of PCA9450CHN _BUCK2 is 0.85 V. The software will change it to 0.85 V for 1.2 GHz operation, 0.95 V for 1.6 GHz, 1.0 V for 1.8 GHz.
2. The default output voltage of PCA9450CHN _BUCK1/3 is 0.85 V. The software will change it to 0.95 V if DDR data rate is above 3200MT/s or overdrive is required for GPU/VPU
3. 1.1V for LPDDR4, 1.2V for DDR4, PCA9450CHN _BUCK6 default output voltage is 1.1 V. Software will change it to the required value in SPL before DDR initialization

4.4 Checking for clock pitfalls

Problems with the external clocks are another board bring-up issue. Ensure that all the clock sources are running as expected.

The XTALI_24M/XTALO_24M, and the RTC_XTALI/RTC_XTALO clocks are the main clock sources for 24 MHz and 32.768 kHz reference clocks. Although not required, the use of low jitter external oscillators to feed CLKIN_1/2 can be an advantage if low jitter or special frequency clock sources are required by modules driven by CLKIN_1/2. See the CCM chapter in the i.MX 8M Plus chip reference manual for details.

When checking crystal frequencies, using an active probe is recommended to avoid excessive loading. A passive probe might inhibit the 24 MHz oscillators from starting up. Use the following guidelines:

- RTC_XTALI/RTC_XTALO is running at 32.768 kHz.
- XTALI_24M/XTALO_24M is running at 24 MHz (used for the PLL reference).

4.5 Avoiding reset pitfalls

Follow these guidelines to ensure that you are booting correctly.

- During initial power-on while asserting the POR_B reset signal, ensure that 24 MHz and 32.768 kHz clock is active before releasing POR_B.
- Follow the recommended power-up sequence specified in the i.MX 8M Plus data sheet.
- Ensure the POR_B signal remains asserted (low) until all voltage rails associated with bootup are ON.

The BOOT_MODE[3:0] balls and internal fuses control boot. For a more detailed description about the boot modes, see the system boot chapter in the chip reference manual.

4.6 Sample board bring-up checklist

The checklist incorporates the recommendations described in the previous sections. Blank cells should be filled in during the bring-up.

Table 32. Board bring-up checklist

Checklist item	Details	Owner	Findings &Status
Note: The following items must be completed serially.			
1. Perform a visual inspection	Check major components to make sure nothing has been misplaced or rotated before powering ON.		
2. Verify all i.MX 8M Plus voltage rails	Confirm that the voltages match the data sheet's requirements. Be sure to check voltages as close to the i.MX 8M Plus as possible (like on a bypass capacitor). This reveals any IR drops on the board that could cause issues later. Ideally, all the i.MX 8M Plus voltage rails should be checked. See guidance below for important rails to check for the i.MX 8M Plus.		
	VDD_SNVS, NVCC_SNVS, VDD_SOC, VDD_ARM, NVCC_DRAM are particularly important voltages, and must fall within the parameters provided in the i.MX 8M Plus data sheet.		
3. Verify power-up sequence	Verify that power on reset (POR_B) is deserted (high) after all power rails have come up and are stable. See the i.MX 8M Plus data sheet for details about power-up sequencing.		
4. Measure/probe input clocks (32.768 kHz, 24 MHz, others)	Without proper clocks, the i.MX 8M Plus will not function correctly.		
5. Check JTAG connectivity	This is one of the most fundamental and basic access points to the i.MX 8M Plus to allow the debug and execution of low level code, and probe/access processor memory.		
Note: The following items may be worked on in parallel with other bring-up tasks.			

Table continues on the next page...

Table 32. Board bring-up checklist (continued)

<table>
<tr><th>Checklist item</th><th>Details</th><th>Owner</th><th>Findings &Status</th></tr>
<tr><td>Access internal RAM</td><td>Verify basic operation of the i.MX 8M Plus in system. The on-chip internal RAM starts at address 0x0090 0000 and is 128 Kbytes in density. Perform a basic test by performing a write-read-verify operation to the internal RAM. No software initialization is required to access internal RAM.</td><td></td><td></td></tr>
<tr><td>Verify CLKOUT1/2 outputs (measure and verify default clock frequencies for desired clock output options) if the board design supports the probing of clock output balls.</td><td>This ensures that the corresponding clock is working and that the PLLs are working. This step requires chip initialization, for example, via the JTAG debugger, to properly set up the IOMUX to output clocks to I/O balls and to set up the clock control module to output the desired clock. See the chip reference manual for more details.</td><td></td><td></td></tr>
<tr><td>Measure boot mode

frequencies. Set the boot configure switch for each boot mode and measure the following (depending on system availability):
NAND (probe CE to verify boot, measure RE frequency)
SPI-NOR (probe slave select and measure clock frequency)
MMC/SD (measure clock frequency)</td><td>This verifies the connectivity of signals between the i.MX 8M Plus and boot device and that the boot mode signals are properly set. See the “System Boot” chapter in the chip reference manual for details for boot mode configurations.</td><td></td><td></td></tr>
<tr><td>Run basic DDR initialization and test memory</td><td>Assuming the use of a JTAG debugger, run the DDR initialization and open a debugger memory window pointing to the DDR memory map starting address.
Try writing a few words and verify if they can be read correctly.
If not, recheck the DDR initialization sequence and whether the DDR has been correctly soldered onto the board. Users should recheck the schematic to ensure that the DDR memory has been connected to the i.MX 8M Plus correctly.</td><td></td><td></td></tr>
</table>

Chapter 5
Using BSDL for board-level testing

5.1 BSDL overview

The Boundary Scan Description Language (BSDL) is used for board-level testing after the components are assembled. The interface for this test uses the JTAG pins. The definition is contained within IEEE Std 1149.1.

5.2 How BSDL works

A BSDL file defines the internal scan chain, which is the serial linkage of the IO cells, within a particular device. The scan chain looks like a large shift register, which provides a means to read the logic level applied to a pin or to output a logic state on that pin. Using JTAG commands, the test tool uses the BSDL file to control the scan chain so that device-board connectivity can be tested.

For example, when using an external ROM test interface, the test tool does the following:

1. It outputs a specific set of addresses and controls to the pins connected to the ROM.
2. It performs a read command and scans out the values of the ROM data pins.
3. It compares the values read with the known golden values.

Based on this procedure, the tool determines whether the interface between the two parts is connected properly and does not contain shorts or opens.

5.3 Downloading the BSDL file

The BSDL file for each i.MX processor is stored at the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

5.4 Pin coverage of BSDL

Each pin is defined as a port within the BSDL file. You can open the file with a text editor (such as Wordpad) to review how each pin functions. The BSDL file defines these functions:

-- PORT DESCRIPTION TERMS

-- in = input only

-- out = three-state output (0, Z, 1)

-- buffer = two-state output (0, 1)

-- inout = bidirectional

-- linkage = OTHER (vdd, vss, analog)

The appearance of a “linkage” in a pin’s file means that the pin cannot be used with a boundary scan. These are usually power pins or analog pins that cannot be defined by a digital logic state.

5.5 Boundary scan operation

The boundary scan operation is controlled by:

- BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3 and JTAG_MOD pins.
- On-chip Fuse bits.

The JTAG_MOD pin state controls the selection of the JTAG to the core logic or boundary scan operation. See the following references for further information:

- The “System JTAG Controller (SJC)” chapter in the chip reference manual for the definitions of the JTAG interface operations.
- The “JTAG Security Modes” section in the same chapter for an explanation of the operation of the e-Fuse bit definitions in Table 33.
- The “Fusemap” chapter in the chip reference manual for the fusemap tables.

Table 33. System considerations for BSDL

Pin name	Logic state	Description
JTAG_MOD	1	IEEE 1149.1 JTAG compliant mode
BOOT_MODE[3:0]	Others [1:1:1:1]	Normal boot function Reserved for Boundary Scan
POR_B	1	Power On Reset for the device
e-Fuse bits		
JTAG_SMODE[1:0]	[0:0] [0:1]	JTAG enable mode Secure JTAG mode
SJC_DISABLE	0	Secure JTAG Controller is enabled

NOTE

When using the BSDL file to do boundary scan test on i.MX8M Plus:

1. COMPLIANCE_PATTERNS of IMX8MP: entity is "(BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD, POR_B) (111111)". On 8MPLUSLPD4 EVK, this is done by populating R313 and setting the SWITCH SW4 [1-4]: 1111.
2. When trying to toggle IO logic states using EXTEST instruction, make sure that PMIC_ON_REQ is set to driving high and PMIC_STBY_REQ is set to driving low before executing EXTEST instruction. These two pins control system power and may cause system reset or power down if their logic states are not set correctly.

5.6 I/O pin power considerations

The boundary scan operation uses each of the available device pins to drive or read values within a given system. Therefore, the power supply pin for each specific module must be powered for the IO buffers to operate. This is straightforward for the digital pins within the system.

NOTE

The BSDL was only tested at 1.8 V.

5.7 Testing DDR4 connectivity using boundary scan

DDR4 DRAM devices implement connectivity test mode which allows the memory controller to test connectivity with DRAM devices using boundary scan. In this mode, the DRAM device appears as an asynchronous logic device to the memory controller. When the memory controller applies a certain test pattern on test input pins, the connectivity test results are available for extraction in parallel at the test output pins after a fixed propagation delay time. Table 34 shows pin functionality of DDR4 DRAM device in connectivity test mode.

Table 34. Pin functionality of DDR4 DRAM device in connectivity test mode

Pin functionality in connectivity test mode	Pin names during normal memory operation
Test Enable	TEN
Chip select	CS_n
Test Input	BA0-1, BG0-1, A0-A9, A10/AP, A11, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, RESET_n, CKE, ACT_n, ODT, CLK_t, CLK_c, DML_n, DBIL_n, DMU_n/DBIU_n, Parity, Alert_n
Test output	DQ0-DQ15, DQSU_t, DQSU_c, DQSL_t, DQSL_c

To make the DRAM device enter connectivity test mode, TEN pin should be pulled HIGH, and RESET_n pin should also be held HIGH. However, in i.MX 8M Plus A0 silicon, the output of DRAM_RESET_N pin will be fixed LOW in boundary scan mode and cannot be controlled by the boundary scan logic. As a workaround, the external circuitry shown in Figure 8 can be added to control the logic state of RESET_n input using DRAM_ALERT_N signal in boundary scan mode. The i.MX 8M Plus DRAM_ALERT_N signal is connected to DRAM RESET_n pin through several logic gates instead of direct connection. For normal operation, JTAG_MOD=0 so we have RESET_n= DRAM_RESET_N. But when in boundary scan mode, JTAG_MOD=1 so we have RESET_n= DRAM_RESET_N+DRAM_ALERT_N. Since DRAM_RESET_N is fixed at 0 in boundary scan mode, the logic state of RESET_n gets controlled by DRAM_ALERT_N. It should be noted that the logic gates used in this circuitry must support 1.2V supply voltage and can tolerate 1.8V input because the logic level of JTAG_MOD is 1.8V while the other signals are 1.2V. For example, use NC7SV08 as the AND gate and NC7SV32 as the OR gate. The limitation of this workaround is that DRAM_ALERT_N must be kept HIGH during connectivity test since it controls the logic state of RESET_n, which might impact the connectivity test of DRAM_ALERT_N signal itself.

In i.MX 8M Plus A1 silicon, this issue is resolved by recovering full boundary scan functionality for DRAM_RESET_N. So, the workaround is no longer needed.

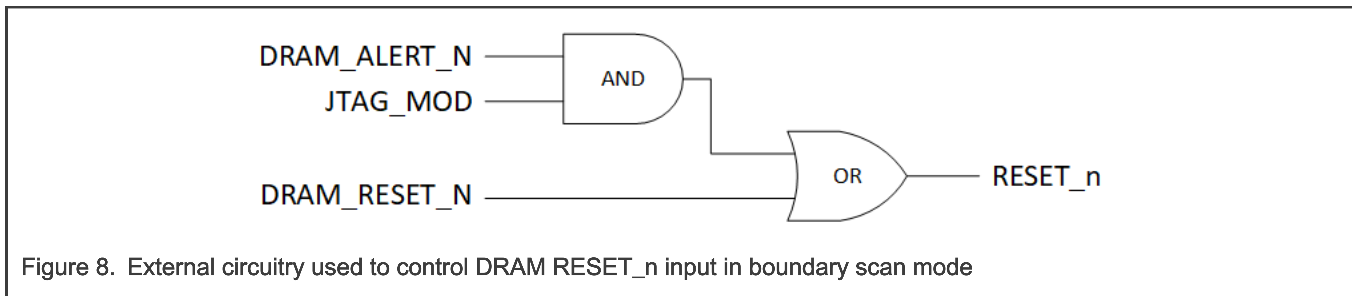

Figure 8. External circuitry used to control DRAM RESET_n input in boundary scan mode

Chapter 6
Thermal considerations

6.1 Introduction

This chapter introduces basic thermal considerations that need to be considered, when designing an i.MX 8M Plus processor-based system. PCBs should be designed with the thermal requirements factored in early as only remedial actions are possible after. Factoring thermal management at the end of the design cycle will increase the cost of the overall design and delay productization. This section provides a few key design considerations to improve the thermal management of the final i.MX 8M Plus processor-based system/product.

The Thermal Design Power (TDP), represents the maximum sustained power dissipated by the processor, across a set of realistic applications. The activity profile of the application can have a significant impact on the thermal management techniques used and on the TDP.

If the customer application requires high performance for extended periods and/or if the product is required to function in high ambient temperatures, the usage of passive thermal management techniques such as a heat sink becomes necessary. For very high ambient operating environments active thermal management techniques such a cooling fan or forced convection may also be required in addition to the heat sink.

For less demanding applications it may be feasible to consider the PCB as one of the primary heat dissipation media if good design practices are followed. In such cases, NXP recommends passive heat sinks as a minimum to be mounted to the lid of the processor using thermal paste or appropriate Thermal Interface Materials(TIM).

6.2 PCB dimensions

The dimensions of the PCB directly affect its capability to dissipate the heat. Typically, more than 80% of the heat generated by a high-power component is dissipated through the system board, when no other thermal solution is implemented. The bigger the board is, the larger the surface area through which heat can spread away from the source component and also can be transferred more efficiently into free space.

NXP conducted PCB sensitivity simulation showed that a 50% reduction in PCB x-y dimensions results in an increase of between 44-65% in package thermal resistance due to the loss in conductive volume to dissipate heat. System designers hence need to be careful when designing smaller form factor boards that have multiple high-power components.

6.3 Copper volume

Increasing the heat dissipation (reducing thermal resistance) can also be achieved by increasing the metallization in the system board. PCBs are made up of copper and dielectric material, with the copper being orders of magnitude more thermally conductive. Copper volume influences the heat capacity of the board. With higher copper volume the board can accept more heat, so a i.MX 8M Plus processor-based system can operate in high performance state (or near the max TDP) for longer time periods. The copper volume can be increased by increasing the dimensions of the board, by addition of ground layers or by increasing the thicknesses of the layers on which power and ground planes are located. Refer to Table 17 and Table 18 for stack-up of the EVK.

6.4 PCB material selection

As previously discussed PCB material selection is extremely important for systems with high speed routing. Thermal properties should also be considered in selecting PCB materials for multilayer designs in which the system is expected to endure excessive short-term thermal steps. Specific attention should be paid to the fact that thermal properties of dielectrics are often different in horizontal and vertical directions.

Material characteristics such as the Coefficient of Thermal Expansion (CTE) should be considered. The CTE describes how a material changes dimension with temperature. Ideally, a PCB material's CTE should be closely matched to copper, which is about 17 ppm°C. CTE is a concern because as the PCB expands during heating, it can elongate plated via holes and cause fracturing.

If the CTE is closely matched to copper, expansion of the PCB material and copper will be more uniform and the plated via holes will be more robust during thermal cycling.

6.5 Thermal resistance

Reducing the thermal resistance close to the die and package is mandatory for good thermal performance. The actual semiconductor die dimensions are relatively small compared to the size of a typical PCB, which results in a very high heat flux in the die, package and its immediate vicinity. Therefore, thermal resistance encountered early in the thermal path causes a large temperature gradient. The most effective place to focus resources to reduce thermal resistance is where the thermal gradient is the highest. To efficiently dissipate the heat through the board, thermal resistance between the SoC and the board needs to be minimized. This can be achieved by utilizing all the ground pads of the component and using board level underfill with good thermal conductivity properties.

6.5.1 Heat spreaders

Thermal resistance can be reduced when a heat spreader is mounted on the top of SoC package using a Thermal Interface Material (TIM) with good thermal conductivity properties (thermal paste). If the heat spreader is also thermally connected with the PCB, an alternative route for the heat is created, reducing the global thermal resistance. Spreading the heat at the beginning of the thermal path not only reduces the thermal resistance near the source component, but it also provides a broader area to further disseminate the heat.

The type of heat spreader to be used is dependent on the customers’ application available enclosure space and budget considerations. Graphite heat spreaders are quite common as they match the thermal performance of copper in two directions (x, y), at a lower weight and cost. The high in-plane (basal) thermal conductivity results in spreading and evening out of the hot spots Due its low cost the area that the graphite heat spreader covers, could be potentially larger covering all heat generating components on the system board.

6.5.2 Thermal vias

Using a continuous low thermal impedance path from the processor to ambient conditions is important and a low thermal resistance has to be maintained throughout the PCB. Any small break in the low impedance path is highly detrimental. System designers should provide redundant thermal paths where possible. This can be achieved by adding an appropriate amount of thermal vias to connect all the ground planes together and allow the heat to spread uniformly through other layers of the PCB. System designers should allocate enough plated through vias around the ground and power balls of the i.MX 8M Plus processor and other heat generating components.

6.6 Power net design

Modern power electronics devices can have very low on-resistances. It’s quite possible that the PCB traces and connector pins that feed current to these devices contribute more ohmic losses to the system than the power transistors do. Such heating may be avoidable if traces are up-sized. Reducing trace ohmic losses may be the least expensive way to reduce the design's total power dissipation. Trace width calculators, which also predict trace temperature rise, are readily available on the internet. Using over-sized power transistors is a way to cut total power and subsequent heat dissipation.

6.7 Component placement

The i.MX 8M Plus processor should always be placed away from edges in the center of the PCB so that heat can effectively spread in all directions. Placing the device on the edge or even on the corner of the PCB significantly reduces heat transfer from the device and dissipation capabilities of the to the PCB, as the heat cannot efficiently spread in the directions where the edges are present. This eventually results in local hot spots and rapid heating of the source component.

In addition, the processor should be mounted on the top side of the PCB, away from the chassis side walls unless the side walls are being used as thermal solution path for the package. System designers should place heat generating components as far apart as possible to reduce thermal coupling effects. The thermal gradient is high near a power dissipating device, so even small amounts of separation help reduce thermal coupling.

A NXP conducted PCB sensitivity simulation showed that a non-centered bare i.MX 8M Plus FCBGA package on the PCB will cause approximately 8-10% increase in junction temperature due to uneven heat propagation. This study highlights the need for centered component placement.

6.8 PCB surroundings

The surroundings of the PCB also influence the efficiency of heat transfer from the board into free space (air). There should be enough clearance from the top and bottom sides of the PCB. If narrow gaps are created, air flow is significantly limited, resulting in accumulation of hot air in the gap. The board cannot therefore effectively transfer heat in such areas. Also, the casing should be designed in a way that natural air convection could be utilized to improve heat transfer.

If a narrow gap at the bottom side cannot be avoided (quite common for System on Modules - SOMs), it should be considered to fill the gap under the i.MX 8M Plus processor by thermally conductive gap filler. To further improve heat transfer, exposed copper pads should be added to the base board at the mounting spot of the filler.

6.8.1 Air flow considerations

Heat convection is more efficient for a vertically mounted board. Remember that components above heat producing devices run hotter than those below. If the board is to be horizontally mounted, place heat generating components on the PCB's topside, if possible. A thermal plume (the chimney effect) forms more readily on a board's topside and it helps disperse heat.

- Consider the system level air flow and air mover placement in the enclosure
- Avoid sub-optimal component placement that might hinder airflow or natural convection
- Avoid placing tall or bulky devices in the air flow path
- Avoid routing circuitry in an area where mounting holes would need to go
- Plan to make space for the thermal management solution early in the system design phase and consider the complete board and packaging form factor (enclosure)

6.9 Heat sink considerations

The most frequently employed passive cooling device is the heat sink. It is a mass of thermally conductive metal which is physically mounted to a heat generating component. Adding a heat sink to the processor is an excellent method to dissipate heat. Commonly used heat sink materials are copper and aluminum.

- Copper has better thermal conductivity but is more expensive and difficult to process. It is heavier (lots of copper radiators exceed the CPU weight limit), it has small heat capacity and easily oxidizes.
- For most applications, an aluminum alloy heat sink is sufficient.

There are various parameters that affect not only the heat sink performance itself, but also the overall performance of the system. Choosing the correct type of heat sink depends largely on the thermal budget allowed for the heat sink and external conditions surrounding the heat sink.

A few design considerations when planning to add a heat sink in your design are listed below:

- Ensure adequate spacing around the device to accommodate the heat sink.
- Avoid routing circuitry in the area where mounting holes will be placed
  - — Space is needed for anchoring the heat sink such as, spring loaded screws, a clip or push pins
- Consider also the bottom side of the PCB where space for reinforcing support or securing mechanisms may be required.
  - — A backing plate may be necessary on the back side of the printed circuit board opposite the flip-chip device to prevent board warpage
- Consider temperature limits beneath the heat sink and ensure that temperature sensitive components are not placed there to prevent overheating and damage
- Ensure the orientation and spacing of the fins cause the heat to move as quickly as possible from the heat source (refer to Air Flow Considerations)

— Improper orientation can inhibit the thermal performance of the heat sink

For more details on heat sink handling, refer to AN4871.

6.10 Thermal simulations

As illustrated in this section, thermal management is a very complex discipline with numerous variables that need to be considered. In order to determine whether the system is capable of stable operation (no thermal runaways) in the given use case or to identify potentially overlooked issues, thermal simulations have to be performed.

NXP can provide FloTHERM FloTHERM® or Icepak® simulation models for i.MX 8M Plus processor series processor family and strongly encourages customers to perform thermal simulations using these models in their form factor designs and specific use cases to get a holistic system thermal design & identify possible thermal bottlenecks. Thermal simulations become increasingly important in small form factor designs and operation in high ambient temperatures.

6.11 Software optimizations

Software based power and thermal management techniques can be very effective in reducing the need for more elaborate active or passive thermal management solutions and add little or no additional cost to the system design. Attention should be paid to the required system performance and power requirements, as lower the i.MX 8M Plus processor power consumption lower the heat generated by the processor.

The i.MX 8M Plus incorporates several low-power design techniques, to meet requirements of low-power design, while sustaining high performance operation. The activity profile of the customer application can have a significant impact on the thermal management techniques used and on the TDP. Carefully defining the system's worst case operating conditions can be an effective way to reduce power and thermal dissipation.

- System designers should utilize and enable all software power management techniques available for the i.MX 8M Plus
- The SoC voltages and core frequencies of modules should be kept at the minimum specified levels and scaled dynamically with respect to the current performance demands of the application where possible
- The processor should enter low power modes under certain use cases whenever possible
- All unused power rails should be turned off from the PMIC and power gate unused domains if possible
- All unused module clocks should be turned off (Dynamically handled by NXP Linux BSP)
- Customers are encouraged to use the latest Linux BSP GA release available on nxp.com, that leverages the i.MX 8M Plus processor power management features and incorporates various Linux software power management techniques

For more details on the power consumption, refer to AN13054.

6.12 The Thermal checklist

NXP recommends using the checklist below as a high-level guide for designing an optimal thermal management solution for your end product:

Item	Activity	Check
1	Determine the TDP (Thermal Design Power)	
2	Determine the Activity Profile (use case dependent)	
3	Determine the product form factor constraints (orientation, x, y & z limits etc.)	
4	Determine the environmental operating conditions (ambient temperature, airflow regime - Forced or Natural Convection)	

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Item	Activity	Check
5	Determine the Tj for the i.MX 8M Plus device to use (Industrial, consumer etc.)	
6	Factor in board design considerations early (PCB layers, metallization, layout, component placement)	
7	Run thermal simulations to determine the best thermal management approach using form factor design and use cases	
8	Investigate adding heat spreading techniques, heat sinks to alleviate thermal bottlenecks	
9	Enable all software power management techniques which can minimize power consumption (less power, less heat)	
10	Consider lower power memory and other system components, or retarget use case. NXP highly recommends the use of LPDDR4 memories to lower power consumption.	

Chapter 7
Revision history

Table 35. Revision history

Revision number	Date	Substantive changes
0	03/2021	Initial release

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