ISL79987, ISL79988

4-Channel Differential Input Video Decoder with MIPI-CSI2/BT.656 Output for Around View Applications

FN8907
Rev.1.00
Mar 19, 2019

The ISL79987 and ISL79988 integrate four, high-quality NTSC/PAL/SECAM video decoders that convert analog composite video signals to digital component YCbCr data for automotive applications. Each channel contains a 10-bit ADC that supports single-ended, differential, and pseudo differential composite video inputs. The ISL79987 and ISL79988 use a 4H-comb filter for separating luminance and chrominance to reduce cross noise artifacts, and proprietary clamp and gain controllers. Integrated short-to-battery and short-to-ground detection, advanced image enhancement capabilities such as the programmable Automatic Contrast Adjustment (ACA), and the MIPI-CSI2/ITU-R BT.656 output interface make the ISL79987 and ISL79988 an ideal solution for the demands of automotive around view applications.

Applications

- Automotive around view

Related Literature

- For a full list of related documents, visit our website:
  - ISL79987, ISL79988 device pages

Features

Analog Video Decoder

- Software-selectable analog input control allows for combinations of single-ended CVBS and differential CVBS
- Integrated, four-video analog anti-aliasing filters and 10-bit CMOS ADCs with differential and single-ended inputs
- Fully programmable static gain or automatic gain control for the Y-channel
- Programmable white peak control for the Y-channel
- 4-H adaptive comb filter Y/C separation
- PAL delay line for color phase error correction
- Digital subcarrier PLL for accurate color decoding
- Digital horizontal PLL for synchronization processing and pixel sampling
- Advanced synchronization processing and sync detection for handling non-standard and weak signals
- Automatic color control and color killer
- Chroma IF compensation
- Programmable output cropping

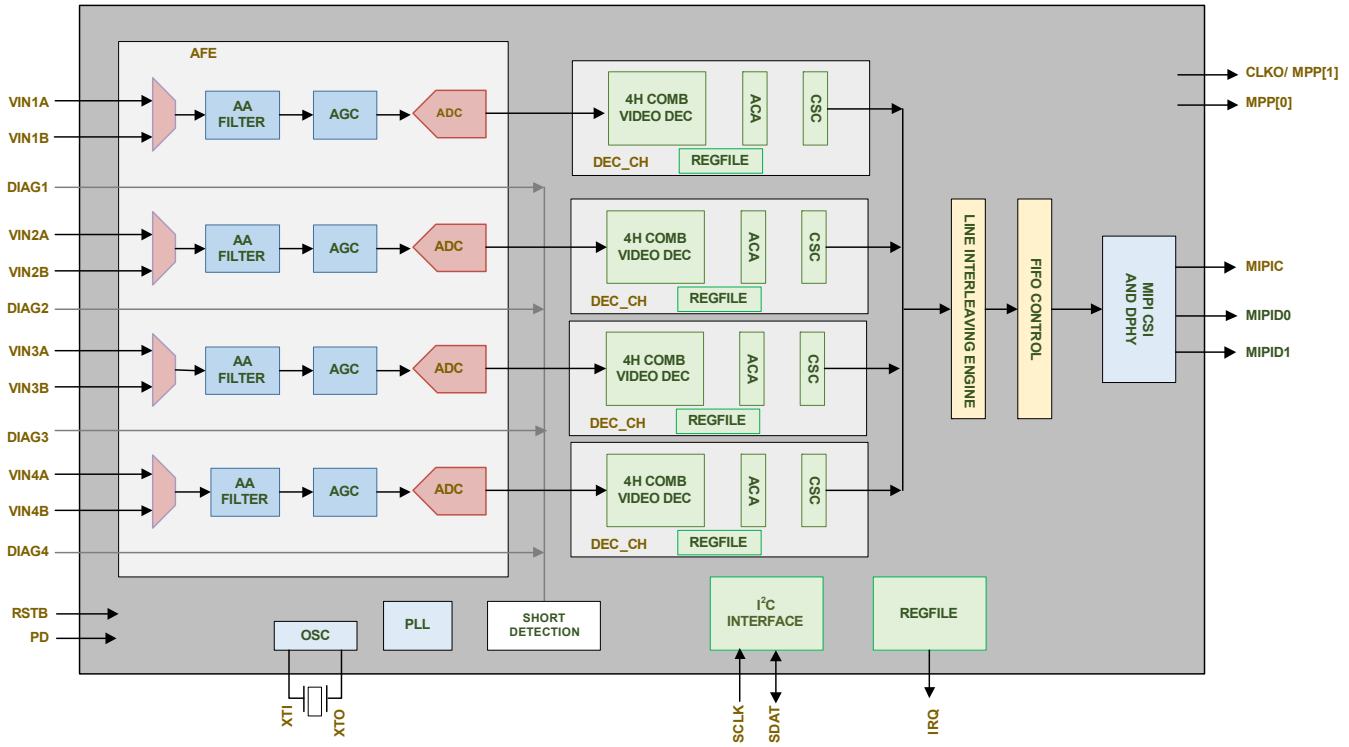

FIGURE 1. ISL79987 BLOCK DIAGRAM

Features (continued)

Video Processing

- Automatic Contrast Adjustment (ACA)
- Programmable hue, brightness, saturation, contrast, and sharpness
- Image enhancement with peaking and CTI

MIPI Output

- MIPI CSI-2 version 1.1 compliant unidirectional output
- Standard virtual identification channel support
- Non-standard pseudo virtual channel support
- One or two data lanes
- YUV422 or RGB565 output format

Digital Output

- Supports standard ITU-R BT.656 format or time multiplexed output with 27/54/108MHz
- Output voltage 1.8V to 3.3V

Miscellaneous

- Low power consumption
- Power save and power-down mode
- Short-to-battery detection
- Short-to-ground detection
- Two wire MPU serial bus interface
- Supports real time control interface
- Single 27MHz crystal for all operations
- 1.2V/3.3V power supply
- 48 Ld QFN package
- ISL79987ARZ and ISL79988ARZ are AEC-Q100 qualified

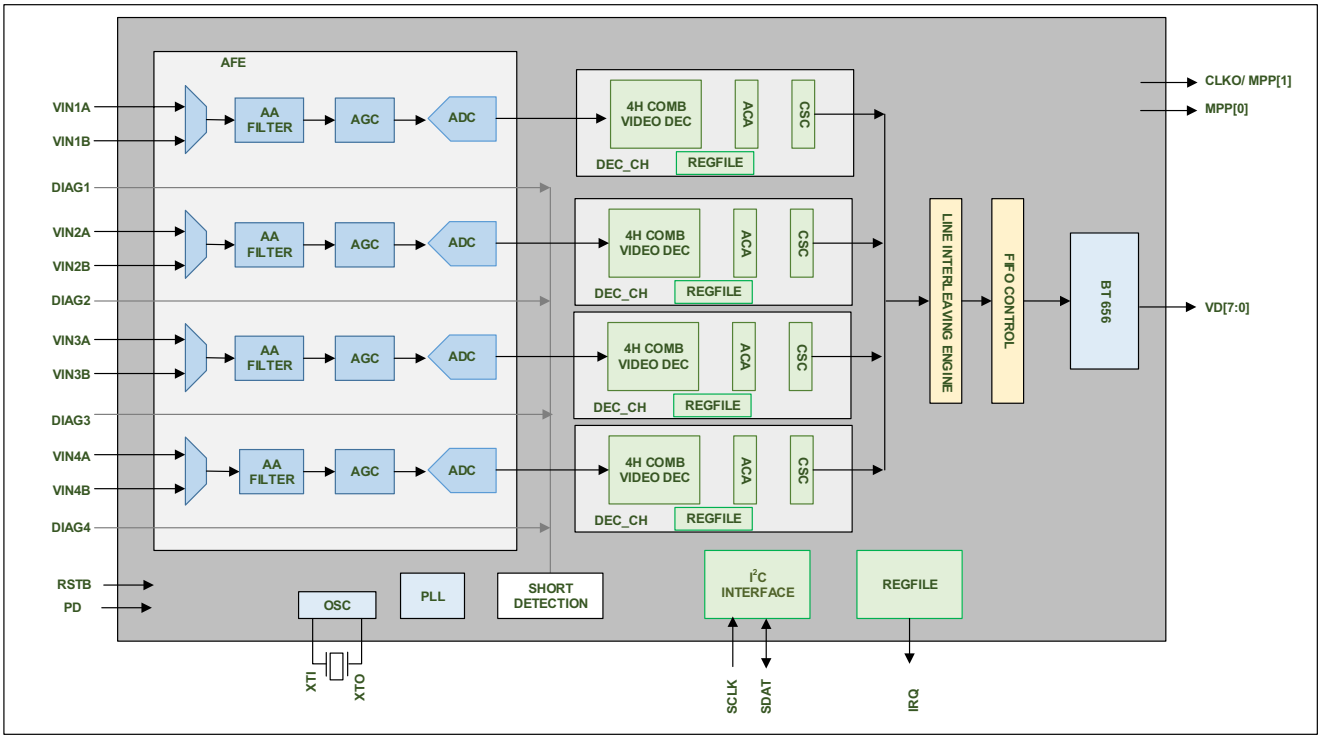

FIGURE 2. ISL79988 BLOCK DIAGRAM

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Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP RANGE (°C)	TAPE AND REEL (Units) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL79987ARZ	ISL79987 ARZ	-40 to +105	-	48 Ld QFN (7mmx7mm)	L48.7x7W
ISL79987ARZ-T	ISL79987 ARZ	-40 to +105	3k	48 Ld QFN (7mmx7mm)	L48.7x7W
ISL79987IRZ	ISL79987 IRZ	-40 to +85	-	48 Ld QFN (7mmx7mm)	L48.7x7W
ISL79987IRZ-T	ISL79987 IRZ	-40 to +85	3k	48 Ld QFN (7mmx7mm)	L48.7x7W
ISL79988ARZ	ISL79988 ARZ	-40 to +105	-	48 Ld QFN (7mmx7mm)	L48.7x7W
ISL79988ARZ-T	ISL79988 ARZ	-40 to +105	3k	48 Ld QFN (7mmx7mm)	L48.7x7W
ISL79988IRZ	ISL79988 IRZ	-40 to +85	-	48 Ld QFN (7mmx7mm)	L48.7x7W
ISL79988IRZ-T	ISL79988 IRZ	-40 to +85	3k	48 Ld QFN (7mmx7mm)	L48.7x7W
ISL79987-EVAL	Evaluation Board				
ISL79988-EVAL	Evaluation Board				

NOTES:

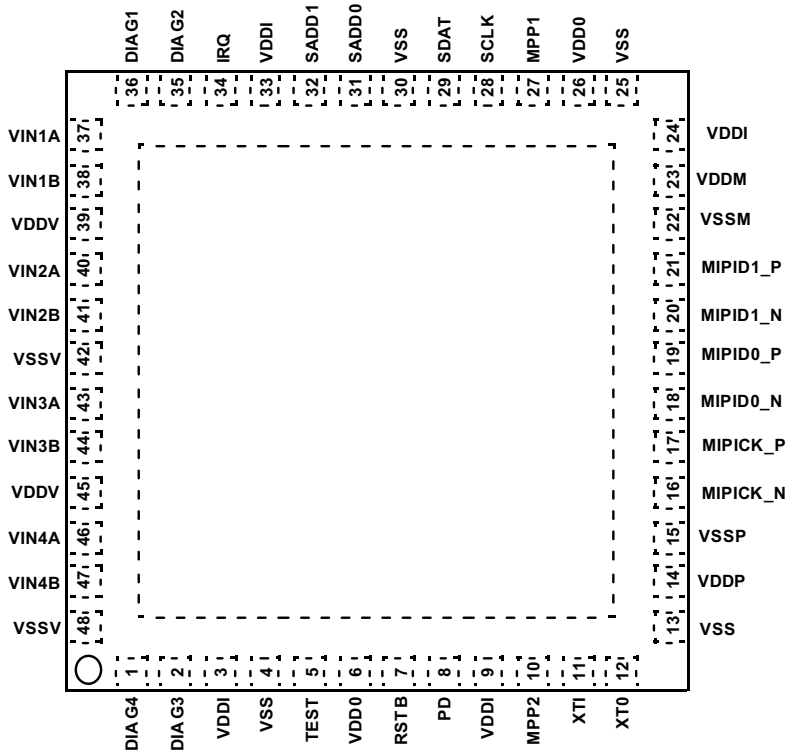
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL79987 and ISL79988 device pages. For more information about MSL, see TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

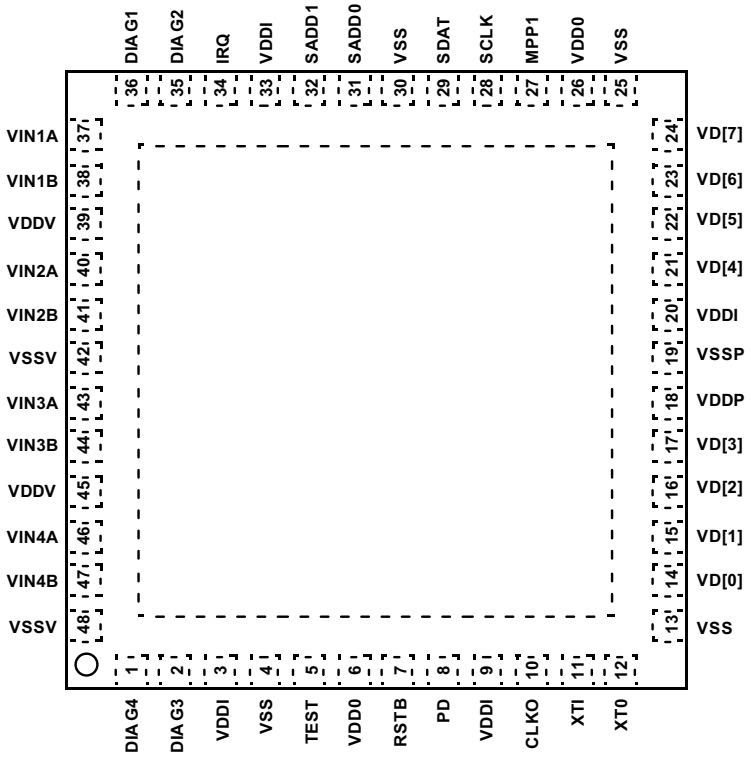
PARAMETERS	PART FAMILY		ALTERNATIVES		
	ISL79987	ISL79988	TW9984	TW9966	TW9992
Number of Inputs	8	8	8	8	8
Number of Channels/Device	4	4	4	4	1
Resolution	D1	D1	D1	D1	D1
Video DAC	No	No	Yes	Yes	No
Comb Filter	2D	2D	2D	2D	2D
Interface Type	MIPI1.1	BT.656	BT.656	BT.656, BT601	MIPI1.1
Analog Output	No	No	CVBS	CVBS	No
Qualification Level	Automotive	Automotive	Automotive	Automotive	Automotive
Function	Video Decoder	Video Decoder	Video Decoder	Video Decoder	Video Decoder

Pin Configurations

ISL79987
48 LD QFN
TOP VIEW



ISL79988
48 LD QFN
TOP VIEW



Pin Descriptions (ISL79987 - MIPI)

PIN#	I/O	PIN NAME	DESCRIPTION
ANALOG VIDEO SIGNAL			
37	I	VIN1A	Single-ended analog CVBS Input 1A/Differential CVBS positive Input 1
38	I	VIN1B	Single-ended analog CVBS Input 1B/Differential CVBS negative Input 1
40	I	VIN2A	Single-ended analog CVBS Input 2A/Differential CVBS positive Input 2
41	I	VIN2B	Single-ended analog CVBS Input 2B/Differential CVBS negative Input 2
43	I	VIN3A	Single-ended analog CVBS Input 3A/Differential CVBS positive Input 3
44	I	VIN3B	Single-ended analog CVBS Input 3B/Differential CVBS negative Input 3
46	I	VIN4A	Single-ended analog CVBS Input 4A/Differential CVBS positive Input 4
47	I	VIN4B	Single-ended analog CVBS Input 4B/Differential CVBS negative Input 4
36	I	DIAG1	Short detection Input 1
35	I	DIAG2	Short detection Input 2
2	I	DIAG3	Short detection Input 3
1	I	DIAG4	Short detection Input 4
MIPI SIGNALS			
17	O	MIPICK_P	MIPI clock channel
16	O	MIPICK_N	
19	O	MIPID0_P	MIPI data Channel 0
18	O	MIPID0_N	
21	O	MIPID1_P	MIPI data Channel 1
20	O	MIPID1_N	
CRYSTAL CLOCK SIGNALS			
12	O	XTO	Crystal clock output. Open when a single-ended oscillator is connected to XTI.
11	I	XTI	Crystal clock input. A 27MHz fundamental (or third overtone) crystal or a single-ended oscillator can be connected.
GENERAL SIGNALS			
34	O	IRQ	Interrupt request output signal
27	I/O	MPP1	Multi-purpose IO 1
10	I/O	MPP2	Multi-purpose IO 2
8	I	PD	Power-down control pin. (1: Power-down 0: Normal operation). When active, the XTI stops oscillation and all inputs to the analog module are inactive.
7	I	RSTB	Reset input. Low active.
5	I	TEST	Test pin. Connect to ground.
SERIAL IO INTERFACE			
28	I	SCLK	MPU serial interface clock line
29	I/O	SDAT	MPU serial interface data line
31	I	SADD0	Serial IO bus address selection LSB
32	I	SADD1	Serial IO bus address selection LSB+1

Pin Descriptions (ISL79987 - MIPI) (Continued)

PIN#	I/O	PIN NAME	DESCRIPTION
POWER AND GROUND PINS			
3, 9, 24, 33	PWR	VDDI	1.2V digital core power
4, 13, 25, 30	GND	VSS	Ground return for digital core and IO ring
6, 26	PWR	VDDO	3.3 or 1.8V digital I/O power
39, 45	PWR	VDDV	3.3V analog power for video ADC
42, 48	GND	VSSV	Ground return for video ADC
23	PWR	VDDM	1.2V analog power for MIPI
22	GND	VSSM	Ground return for MIPI
14	PWR	VDDP	1.2V analog power for PLL and BG
15	GND	VSSP	Ground for PLL and BG

NOTE: Connect unused input pin to AGND through 0.1µF capacitor.

Pin Descriptions (ISL79988 - ITU-R BT.656)

PIN#	I/O	PINNAME	DESCRIPTION
37	I	VIN1A	Single-ended analog CVBS Input 1A/differential CVBS positive Input 1
38	I	VIN1B	Single-ended analog CVBS Input 1B/differential CVBS negative Input 1
40	I	VIN2A	Single-ended analog CVBS Input 2A/differential CVBS positive Input 2
41	I	VIN2B	Single-ended analog CVBS Input 2B/differential CVBS negative Input 2
43	I	VIN3A	Single-ended analog CVBS Input 3A/differential CVBS positive Input 3
44	I	VIN3B	Single-ended analog CVBS Input 3B/differential CVBS negative Input 3
46	I	VIN4A	Single-ended analog CVBS Input 4A/differential CVBS positive Input 4
47	I	VIN4B	Single-ended analog CVBS Input 4B/differential CVBS negative Input 4
36	I	DIAG1	Short detection Input 1
35	I	DIAG2	Short detection Input 2
2	I	DIAG3	Short detection Input 3
1	I	DIAG4	Short detection Input 4
BT.656 SIGNALS			
10	O	CLKO	BT.656 clock output
24	O	VD[7]	BT.656 data Bit 7
23	O	VD[6]	BT.656 data Bit 6
22	O	VD[5]	BT.656 data Bit 5
21	O	VD[4]	BT.656 data Bit 4
17	O	VD[3]	BT.656 data Bit 3
16	O	VD[2]	BT.656 data Bit 2
15	O	VD[1]	BT.656 data Bit 1
14	O	VD[0]	BT.656 data Bit 0

Pin Descriptions (ISL79988 - ITU-R BT.656) (Continued)

PIN#	I/O	PINNAME	DESCRIPTION
CRYSTAL CLOCK SIGNALS			
12	O	XTO	Crystal clock output. Open when a single-ended oscillator is connected to XTI.
11	I	XTI	Crystal clock input. A 27MHz fundamental (or third overtone) crystal or a single-ended oscillator can be connected.
GENERAL SIGNALS			
34	O	IRQ	Interrupt request output signal
27	I/O	MPP1	Multi-purpose IO 1
8	I	PD	Power-down control pin. (1: Power-down 0: Normal operation). When active, the XTI stops oscillation and all inputs to analog module are inactive.
7	I	RSTB	Reset input. Low active.
5	I	TEST	Test pin. Connect to ground.
SERIAL IO INTERFACE			
28	I	SCLK	MPU serial interface clock line
29	I/O	SDAT	MPU serial interface data line
31	I	SADD0	Serial IO bus address selection LSB
32	I	SADD1	Serial IO Bus address selection LSB+1
POWER AND GROUND PINS			
3, 9, 20, 33	PWR	VDDI	1.2V digital core power
4, 13, 25, 30	GND	VSS	Ground return for digital core and IO ring
6, 26	PWR	VDDO	3.3 or 1.8V digital I/O power
39, 45	PWR	VDDV	3.3V analog power for video ADC
42, 48	GND	VSSV	Ground return for video ADC
18	PWR	VDDP	1.2V analog power for PLL and BG
19	GND	VSSP	Ground for PLL and BG

NOTE: Connect unused input pins to AGND through 0.1µF capacitor.

Absolute Maximum Ratings

VDDI to VSS . . . . . -0.5V to +1.6V
VDDO to VSS . . . . . -0.5V to +4.2V
VDDV to VSSV . . . . . -0.5V to +4.2V
VDDP to VSSP . . . . . -0.5V to +1.6V
VDDM to VSSM . . . . . -0.5V to +1.6V
Any Digital Pin to VSS . . . . . -0.5V to +4.2V
AFE Analog Pin to VSSV . . . . . -0.5V to +2.3V
MIPI Analog Pin to VSSM . . . . . -0.5V to +1.6V
ESD Ratings
Human Body Model (Tested per AEC-Q100-002) 2kV
Machine Model (Tested per AEC-A100-003) 200V
Charged Device Model (Tested per AEC-Q100-011) 750V
Latch-Up (Per JESD-78D; Class 2, Level A; AEC-Q100-004) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld 7x7 QFN (Notes 4, 5)	24	1

Junction Temperature Range . . . . . -65°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

VDDI . . . . . +1.1V to +1.3V
VDDO . . . . . +1.62V to +3.6V
VDDV . . . . . +2.97V to +3.6V
VDDP, VDDM . . . . . +1.1V to +1.3V
Ambient Temperature Range (ISL79987/8IRZ) . . . . . -40°C to +85°C
Ambient Temperature Range (ISL79987/8ARZ) . . . . . -40°C to +105°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

VDDI = VDDM = VDDP = 1.2V, VDD33 = VDDO = VDDV = 3.3V, unless otherwise noted, typical values are at T_A = +25°C.

PARAMETER	SYMBOL	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
DIGITAL INPUTS					
Input High Voltage (at VDDO = 3.3V)	V_{IH}	2.0		3.6	V
Input Low Voltage (at VDDO = 3.3V)	V_{IL}	-0.3		0.8	V
Input High Voltage (at VDDO = 1.8V)	V_{IH}	1.17		1.98	V
Input Low Voltage (at VDDO = 1.8V)	V_{IL}	-0.3		0.63	V
Input Leakage Current (at V_I = 3.3V or 0V)	I_L			±10	µA
Input Capacitance	C_{IN}		6		pF
DIGITAL OUTPUTS					
Output High Voltage (at VDDO = 3.3V)	V_{OH}	2.4			V
Output Low Voltage (at VDDO = 3.3V)	V_{OL}			0.4	V
Output High Voltage (at VDDO = 1.8V)	V_{OH}	1.35			V
Output Low Voltage (VDDO = 1.8V)	V_{OL}			0.45	V
High Level Output Current (at VDDO = 1.8V)	I_{OH}	2.4			mA
Low Level Output Current (at VDDO = 1.8V)	I_{OL}	3.5			mA
Tri-State Output Leakage Current (at V_O = 3.3V or 0V)	I_{OZ}			±10	µA
Output Capacitance	C_O		6		pF
Analog Pin Input Capacitance	C_A		6		pF
ANALOG INPUT					
VIN1~4 Input Range (AC coupling)	V_{P-P}	0.5	1.0	2.0	V
Analog Pin Input Capacitance	C_A		6		pF

Electrical Specifications VDDI = VDDM = VDDP = 1.2V, VDD33 = VDDO = VDDV = 3.3V, unless otherwise noted, typical values are at T_A = +25°C. (Continued)

PARAMETER	SYMBOL	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SUPPLY CURRENT					
Analog Video ADC Supply Current (VDDV, 3.3V)	I_{DDV}		46.8		mA
MIPI Supply Current (VDDM, 1.2V)	I_{DDM}		12.3		mA
Clock PLL Supply Current (VDDP, 1.2V)	I_{DDP}		5.1		mA
Digital Internal Supply Current (VDDI, 1.2V)	I_{DDI}		65.5		mA
Digital I/O Supply Current (VDDO, 3.3/1.8V)	I_{DDO}		1.2/4.3		mA
Total Power Dissipation (VDDO = 1.8/3.3V)	P		258/270		mW
MIPI OUTPUT LOW POWER					
Output High Voltage	V_{OH_LP}	1.1	1.2	1.3	V
Output Low Voltage	V_{OL_LP}	-50		50	mV
Output Impedance	ZO_LP	110			Ω
Slew Rate at C_{LOAD} = 0 to 70pF (Rising Edge Only)	δV/δtSR	30			mV/ns
Slew Rate at C_{LOAD} = 0 to 70pF (Rising Edge Only) for V400mV < VO <700mV	δV/δtSR	30			mV/ns
Slew Rate at C_{LOAD} = 0 to 70pF (Rising Edge Only) for VO > 700mV (VO, INST is the Instantaneous Output Voltage, VDP or VDN, in mV)	δV/δtSR	30 – 0.075 * (VO, INST – 700)			mV/ns
MIPI OUTPUT HIGH SPEED					
Static Common-Mode Voltage	V_{CMTX}	150	200	250	mV
V_{CMTX} Mismatch between $V_{OD(0)}$ and V_{OD}	$\lvert DV_{CMTX(1,0)} \rvert$			5	mV
V_{CMTX} Common Level Variation	$DV_{CMTX(LF)}$			25	mV_{PEAK}
Differential Voltage	$\lvert V_{OD} \rvert$	140	200	270	mV/ns
V_{OD} Mismatch Between $V_{OD(0)}$ and V_{OD}	$\lvert DV_{OD} \rvert$			14	mV/ns
Output High Voltage	V_{OHHS}			360	mV/ns
Single-Ended Output Impedance	Z_{OS}	40	50	62.5	Ω
Z_{OS} Mismatch	$\lvert DZ_{OS} \rvert$			10	%

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

TABLE 2. CRYSTAL REQUIREMENT SPECIFICATION

PARAMETER	SYMBOL	TYP	MAX	UNIT
Nominal Frequency (Fundamental)		27		MHz
Deviation			±50	ppm
Load Capacitance	C_L	20		pF
Series Resistor	R_S	80		Ω

Serial Host Interface Timing

TEST PARAMETER	SYMBOL	MIN (Note 7)	MAX (Note 7)	UNIT
Bus Free Time between STOP and START	t_{BF}	500		ns
SDAT Set-Up Time	t_{sSDAT}	50		ns
SDAT Hold Time	t_{hSDAT}	0		ns
Set-Up Time for START Condition	t_{sSTA}	260		ns
Set-Up Time for STOP Condition	t_{sSTOP}	260		ns
Hold Time for START Condition	t_{hSTA}	260		ns
Rise Time for SCLK and SDAT	t_{R_SB}		120	ns
Fall Time for SCLK and SDAT	t_{F_SB}		120	ns
SCLK Low Time	tLoW	260		ns
SCLK High Time	tHIGH	500		ns
Capacitive Load for Each Bus Line	C_{BUS}		550	pF
SCLK Clock Frequency	f_{SCLK}		1000	kHz

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

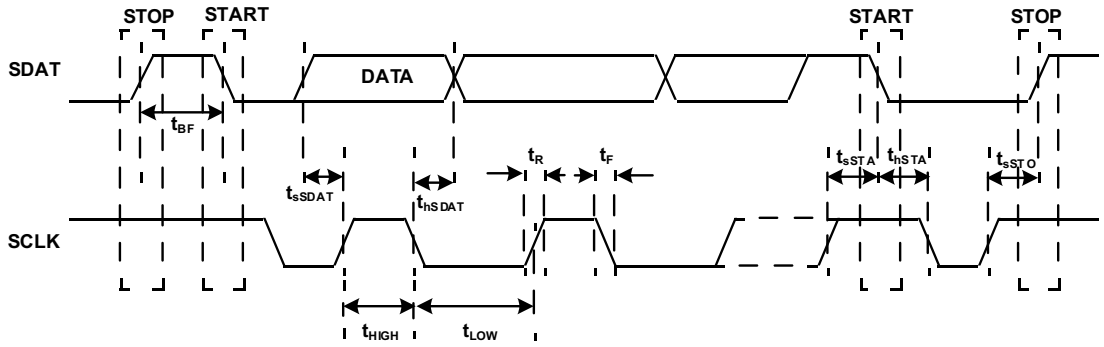


FIGURE 3. SERIAL HOST INTERFACE TIMING DIAGRAM

ISL79987 MIPI Low Power AC Timing

TEST PARAMETER	SYMBOL	MIN (Note 7)	TYP	MAX (Note 7)	UNIT	NOTES
Rise/Fall Time 15% to 85% of V_{OH} to V_{OL}	t_{RLP}/t_{FLP}			25	ns	C_{LOAD} ≤70pF
Rise/Fall Time 30% to 85% from HS Differential Amplitude Drops Below 70mV to V_{DP} = 880mV	T_{REOT}			35	ns	C_{LOAD} ≤70pF with additional C_{cM} up to 60pF
Pulse Width of LP XOR Clock	$t_{LP-PULSE-TX}$	40			ns	First/last pulse after/before Stop state
	$t_{LP-PULSE-TX}$	20			ns	All other pulses
Period of LP XOR Clock	$t_{LP-PER-TX}$	90			ns	
Transmitted Length (duration) of Any Low Power State	t_{LPX}	50			ns	This is an internal parameter

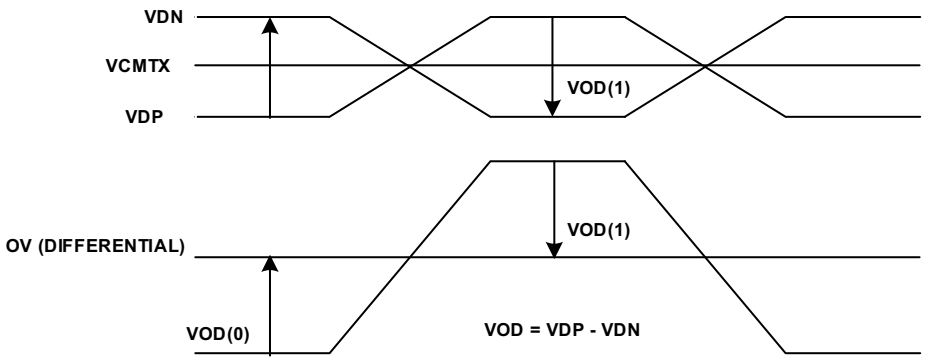


FIGURE 4. ISL79987 MIPI LOW POWER AC TIMING

ISL79987 MIPI High Speed AC Timing

TEST PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Unit Interval Instantaneous	UI_{INST}		4.629/ 2.314/ 1.157		ns	
UI Variation	ΔUI	-10%		10%	UI	Variation within a single burst with UI ≥ 1ns
Clock Lane DDR Clock Frequency (= 1/(2*$UI_{INST\ MIN}$))	fh_{MAX}		108/ 216/ 432		MHz	f_{XTAL} = 27MHz with 8b line coding
Rise/Fall Time 20% to 80%	t_R /t_F			0.3	UI	UI ≥ 1ns
		150			ps	
Data to Clock Skew	T_{SKEW}	-0.15		0.15	UI_{INST}	UI ≥ 1ns

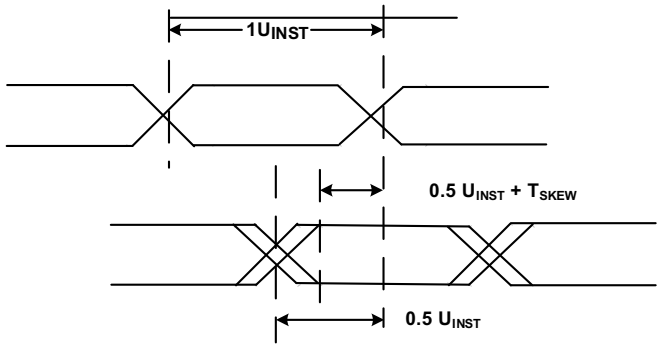


FIGURE 5. ISL79987 MIPI SPEED POWER AC TIMING

ISL79988 Video Data/Sync Timing

TEST PARAMETER	SYMBOL	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Hold from CLKO to Video Data/Sync (27MHz)	2a	3			ns
Delay from CLKO to Video Data/Sync (27MHz)	2b			7	ns
Hold from CLKO to Video Data/Sync (54MHz)	4a	3			ns
Delay from CLKO to Video Data/Sync (54MHz)	4b			7	ns
Hold from CLKO to Video Data/Sync (108MHz)	6a	3			ns
Delay from CLKO to Video Data/Sync (108MHz)	6b			7	ns

NOTE:

8. CLKO timing is related to CLKO_DEL register value. Figure 6 illustrates an example where the CLKO_DEL is set to 0 hex and CLKO_POL is set to 0.

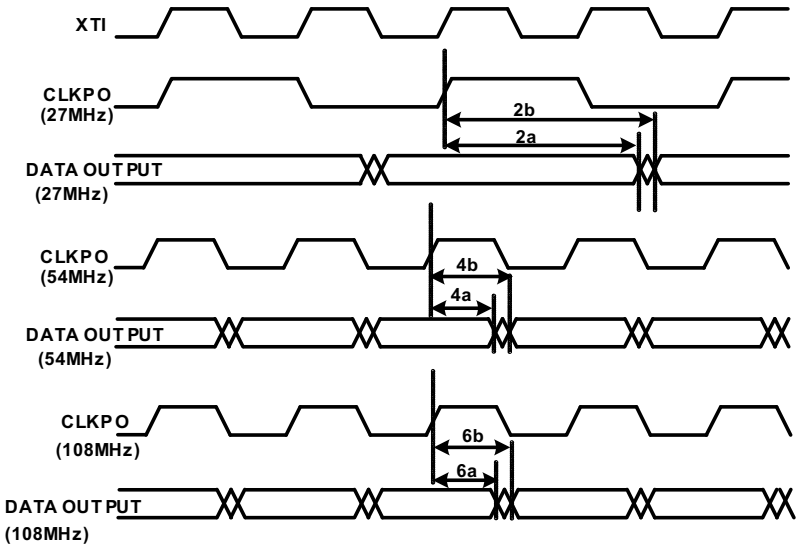


FIGURE 6. ISL79988 VIDEO DATA/SYNC TIMING

Functional Description

Video Input Formats

The ISL79987 and ISL79988 has built-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency, and frame rate to identify NTSC, PAL, or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60), and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The exceptions are the base standard NTSC and PAL, which are always enabled. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

ISL79987 and ISL79988 support all common video formats shown in Table 3.

TABLE 3. VIDEO INPUT FORMATS SUPPORTED BY THE ISL79987, ISL79988

FORMAT	LINES	FIELDS	FSC (MHz)	COUNTRY
NTSC-M	525	60	3.579545	U.S., many others
NTSC-Japan (Note 9)	525	60	3.579545	Japan
PAL-B, G, N	625	50	4.433619	Many
PAL-D	625	50	4.433619	China
PAL-H	625	50	4.433619	Belgium
PAL-I	625	50	4.433619	Great Britain, others
PAL-M	525	60	3.575612	Brazil
PAL-CN	625	50	3.582056	Argentina
SECAM	625	50	4.406, 4.25	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619	China
NTSC (4.43)	525	60	4.433619	Transcoding

NOTE:

9. NTSC-Japan has 0 IRE setup.

Analog Front-End

The ISL79987 and ISL79988 contain four 10-bit Analog to Digital Converters (ADCs) to digitize the analog video inputs. The ADCs can be put into power-down mode by the ADC_PD register (0x36[6] at Pages 1, 2, 3, 4). The ISL79987 and ISL79988 also contain an anti-aliasing filter to prevent out-of-band frequencies in the analog video input signal. As a result, there is no need for external components in front of the analog input pins, except for the AC coupling capacitor and termination resistor.

Figure 7 shows the frequency response of the anti-aliasing filter.

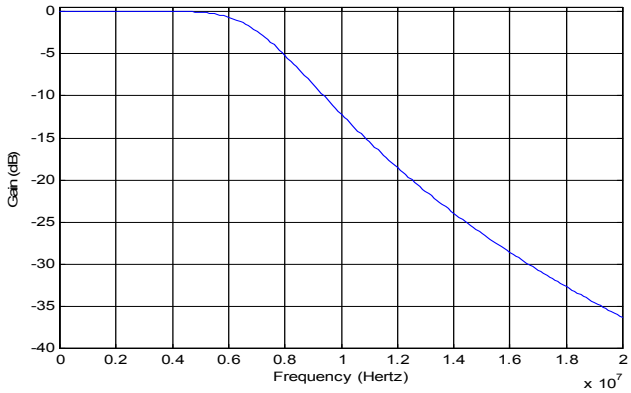


FIGURE 7. FREQUENCY RESPONSE OF THE ANTI-ALIASING FILTER

Decimation Filter

The digitized composite video data is over-sampled to simplify the design of the analog filter. The decimation filter is required to achieve optimum performance and prevent high-frequency components from being aliased back into the video image when down-sampled. Figure 8 shows the characteristic of the decimation filter.

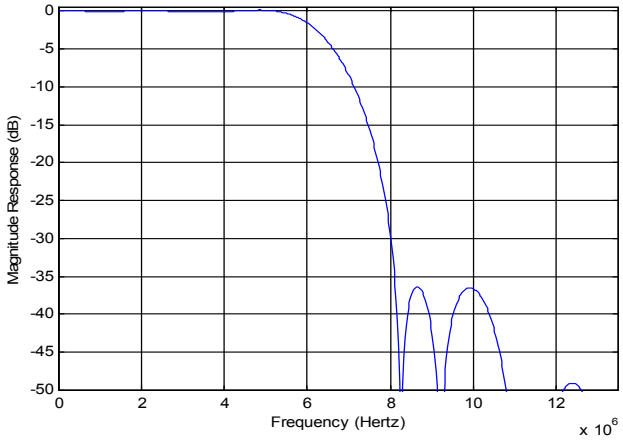


FIGURE 8. FREQUENCY RESPONSE OF THE DECIMATION FILTER

Automatic Gain Control and Clamping

All four analog channels have a built-in clamping circuit that restores the signal's DC level. The video input restores the back porch of the digitized video to a level of 60. This operation is automatic through an internal feedback loop. The Automatic Gain Control (AGC) of the video input adjusts the input gain so that the sync tip is at a desired level. Programmable white peak protection logic is included to prevent saturation in the case of an abnormal signal proportion between the sync and white peak level.

Sync Processing

The ISL79987 and ISL79988 sync processor detects horizontal synchronization and vertical synchronization signals in the composite video signal. The processor contains a digital Phase-Locked Loop (PLL) and decision logic to achieve reliable sync detection in a stable signal and in an unstable signal such as those from a VCR fast forward or rewind.

The vertical sync separator detects the vertical synchronization pattern in the input video signals. In addition, the actual sync determination is controlled by a detection window to provide more reliable synchronization. An option is available to provide faster responses for certain applications. The field status is determined at the vertical synchronization time. The field logic can also be controlled to toggle automatically while tracking the input.

Y/C Separation

The color-decoding block contains the luma/chroma separation for a composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, an adaptive notch/band-pass filter is used. The default selection for NTSC/PAL is a comb filter.

When using the comb filter, the ISL79987 and ISL79988 separate the luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary 4H adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current, and next lines. This technique leads to excellent Y/C separation with small cross luma and cross color at both the horizontal and vertical edges.

Due to the fact that a line buffer is used in the comb filter, there is always a two-line processing delay in the output.

Figures 9 and 10 shows the characteristics of the filters when notch/band-pass filter is selected.

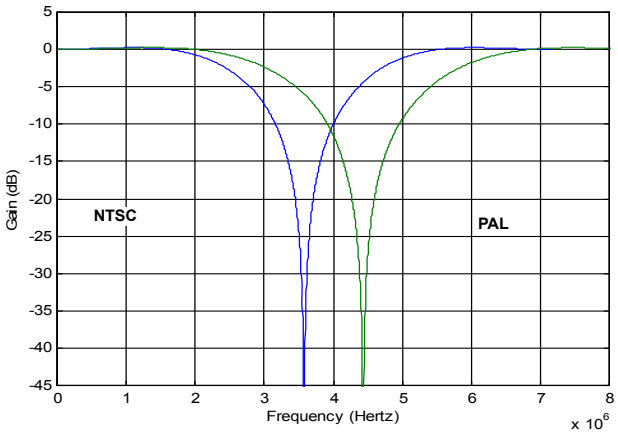


FIGURE 9. CHARACTERISTICS OF LUMINANCE NOTCH FILTER FOR PAL

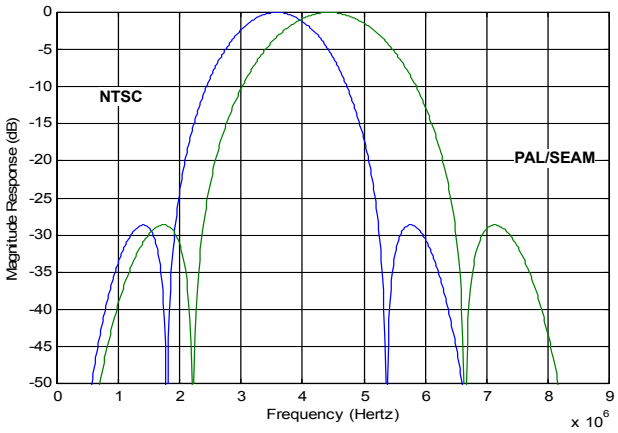


FIGURE 10. CHROMA BAND-PASS FILTER CURVES

Color Decoding

CHROMINANCE DEMODULATION

The color demodulation for NTSC and PAL standards is done by first quadrature mixing the chroma signal to the base band. A low-pass filter is then used to remove the carrier signal and yield chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid in the PAL color demodulation.

For SECAM, the color information is FM modulated onto a different carrier. The demodulation process therefore consists of FM demodulator and de-emphasis filter. During the FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

Note: The subcarrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input subcarrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

Figure 11 shows the frequency response of chrominance low-pass filter curves.

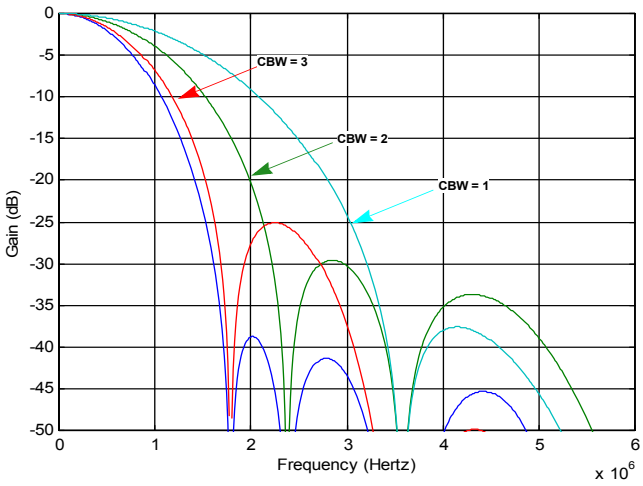


FIGURE 11. CHROMINANCE LOW-PASS FILTER CURVES

AUTOMATIC CHROMA GAIN CONTROL (ACC)

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in the video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. It is measured to control the chroma output gain. The range of ACC control is –6dB to +24dB.

Chrominance Processing

CHROMINANCE GAIN, OFFSET, AND HUE ADJUSTMENT

When decoding NTSC signals, the ISL79987 and ISL79988 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift of NTSC decoding can be programmed through a control register. For the PAL standard, the PAL delay line is provided to compensate any hue error; therefore, no hue adjustment is available. The color saturation can be adjusted by changing the gain of the Cb and Cr signals for all NTSC, PAL, and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

COLOR TRANSIENT IMPROVEMENT (CTI)

The Color Transient Improvement (CTI) function to further enhances the image quality. The CTI enhances the color edge transient without any overshoot or undershoot.

Luminance Processing

The ISL79987 and ISL79988 adjust brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The ISL79987 and ISL79988 also provide programmable peaking function to further enhance the video sharpness. The peaking control has a built-in coring function to prevent enhancement of noise. Figure 12 on page 18 shows the characteristic of the peaking filter for four different gain modes and different center frequencies.

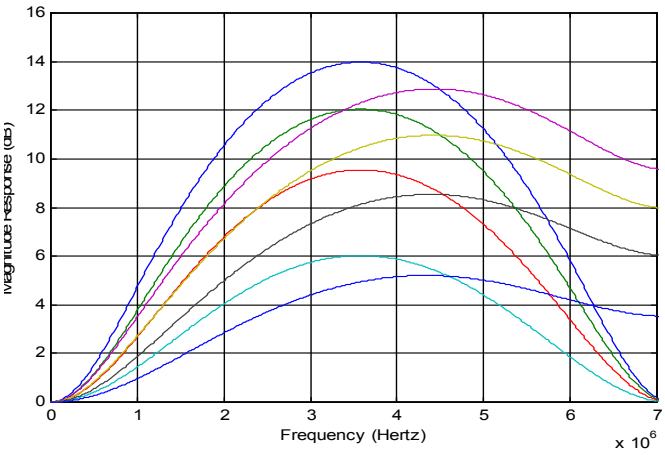


FIGURE 12. CHARACTERISTIC OF THE LUMINANCE PEAKING FILTER

Short Diagnostics

SHORT-TO-BATTERY AND SHORT-TO-GROUND

The ISL79987 and ISL79988 provide a Short-to-Battery (STB) and Short-to-Ground (STG) detection capability. The short diagnostics module has four channels, one for each video input. Both STB and STG support 8-step programmable threshold levels (3 bits per threshold). The Short-to-Ground thresholds range from 1/152 to 8/152 of the 3.3V power supply. The Short-to-Battery thresholds range from 20/152, 26/152, 32/152, ..., 62/152 of the 3.3V power supply. STB and STG events can be detected by either polling registers or by using the interrupt pin.

Video Cropping

Cropping allows only a subsection of a video image to be output. The active video region is determined by the HDELAY, HACTIVE, VDELAY, and VACTIVE registers. The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY, and VACTIVE registers. These registers are eight bits wide; the lower eight bits are, respectively, in HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. Their upper two bits share the same register CROP_HI.

The Horizontal Delay register (HDELAY) determines the number of pixels delay between the leading edge of HSYNC and the leading edge of the HACTIVE. Note that this value is referenced to the unscaled pixel number. The Horizontal Active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the unscaled pixel number. Therefore, if the scaling ratio is changed, the active video region used for scaling remains unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to downscaling. For the cropping to work properly, Equation 1 should be satisfied.

$$HDELAY + HACTIVE < \text{Total number of pixels per line} \quad \text{(EQ. 1)}$$

For NTSC output at 13.5MHz pixel rate, the total number of pixels is 858. For PAL output at 13.5MHz rate, the total number of pixels is 864. HACTIVE should be set to 720.

The Vertical Delay register (VDELAY) determines the number of lines delay between the leading edge of the VSYNC and the start of the active video lines. It indicates the number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the vertical scaling. The number of scan lines is 525 for the 60Hz systems and 625 for the 50Hz systems. The Vertical Active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register depending on the vertical scaling ratio. For the vertical cropping to work properly, Equation 2 should be observed.

$$VDELAY + VACTIVE < \text{Total number of lines per field} \quad \text{(EQ. 2)}$$

Test Pattern Generator

For each input video channel, the chip provides a corresponding test pattern generator that can be used to replace the real input video for testing purposes. Each generator can be programmed to output NTSC or PAL format, and can generate fixed-sync or variable-sync timing to emulate real video source timings with a much wider variation range.

ISL79988 - BT.656 Line-Interleaved Output

The ISL79988 supports up to 4-channel CVBS inputs and merges multi-video streams into a single BT.656 output bus. If streaming two or more channels, a line-interleaved method is employed. The ISL79988 supports one single video stream format and two multi-video stream formats that are clocked at 27MHz, 54MHz, and 108MHz (see Table 4 for details). When outputting multi-video stream on the BT.656 bus, channel IDs are inserted in sync word. Each line starts with an EAV, followed by horizontal blank data, SAV, and active data. The channel ID is embedded into SAV/EAV's least-significant two bits and in horizontal blank data on the least-significant two bits.

TABLE 4. VIDEO OUTPUT FORMAT

VIDEO OUTPUT FORMAT	OUTPUT CLOCK FREQUENCY (MHz)
1-CH with 480i	27
2-CH with 480i	54
4-CH WITH 480i	108

Figure 13 on page 19 illustrates that the four independent channels' video data are merged by the line-interleaved method to the BT.656 output.

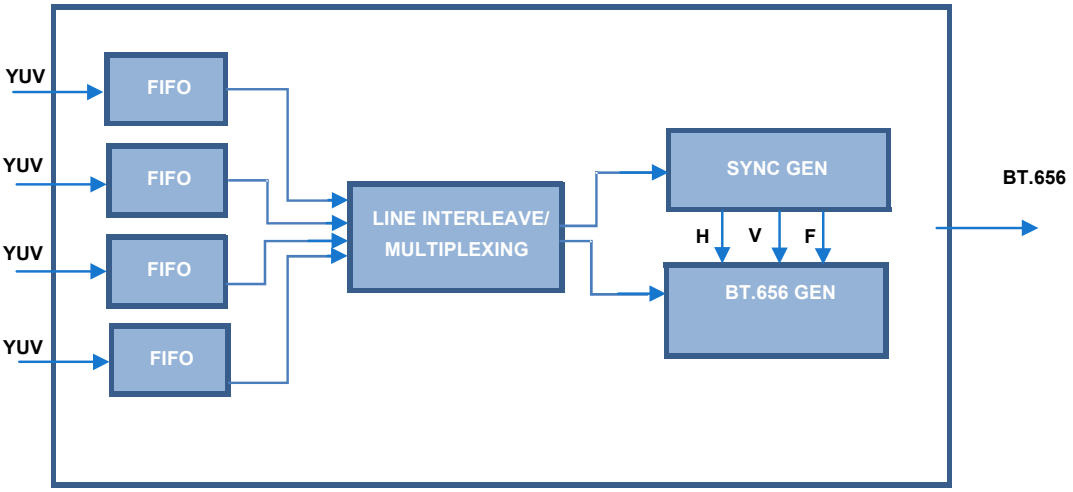


FIGURE 13. ISL79988 - BT.656 LINE-INTERLEAVED OUTPUT

BT.656 Preamble Format

The receiver should detect the EAV and SAV by looking for the 8-bit FFh-00h-00h-XXh preamble sequence. The last status byte of the preamble sequence indicates channel ID, field, VSYNC, and HSYNC information.

PREAMBLE	D7	D6	D5	D4	D3	D2	D1	D0
STATUS WORD	1	F	V	H	0	0	CH ID[1]	CH ID[0]

BT.656 Interleaved Data Transmission with Channel ID

The channel ID is updated in preamble EAV on each line and retains the channel ID information for the horizontal blank data and the preamble SAV. Every output line always starts with an EAV followed by Horizontal Blank, SAV, and active data on the same channel. However, the channel order may not be sequential due to the sync-variation between different channels, which means that it is possible to output two consecutive lines from the same channel before switching to another channel. Figure 14 on page 20 shows an example of an output sequence.

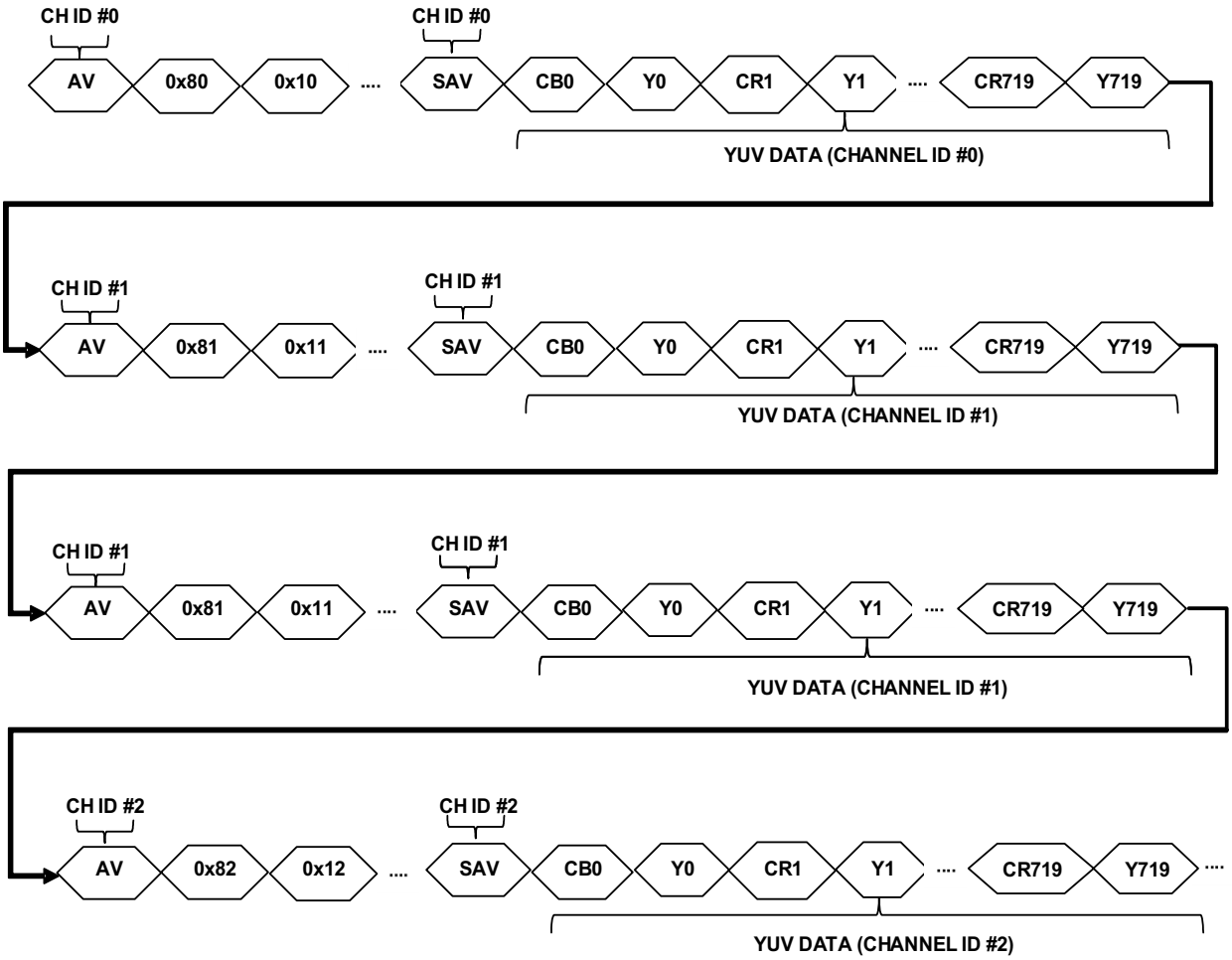


FIGURE 14. BT.656 INTERLEAVED DATA TRANSMISSION WITH CHANNEL ID

BT.656 Optional Header

In addition to the channel ID in EAV, Horizotnal blank, and SAV sequence, there is an optional 8-byte header insert followed by each SAV to provide additional information for that horizontal line. In this case, each horizontal line has 1448 bytes of active data instead of 1440 bytes. This special 8-byte header is defined to avoid conflict with the SAV and EAV byte sequence.

HD1 is sent out first and HD2 follows it. HD8 is the last byte that is sent out. Active video data follows HD8.

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HD1	'1'	'0'	'1'	'0'	Frame[3:0]			
HD2	'1'	'0'	'1'	'0'	'0'	'0'	'0'	Field
HD3	'1'	'0'	'1'	'0'	Line[11:8]			
HD4	'1'	'0'	'1'	'0'	Line[7:4]			
HD5	'1'	'0'	'1'	'0'	Line[3:0]			
HD6	'1'	'0'	'1'	'0'	'0'	'0'	CHID[1:0]	
HD7	'1'	'0'	'1'	'0'	VDLOSS	HLOCK	SLOCK	VLOCK
HD8	'1'	'0'	'1'	'0'	MONO	DET50	DETSTUS	V_ STABLE

- CHID - Video channel ID, from 0 to 3
- Line - Line number
- Field - Field indicator. 0 is first (top) field. 1 is second (bottom) field
- Frame - Frame number
- VDLOSS - Same as 0x103[7]
- HLOCK, SLOCK, VLOCK - Same as 0x103[6], 0x103[5], 0x103[3]
- MONO - Same as 0x103[1]
- DET50 - Same as 0x103[0]
- DETSTUS - Same as 0x11c[7]
- V_STABLE - Video data stable flag when video is detected and all syncs are in lock

ISL79987 - MIPI OUTPUT

The MIPI transmitter consists of a protocol module that is compatible with the MIPI CSI-2 v1.1 interface standard, and a physical layer module that is compatible with the MIPI D-PHY V1.1 standard.

In the protocol module, up to four (one, two, or four) independent NTSC or PAL standard video channels are line-interleaved into a single data stream, which is then de-multiplexed into one or two data lanes following the CSI-2 specification. The digital data, along with the MIPI-specific clock and data digital control signals, are fed to the analog D-PHY module.

In the D-PHY module, the data, clock, and control signals are converted into MIPI-compatible, serialized data ready for output. Depending on the input and output configuration, the chip supports the following five major modes of operation. Different output clock frequencies are generated by an on-chip PLL module, which uses a unique 27MHz crystal input reference clock.

- 1-channel input with 1-data-lane mode: MIPI clock is 108MHz with 216Mbps data rate.
- 2-channel input with 1-data-lane mode: MIPI clock is 216MHz with 432Mbps data rate.
- 2-channel input with 2-data-lanes mode: MIPI clock is 108MHz with 216Mbps data rate.
- 4-channel input with 1-data-lane mode: MIPI clock is 432MHz with 864Mbps data rate.
- 4-channel input with 2-data-lanes mode: MIPI clock is 216MHz with 432Mbps data rate.

VIDEO OUTPUT FORMAT	OUTPUT MIPI CLOCK FREQUENCY (MHz)
1-CH with 480i	108 (1 lane)
2-CH with 480i	216 (1 Lane)
2-CH with 480i	108 (2 Lanes)
4-CH with 480i	432 (1 Lane)
4-CH with 480i	216 (2 Lanes)

Figure 15 on page 22 illustrates that the four independent channels' video data are merged by the line-interleaved method to the BT.656 output.

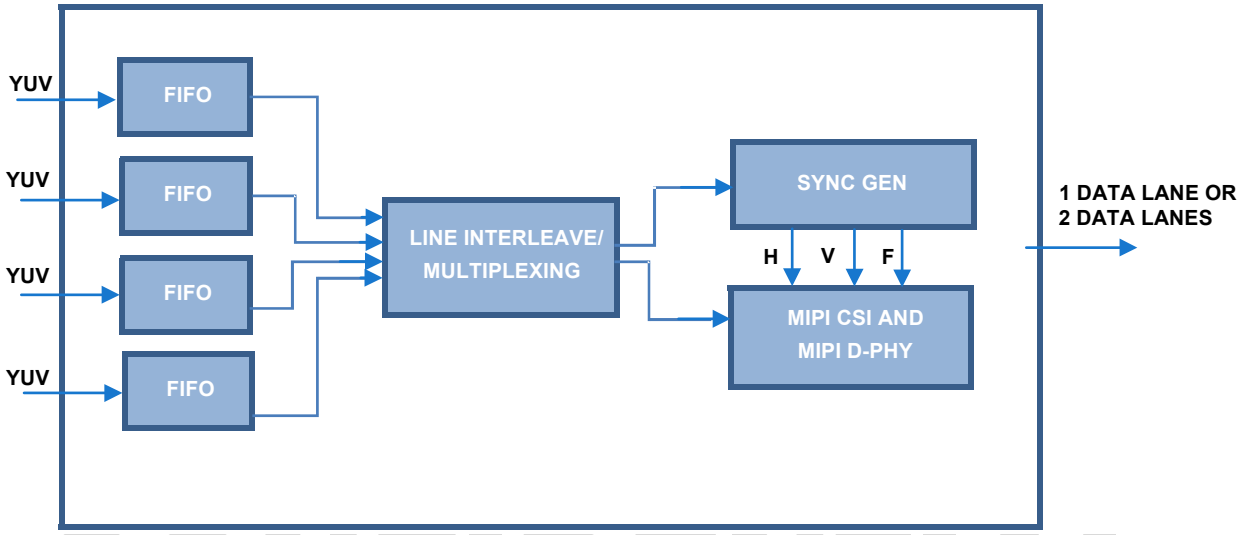


FIGURE 15. D-PHY TIMING

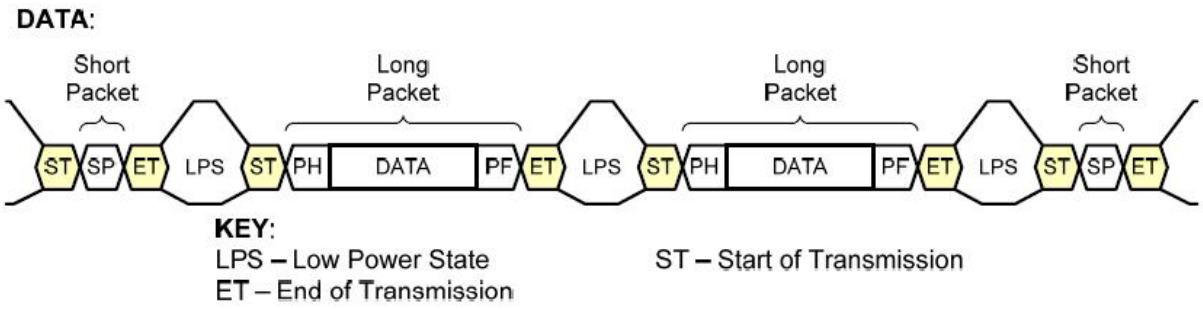


FIGURE 16. SHORT AND LONG PACKETS

Programmable D-PHY Timing

The low-power and high-speed data timing, and the clock-to-data timing are programmable based on the input channel-number and data-lane selections.

SHORT AND LONG PACKETS

The ISL79987 supports two types of short packets, Frame-Start (FS, 0x00) and Frame-End (FE, 0x01), which specify the start and end of a picture. There are also two types of long packets: YUV422 8-bit (0x1E) and YUV422 8-bit-user defined (0x30). The 0x30 data type is used to refer to the specific histogram-line data. Note that when the histogram-line option is selected, the 128-bin histogram data of an incoming picture is attached following the last line of the picture. Because the histogram-bin data is considerably different from the regular video format, it is sufficient to use a different data type “30” to designate it to the MIPI receiver. Figure 16 on page 22 shows an example of long and short packets.

CHANNEL DELINEATION

Two options for merging mutli-channel video onto a single MIPI link are:

- CSI-2 Standard mode
- Pseudo Single-Frame mode

These modes are described in the following sections.

CSI-2 Standard Mode

A 2-bit, Virtual-Channel (VC) field is embedded in the long-packet header’s Data-ID field and short-packet Data-ID field, Bits 7-6, to specify which channel the upcoming long and short packet belongs to. As defined in CSI-2 standard, each long packet should contain a complete horizontal line data. Each virtual channel has its own FS and FE packets. All the short and long packets from the four channels are interleaved into a single MIPI data stream following the original sync and data timing as close as possible. Therefore, the channel order may not be sequential due to sync-variation between different channels.

Pseudo Single-Frame Mode

In Pseudo Single-Frame mode, the MIPI receiver should treat the received 4-channel data as a pseudo one-channel data. In this case, only one Frame-Start (FS) and one Frame-End (FE) short packets are sent following either:

- The first channel’s vertical sync timing, or
- A fixed line-accummulator’s line-counter setting

The spacing between FE to the next FS is crucial for the receiver to finish its interrupt service routine and is limited to be no more than two lines due to the finite line-FIFO size constraint of the MIPI transmitter. Due to the asynchorous nature of multi-video input, the number of long packets (lines) between FS to FE can vary in the first case, while in the second case, the number of long packets are fixed. Only active data and auxliary data are transmitted in a long packet. Figure 17 and the following bit table show an example of a transmission sequence.

An 8-byte header is embedded immediately following the MIPI 4-byte long Packet Header (PH) for the receiver to identify the channel data. The 8-byte source video header has to be parsed by the receiver’s host processor to decide where to store the received data pertaining to the received channel. The special 8-byte header is defined to avoid emulation of “00” or “FF” bytes.

SHD1 is sent out first and HD2 follows it. The first active video data follows the HD8 byte.

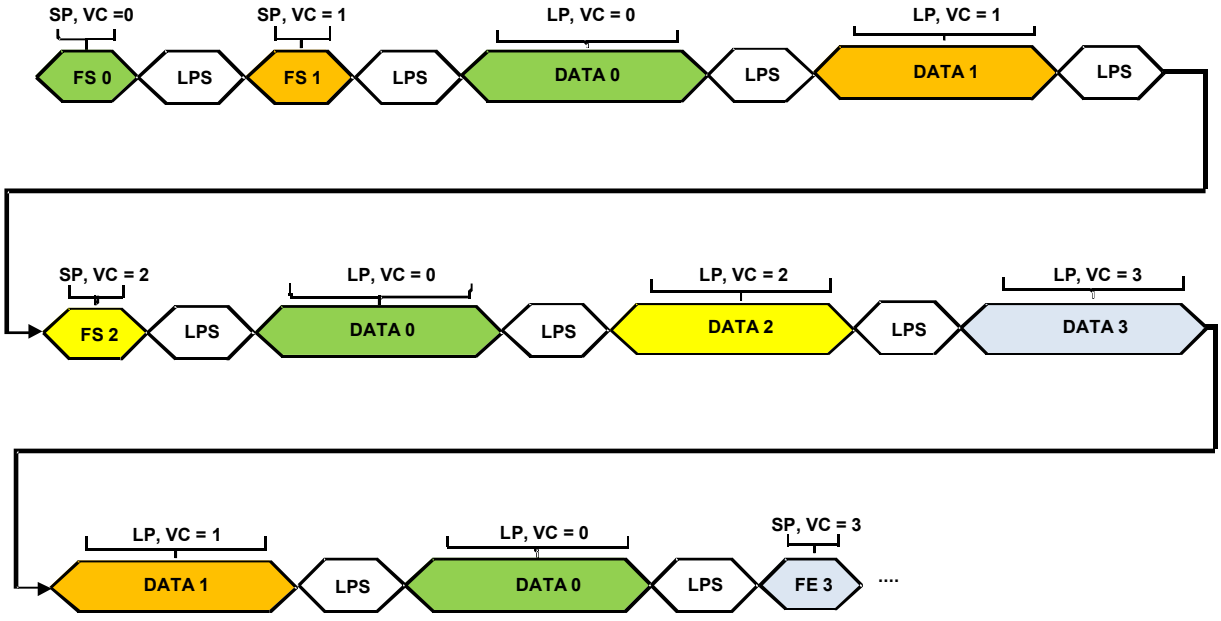


FIGURE 17. CHANNEL DELINEATION

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HD1	'1'	'0'	'1'	'0'	Frame[3:0]			
HD2	'1'	'0'	'1'	'0'	'0'	'0'	'0'	Field
HD3	'1'	'0'	'1'	'0'	Line[11:8]			
HD4	'1'	'0'	'1'	'0'	Line[7:4]			
HD5	'1'	'0'	'1'	'0'	Line[3:0]			
HD6	'1'	'0'	'1'	'0'	'0'	'0'	CHID[1:0]	
HD7	'1'	'0'	'1'	'0'	VDLOSS	HLOCK	SLOCK	VLOCK
HD8	'1'	'0'	'1'	'0'	MONO	DET50	DETSTUS	V_STABLE

- CHID - Video channel ID, from 0 to 3
- Line - Line number
- Field - Field indicator. 0 is the first (top) field. 1 is the second (bottom) field
- Frame - Frame number
- VDLOSS - Same as 0x103[7]
- HLOCK, SLOCK, VLOCK - Same as 0x103[6], 0x103[5], 0x103[3]
- MONO - Same as 0x103[1]
- DET50 - Same as 0x103[0]
- DETSTUS - Same as 0x11c[7]
- V_STABLE - Video data stable flag when video is detected

Optional Histogram as Additional Pixel Data

To enable histogram-line output on either a MIPI or BT.656 output, the following register bits need to be set:

- Reg0x1C0[7] = master (four separate histograms)
- Reg0x1C0[6] = union (4-in-1 histogram)
- Reg0x1E7[0] = hist_on1 = 1 in both master or union mode
- Reg0x2E7[0] = hist_on2 = 1 in master mode only
- Reg0x3E7[0] = hist_on3 = 1 in master mode only
- Reg0x4E7[0] = hist_on4 = 1 in master mode only

Because VActiveNs do not line up in union mode, Channels 2-4 evaluate the histogram following Channel 1's Vactive. The reported histogram is the partial frame of Channels 2-4. In the union mode, there is no need to turn on histogram-line for Channels 2-4, because they are not precisely one-frame's histogram and they are not in use.

There are two modes in sending histogram[18:0] over to the SoC receiver. Both modes stretch 19 bits to 4 bytes.

- MIPI-mode: {8'h00},
  {8'h00},
  {8'h00},
  {8'h00},
  {8'h00},
  {5'h00, histogram[18:16],
  {histogram[15:8]},
  {histogram[7:0]} }
- CCIR656-mode: {8'h55},
  {8'h55},
  {8'h55},
  {4'h5, 1'h0, histogram[18:16]},
  {4'h5, histogram[15:12]},
  {4'h5, histogram[11:8]},
  {4'h5, histogram[7:4]},
  {4'h5, histogram[3:0]} }

The format is cast in the decif_csc module and cannot be changed in the CSI because there is no need to furnish both simultaneously.

The accumulated histogram of each picture is allocated to 128-bins by grouping two levels into one bin.

At the end of a picture, the video-active is extended by one or more lines and the last line contains histogram data.

These 128 bins are transmitted as the first 1024 active pixels according to the above format. The remaining (1440-1024) active pixels are filled with the black pixels "8'h80" and "8'h10".

PCB Layout Considerations

In the Printed Circuit Board (PCB) layout, ground is the most important consideration to achieve a low level of noise. In general, avoid long current loops, especially when mixing analog signals with digital signals. The best way to achieve this is to partition the analog and digital portions very carefully so that the signal and return paths can be localized in their vicinity. Strategic partitioning and placement may make splitting the plane into digital and analog ground unnecessary. This helps prevent the split planes from creating longer loops that are bad for EMC and can spread interference to other sections.

The ground plane should cover most of the PCB area with separated digital and analog ground planes surrounding the chip. These two planes should be at the same electrical potential and connected together under the ISL79987 and ISL79988. Figure 18 shows a ground plane layout example.

To minimize crosstalk, separate the digital signals of the ISL79987 and ISL79988 from the analog circuitry. The digital signals should not cross over the analog power and ground plane. Avoid running parallel digital lines for long distance.

For the QFN package, the exposed die pad (ground bond) can be either floating or soldered to the PCB ground to enhance thermal performance, see Figure 19.

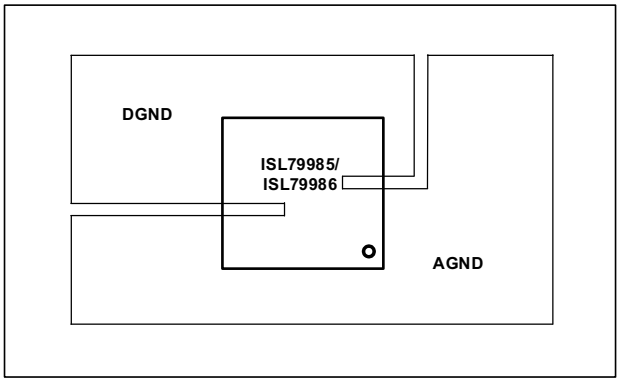


FIGURE 18. GROUND PLANES

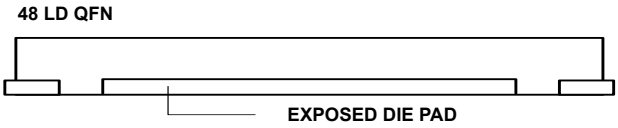


FIGURE 19. EXPOSED DIE PAD

Thermal PAD Considerations

Thermal Pad Land Design Input

The size of the thermal land should at least match the exposed die flag size. However, it is necessary to avoid solder bridging between thermal pad and the perimeter pads. Renesas recommends a clearance of 0.15mm between thermal pad and perimeter pads.

Thermal Via Design

To take full advantage of QFN thermal performance, thermal vias are needed to provide a thermal path from top to inner/bottom layers of the motherboard to remove the heat.

- Via size (in diameter): 0.3 ~ 0.33mm
- Via pitch: 1.0 ~ 1.2mm
- # of thermal vias: depends on the application

Stencil Recommendation

Use small multiple openings instead of one large opening.

- 60 ~ 85% solder paste coverage
- Rounded corners to minimize clogging
- Positive taper with bottom opening larger than the top

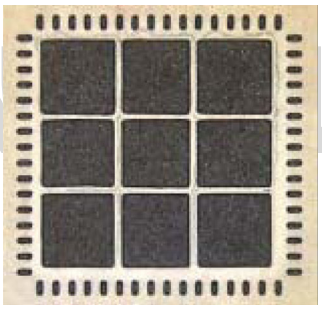


FIGURE 20A. DO NOT RECOMMEND COVERAGE 91%

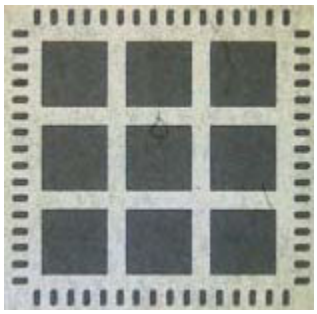


FIGURE 20B. RECOMMENDED COVERAGE 77%

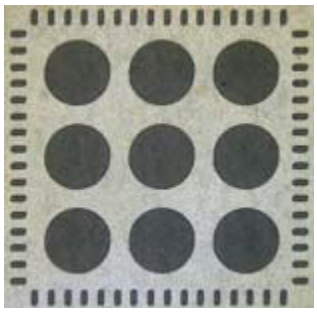


FIGURE 20C. RECOMMENDED COVERAGE 65%

FIGURE 20. STENCIL RECOMMENDED COVERAGE

ISL79987, ISL7998788 Register Summary

The registers are organized in functional groups.

TABLE 5. COMMON REGISTERS (PAGE 0)

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
FF	-				PAGE				00
00	ID								87/88
01	REV								00
02	RSTALL	-		MIPIRST	VDEC4 RST	VDEC3 RST	VDEC2 RST	VDEC1 RST	00
03	EXTCLK	LOCK_WTX	LOCK_RDX	AINC	OEN	TRI656	LS_DRV STR	HS_DRV STR	0C
04	-	CK2S		CK1S		-	CLK_DRVST	DNB_REV	00
05	PD_PEX	MPP2_PEX	MPP1_PEX	IRQ_PEX	SADD0_PEX	SADD1_PEX	-		00
06	PDSYSCK	-							00
07	CH_SEL		SEC_CH		PRI_CH		MODE_CH		12
08	PLL_NDIV		PLLM_DIV						1F
09	-	PLL_P1DIV_EN	PLL_P1DIV						43
0A	-	PLL_P2DIV_EN	PLL_P2DIV						4F
0B	-	PLL_P3DIV_EN	PLL_P3DIV						41
0C	MPP1IN	MPP1OE	MPP1POL	MPP1SEL					00
0D	MPP2IN	MPP2OE	MPP2POL	MPP2SEL					00
0E	IRQIN	IRQOE	IRQPOL	IRQSEL					00
10	-			SHDIRQ	CH4IRQ	CH3IRQ	CH2IRQ	CH1IRQ	00
11	-				CH1 VDLOSS	CH1 DET50	CH1 SLOCK	CH1 HVLOCK	00
12	-				CH2 VDLOSS	CH2 DET50	CH2 SLOCK	CH2 HVLOCK	00
13	-				CH3 VDLOSS	CH3 DET50	CH3 SLOCK	CH3 HVLOCK	00
14	-				CH4 VDLOSS	CH4 DET50	CH4 SLOCK	CH4 HVLOCK	00
15	SHT_BAT4	SHT_BAT3	SHT_BAT2	SHT_BAT1	SHT_GND4	SHT_GND3	SHT_GND2	SHT_GND1	00
16	-				CH1IRQ_EN				00
17	-				CH2IRQ_EN				00
18	-				CH3IRQ_EN				00
19	-				CH4IRQ_EN				00
1A	SHTIRQ_EN								00
1B	-				CH1VD LOSS_STS	CH1DET 50_STS	CH1S LOCK_STS	CH1HV LOCK_STS	-
1C	-				CH2VD LOSS_STS	CH2DET 50_STS	CH2S LOCK_STS	CH2HV LOCK_STS	-
1D	-				CH3VD LOSS_STS	CH3DET 50_STS	CH3S LOCK_STS	CH3HV LOCK_STS	-
1E	-				CH4VD LOSS_STS	CH4DET 50_STS	CH4S LOCK_STS	CH4HV LOCK_STS	-
1F	SHT_BAT4_ STS	SHT_BAT3_ STS	SHT_BAT2_ STS	SHT_BAT1_ STS	SHT_GND4_ STS	SHT_GND3_ STS	SHT_GND2_ STS	SHT_GND1_ STS	-
20	-					CLKO_DLY			00

TABLE 6. DECODER REGISTERS (4 PAGES 1, 2, 3, and 4)

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
02	-	FC27	IFSEL		-				48
03	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	-	MONO	DET50	-
04	-	CKHY		-					00
06	-			AGC_EN	-				00
07	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		02
08	VDELAY_LO								12
09	VACTIVE_LO								F0
0A	HDELAY_LO								0F
0B	HACTIVE_LO								D0
0C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CC
0D	-	NTSC656	-						00
10	BRIGHTNESS								00
11	CONTRAST								64
12	SCURVE	VSF	CTI		SHARP				11
13	SAT_U								80
14	SAT_V								80
15	HUE								00
17	SHCOR				-	VSHP			80
18	CTCOR		CCOR		VCOR		CIF		44
1C	DETSTS	STDNOW			ATREG	STANDARD			07
1D	ATSTART	PAL60_EN	PALCN_EN	PALM_EN	NTSC44_EN	SECAM_EN	PALB_EN	NTSC_EN	7F
20	CLPEND				CLPST				50
21	NMGAIN				WPGAIN			AGCGAIN8	22
22	AGCGAIN								F0
23	PEAKWT								D8
24	CLMPLD	CLMPL							BC
25	SYNCTD	SYNCT							B8
26	MISSCNT				HSWIN				44
27	PCLAMP								38
28	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00
29	BSHT			VSHT					00
2A	CKILLMAX		CKILLMIN						78
2B	FCOMB	HTL			VTL1	VTL			44
2C	CKLM	YDLY			HFLT				30
2D	-	EVCNT	-	SDET	TBC_EN	BYPASS	SYOUT	-	14
2E	HPM		ACCT		SPM		CBW		A5
2F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	E0
30	SID_FAIL	PID_FAIL	FSC_FAIL	SLOCK_FAIL	CSBAD	MVCSN	CSTRIPE	CTYPE	-
31	VCR	WKAIR2	WKAIR1	VSTD	NINTL	WSSDET	EDSDET	CCDET	-

TABLE 6. DECODER REGISTERS (4 PAGES 1, 2, 3, and 4) (Continued)

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
32	HFREF/GVAL/PHERRDO/CGAINO/BAMPO/MINAVG/SYTHRD/SYAMP								-
33	FRM		YNR		CLMD		PSP		05
34	INDEX		NSEN/SSEN/PSEN/WKTH						1A
35	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	00
36	AALPF_EN	ADCPD	ACLAMP_EN	DCLAMP_EN	CL_MARGIN	TOGGLE_ MODE	CM_CLAMP_MODE		B0
37	GAIN_SEL		-		PD_BIAS	BIAS_CTRL			06
38	-	DCLAMP_ATTEN			ACLAPM_ATTEN		-		2C
39	-		PASSIVE_ CLAMP	RES_REF	PASSIVE _VREF	PRECON	DIFF	SE	00
3A	-	SHT_THRESH_GND			-	SHT_THRESH_BAT			00
3B	-					SHT_DIAG_PD	SHT_GND_EN	SHT_BAT_EN	04
3C	-					AN_TEST_EN	AN_TEST_SEL		00
3D	DISRSTH	DISRTSV	USE_ DETSTUS	USE_LOCK	USE_VACT_ MOD	Y16	BT7	RGB565	08
3F	INTERNAL_TEST MODE								-
43	-							HDELAY_CTRL	01
44	-						HDELAY2[9:8]		00
45	HDELAY2[7:0]								09

TABLE 7. ACA REGISTERS (4 PAGES 1, 2, 3, and 4)

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
80	ACA_DBG	HIST_WIN_EN	-	ACA_ BYPASS	LPOFF	MLH COMP	MDLTON	ACA_ON	06
81	-		ACA_GAIN						20
82	-		YAVGHLIM						A0
83	-		YAVGLLIM						08
84	-				YMINMAXR				09
85	-			BLKLVL					10
87	-			WHTLVL					00
88	-	MOFSLIM							38
89	-			MOFSSLOPE					10
8A	-		MOFSUPGAIN						1C
8B	-		MOFSDNGAIN						14
8C	-			MDLTCUT					0A
8D	-			MDLTSLOPE					1F
8E	-		YLHAVGDIFF						1A
8F	-			LMAXGRAD					0C
90	-			HMAXGRAD					0C
91	-			LGRADUP					0C
92	-			LGRADDN					08
93	-			HGRADUP					04
94	-			HGRADDN					0C
95	-				LPFCOEFF				04
96	PDF_INDEX						ACA_MASK	READ_EN	00
97	HAVST_HIST								00
98	-							HAVSIZE _HIST_HI	01
99	HAVSIZE_HIST_LO								68
9A	VAVST_HIST								00
9B	-							VAVSIZE _HIST_HI	01
9C	VAVSIZE_HIST_LO								20
A0	YAVG_RAW								-
A1	YAVG_LIM								-
A2	LOW_AVG								-
A3	HIGH_AVG								-
A4	Y_MAX								-
A5	Y_MIN								-
A6	MOFFSET								-
A7	LGRAD								-

TABLE 7. ACA REGISTERS (4 PAGES 1, 2, 3, and 4) (Continued)

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
A8	HGRAD								-
A9	LL_SLOPE								-
AA	LH_SLOPE								-
AB	HL_SLOPE								-
AC	HH_SLOPE								-
AD	X_LOW								-
AE	X_MEAN								-
AF	X_HIGH								-
B0	Y_LOW								-
B1	Y_MEAN								-
B2	Y_HIGH								-
B3	-						DIS_LINE_EN		02
B4	-							DIS_LINE_SP_HI	00
B5	DIS_LIEN_SP_LO								00
C0	MASTER	ACA_H_4x1_EN	-				F_WIN_EN	F_WIN_HIST_EN	00
C1	-						TL_VERTEX_X0[9:8]		00
C2	TL_VERTEX_X0[7:0]								00
C3	-			TL_VERTEX_Y0[8:8]					00
C4	TL_VERTEX_Y0[7:0]								00
C5	-						TR_VERTEX_X1[9:8]		02
C6	TR_VERTEX_X1[7:0]								CF
C7	-							TR_VERTEX_Y1[8:8]	00
C8	TR_VERTEX_Y1[7:0]								00
C9	-						BL_VERTEX_X2[9:8]		00
CA	BL_VERTEX_X2[7:0]								00
CB	-							BL_VERTEX_Y2[8:8]	00
CC	BL_VERTEX_Y2[7:0]								EF
CD	-						BR_VERTEX_X3[9:8]		02
CE	BR_VERTEX_X3[7:0]								CF
CF	-							BR_VERTEX_Y3[8:8]	00
D0	BR_VERTEX_Y3[7:0]								EF
D1	-						LM_VERTEX_X4[9:8]		00
D2	LM_VERTEX_X4[7:0]								00
D3	-							LM_VERTEX_Y4[8:8]	00
D4	LM_VERTEX_Y4[7:0]								77

TABLE 7. ACA REGISTERS (4 PAGES 1, 2, 3, and 4) (Continued)

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
D5	-						TM _VERTEX_X5[9:8]		00
D6	TM _VERTEX_X5[7:0]								00
D7	-							TM_VERTEX_Y5[8:8]	00
D8	TM _VERTEX_Y5[7:0]								00
D9	-						BM_VERTEX_X6[9:8]		01
DA	BM_VERTEX_X6[7:0]								67
DB	-							BM_VERTEX_Y6[8:8]	00
DC	BM_VERTEX_Y6[7:0]								EF
DD	-						RM_VERTEX_X7[9:8]		02
DE	RM_VERTEX_X7[7:0]								CF
DF	-							RM_VERTEX_Y7[8:8]	00
E0	RM_VERTEX_Y7[7:0]								77
E1	HISTORAM_DAT[7:0]								-
E2	HISTORAM_DAT[15:8]								-
E3	-					HISTORAM_DAT[18:16]			-
E4	F_WIN_COLOR_Y								19
E5	F_WIN_COLOR_CB								BD
E6	F_WIN_COLOR_CR								50
E7								TRAN_HISTO_EN	00

TABLE 8. LINE INTERLEAVE ENGINE REGISTERS (PAGE 5)

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
00	PD_MIPI	TMLS_MIPI	TMHS_MIPI	-		LANE_NO			82
01	LNINC1	SWAP_CRC	FRAME_MODE	PIC_WIDTH[12:8]					85
02	PIC_WIDTH[7:0]								A0
03	SWAP_YC	HS_DPHY_TEST	-	RST_FIFO	TOP_ONLY	-			18
04	VC4		VC3		VC2		VC1		E4
05	-	ON_CTRL	SDPROG	RGB565	-	SAV_NORMAL	656_BYTE	-	40
06	FE_FS_ADJ	FIX_LNOUT	8BHDR	VSTABLE	SAMEVC	TYPE30	-	NON_STD_VID	01
07	RD_START								2B
08	-				PF_VB_START	-	DATA2CLK	PF_FLD	00
09	-			8010	-		1FD_TOP	1FD_BOT	00
0A	INT_CTR								00
0B	GEN_BAR_PAT		-	NCNT					00
0C	PCNT								00

TABLE 8. LINE INTERLEAVE ENGINE REGISTERS (PAGE 5) (Continued)

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
0D	INT_PAT1	INT_PAT2	INT_PAT3	INT_PAT4	GEN_COLOR		FORCE_FRM	ADD_VBLK	00
0E	VB_COUNT								6C
0F	GEN_FLDPOL	GEN_NOVID	ULPS_FSYNC	-	HSCK_ ALWAYS_ON	GEN_PAL	ESC_TEST	ESC_GO	00
10	WORD_COUNT[15:8]								05
11	WORD_COUNT[7:0]								A0
12	LPX_CNT				HS_PREPARE				76
13	HS_ZERO								17
14	HS_TRAIL								0E
15	CLK_TO_DATA								36
16	CLK_POST								12
17	MARK_WAIT								F6
18	-	FORCE_ULPS	ESC_EXIT	LPDT_MODE	RST_MODE	-	ESC_MODE	-	00
19	WAIT_FRAMES								03
1A	EOT_PERIOD								0A
1B	CLK_PREPARE				CLK_PRE				61
1C	LP11_CNT				CLK_TRAIL				7A
1D	CLK_ZERO								0F
1E	SHORT_PKT_DLY				CLK_SOT_CNT				8C
1F	ULPS_LP11_CNT								06
20	PRBS_ER_ RSTB	ATG_RESYNC	-	TESTSET0	ATG_INV8	PRBS_SEL	HSTEST_SEL	ATEST_EN	00
21	ESC_DELAY								0C
22	PRBS_ERR_ DET	-							-
23					CLK_TRAIL_SHORT_PKT				0A
24	-					INPUT_PIC_HEIGHT[10:8]			-
25	IN_PIC_HEIGHT[7:0]								-
26	HS_TRAIL_SPKT								07
28	-					FIFO_THRESHOLD[10:8]			01
29	FIFO_THRESHOLD								0E
2A	RANDOM_SYNC4				RANDOM_SYNC3				00
2B	RANDOM_SYNC2				RANDOM_SYNC1				00
2C	-					FE_BOTTOM[10:8]			01
2D	FE_BOTTOM[7:0]								04
2E	-					FE_TOP[10:8]			01
2F	FE_TOP[7:0]								05
30	CTRL_BIT_DATA1								00
31	CTRL_BIT_DATA2								00
32	CTRL_BIT_CLK								00

TABLE 8. LINE INTERLEAVE ENGINE REGISTERS (PAGE 5) (Continued)

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
33	PLL_ITUNE								00
34	PLL_RON	PLL_LOWF	PLL_RST_OFF	PLL_RSTB	PLL_DPHY_RSTB	PWD_BG	PLL_PWD	-	06
35	-				PWD_DATA			PWD_CLK	07
36	-						CK_POL	PLL_TEST_EN	00
38	TOTAL_PFLINE[15:8]								03
39	TOTAL_PFLINE[7:0]								C0
3A	-			HLINE_CNT[12:8]					06
3B	HLINE_CNT								B3
3C	-					HIST_LINE[10:8]			00
3D	HIST_LINE								F1

ISL79987 and ISL79988 Register Detail

BIT	FUNCTION	R/W	DESCRIPTION	RESET
Common Registers - Page 0				
REG 0XFF – PAGE REGISTER				
7-4	RESERVED	R/W	Reserved	0
3-0	PAGE	R/W	Select the register page to be accessed 0 – Page 0 Common Register 1 – Page 1 Decoder 1 Register 2 – Page 2 Decoder 2 Register 3 – Page 3 Decoder 3 Register 4 – Page 4 Decoder 4 Register 5 – Page 5 MIPI Register F – Select Page 1/2/3/4 for register Write access. Not valid in read time.	
REG 0X00 – PRODUCT ID CODE REGISTER (ID)				
7-0	ID	R	Product ID code	87/88
REG 0X01 – PRODUCT REVISION CODE REGISTER (ID)				
7-0	REV	R	Revision number	00
REG 0X02 – SOFTWARE RESET CONTROL REGISTER				
7	RSTALL	R/W	Self cleared soft reset.	0
6-5	RESERVED	R/W	Reserved	0
4	MIPIRST	R/W	A '1' written into this bit resets the MIPI control logic to its default state, but all register contents remain unchanged. Write 0 to exit the reset state.	0
3	VDEC4RST	R/W	A '1' written into this bit resets the Video Decoder 4 control logic to its default state, but all register contents remain unchanged. Write 0 to exit the reset state.	0
2	VDEC3RST	R/W	A '1' written into this bit resets the Video Decoder 3 control logic to its default state, but all register contents remain unchanged. Write 0 to exit the reset state.	0
1	VDEC2RST	R/W	A '1' written into this bit resets the Video Decoder 2 control logic to its default state, but all register contents remain unchanged. Write 0 to exit the reset state.	0
0	VDEC1RST	R/W	A '1' written into this bit resets the Video Decoder 1 control logic to its default state, but all register contents remain unchanged. Write 0 to exit the reset state.	0
REG 0X03 – IO BUFFER CONTROL				
7	EXTCLK	R/W	Test mode only replacing mux_clk and lps_clk with external clock source from SADD0.	0
6	LOCK_WTX	R/W	Serial interface multi-byte write lock function 1 = Disable (no lock, each byte takes effect after written) 0 = Enable	0
5	LOCK_RDX	R/W	Serial interface multi-byte read lock function 1 = Disable 0 = Enable	0
4	AINC	R/W	Serial interface auto-indexing control 1 = Non-auto 0 = Auto-increment	0
3	OEN	R/W	Tri-State all digital signal outputs 0 = Release overall tri-state, output enable depends on each signal pin's tri-state control 1 = Tri-State	1
2	TRI656	R/W	Tri-State the VD bus and VDCLK	1
1	LS_DRVSTR	R/W	Digital output buffer driver strength selection for low-speed buffers 0 = 4mA 1 = 8mA	0
0	HS_DRVSTR	R/W	Digital output buffer driver strength selection for high-speed buffers 0 = 4mA 1 = 8mA	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X04 – IO BUFFER CONTROL 1				
7	RESERVED	R/W	Reserved	0
6-5	CK2S	R/W	Clock multpixer control on CLKO pad 0 = Line interleaving clock 1 = AFE clock output 2 = CLK27/2 clock 3 = CLK27/4 clock	0
4-3	CK1S	R/W	Clock polarity control on CLKO pad CK1S[0] – 0 = Clock selected by CK2S 1 = Inverted version CK1S[1] - Reserved	0
2	RESERVED	R/W	Reserved	0
1	CLK_DRVST	R/W	Digital output buffer driver strength selection for clock output pad (BT.656) 0 = 4mA 1 = 8mA	0
0	DNB_REV	R/W	Test mode output data reversal of MSB and LSB during clock high and low periods.	0
REG 0X05 – IO PAD PULL ENABLE CONTROL				
7	PD_PEX	R/W	PD pin pull enable control. 0 = Enable 1 = Disable	0
6	MPP2_PEX	R/W	CLKO_MPP2 pin pull enable control. 0 = Enable 1 = Disable	0
5	MPP1_PEX	R/W	MPP1 pin pull enable control. 0 = Enable 1 = Disable	0
4	IRQ_PEX	R/W	IRQ pin pull enable control. 0 = Enable 1 = Disable	0
3	SADD0_PEX	R/W	SADD0 pin pull enable control. 0 = Enable 1 = Disable	0
2	SADD1_PEX	R/W	SADD1 pin pull enable control. 0 = Enable 1 = Disable	0
1-0	RESERVED	R/W	Reserved	0
REG 0X06 – IO BUFFER CONTROL 1				
7	PDSYSCK	R/W	Power-down (or stop) the 27MHZ clock to all modules except I^2C.	0
6-0	RESERVED	R/W	Reserved	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X07 – VIDEO INPUT CHANNEL CONTROL				
7-6	CH_SEL	R/W	Selects which channel outputs are selected on to the SYNC outputs 0 = Channel 1 1 = Channel 2 2 = Channel 3 3 = Channel 4	0
5-4	SEC_CH	R/W	Selection of the video channel as a second channel for two-channel configuration 0 = Video Channel 1 1 = Video Channel 2 2 = Video Channel 3 3 = Video Channel 4	1
3-2	PRI_CH	R/W	Selection of the video channel as a primary channel for one/two-channel configuration 0 = Video Channel 1 1 = Video Channel 2 2 = Video Channel 3 3 = Video Channel 4	0
1-0	MODE_CH	R/W	Video input channel mode 0 = 1 Channel Mode 1 = 2 Channel Mode 2 = 4 Channel Mode 3 = Reserved	2
REG 0X08 – CLOCK CONTROL 1				
7-6	PLL_NDIV	R/W	Input clock divider. Always has to be zero for this part.	0
5-0	PLL_MDIV	R/W	VCO clock frequency feedback divider. Divided by value (PLL_MDIV+1)	1F
REG 0X09 – CLOCK CONTROL 2				
7	RESERVED	R/W	Reserved	0
6	PLL_P1DIV_EN	R/W	Output divider P1 enable 0 = Disabled (no clock output) 1 = Enabled	1
5-0	PLL_P1DIV	R/W	PLL P1 output divider value. Control the MUX clock/line interleave clock. 0 = Divide by 1 1 = Divide by 2 2 = Divide by 4 3 to 63 = Divide (2*(PLL_P1DIV+1))	03
REG 0X0A – CLOCK CONTROL 3				
7	RESERVED	R/W	Reserved	0
6	PLL_P2DIV_EN	R/W	Output divider P2 enable 0 = Disabled (no clock output) 1 = Enabled	1
5-0	PLL_P2DIV	R/W	PLL P2 output divider value. Controls the video clock for future use (can be reserved for ISL79987) 0 = Divide by 1 1 = Divide by 2 2 = Divide by 4 3 to 63 = Divide (2*(PLL_P2DIV+1))	0F

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X0B – CLOCK CONTROL 4				
7	RESERVED	R/W	Reserved	0
6	PLL_P3DIV_EN	R/W	Output divider P3 enable 0 = Disabled (no clock output) 1 = Enabled	1
5-0	PLL_P3DIV	R/W	PLL P3 output divider value. Controls the MIPI TX Clock. 0 = Divide by 1 1 = Divide by 2 2 = Divide by 4 3-63 = Divide (2*(PLL_P3DIV+1))	01
REG 0X0C – MPP1 SYNC CONTROL				
7	MPP1IN	R	MPP1 input data	0
6	MPP1OE	R/W	MPP1 output enable 0 = Disable 1 = Output Enable	0
5	MPP1POL	R/W	MPP1 output polarity 0 = Normal 1 = Inverted	0
4-0	MPP1SEL	R/W	Selects one of the below signals to MPP1. The channel is defined by CH_SEL. 0x00 = 0 0x01 = 1 0x02 = CHx_HSYNC 0x03 = CHX_HACT 0x04 = CHX_HLOCK 0x05 = CHX_ASYNCW 0x06 = CHX_CLMP_UP 0x07 = CHX_PKSYNC 0x08 = CHX_SAV 0x09 = CHX_VSYNC 0x0A = CHX_VACT 0x0B = CHX_VBURST 0x0C = CHX_CLMP_DN 0x0D = CHX_DR 0x0E = CHX_VLOCK 0x0F = CHX_FLD 0x10 = CHX_VDLOSS 0x11 = CHX_SLOCK 0x12 = CHX_MONO 0x13 = CHX_DET50 0x14 = CHX_RTCOUT 0x15 = CHX_BPG 0x16 = CHX_VDET 0x17 = CHX_CGATE 0x18 = CHX_DQSYNC 0x19 = CHX_MCVSN 0x1A = CHX_ACT_VIDEO	00

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X0D – MPP2 SYNC CONTROL (DURING MIPI MODE ONLY)				
7	MPP2IN	R	MPP2 input data	0
6	MPP2OE	R/W	MPP2 output enable 0 = Disable 1 = Output Enable	0
5	MPP2POL	R/W	MPP2 output polarity 0 = Normal 1 = Inverted	0
4-0	MPP2SEL	R/W	Selects one of the below signals to MPP2. The channel is defined by CH_SEL. 0x00 = CLKOUT 0x01 = 1 0x02 = CHx_HSYNC 0x03 = CHX_HACT 0x04 = CHX_HLOCK 0x05 = CHX_ASYNCW 0x06 = CHX_CLMP_UP 0x07 = CHX_PKSYNC 0x08 = CHX_SAV 0x09 = CHX_VSYNC 0x0A = CHX_VACT 0x0B = CHX_VBURST 0x0C = CHX_CLMP_DN 0x0D = CHX_DR 0x0E = CHX_VLOCK 0x0F = CHX_FLD 0x10 = CHX_VDLOSS 0x11 = CHX_SLOCK 0x12 = CHX_MONO 0x13 = CHX_DET50 0x14 = CHX_RTCOUT 0x15 = CHX_BPG 0x16 = CHX_VDET 0x17 = CHX_CGATE 0x18 = CHX_DQSYNC 0x19 = CHX_MCVSN 0x1A = CHX_ACT_VIDEO	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X0E – IRQ SYNC CONTROL				
7	IRQIN	R	IRQ input data	0
6	IRQOE	R/W	IRQ output enable 0 = Disable 1 = Output Enable	0
5	IRQPOL	R/W	IRQ output polarity 0 = Normal 1 = Inverted	0
4-0	IRQSEL	R/W	Selects one of the below signals to IRQ. The channel is defined by CH_SEL. 0x00 = IRQOUT 0x01 = 1 0x02 = CHx_HSYNC 0x03 = CHX_HACT 0x04 = CHX_HLOCK 0x05 = CHX_ASYNCW 0x06 = CHX_CLMP_UP 0x07 = CHX_PKSYNC 0x08 = CHX_SAV 0x09 = CHX_VSYNC 0x0A = CHX_VACT 0x0B = CHX_VBURST 0x0C = CHX_CLMP_DN 0x0D = CHX_DR 0x0E = CHX_VLOCK 0x0F = CHX_FLD 0x10 = CHX_VDLOSS 0x11 = CHX_SLOCK 0x12 = CHX_MONO 0x13 = CHX_DET50 0x14 = CHX_RTCOUT 0x15 = CHX_BPG 0x16 = CHX_VDET 0x17 = CHX_CGATE 0x18 = CHX_DQSYNC 0x19 = CHX_MCVSN 0x1A = CHX_ACT_VIDEO	0
REG 0X10 – DEVICE INTERRUPT STATUS REGISTER				
7-5	RESERVED	R	Reserved	0
4	SHDIRQ	R	Indicates that short diagnostic interrupt is asserted.	0
3	CH4IRQ	R	Indicates that Channel 4 video interrupt is asserted.	0
2	CH3IRQ	R	Indicates that Channel 3 video interrupt is asserted.	0
1	CH2IRQ	R	Indicates that Channel 2 video interrupt is asserted.	0
0	CH1IRQ	R	Indicates that Channel 1 video interrupt is asserted.	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X11 – CHANNEL 1 IRQ REGISTER				
7-4	RESERVED	R/W	Reserved	0
3	CH1VDLOSS	R/W	VDLOSS status change interrupt. Write '1' to clear the active status.	0
2	CH1DET50	R/W	DET50 detection status change interrupt. Write '1' to clear the active status.	0
1	CH1SLOCK	R/W	SLOCK status change interrupt. Write '1' to clear the active status.	0
0	CH1HVLOCK	R/W	HLOCK/VLOCK status change interrupt. Write '1' to clear the active status.	0
REG 0X12 – CHANNEL 2 IRQ REGISTER				
7-4	RESERVED	R/W	Reserved	0
3	CH2VDLOSS	R/W	VDLOSS status change interrupt. Write '1' to clear the active status.	0
2	CH2DET50	R/W	DET50 detection status change interrupt. Write '1' to clear the active status.	0
1	CH2SLOCK	R/W	SLOCK status change interrupt. Write '1' to clear the active status.	0
0	CH2HVLOCK	R/W	HLOCK/VLOCK status change interrupt. Write '1' to clear the active status.	0
REG 0X13 – CHANNEL 3 IRQ REGISTER				
7-4	RESERVED	R/W	Reserved	0
3	CH3VDLOSS	R/W	VDLOSS status change interrupt. Write '1' to clear the active status.	0
2	CH3DET50	R/W	DET50 detection status change interrupt. Write '1' to clear the active status.	0
1	CH3SLOCK	R/W	SLOCK status change interrupt. Write '1' to clear the active status.	0
0	CH3HVLOCK	R/W	HLOCK/VLOCK status change interrupt. Write '1' to clear the active status.	0
REG 0X14 – CHANNEL 4 IRQ REGISTER				
7-4	RESERVED	R/W	Reserved	0
3	CH4VDLOSS	R/W	VDLOSS status change interrupt. Write '1' to clear the active status.	0
2	CH4DET50	R/W	DET50 detection status change interrupt. Write '1' to clear the active status.	0
1	CH4SLOCK	R/W	SLOCK status change interrupt. Write '1' to clear the active status.	0
0	CH4HVLOCK	R/W	HLOCK/VLOCK status change interrupt. Write '1' to clear the active status.	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X15 – SHORT DIAGNOSTIC IRQ REGISTER				
7	SHT_BAT4	R/W	Short-to-battery interrupt (DIAG4). Write '1' to clear the active status.	0
6	SHT_BAT3	R/W	Short-to-battery interrupt (DIAG3). Write '1' to clear the active status.	0
5	SHT_BAT2	R/W	Short-to- battery interrupt (DIAG2). Write '1' to clear the active status.	0
4	SHT_BAT1	R/W	Short-to-battery interrupt (DIAG1). Write '1' to clear the active status.	0
3	SHT_GND4	R/W	Short-to-ground interrupt (DIAG4). Write '1' to clear the active status.	0
2	SHT_GND3	R/W	Short-to- ground interrupt (DIAG3). Write '1' to clear the active status.	0
1	SHT_GND2	R/W	Short-to-ground interrupt (DIAG2). Write '1' to clear the active status.	0
0	SHT_GND1	R/W	Short-to-ground interrupt (DIAG1). Write '1' to clear the active status.	0
REG 0X16 – CHANNEL 1 IRQ ENABLE				
7-4	RESERVED	R/W	Reserved	0
3-0	CH1IRQ_EN	R/W	CH1 IRQ enable register. A '0' for any bit disables the interrupt for that specific bit.	0
REG 0X17 – CHANNEL 2 IRQ ENABLE				
7-4	RESERVED	R/W	Reserved	0
3-0	CH2IRQ_EN	R/W	CH2 IRQ enable REGISTER. A '0' for any bit disables the interrupt for that specific bit.	0
REG 0X18 – CHANNEL 3 IRQ ENABLE				
7-4	RESERVED	R/W	Reserved	0
3-0	CH3IRQ_EN	R/W	CH3 IRQ enable REGISTER. A '0' for any bit disables the interrupt for that specific bit.	0
REG 0X19 – CHANNEL 4 IRQ ENABLE				
7-4	RESERVED	R/W	Reserved	0
3-0	CH4IRQ_EN	R/W	CH4 IRQ enable REGISTER. A '0' for any bit disables the interrupt for that specific bit.	0
REG 0X1A – SHORT DIAGNOSTIC IRQ ENABLE				
7-0	SHTIRQ_EN	R/W	IRQ enable for Short Diagnostic. A '0' for any bit disables the interrupt for that specific bit.	00
REG 0X1B – CHANNEL 1 STATUS REGISTER				
7-4	RESERVED	R	Reserved	-
3	CH1VDLOSS_STS	R	VDLOSS status	-
2	CH1DET50_STS	R	DET50 detection status	-
1	CH1SLOCK_STS	R	SLOCK status	-
0	CH1HVLOCK_STS	R	HLOCK/VLOCK status	-

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X1C – CHANNEL 2 STATUS REGISTER				
7-4	RESERVED	R	Reserved	-
3	CH2VDLOSS_STS	R	VDLOSS status	-
2	CH2DET50_STS	R	DET50 detection status	-
1	CH2SLOCK_STS	R	SLOCK status	-
0	CH2HVLOCK_STS	R	HLOCK/VLOCK status	-
7-4	RESERVED	R	Reserved	-
REG 0X1D – CHANNEL 3 STATUS REGISTER				
7-4	RESERVED	R	Reserved	-
3	CH3VDLOSS_STS	R	VDLOSS status	-
2	CH3DET50_STS	R	DET50 detection status	-
1	CH3SLOCK_STS	R	SLOCK status	-
0	CH3HVLOCK_STS	R	HLOCK/VLOCK status	-
REG 0X1E – CHANNEL 4 STATUS REGISTER				
7-4	RESERVED	R	Reserved	-
3	CH4VDLOSS_STS	R	VDLOSS status	-
2	CH4DET50_STS	R	DET50 detection status	-
1	CH4SLOCK_STS	R	SLOCK status	-
0	CH4HVLOCK_STS	R	HLOCK/VLOCK status	-
REG 0X1F– SHORT DIAGNOSTIC STATUS REGISTER				
7	SHT_BAT4_STS	R	Short-to-battery status (DIAG4).	-
6	SHT_BAT3_STS	R	Short-to-battery status (DIAG3).	-
5	SHT_BAT2_STS	R	Short-to- battery status (DIAG2).	-
4	SHT_BAT1_STS	R	Short-to-battery status (DIAG1).	-
3	SHT_GND4_STS	R	Short-to-ground status (DIAG4).	-
2	SHT_GND3_STS	R	Short-to-ground status (DIAG3).	-
1	SHT_GND2_STS	R	Short-to-ground status (DIAG2).	-
0	SHT_GND1_STS	R	Short-to-ground status (DIAG1).	-
REG 0X20 – CLOCK DELAY REGISTER				
7-3	RESERVED	R/W	Reserved	0
2-0	CLKO_DLY	R/W	CLKO delay selection. 1nS per step	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
Decoder Registers - Page 1, 2, 3, and 4 for Four Decoders				
REG 0X02 – INPUT FORMAT (INFORM)				
7	RESERVED	R/W	Reserved	0
6	FC27	R/W	0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source 1 = Input crystal clock frequency is 27MHz	1
5-4	IFSEL	R/W	0 = Composite video decoding Others = N/A	0
3-0	RESERVED	R/W	Reserved	8
REG 0X03 – DECODER STATUS REGISTER I (STATUS1)				
7	VDLOSS	R	0 = Video detected 1 = Video not present. (Sync is not detected in number of line periods specified by MISSCNT register)	-
6	HLOCK	R	0 = Horizontal sync PLL is not locked 1 = Horizontal sync PLL is locked to the incoming video source	-
5	SLOCK	R	0 = Subcarrier PLL is not locked 1 = Subcarrier PLL is locked to the incoming video source	-
4	FIELD	R	0 = Even field is being decoded 1 = Odd field is being decoded	-
3	VLOCK	R	0 = Vertical logic is not locked 1 = Vertical logic is locked to the incoming video source	-
2	RESERVED	R	Reserved	-
1	MONO	R	0 = Color burst signal detected 1 = No color burst signal detected	-
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual output vertical scanning frequency depends on the current standard invoked.	-
REG 0X04 – HSYNC DELAY CONTROL				
7	RESERVED	R/W	Reserved	-
6-5	CKHY	R/W	Color killer time constant 0 = Fastest 3 = Slowest	0
4-0	RESERVED	R/W	Reserved	-
REG 0X06 – ANALOG CONTROL REGISTER (ACNTL)				
7-5	RESERVED	R/W	Reserved	-
4	AGC_EN	R/W	0 = AGC loop function enabled 1 = AGC loop function disabled. Gain is set by AGCGAIN.	0
3-0	RESERVED	R/W	Reserved	-
REG 0X07 – CROPPING REGISTER, HIGH (CROP_HI)				
7-6	VDELAY_HI	R/W	Bit[9:8] of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	Bit[9:8] of the 10-bit VACTIVE register. See the reg0x1C[3] description on page 46 for its shadow register.	0
3-2	HDELAY_HI	R/W	Bit[9:8] of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	Bit[9:8] of the 10-bit HACTIVE register.	2

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X08 – VERTICAL DELAY REGISTER, LOW (VDELAY_LO)				
7-0	VDELAY_LO	R/W	Bit[7:0] of the 10-bit Vertical Delay register. It defines the number of lines between the leading edge of VSYNC and the start of the active video. The two MSBs are in the CROP_HI register.	12
REG 0X09 – VERTICAL ACTIVE REGISTER, LOW (VACTIVE_LO)				
7-0	VACTIVE_LO	R/W	Bit[7:0] of the 10-bit Vertical Active register. It defines the number of active video lines per frame output. The two MSBs are in the CROP_HI register. The VACTIVE register has a shadow register for use with a 50Hz source when Atreg of Reg0x11C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0
REG 0X0A – HORIZONTAL DELAY REGISTER, LOW (HDELAY_LO)				
7-0	HDELAY_LO	R/W	Bit[7:0] of the 10-bit Horizontal Delay register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The two MSBs are in the CROP_HI register. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. This register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0F
REG 0X0B – HORIZONTAL ACTIVE REGISTER, LOW (HACTIVE_LO)				
7-0	HACTIVE_LO	R/W	Bit[7:0] of the 10-bit Horizontal Active register. It defines the number of active pixels per line output. The two MSBs are in the CROP_HI register.	D0
REG 0X0C – CONTROL REGISTER I (CNTRL1)				
7	PBW	R/W	Combined with VTL[3], there are four different chroma bandwidths that can be selected. 0 = Normal Chroma BPF BW 1 = Wide Chroma BPF BW	1
6	DEM	R/W	Color killer sensitivity 0 = High 1 = Low	1
5	PALSW	R/W	0 = PAL switch sensitivity normal 1 = PAL switch sensitivity low	0
4	SET7	R/W	0 = The black level is the same as the blank level 1 = The black level is 7.5 IRE above the blank level	0
3	COMB	R/W	0 = Notch filter 1 = Adaptive comb filter on for NTSC/PAL	1
2	HCOMP	R/W	0 = Operation mode 0 1 = Operation mode 1 (recommended)	1
1	YCOMP	R/W	Controls the comb operation when there is no color burst. 0 = Comb 1 = No comb	0
0	PDLY	R/W	PAL delay line 0 = Enable 1 = Disable	0
REG 0X0D – CSC CONTROL				
7	RESERVED	R/W	Reserved	-
6	NTSC656	R/W	1 = Number of even field video output line is “the number of odd field video output line - 1." This bit is required for ITU-R BT.656 output for 525 line system standard. 0 = Number of even field video output line is same as the number of odd field video output line.	0
5-0	RESERVED	R/W	Reserved	-
REG 0X10 – BRIGHTNESS CONTROL REGISTER (BRIGHT)				
7-0	BRIGHTNESS	R/W	Controls the brightness. These bits have a value of –128 to 127 in 2’s complement form. A positive value increases brightness. A value of 0 has no effect on the data.	00

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X11 – CONTRAST CONTROL REGISTER (CONTRAST)				
7-0	CONTRAST	R/W	Controls the contrast. These bits have value of 0 to 3.98 (FFh). A value of 100 (64h) yields a gain of 100%. The gain ranges from 0 to 255%.	64
REG 0X12 – SHARPNESS CONTROL REGISTER I (SHARPNESS)				
7	SCURVE	R/W	Controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = Low 1 = Center	0
6	VSF	R/W	For internal use only	0
5-4	CTI	R/W	Color transient improvement level control. There are four enhancement levels. 0 is the lowest and 3 is the highest.	1
3-0	SHARP	R/W	Controls the amount of sharpness enhancement on the luminance signals. There are 16 levels of control. ‘0’ has no effect on the output image and ‘15’ has the strongest effect.	1
REG 0X13 – CHROMA (U) GAIN REGISTER (SAT_U)				
7-0	SAT_U	R/W	Controls the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80
REG 0X14 – CHROMA (V) GAIN REGISTER (SAT_V)				
7-0	SAT_V	R/W	Controls the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80
REG 0X15 – HUE CONTROL REGISTER (HUE)				
7-0	HUE	R/W	Controls the color hue. The value is in 2’s complement form with 0 as the center value. A positive value results in red hue and a negative value gives green hue.	00
REG 0X17 – VERTICAL PEAKING CONTROL I				
7-4	SHCOR	R/W	Provides coring function for the sharpness control.	8
3	RESERVED	R/W	Reserved	-
2-0	VSHP	R/W	Vertical peaking gain control	0
REG 0X18 – CORING CONTROL REGISTER (CORING)				
7-6	CTCOR	R/W	Controls the coring function for the CTI. It has an internal step size of 2.	1
5-4	CCOR	R/W	Controls the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	Controls the coring function of the vertical peaking logic. It has an internal step size of 2.	1
1-0	CIF	R/W	Controls the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X1C – STANDARD SELECTION (SDT)				
7	DETSTS	R	0 = Idle 1 = Detection in progress	-
6-4	STDNOW	R	Current standard invoked 0 = NTSC (M) 1 = PAL (B, D, G, H, I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = N/A	-
3	ATREG	R/W	1 = Disable the shadow registers 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STANDARD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B, D, G, H, I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7
REG 0X1D – STANDARD RECOGNITION (SDTR)				
7	ATSTART	R/W	Writing 1 to this self-resetting bit manually initiates the auto format detection process.	0
6	PAL60_EN	R/W	1 = Enable recognition of PAL60 0 = Disable recognition	1
5	PALCN_EN	R/W	1 = Enable recognition of PAL (CN) 0 = Disable recognition	1
4	PALM_EN	R/W	1 = Enable recognition of PAL (M) 0 = Disable recognition	1
3	NTSC44_EN	R/W	1 = Enable recognition of NTSC 4.43 0 = Disable recognition	1
2	SECAM_EN	R/W	1 = Enable recognition of SECAM 0 = Disable recognition	1
1	PALB_EN	R/W	1 = Enable recognition of PAL (B, D, G, H, I) 0 = Disable recognition	1
0	NTSC_EN	R/W	1 = Enable recognition of NTSC (M) 0 = Disable recognition	1
REG 0X20 – CLAMPING GAIN (CLMPG)				
7-4	CLPEND	R/W	Sets the end time of the clamping pulse in the increment of eight system clocks. The clamping time is determined by this setting together with CLPST.	5
3-0	CLPST	R/W	Sets the start time of the clamping pulse in the increment of eight system clocks. It is referenced to the PCLAMP position.	0
REG 0X21 – INDIVIDUAL AGC GAIN (IAGC)				
7-4	NMGAIN	R/W	Controls the normal AGC loop maximum correction value.	2
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN8	R/W	The MSB of the 9-bit register that controls the AGC gain when the AGC loop is disabled.	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X22 – AGC GAIN (AGCGAIN)				
7-0	AGCGAIN	R/W	The lower eight bits of the 9-bit register that controls the AGC gain when the AGC loop is disabled.	F0
REG 0X23 – WHITE PEAK THRESHOLD (PEAKWT)				
7-0	PEAKWT	R/W	Controls the white peak detection threshold.	D8
REG 0X24– CLAMP LEVEL (CLMPL)				
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL 1 = Clamping level preset at 60d	1
6-0	CLMPL	R/W	Determines the clamping level of the Y-channel	3C
REG 0X25– SYNC AMPLITUDE (SYNCT)				
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT 1 = Reference sync amplitude is preset to 38h	1
6-0	SYNCT	R/W	Determines the standard sync pulse amplitude for AGC reference.	38
REG 0X26 – SYNC MISS COUNT REGISTER (MISSCNT)				
7-4	MISSCNT	R/W	Sets the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	Sets the size for the horizontal sync detection window.	4
REG 0X27 – CLAMP POSITION REGISTER (PCLAMP)				
7-0	PCLAMP	R/W	Sets the clamping position from the PLL sync edge.	38
REG 0X28 – VERTICAL CONTROL I				
7-6	VLCKI	R/W	Vertical lock in time 0 = Fastest 3 = Slowest	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = Fastest 3 = Slowest	0
3	VMODE	R/W	Vertical detection window 0 = Vertical count down mode 1 = Search mode	0
2	DETV	R/W	0 = Normal VSYNC logic 1 = Recommended for special application only	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 0 = Short 1 = Normal	0
REG 0X29 – VERTICAL CONTROL II				
7-5	BSHT	R/W	Burst PLL center frequency control	0
4-0	VSHT	R/W	VSYNC output delay control in the increment of half line length	0
REG 0X2A – COLOR KILLER LEVEL CONTROL				
7-6	CKILMAX	R/W	Controls the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	Controls the color killer threshold. Larger values give lower killer levels.	38

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X2B – COMB FILTER CONTROL				
7	FCOMB	R/W	0 = Adaptive comb 1 = Non-adaptive comb	0
6-4	HTL	R/W	Adaptive comb filter control (factory use only)	4
3	VTL1	R/W	Comb filter bandwidth control	0
2-0	VTL	R/W	Adaptive comb filter threshold control (factory use only)	4
REG 0X2C – LUMA DELAY AND HFILTER CONTROL				
7	CKLM	R/W	Color killer mode. 0 = Normal 1 = Fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. The 2's complement number provides –4 to +3 unit delay control.	3
3-0	HFLT	R/W	Peaking control 2. The peaking curve is controlled by the SCURVE bit.	0
REG 0X2D – MISCELLANEOUS CONTROL REGISTER I (MISC1)				
7	RESERVED	R/W	Reserved	-
6	EVCNT	R/W	0 = Normal operation 1 = Even field counter in special mode	0
5	RESERVED	R/W	Reserved	-
4	SDET	R/W	ID detection sensitivity. '1' is recommended.	1
3	TBC_EN	R/W	0 = TBC off 1 = Internal TBC enabled (test purpose only)	0
2	BYPASS	R/W	Controls the standard detection and should be set to '1' in normal use	1
1	SYOUT	R/W	0 = HSYNC is always generated 1 = HSYNC is disabled when video loss is detected	0
0	RESERVED	R/W	Reserved	-
REG 0X2E – MISCELLANEOUS CONTROL REGISTER II (MISC2)				
7-6	HPM	R/W	Horizontal PLL acquisition time 0 = Slow 1 = Medium 2 = Auto 3 = Fast	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = Slow 2 = Medium 3 = Fast	2
3-2	SPM	R/W	Burst PLL control 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control 0 = Low 1 = Medium 2 = High 3 = NA	1

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X2F – MISCELLANEOUS CONTROL III (MISC3)				
7	NKILL	R/W	0 = Disable 1 = Enable noisy signal color killer function in NTSC mode	1
6	PKILL	R/W	0 = Disable 1 = Enable automatic noisy color killer function in PAL mode	1
5	SKILL	R/W	0 = Disable 1 = Enable automatic noisy color killer function in SECAM mode	1
4	CBAL	R/W	1 = Special output mode 0 = Normal output	0
3	FCS	R/W	0 = Disable 1 = Force decoder output value determined by CCS	0
2	LCS	R/W	0 = Disable 1 = Enable per-determined output value indicated by CCS when video loss is detected	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two display colors can be selected. 0 = Black 1 = Blue color	0
0	BST	R/W	0 = Disable 1 = Enable blue stretch	0
REG 0X30 – MACROVISION DETECTION (MVSN)				
7	SID_FAIL	R	SECAM ID detection failed	-
6	PID_FAIL	R	PAL ID detection failed	-
5	FSC_FAIL	R	FSC frequency detection failed	-
4	SLOCK_FAIL	R	Subcarrier lock detection failed	-
3	CSBAD	R	Macrovision color stripe detection may be unreliable	-
2	MVCSN	R	0 = Not detected 1 = Macrovision AGC pulse detected	-
1	CSTRIPE	R	0 = Not detected 1 = Macrovision color stripe protection burst detected	-
0	CTYPE	R	This bit is valid only when color stripe protection is detected, that is, Cstripe = 1 0 = Type 3 color stripe protection 1 = Type 2 color stripe protection	-
REG 0X31 – CHIP STATUS II (CSTATUS2)				
7	VCR	R	VCR signal indicator	-
6	WKAIR2	R	Weak signal indicator 2	-
5	WKAIR1	R	Weak signal indicator 1	-
4	VSTD	R	Standard line per field indicator	-
3	NINTL	R	Non interlaced signal indicator	-
2	WSSDET	R	0 = Not detected 1 = WSS data detected	-
1	EDSDET	R	0 = Not detected 1 = EDS data detected	-
0	CCDET	R	0 = Not detected 1 = CC data detected	-

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X32 – H MONITOR (HFREF)				
7-0	HFREF, etc.	R	Horizontal line frequency indicator HREF[9:2]/GVAL[8:1 /PHERRDO/CGAINO/BAMPO/MINAVG/SYTHRD/SYAMP	-
REG 0X33 – CLAMP MODE (CLMD)				
7-6	FRM	R/W	Free-run mode 0 = Auto mode 1 = Auto mode 2 = 60Hz 3 = 50Hz	0
5-4	YNR	R/W	Y HF Noise Reduction 0 = None 1 = Smallest 2 = Small 3 = Medium	0
3-2	CLMD	R/W	Clamping mode control 0 = Sync top 1 = Auto 2 = Pedestal 3 = NA	1
1-0	PSP	R/W	Slice level 0 = Low 1 = Medium 2 = High 3 = NA	1
REG 0X34 – ID DETECTION CONTROL (NSEN/SSEN/PSEN/WKTH)				
7-6	INDEX	R/W	Indicates which of the four lower 6-bit registers is currently being controlled. The write sequence is a two-step process unless the same register is written. A write of {INDEX,000000} selects one of the four registers to be written. A subsequent write actually writes into the register.	0
5-0	NSEN/ SSEN/ PSEN/ WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A/ 20/ 1C/ 11
REG 0X35 – CLAMP CONTROL (CLCNTL)				
7	CTEST	R/W	Clamping control for debug use	0
6	YCLEN	R/W	0 = Enable Y-channel clamp 1 = Disable	0
5-4	RESERVED	R/W	Reserved	0
3	GTEST	R/W	0 = Normal operation 1 = Test mode	0
2	VLPF	R/W	Sync filter bandwidth control	0
1	CKLY	R/W	Clamping current control 1	0
0	CKLC	R/W	Clamping current control 2	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X36 – DIFFERENTIAL CLAMPING CONTROL 1				
7	AALPF_EN	R/W	0 = Disable Y-channel anti-aliasing filter (RGB mode) 1 = Enable Y-channel anti-aliasing filter (decoder mode)	1
6	ADC_PD	R/W	0 = ADC normal operation 1 = ADC power-down	0
5	ACLAMP_EN	R/W	Enables differential clamp for normal operation. Disable for test.	1
4	DCLAMP_EN	R/W	Enables single-ended clamp for normal operation. Disable for test.	1
3	CL_MARGIN	R/W	Adjusts the timing spacing between the two non-overlapping clocks that operate in the toggle-mode. 0 = 3 to 27MHz clock periods 1 = 6 to 27MHz clock periods	0
2	TOGGLE_MODE	R/W	Enables the toggle-mode, which eliminates systematic offsets between the two output phases of the common-mode restore amp by swapping them from line to line. 0 = Disable toggle mode 1 = Enable	0
1-0	CM_CLAMP_MODE	R/W	Selects between four modes of operation for the common-mode restore. The table needed is derived from the Verilog module. 0 = Clamp counter 1= Blanking period 2= Burst period 3= Back-porch counter	0
REG 0X37 – DIFFERENTIAL CLAMPING CONTROL 2				
7-6	GAIN_SEL	R/W	Analog front-end pre-amplifier gain control 0 = 1x 1 = 2x 2 = 4x 3 = 4x	0
5-4	RESERVED	R/W	Reserved	0
3	BIAS_PD	R/W	Bias PD 0 = Bias normal operation 1 = Bias power-down	0
2-0	BIAS_CTRL	R/W	Shared ADC bias control for all four channels. Always set to 3h	6
REG 0X38 – DIFFERENTIAL CLAMPING CONTROL 3				
7	RESERVED	R/W	Reserved	0
6-4	DCLAMP_ATTEN	R/W	Attenuates digital clamp current. Register shared by all four channels. 1x current is: 0 = 15µA 1 = 7.5µA 2 = 5µA 3 = 3.75µA 4 = 3µA 5 = 2.5µA 6 = 2.1µA 7 = 1.9µA	2
3-2	ACLAMP_ATTEN	R/W	Reduces the strength of the common-mode restore clamp 0 = 5µA 1 = 6.7µA 2 = 10µA 3 = 20µA	3
1-0	RESERVED	R/W	Reserved	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X39 – DIFFERENTIAL CLAMPING CONTROL 4				
7-6	RESERVED	R/W	Reserved	0
5	PASSIVE_CLAMP	R/W	Selects between current mode (active amplifier) and voltage mode (passive resistor network) for the common-mode restore function. 0 = Passive resistor network for the common-mode restore function 1 = Active amplifier for common-mode restore	0
4	RES_REF	R/W	Selects alternate common-mode reference. Normal operation mode is 0.	0
3	PASSIVE_VREF	R/W	Enables the use of un-buffered ADC V reference. 0 = Buffered 1 = Unbuffered	0
2	PRECON	R/W	Enables common-mode input preconditioning. Forces unused (unselected) inputs to half supply. 0 = Disable 1 = Enable	0
1	DIFF	R/W	Differential Mode on AFE 0 = Single-ended 1 = Differential	0
0	SE	R/W	Input channel selection when it is in single-ended. 0 = AINO (+ve) SE_COM (-ve) 1 = AIN1 (+ve) SE_COM (-ve)	0
REG 0X3A – SHORT DETECTION CONTROL				
7	RESERVED	R/W	Reserved	0
6-4	SHT_THRESH_GND	R/W	Selects threshold for short-to-ground detection for DIAG0, DIAG1, and DIAG2	0
3	RESERVED	R/W	Reserved	0
2-0	SHT_THRESH_BAT	R/W	Selects threshold for short-to-battery detection for DIAG0, DIAG1, and DIAG2	0
REG 0X3B – SHORT DETECTION CONTROL 1				
7-3	RESERVED	R/W	Reserved	0
2	SHT_DIAG_PD	R/W	Power-down diagnostic circuit 0 = Normal operation 1 = Power-down	1
1	SHT_GND_EN	R/W	Enables short-to-ground detection for DIAGx 0 = Disable 1 = Enable	0
0	SH_BAT_EN	R/W	Enables short-to-battery detection for DIAGx (battery or high-side supply) 0 = Disable 1 = Enable	0
REG 0X3C – AFE TEST MUX CONTROL				
7-3	RESERVED	R/W	Reserved	0
2	AN_TEST_EN	R/W	Enables the analog test multiplexers 0 = Disable multiplexers 1 = Enable multiplexers	0
1-0	AN_TEST_SEL	R/W	Selects analog signals from the AFE for the test multiplexers 0 = input multiplexers output 1 = PREAMP/PGA/AAF output 2 = VREFP, VREFN 3 = VCMREF, VCOM_ADC	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X3D – DATA CONVERSION				
7	DISRSTH	R/W	Decifer FIFO reset per line	0
6	DISRSTV	R/W	Decifer FIFO reset per field	0
5	USE_DETSTUS	R/W	Use the “DETSTUS” flag to evaluate the v_stable flag that turns off MIPI when video is unstable	0
4	USE_LOCK	R/W	Use both “VLOCK” and “HLOCK” flags to evaluate the v_stable flag that turns off MIPI when video is unlocked	0
3	USE_VACT_MOD	R/W	1 = Deactivate “vact601” when the “field” bit is repeated in the following field, an error condition, which is used to turn off MIPI transmission to maintain a complete odd-even pair output for the MIPI-receiver.	1
2	Y16	R/W	Y pedestal level selection of YUV to RGB conversion. 0 = No offset adjustment 1 = Decimal 16 level becomes black level	0
1	BT7	R/W	Conversion matrix selection of YUV to RGB conversion. 0 = Matrix for SDTV standard 1 = Matrix for HDTV standard	0
0	RGB565	R/W	Output data format 0 = YUV422 1 = RGB565	0
REG 0X3F -- INTERNAL TEST				
7-0	INTERNAL TEST MODE	R/W	For internal test only.	-
REG 0X43 -- HORIZONTAL DELAY CONTROL REGISTER				
7-1	RESERVED	R/W	Reserved	0
0	HDELAY_CTRL	R/W	Enables separate HDELAY control. When set to “0”, the HDELAY2 has no effect. When set to “1”, the HDELAY2 assumes the function described in the HDELAY register (reg0x07[3:2] # reg0x0A) while the HDELAY is used by the interface circuit between decoder and MIPI controller.	1
REG 0X44 -- HORIZONTAL DELAY II REGISTER, HIGH				
7-2	RESERVED	R/W	Reserved	0
1-0	HDELAY2_HI	R/W	Higher two bits of HDELAY2[9:0] register	0
REG 0X45 -- HORIZONTAL DELAY II REGISTER, LOW				
7-0	HDELAY2_LO	R/W	Lower eight bits of HDELAY2[9:0] register	09

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
ACA Registers – Page 1, 2, 3 and 4				
REG 0X80 – ACA CONTROL				
7	ACA_DBG	R/W	ACA debug function 0 = Disable 1 = Enable	0
6	HIST_WIN_EN	R/W	Histogram measure window enable 0 = Disable 1 = Enable	0
5	RESERVED	R/W	Reserved	0
4	ACA_BYPASS	R/W	ACA function bypass 0 = Disable 1 = Enable	0
3	LPOFF	R/W	Low pass filter disable 0 = Enable 1 = Disable	0
2	MLHCOMP	R/W	Low/High offset compensation enable 0 = Disable 1 = Enable	1
1	MDLTON	R/W	Y Delta compensation enable 0 = Disable 1 = Enable	1
0	ACA_ON	R/W	ACA function enable 0 = Disable 1 = Enable	0
REG 0X81 – ACA GAIN CONTROL				
7-6	RESERVED	R/W	Reserved	0
5-0	ACA_GAIN	R/W	ACA gain control 00 = ACA off 20 = Maximum	20
REG 0X82 – Y AVERAGE HIGH LIMIT CONTROL				
7-6	RESERVED	R/W	Reserved	0
5-0	YAVGHLIM	R/W	Y average high limit control For internal test only, use default setting.	20
REG 0X83 – Y AVERAGE LOW LIMIT CONTROL				
7-6	RESERVED	R/W	Reserved	0
5-0	YAVGLLIM	R/W	Y average low limit control For internal test only, use default setting.	08
REG 0X84 – Y DETECTION THRESHOLD				
7-4	RESERVED	R/W	Reserved	0
3-0	YMINMAXR	R/W	Y min/max detection threshold control For internal test only, use default setting.	9
REG 0X85 – BLACK LEVEL				
7-5	RESERVED	R/W	Reserved	0
4-0	BLKLVL	R/W	Y black level control 00 = Minimal 10 = Maximum	10
REG 0X86 – CENTER LEVEL				
7-4	RESERVED	R/W	Reserved	0
3-0	YCENTER	R/W	Y center level control	6
REG 0X87 – WHITE LEVEL				
7-5	RESERVED	R/W	Reserved	0
4-0	WHTLVL	R/W	Y white level control	00

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X88 – MEAN OFFSET LIMIT				
7	RESERVED	R/W	Reserved	0
6-0	MOFSLIM	R/W	Y mean offset limit control (40 = Maximum) For internal test only, use default setting.	38
REG 0X89 – MEAN OFFSET SLOPE				
7-5	RESERVED	R/W	Reserved	0
4-0	MOFSSLOPE	R/W	Y mean offset slope control (10 = Maximum) For internal test only, use default setting.	10
REG 0X8A – MEAN OFFSET UP-GAIN				
7-6	RESERVED	R/W	Reserved	
5-0	MOFSUPGAIN	R/W	Y mean offset up-gain (20 = Maximum) For internal test only, use default setting.	1C
REG 0X8B – MEAN OFFSET DOWN-GAIN				
7-6	RESERVED	R/W	Reserved	0
5-0	MOFSDNGAIN	R/W	Y mean offset down-gain (20 = Maximum) For internal test only, use default setting.	14
REG 0X8C – DELTA CUTOFF THRESHOLD				
7-5	RESERVED	R/W	Reserved	0
4-0	MDLTCUT	R/W	Y delta cutoff threshold level control For internal test only, use default setting.	0A
REG 0X8D – DELTA SLOPE				
7-5	RESERVED	R/W	Reserved	0
4-0	MDLTSLOPE	R/W	Y delta slope control For internal test only, use default setting.	1F
REG 0X8E – LOW/HIGH AVERAGE THRESHOLD				
7-6	RESERVED	R/W	Reserved	0
5-0	YLHAVGDIFF	R/W	Y low/high average difference threshold control For internal test only, use default setting.	1A
REG 0X8F – LOW MAX LEVEL CONTROL				
7-5	RESERVED	R/W	Reserved	0
4-0	LMAXGRAD	R/W	Low max level control (10 = Maximum) For internal test only, use default setting.	0C
REG 0X90 – HIGH MAX LEVEL CONTROL				
7-5	RESERVED	R/W	Reserved	0
4-0	HMAXGRAD	R/W	High max level control (10 = Maximum) For internal test only, use default setting.	0C
REG 0X91 – LOW UP-GAIN CONTROL				
7-5	RESERVED	R/W	Reserved	0
4-0	LGRADUP	R/W	Low up-gain control (10 = Maximum) For internal test only, use default setting.	0C

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X92 – LOW DOWN-GAIN CONTROL				
7-5	RESERVED	R/W	Reserved	0
4-0	LGRADDN	R/W	Low down-gain control (10 = Maximum) For internal test only, use default setting.	08
REG 0X93 – HIGH UP-GAIN CONTROL				
7-5	RESERVED	R/W	Reserved	0
4-0	HGRADUP	R/W	High up gain control (10 = Maximum) For internal test only, use default setting.	04
REG 0X94 – HIGH DOWN-GAIN CONTROL				
7-5	RESERVED	R/W	Reserved	0
4-0	HGRADDN	R/W	High down gain control (10 = Maximum) For internal test only, use default setting.	0C
REG 0X95 – LOW PASS FILTER COEFFICIENT				
7-4	RESERVED	R/W	Reserved	0
3-0	LPFCOEF	R/W	Low pass filter coefficient control	4
REG 0X96 – PDF INDEX				
7-2	PDF_INDEX	R/W	For internal test only, use default setting.	00
1	ACA_MASK	R/W	For internal test only, use default setting.	0
0	READ_EN	R/W	For internal test only, use default setting.	0
REG 0X97 – HISTOGRAM WINDOW H START				
7-0	HAVST_HIST	R/W	Histogram measure window horizontal start from H active	00
REG 0X98 – HISTOGRAM WINDOW H SIZE				
7-1	RESERVED	R/W	Reserved	00
0	HAVSIZE_HIST_HI	R/W	MSB of histogram measure window horizontal size, totals nine bits	1
REG 0X99 – HISTOGRAM WINDOW H SIZE				
7-0	HAVSIZE_HIST_LO	R/W	LSB of histogram measure window horizontal size, totals nine bits	68
REG 0X9A – HISTOGRAM WINDOW V START				
7-0	VAVST_HIST	R/W	Histogram measure window vertical start from V active	00
REG 0X9B – HISTOGRAM WINDOW V SIZE				
7-1	RESERVED	R/W	Reserved	00
0	VAVSIZE_HIST_HI	R/W	MSB of histogram measure window vertical size, totals nine bits	1
REG 0X9C – HISTOGRAM WINDOW V SIZE				
7-0	VAVSIZE_HIST_LO	R/W	LSB of histogram measure window vertical size, totals nine bits	20
REG 0XA0 – Y AVERAGE				
7-0	YAVG_RAW	R	Reserved for internal test only.	-
REG 0XA1 – Y AVERAGE LIMIT				
7-0	YAVG_LIM	R	Reserved for internal test only.	-
REG 0XA2 – LOW AVERAGE				
7-0	LOW_AVG	R	Reserved for internal test only.	-

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0XA3 – LOW AVERAGE				
7-0	HIGH_AVG	R	Reserved for internal test only.	-
REG 0XA4 – Y MAX				
7-0	Y_MAX	R	Reserved for internal test only.	-
REG 0XA5 – Y MIN				
7-0	Y_MIN	R	Reserved for internal test only.	-
REG 0XA6 – MOFFSET				
7-0	MOFFSET	R	Reserved for internal test only.	-
REG 0XA7 – LOW GAIN				
7-0	LGRAD	R	Reserved for internal test only.	-
REG 0XA8 – HIGH GAIN				
7-0	HGRAD	R	Reserved for internal test only.	-
REG 0XA9 – LL SLOPE				
7-0	LL_SLPOE	R	Reserved for internal test only.	-
REG 0XAA – LH SLOPE				
7-0	LH_SLOPE	R	Reserved for internal test only.	-
REG 0XAB – HL SLOPE				
7-0	HL_SLOPE	R	Reserved for internal test only.	-
REG 0XAC – HH SLOPE				
7-0	HH_SLPOE	R	Reserved for internal test only.	-
REG 0XAD – X LOW				
7-0	X_LOW	R	Reserved for internal test only.	-
REG 0XAE – X MEAN				
7-0	X_MEAN	R	Reserved for internal test only.	-
REG 0XAF – X HIGH				
7-0	X_HIGH	R	Reserved for internal test only.	-
REG 0XB0 – Y LOW				
7-0	Y_LOW	R	Reserved for internal test only.	-
REG 0XB1 – Y MEAN				
7-0	Y_MEAN	R	Reserved for internal test only.	-
REG 0XB2 – Y HIGH				
7-0	Y_HIGH	R	Reserved for internal test only.	-
REG 0XB3 – ACA CONTROL				
7-2	RESERVED	R/W	Reserved	00
1-0	DIS_LINE_EN	R/W	Reserved for internal test only.	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0XB4 – ACA CONTROL				
7-1	RESERVED	R/W	Reserved	00
0	DIS_LINE_SP_HI	R/W	Reserved for internal test only.	0
REG 0XB5 – ACA CONTROL				
7-0	DIS_LINE_SP_LO	R/W	Reserved for internal test only.	00
REG 0XC0 – ACA FLEXIBLE WINDOW HISTOGRAM CONTROL				
7	MASTER	R/W	0 = SLAVE (4x1 Histogram Management) 1 = MASTER (If 4x1 Histogram is turned on, the first channel ACA has to set master, others have to set slave).	1
6	ACA_H_4x1_EN	R/W	0 = Disable Histogram 4x1 mode 1 = Enable Histogram 4x1 mode	0
5-2	RESERVED	R/W	Reserved	0
1	F_WIN_EN	R/W	0 = Disable flexible window on the display 1 = Enable flexible window on the display	0
0	F_WIN_HIST_EN	R/W	0 = Disable flexible window histogram 1 = Enable flexible window histogram	0
REG 0XC1 – X[9:8] OF TOP-LEFT VERTEX IN ACA FLEXIBLE WINDOW				
7-2	RESERVED	R/W	Reserved	00
1-0	TL_VERTEX_X0[9:8]	R/W	X-coordinate of top-left VERTEX[9:8] in ACA flexible window	0
REG 0XC2 – X[7:0] OF TOP-LEFT VERTEX IN ACA FLEXIBLE WINDOW				
7-0	TL_VERTEX_X0[7:0]	R/W	X-coordinate of top-left VERTEX[7:0] in ACA flexible window	00
REG 0XC3 – Y[8:8] OF TOP-LEFT VERTEX IN ACA FLEXIBLE WINDOW				
7-1	RESERVED	R/W	Reserved	00
0	TL_VERTEX_Y0[8:8]	R/W	Y-coordinate of top-left VERTEX[8:8] in ACA flexible window	0
REG 0XC4 – Y[7:0] OF TOP-LEFT VERTEX IN ACA FLEXIBLE WINDOW				
7-0	TL_VERTEX_Y0[7:0]	R/W	Y-coordinate of top-left VERTEX[7:0] in ACA flexible window	00
REG 0XC5 – X[9:8] OF TOP-RIGHT VERTEX IN ACA FLEXIBLE WINDOW				
7-2	RESERVED	R/W	Reserved	00
1-0	TR_VERTEX_X1[9:8]	R/W	X-coordinate of top-right VERTEX[9:8] in ACA flexible window	2
REG 0XC6 – X[7:0] OF TOP-RIGHT VERTEX IN ACA FLEXIBLE WINDOW				
7-0	TR_VERTEX_X1[7:0]	R/W	X-coordinate of top-right VERTEX[7:0] in ACA flexible window	CF
REG 0XC7 – Y[8:8] OF TOP-RIGHT VERTEX IN ACA FLEXIBLE WINDOW				
7-1	RESERVED	R/W	Reserved	00
0	TR_VERTEX_Y1[8:8]	R/W	Y-coordinate of top-right VERTEX[8:8] in ACA flexible window	0
REG 0XC8 – Y[7:0] OF TOP-RIGHT VERTEX IN ACA FLEXIBLE WINDOW				
7-0	TR_VERTEX_Y1[7:0]	R/W	Y-coordinate of top-right VERTEX[7:0] in ACA flexible window	00
REG 0XC9 – X[9:8] OF BOTTOM-LEFT VERTEX IN ACA FLEXIBLE WINDOW				
7-2	RESERVED	R/W	Reserved	00
1-0	BL_VERTEX_X2[9:8]	R/W	X-coordinate of bottom-left VERTEX[9:8] in ACA flexible window	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0XCA – X[7:0] OF BOTTOM-LEFT VERTEX IN ACA FLEXIBLE WINDOW				
7-0	BL_VERTEX_X2[7:0]	R/W	X-coordinate of bottom-left VERTEX[7:0] in ACA flexible window	00
REG 0XCB – Y[8:8] OF BOTTOM-LEFT VERTEX IN ACA FLEXIBLE WINDOW				
7-1	RESERVED	R/W	Reserved	00
0	BL_VERTEX_Y2[8:8]	R/W	Y-coordinate of bottom-left VERTEX[8:8] in ACA flexible window	0
REG 0XCC – Y[7:0] OF BOTTOM-LEFT VERTEX IN ACA FLEXIBLE WINDOW				
7-0	BL_VERTEX_Y2[7:0]	R/W	Y-coordinate of bottom-left VERTEX[7:0] in ACA flexible window	EF
REG 0XCD – X[9:8] OF BOTTOM-RIGHT VERTEX IN ACA FLEXIBLE WINDOW				
7-2	RESERVED	R/W	Reserved	00
1-0	BR_VERTEX_X3[9:8]	R/W	X-coordinate of bottom-right VERTEX[9:8] in ACA flexible window	2
REG 0XCE – X[7:0] OF BOTTOM-RIGHT VERTEX IN ACA FLEXIBLE WINDOW				
7-0	BR_VERTEX_X3[7:0]	R/W	X-coordinate of bottom-right VERTEX[7:0] in ACA flexible window	CF
REG 0XCF – Y[8:8] OF BOTTOM-RIGHT VERTEX IN ACA FLEXIBLE WINDOW				
7-1	RESERVED	R/W	Reserved	00
0	BR_VERTEX_Y3[8:8]	R/W	Y-coordinate of bottom-right VERTEX[8:8] in ACA flexible window	0
REG 0XD0 – Y[7:0] OF BOTTOM-RIGHT VERTEX IN ACA FLEXIBLE WINDOW				
7-0	BR_VERTEX_Y3[7:0]	R/W	Y-coordinate of bottom-right VERTEX[7:0] in ACA flexible window	EF
REG 0XD1 – X[9:8] OF LEFT-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-2	RESERVED	R/W	Reserved	00
1-0	LM_VERTEX_X4[9:8]	R/W	X-coordinate of left-middle VERTEX[9:8] in ACA flexible window	0
REG 0XD2 – X[7:0] OF LEFT-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-0	LM_VERTEX_X4[7:0]	R/W	X-coordinate of left-middle VERTEX[7:0] in ACA flexible window	00
REG 0XD3 – Y[8:8] OF LEFT-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-1	RESERVED	R/W	Reserved	00
0	LM_VERTEX_Y4[8:8]	R/W	Y-coordinate of left-middle VERTEX[8:8] in ACA flexible window	0
REG 0XD4 – Y[7:0] OF LEFT-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-0	LM_VERTEX_Y4[7:0]	R/W	Y-coordinate of left-middle VERTEX[7:0] in ACA flexible window	77
REG 0XD5 – X[9:8] OF TOP-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-2	RESERVED	R/W	Reserved	00
1-0	TM_VERTEX_X5[9:8]	R/W	X-coordinate of top-middle VERTEX[9:8] in ACA flexible window	1
REG 0XD6 – X[7:0] OF TOP-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-0	TM_VERTEX_X5[7:0]	R/W	X-coordinate of top-middle VERTEX[7:0] in ACA flexible window	67
REG 0XD7 – Y[8:8] OF TOP-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-1	RESERVED	R/W	Reserved	00
0	TM_VERTEX_Y5[8:8]	R/W	Y-coordinate of top-middle VERTEX[8:8] in ACA flexible window	0
REG 0XD8 – Y[7:0] OF TOP-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-0	TM_VERTEX_Y5[7:0]	R/W	Y-coordinate of top-middle VERTEX[7:0] in ACA flexible window	00

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0XD9 – X[9:8] OF BOTTOM-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-2	RESERVED	R/W	Reserved	00
1-0	BM_VERTEX_X6[9:8]	R/W	X-coordinate of bottom-middle VERTEX[9:8] in ACA flexible window	1
REG 0XDA – X[7:0] OF BOTTOM-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-0	BM_VERTEX_X6[7:0]	R/W	X-coordinate of bottom-middle VERTEX[7:0] in ACA flexible window	67
REG 0XDB – Y[8:8] OF BOTTOM-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-1	RESERVED	R/W	Reserved	00
0	BM_VERTEX_Y6[8:8]	R/W	Y-coordinate of bottom-middle VERTEX[8:8] in ACA flexible window	0
REG 0XDC – Y[7:0] OF BOTTOM-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-0	BM_VERTEX_Y6[7:0]	R/W	Y-coordinate of bottom-middle VERTEX[7:0] in ACA flexible window	EF
REG 0XDD – X[9:8] OF RIGHT-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-2	RESERVED	R/W	Reserved	00
1-0	RM_VERTEX_X7[9:8]	R/W	X-coordinate of right-middle VERTEX[9:8] in ACA flexible window	2
REG 0XDE – X[7:0] OF RIGHT-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-0	RM_VERTEX_X7[7:0]	R/W	X-coordinate of right-middle VERTEX[7:0] in ACA flexible window	CF
REG 0XDF – Y[8:8] OF RIGHT-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-1	RESERVED	R/W	Reserved	00
0	TM_VERTEX_Y7[8:8]	R/W	Y-coordinate of right-middle VERTEX[8:8] in ACA flexible window	0
REG 0XE0 – Y[7:0] OF RIGHT-MIDDLE VERTEX IN ACA FLEXIBLE WINDOW				
7-0	RM_VERTEX_Y7[7:0]	R/W	Y-coordinate of right-middle VERTEX[7:0] in ACA flexible window	77
REG 0XE1 – HISTOGRAM DATA [7:0]				
7-0	HISTOGRAMDAT[7:0]	R	Histogram data [7:0]	-
REG 0XE2 – HISTOGRAM DATA [15:8]				
7-0	HISTOGRAMDAT[15:8]	R	Histogram data [15:8]	-
REG 0XE3 – HISTOGRAM DATA [18:16]				
7-3	RESERVED	R	Reserved	-
2-0	HISTOGRAMDAT[18:16]	R	Histogram data [18:16]	-
REG 0XE4 – FLEXIBLE WINDOW Y COLOR [7:0]				
7-0	F_WIN_COLOR_Y	R	Flexible Window Y Color	-
7-0	F_WIN_COLOR_Y	R	Flexible Window Y Color	-
REG 0XE5 – FLEXIBLE WINDOW CB COLOR [7:0]				
7-0	F_WIN_COLOR_CB	R	Flexible Window CB Color	-
REG 0XE6 – FLEXIBLE WINDOW CR COLOR [7:0]				
7-0	F_WIN_COLOR_CR	R	Flexible Window CR Color	-
REG 0XE7 – TRANSFER HISTOGRAM TO HOST				
7-1	RESERVED	R/W	Reserved	00
0	TRAN_HISTO_EN	R/W	0 = Disable 1 = Transfer histogram to host in CCIR656 or MIPI	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
Line Interleave Engine Registers -- Page 5				
REG 0X00 – LINE INTERLEAVE ENGINE CONTROL				
7	PD_MIPI	R/W	0 = Power-on line interleave engine 1 = Power-off line interleave engine	1
6	TMLS_MIPI	R/W	0 = Disable test 1 = Enable low-speed test mode	0
5	TMHS_MIPI	R/W	0 = Disable test 1 = Enable high-speed test mode	0
4-3	RESERVED	R/W	Reserved	0
2-0	LANE_NO	R/W	MIPI-data-lane numbers, supports up to two lanes. 001 = one lane 010 = two lanes	2
REG 0X01 – LI-ENGINE LINE CONTROL				
7	LNINC1	R/W	0 = Enable line-increment of 2 1 = Enable line-increment of 1	1
6	SWAP_CRC	R/W	1 = Swap MSB-Byte and LSB-Byte of CRC[15:0] output order.	0
5	FRAME_MODE	R/W	1 = One pair of FS/FE per frame which includes a set of top and bottom fields 0 = One pair of FS/FE per field, or two pairs of FS/FE per frame	0
4-0	PIC_WIDTH [12:8]	R/W	Picture width[12:8] upper bits	05
REG 0X02 – LI-ENGINE PICTURE WIDTH				
7-0	PIC_WIDTH [7:0]	R/W	Picture width[7:0] lower bits	A0
REG 0X03 – LI-ENGINE SYNC CONTROL				
7	SWAP_YC	R/W	1 = Swap pattern generator's YC output order	0
6	HS_DPHY_TEST	R/W	0 = Disable test 1 = Enable high speed MIPI test mode with clock and data lane timing	0
5	RESERVED	R/W	Reserved	0
4	RST_FIFO	R/W	1 = Enable line buffer reset logic	1
3	TOP_ONLY	R/W	1 = Start operation at the beginning of input video's top field to align interlaced video	1
2-0	RESERVED	R/W	Reserved	0
REG 0X04 – LI-ENGINE VIRTUAL-CHANNEL ASSIGNMENT				
7-6	VC4	R/W	Virtual Channel 4 assignment	3
5-4	VC3	R/W	Virtual Channel 3 assignment	2
3-2	VC2	R/W	Virtual Channel 2 assignment	1
1-0	VC1	R/W	Virtual Channel 1 assignment	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X05 – LI-ENGINE TYPE CONTROL				
7	RESERVED	R/W	Reserved	0
6	ON_CTRL	R/W	0 = Turn-on and turn-off MIPI at either top or bottom field boundary; used for testing. 1 = Turn-on and turn-off MIPI only at top-field boundary after preset number of wait frames set in Reg0x519. This allows receivers, which do not decode the field-bit from line-number or frame-number, to display interlaced video properly.	1
5	SDPROG	R/W	1 = 720x480 or 720x576 Standard Definition Progressive mode operation. For internal test only.	0
4	RGB565	R/W	1= Enable RGB565 color mode with its specific MIPI data-type.	0
3	RESERVED	R/W	Reserved	0
2	SAV_NORMAL	R/W	1 = Use parity[3:0] for SAV/EAV[3:0] 0 = Use channel_number[3:0] for SAV/EAV[3:0] (BT.656 Only)	0
1	656_BYTE	R/W	(ISL79988 only) 0 = Feed CCIR656 line-interleaved output to output pads 1 = Feed CCIR656 byte-interleaved output to output pads	0
0	RESERVED	R/W	Reserved	0
REG 0X06 – LI-ENGINE FIFO CONTROL				
7	FE_FS_ADJ	R/W	0 = Enable a preset (2-line – T_FIFO_DEP) FE-to-FS spacing for the Pseudo Single-Frame mode 1 = Enable an adjustable FE-to-FS spacing mechanism for the Pseudo Single-Frame mode, with 0x50b[4:0] = NCNT and 0x50C[7:0] = PCNT for a programmable (NCNT-line + (PCNT*8) -pixel – T_FIFO_DEP) spacing. T_FIFO_DEP is the variable run time active FIFO depletion time, measured in 27MHz input-line-time, before FE is asserted. T_FIFO_DEP assumes the following operational ranges depending on the setting of 0x007[1:0] = MODE_CH T_FIFO_DEP = 0 when MODE_CH = 2'b00 (one-channel) T_FIFO_DEP = (0 to 1/2-line) when MODE_CH = 2'b01 (two-channel) T_FIFO_DEP = (0 to 1/4-line) when MODE_CH = 2'b10 (four-channel)	0
6	FIX_LNOUT	R/W	1 = Use fixed-line-output-per-pseudo-frame for Pseudo Single-Frame mode 0 = Use channel-1 VActive to control pseudo-frame size for Pseudo Single-Frame mode	1
5	8BHDR	R/W	1 = Add the 8-byte header in the MIPI output(1448 bytes in the long-packet payload) 0 = No 8-byte header in the MIPI output (1440 bytes in the long-packet payload) This bit only affects the non-standard-mode when 0x506[0] = 1. For standard-mode 0x506[0] = 0, the 8-byte header is always included in each line output.	1
4	VSTABLE	R/W	0 = Ignore the 'VSTABLE" flag from decoders, always do normal output transmission. 1 = Use the "VSTABLE" flag from decoders to perform normal output transmission or stop the output transmission.	0
3	SAME_VC	R/W	0 = Disable SAME_VC mode, normal operation 1 = Enable SAME_VC mode to drive special MIPI receivers in test	0
2	TYPE_30	R/W	1 = Apply data-type-30 (user defined) to the histogram line MIPI output.	0
1	RESERVED	R/W	Reserved	0
0	PSEUDO_S_FRM	R/W	1= Add a special 8-byte header at line-start for non-standard SOC receivers that do not decode virtual-channel (VC) in the CSI packet headers (Pseudo Single-Frame mode).	1
REG 0X07 – MIPI READ-START CONTROL				
7-0	RD_START	R/W	Special Read Start Count fixed at 17h for 1-ch-1-lane, 24h for 2-ch-2-lane, and 2Bh for other modes.	2B

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X08 – PSEUDO FRAME FIELD CONTROL				
7-4	RESERVED	R/W	Reserved	0
3	PF_VB_START	R/W	1 = Start pseudo-frame's interleaved BT.656 output from the vertical-blanking area 0 = Start pseudo-frame's interleaved BT.656 output from the vertical-active area (default)	1
2	RESERVED	R/W	Reserved	0
1	DATA2CLK	R/W	1 = Copy the data-lane esc-mode control pattern to the clock lane for a special Tektronix scope conformance test measurement; this is not a MIPI standard.	1
0	PF_FLD	R/W	1 = BT.656 output in pseudo-frame mode contains both F = 0 and F = 1 as in a interlaced video, to make it essentially a Pseudo-Field mode. 0 = BT.656 output in pseudo-frame mode contains both F = 0 as in a progressive video.	0
REG 0X09 – ONE FIELD MODE CONTROL				
7-5	RESERVED	R/W	Reserved	0
4	8010	R/W	1 = Fill "8010" in horizontal-blanking data 0 = Fill with channel-number in the lower nibble	0
3-2	RESERVED	R/W	Reserved	0
1	1FLD_TOP	R/W	1 = Output the top-field-only in the one-field mode	0
0	1FLD_BOT	R/W	1 = Output the bottom-field-only in the one-field mode	0
REG 0X0A – MIPI INTERNAL HARDWARE TEST COUNTER (INTERNAL TEST ONLY, FOR BOTH MIPI AND BT.656)				
7-0	INT_CTR	R/W	Special hardware counter to control spacing between long packets in interleaving, (INT_CTR*8) is the number of pixels per MIPI-line transmission, which includes the following four sections: (LP_to_HS protocol + HS_Active_Line + HS_to_LP protocol + Horizontal_blanking) Increasing the counter from the default setting equalizes the horizontal_blanking between consecutive MIPI-lines, but a very sensitive adverse effect on overflowing line buffers and breaking output pictures may happen. (62h is a safe value that meets MIPI protocol and hardware's FIFO-size constraint in various interleaving operations for all channel selections and MIPI-data-lane-selections.) Note this register controls the spacing between interleaved lines, and it affects both MIPI and BT.656 output.	62
REG 0X0B – GENERATOR BAR PATTERN				
7-6	GEN_BAR_PATTERN	R/W	Test pattern generator black and white bar pattern control. 0 = (bbbbwb) 1 = (bbbwwb) 2 = (bbwbwb) 3 = (bbwwwb)	0
5	RESERVED	R/W	Reserved	0
4-0	NCNT		Number of line count for FE-to-FS spacing when FE-FS-ADJ (0x506[7]) mode is set. Note that increasing this setting beyond three overflows the four line buffers and breaks the four pictures. This register is reserved as HARDWARE-TEST only.	02
REG 0X0C – MIPI PCNT FOR PSEUDO SINGLE-FRAME MODE				
7-0	PCNT	R/W	Number of pixel-count for FE-to-FS spacing when FE-FS-ADJ (0x506[7]) mode is set The setting multiplied by eight is the number of pixels that are added to the FE-to-FS spacing. For example, to add a quarter line of spacing, set this as 36h for the 4-ch case. To add a half-line spacing, set this as 6Bh for the 2-ch case.	00

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X0D – LI-ENGINE TEST PATTERN-GENERATOR CONTROL				
7	INT_PAT1	R/W	0 = Use the first decoder for the first channel input. 1 = Use the first test pattern generator as specified by MODE_CH[1:0] for the first channel input.	0
6	INT_PAT2	R/W	0 = Use the second decoder output for the second channel input. 1 = Use the second test pattern generator as specified by MODE_CH[1:0] for the second channel input.	0
5	INT_PAT3	R/W	0 = Use the third decoder output for the third channel input. 1 = Use the third test pattern generator as specified by MODE_CH[1:0] for the third channel input.	0
4	INT_PAT4	R/W	0 = Use the forth decoder output for the forth channel input. 1 = Use the forth test pattern generator as specified by MODE_CH[1:0] for the forth channel input.	0
3-2	GEN_COLOR	R/W	Test pattern generator top-screen color selection. 00(yellow), 01(blue), 10(green), 11(pink)	0
1	FORCE_FRM	R/W	1 = Force interlaced input with F = 0 and F = 1 in SAV/EAV to have only F = 0 for progressive input. This is used only in pseudo-frame mode with BT.656 output. The field bit affects both the SAV/EAV and the 8-byte header's F-bit	0
0	ADD_VBLK	R/W	1 = Add one blank line to the end of each channel, so that some decoders can use the V = 1 in SAV/EAV timing as a reference to generate their VSYNC properly. 0 = BT.656 line-interleaved output contains only V = 0 in SAV/EAV, and decoders need to generate their own VSYNC after a fixed number of lines have been captured. This control bit is only needed for normal-mode BT.656 output, which does not contain a frame-end signal and its blanking period has no H Active signal.	0
REG 0X0E – PSEUDO FRAME VERTICAL BLANKING COUNT FOR PSEUDO SINGLE-FRAME				
7-0	VB_CNT	R/W	Number of cycle count for FE-to-FS spacing when FIX_LNOUT (0x506[6]) mode is set The setting multiplied by 128 is the number of pixels that are set to the FE-to-FS spacing. For example, to add two lines of spacing for the 4-channel case, set 1728x2x4/128 = 108 = 0x6C.	6C
REG 0X0F – LI-ENGINE CONTROL				
7	GEN_FLDPOL	R/W	0 = Normal field polarity 1 = Invert generators' field polarity	0
6	GEN_NOVID	R/W	0 = Disable TEST, normal operation 1 = Enable NO-VIDEO-ID option for pattern generators	0
5	ULPS_FSYNC	R/W	1 = Enable MIPI Ultra Low Power State (ULPS) operation at frame-sync time	0
4	RESERVED	R/W	Reserved	0
3	HSCK_ALWAYS_ON	R/W	0 = Normal operation with low-speed and high-speed transitions 1 = Enable high-speed MIPI clock all the time without following the DPHY specification	0
2	GEN_PAL	R/W	0 = Enable NTSC mode operation 1 = Enable PAL mode operation	0
1	ESC_TEST	R/W	1 = Enable Tektronix's specific escape-mode test pattern with a preceding long flat LP11 idle state to initialize its scope capture and timing/voltage measurement, this is not a MIPI standard.	0
0	ESC_GO	R/W	1 = Enable Tektronix's repeated escape-mode test pattern to be repeated during this register's set period to ease the data capture of its scope. This is not a MIPI standard.	0
REG 0X10 – WORD-COUNT CONTROL (MIPI ONLY)				
7-0	WORD_COUNT [15:8]	R/W	Fixed word-count field in the MIPI long-packet header	05
REG 0X11 – WORD-COUNT CONTROL (MIPI ONLY)				
7-0	WORD_COUNT [7:0]	R/W	Fixed word count field in the MIPI long-packet header	A4

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X12 – MIPI DPHY TIMING CONTROL (MIPI ONLY)				
7-4	LPX_CNT	R/W	DPHY's T-LPX period control counter	7
3-0	HS_PREPARE	R/W	DPHY's T-HS_PREPARE period control counter	6
REG 0X13 – MIPI DPHY TIMING CONTROL (BOTH MIPI AND BT.656)				
7-0	HS_ZERO	R/W	DPHY's T-HS_ZERO period control counter	17
REG 0X14 – MIPI DPHY TIMING CONTROL (MIPI ONLY)				
7-0	HS_TRAIL	R/W	DPHY's T-HS_TRAIL period control counter	0E
REG 0X15 – MIPI DPHY TIMING CONTROL (MIPI ONLY)				
7-0	CLK_TO_DATA	R/W	DPHY's CLK-to-DATA period control counter	36
REG 0X16 – MIPI DPHY TIMING CONTROL (MIPI ONLY)				
7-0	CLK_POST	R/W	DPHY's T-CLK_POST period control counter	12
REG 0X17 – MIPI DPHY TIMING CONTROL (MIPI ONLY)				
7-0	MARK_WAIT	R/W	ULPS mode exit wait time / 512, 0x37(27MHz), 0x70(54MHz), 0xf6(108MHz)	70
REG 0X18 – MIPI D-PHY PARAMETERS (MIPI ONLY)				
7	RESERVED	R/W	Reserved	0
6	FORCE_ULPS	R/W	1 = Force D-PHY to enter ULPS mode	0
5	ESC_EXIT	R/W	1 = Force ESC-mode to exit ULPS mode, TRIGGER mode, or LPDT mode	0
4	LPDT_MODE	R/W	1 = Include MIPI-LPDT mode to D-PHY output	0
3	RST_MODE	R/W	1 = Include MIPI-RESET mode to D-PHY output	0
2	RESERVED	R/W	Reserved	0
1	ESC_MODE	R/W	1 = Include MIPI-ESCAPE mode to D-PHY output	0
0	RESERVED	R/W	Reserved	0
REG 0X19 – SOT_PERIOD IN D-PHY (MIPI ONLY)				
7-0	WAIT_FRAMES	R/W	Number of frames to wait before MIPI starts; works only with Reg0x505[6] = 1.	03
REG 0X1A – EOT_PERIOD IN D-PHY				
7-0	EOT_PERIOD	R/W	End_of_Transmission period in "UI" unit for D-PHY	0A
REG 0X1B – MIPI D-PHY PARAMETERS (MIPI ONLY)				
7-4	CLK_PREPARE	R/W	CLK_PREPARE [38ns, 95ns]	6
3-0	CLK_PRE	R/W	CLK_PRE, 8*UI	1
REG 0X1C – MIPI DPHY TIMING CONTROL (MIPI ONLY)				
7-4	LP_11	R/W	SOT LP11 state wait time	7
3-0	CLK_TRAIL	R/W	CLK_TRAIL 60ns	A
REG 0X1D – MIPI DPHY TIMING CONTROL (MIPI ONLY)				
7-0	CLK_ZERO	R/W	CLK_ZERO, >240ns	0F
REG 0X1E – MIPI DPHY TIMING CONTROL (MIPI ONLY)				
7-4	SHORT_PKT_DLY	R/W	SHORT-PACKET-DELAY is used to control short-packets' HS_ZERO timing period.	8
3-0	CLK_SOT_CNT	R/W	CLK_SOT wait time	C

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X1F – MIPI DPHY TIMING CONTROL (MIPI ONLY)				
7-0	ULPS_LP11_CNT	R/W	ULPS LP11 wait time	06
REG 0X20 – TEST PATTERN GENERATOR (MIPI ONLY)				
7	PRBS_ERR_RSTB	R/W	1 = Reset PRBS error in TEST mode	0
6	ATG_RESYNC	R/W	Generate a HS_RESYNC pulse when value change from 0 to 1. 0 = No effect 1 = Generate a pulse	0
5	RESERVED	R/W	Reserved	0
4	TESTSET0	R/W	Control the TXCKSET0 when MIPIAFE_TEST_EN is '1'	0
3	ATG_INV_8B	R/W	1 = Select inverted 8-bit HS pattern for testing	0
2	ATG_PRBS_SEL	R/W	1 = Select PRBS-9 HS test pattern	0
1	HS_TEST_SEL	R/W	0 = Select low-power test 1 = Select high-speed HS test	0
0	ATEST_EN	R/W	1 = Start to do automatic test	0
REG 0X21 – ESCAPE_MODE TIMING CONTROL (MIPI ONLY)				
7-0	ESC_DELAY	R/W	Data-lane delay from clock-lane in escape-mode	0C
REG 0X22 – AUTOMATIC TEST ERROR DETECTION				
7	PRBS_ERR_DET	R	1 = Error detected during PRBS test	-
6-0	RESERVED	R	Reserved	-
REG 0X23 – MIPI TIMING (MIPI ONLY)				
7-4	RESERVED	R	Reserved	-
3-0	CLK_TRAIL_SHORT_PKT	R	CLK_TRAIL_SHORT_PACKET period control	A
REG 0X24 – PICTURE_HEIGHT HIGH BITS				
7-3	RESERVED	R	Reserved	-
2-0	IN_PIC_HEIGHT[10:8]	R	Captured PICTURE-HEIGHT[10:8] per field or frame	-
REG 0X25 – PICTURE_HEIGHT LOW BYTE				
7-0	In_PIC_HEIGHT[7:0]	R	Captured PICTURE-HEIGHT[7:0] per field or frame	-
REG 0X26 – MIPI SHORT-PACKET HS_TRAIL CONTROL (MIPI ONLY)				
7-0	HS_TRAIL_SPKT	R/W	MIPI short-packet HS_trail period control count	07
REG 0X28 – FIFO THRESHOLD COUNT				
7-3	RESERVED	R/W	Reserved	00
2-0	FIFO_THRESHOLD[10:8]	R/W	Line Buffers' FIFO_THRESHOLD control, upper bits	1
REG 0X29 – FIFO THRESHOLD COUNT				
7-0	FIFO_THRESHOLD[7:0]	R/W	Line Buffers' FIFO_THRESHOLD control, lower bits	0E
REG 0X2A – TEST PATTERN GENERATORS' RANDOM SYNC CONTROL				
7-4	RANDOM_SYNC4	R/W	Random-sync generator selection control	0
3-0	RANDOM_SYNC3	R/W	Random-sync generator selection control	0
REG 0X2B – TEST PATTERN GENERATORS' RANDOM SYNC CONTROL				
7-4	RANDOM_SYNC2	R/W	Random-sync generator selection control	0
3-0	RANDOM_SYNC1	R/W	Random-sync generator selection control	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X2C – PSEUDO SINGLE-FRAME MODE FIELD-END CONTROL				
7-3	RESERVED	R/W	Reserved	00
2-0	FE_BOTTOM[10:8]	R/W	Bottom-field's end line number upper bits Note that this register affects both MIPI and BT.656 outputs. This bit takes effect when 0x506[6] = 0 and 0x506[0] = 1 are set.	0
REG 0X2D – PSEUDO SINGLE-FRAME MODE FIELD-END CONTROL				
7-0	FE_BOTTOM[7:0]	R/W	Bottom-field's end line number lower bits Note that this register affects both MIPI and BT.656 outputs This bit takes effect when 0x506[6] = 0 and 0x506[0] = 1 are set	F1
REG 0X2E – PSEUDO SINGLE-FRAME MODE FIELD-END CONTROL				
7-3	RESERVED	R/W	Reserved	00
2-0	FE_TOP[10:8]	R/W	Top-field's end line number upper bits Note that this register affects both MIPI and BT.656 outputs. This bit takes effect when 0x506[6] = 0 and 0x506[0] = 1 are set.	0
REG 0X2F – PSEUDO SINGLE-FRAME MODE FIELD-END CONTROL				
7-0	FE_TOP[7:0]	R/W	Top-field's end line number lower bits Note that this register affects both MIPI and BT.656 outputs. This bit takes effect when 0x506[6] = 0 and 0x506[0] = 1 are set.	F1
REG 0X30 – MIPI ANALOG CTRL DATA				
7-0	CTRL_BIT_DATA1	R/W	Control Data 1	00
REG 0X31 – MIPI ANALOG CTRL DATA				
7-0	CTRL_BIT_DATA2	R/W	Control Data 2	00
REG 0X32 – MIPI ANALOG CTRL CLOCK				
7-0	CTRL_BIT_CLK	R/W	Control clock	00
REG 0X33 – PLL ANALOG STATUS				
7-5	RESERVED	R/W	Reserved	0
4-0	ITUNE	R/W	Tune PLL loop bandwidth	00
REG 0X34 – PLL ANALOG CTRL MISC				
7	PLL_RON	R/W	For low frequency operations	0
6	PLL_LOWF	R/W	For low frequency operations	0
5	PLL_RST_OFF	R/W	Disable PLL Reset	0
4	PLL_RSTB	R/W	PLL Reset 0 = Enable (Reset) 1 = Normal operation	0
3	PLL_DPHY_RSTB	R/W	DPHY Reset 0 = Enable (Reset) 1 = Normal operation	0
2	PWD_BG	R/W	Power-down Band Gap 0 = Normal operation 1 = Power-down	1
1	PLL_PWD	R/W	Power-down PLL 0 = Normal operation 1 = Power-down	1
0	RESERVED	R/W	Reserved	0

ISL79987 and ISL79988 Register Detail (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
REG 0X35 – MIPI ANALOG REGISTERS				
7-4	RESERVED	R/W	Reserved	0
3-1	PWD_DATA	R/W	Enable power-down of data lanes	3
0	PWD_CLK	R/W	Enable power-down of the clock lane	1
REG 0X36 – PLL ANALOG REGISTER				
7-2	RESERVED	R/W	Reserved	00
1	CK_POL	R/W	Clock polarity	0
0	PLL_TEST_EN	R/W	Enable PLL test	0
REG 0X38 – TOTAL PSEUDO-FRAME LINE-COUNT CONTROL				
7-0	TOTAL_PF_LINE[15:8]	R/W	Total_pseudo_frame_line_number[15:8], used in the FIX_LNOUT (0x506[6]) mode	03
REG 0X39 – TOTAL PSEUDO-FRAME LINE-COUNT CONTROL				
7-0	TOTAL_PF_LINE[7:0]	R/W	Total_pseudo_frame_line_number[7:0], used in the FIX_LNOUT(0x506[6]) mode. Default value is 0x3C0 for NTSC and 0x480 for PAL in the 4-channel case.	C0
REG 0X3A – HORIZONTAL LINE-COUNT CONTROL				
7-5	RESERVED	R/W	Reserved	0
4-0	HLINE_CNT[10:8]	R/W	H_line_cnt[12:8]; needs to be set differently if the horizontal total-line-width, including blanking and active pixels, is different from the NTSC or PAL format.	06
REG 0X3B – HORIZONTAL LINE-COUNT CONTROL				
7-0	HLINE_CNT[7:0]	R/W	Hline_cnt[7:0]; needs to be set differently if the horizontal total-line-width, including blanking and active pixels, is different from the NTSC or PAL format.	B3
REG 0X3C – HISTOGRAM LINE-COUNT CONTROL				
7-3	RESERVED	R/W	Reserved	00
2-0	HIST_LINE[10:8]	R/W	hist_line_number[10:8]; used in the histogram output mode for the last line in a picture.	0
REG 0X3D – HISTOGRAM LINE-COUNT CONTROL				
7-0	HIST_LINE[7:0]	R/W	hist_line_number[7:0], used in the histogram output mode for the last line in a picture. Default value is 0x0F1 for NTSC and 0x121 for PAL.	F1

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to ensure that you have the latest revision.

DATE	REVISION	CHANGE
Mar 19, 2019	FN8907.1	Updated links throughout the document. Updated ordering information table by adding tape and reel parts to table and updating notes. In the Register Summary section updated Reg 0X37[2-0] from AAFLPF to BIAS_CTRL and Reg 0X38 DCLAMP_ATTEN from Bit 5-4 to Bit 6-4. In the Register Description section updated Reg0x37[2-0] and Reg0x38 information. Removed About Intersil section. Updated disclaimer.
Dec 12, 2016	FN8907.0	Initial release

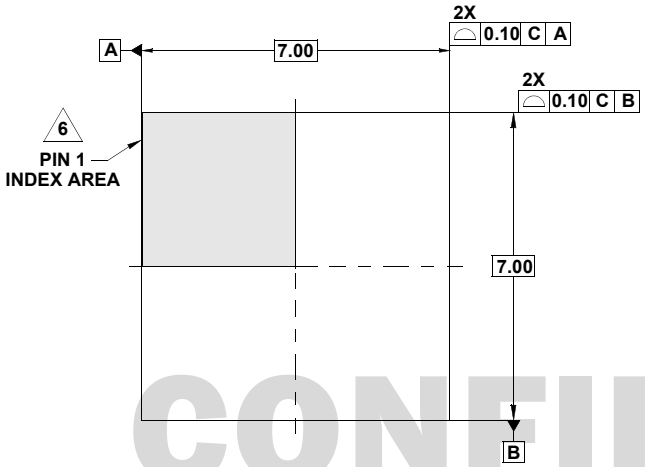
Package Outline Drawing

For the most recent package outline drawing, see L48.7x7W.

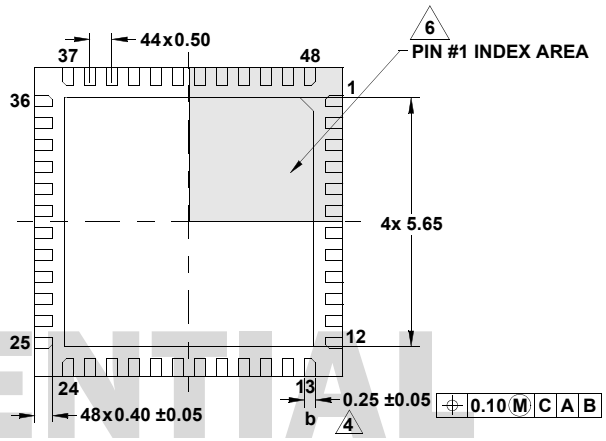
L48.7x7W

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

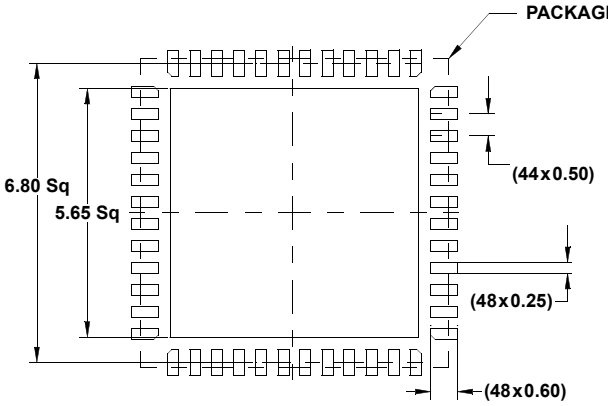
Rev 0, 8/12



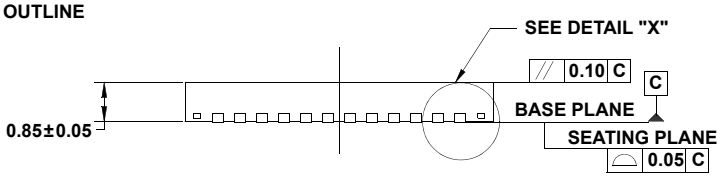
TOP VIEW



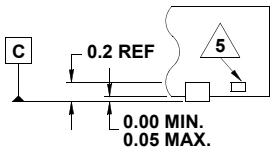
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.20mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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