MCIMX8DXL-WEVKUM

MCIMX8DXL-WEVK Board User Manual

Rev. 1 — 10 March 2023 **User manual**

Document Information

Information	Content
Keywords	MCIMX8DXL-WEVKUM, MCIMX8DXL-WEVK, i.MX 8DXL, i.MX 8DualXLite
Abstract	The MCIMX8DXL-WEVK board provides a comprehensive platform for design and evaluation of most commonly used features of the NXP i.MX 8DXL applications processor

1 Overview

The MCIMX8DXL-WEVK board provides a comprehensive platform for design and evaluation of most commonly used features of the NXP i.MX 8DXL applications processor, in a small and low-cost package.

The MCIMX8DXL-WEVK board is an entry-level development board to familiarize you with the processor, before you invest a large amount of resources in more specific designs. The board is lead-free and RoHS-compliant.

For information on how to set up and boot the board, see *i.MX 8DXL Evaluation Kit Quick Start Guide*, which is available in the MCIMX8DXL-WEVK board kit. To run the preloaded image, the board DIP switch SW1 must be set to make the board boot from processor internal eFuse (default setting). For more details, see Section 1.10.

This document provides detailed information about the MCIMX8DXL-WEVK board interfaces, power supplies, clocks, connectors, jumpers, push buttons, DIP switch, and LEDs.

1.1 Acronyms

The table below lists the acronyms used in this document.

Table 1. Acronyms

Acronym	Meaning
ACM	Audio clock mux
ADC	Analog-to-digital converter
BCU	Board Control Utilities
BSP	Board support package
CAN	Controller Area Network
CC	Configuration channel
DFP	Downstream-Facing Port
DIP	Dual in-line package
DRP	Dual-Role Power
EEPROM	Electrically erasable programmable read-only memory
eMMC	Embedded Multimedia Card
ESD	Electrostatic discharge
FlexCAN	Flexible Controller Area Network
FlexSPI	Flexible Serial Peripheral Interface
I2C	Inter-Integrated Circuit
IC	Integrated circuit
I2S	Inter-IC Sound
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LCDIF	Liquid Crystal Display Interface
LDO	Low-dropout regulator
LED	Light-emitting diode
LPDDR4	Low-Power Double Data Rate Gen4

Table 1. Acronyms...*continued*

Acronym	Meaning
MII	Media-Independent Interface
MPSSE	Multi-protocol synchronous serial engine
MT/s	Megatransfers per second
OS	Operating system
OTG	On-The-Go
PMIC	Power management integrated circuit
PMT	Power Measurement Tool
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media-Independent Interface
RTC	Real-time clock
SAI	Serial Audio Interface
SCU	System controller unit
SD	Secure digital
SDRAM	Synchronous dynamic random-access memory
SPI	Serial Peripheral Interface
TFT	Thin film transistor
UART	Universal Asynchronous Receiver/Transmitter
UFP	Upstream-Facing Port
USDHC	Ultra Secured Digital Host Controller
USB	Universal Serial Bus
V2X	Vehicle-to-everything
WLAN	Wireless local-area network

1.2 Related documentation

The table below lists and explains the additional documents and resources that you can refer to for more information on the board. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 2. Related documentation

Documents	Description	Link / how to obtain
i.MX 8DXL Evaluation Kit Quick Start Guide	Provides information on how to set up and boot the MCIMX8DXL-WEVK board	Available in the MCIMX8DXL-WEVK board kit
i.MX 8DualXLite/8SoloXLite Applications Processor Reference Manual	Intended for system software and hardware developers and applications programmers who want to develop products with this device	Contact NXP FAE / sales representative
i.MX 8XLite Automotive and Infotainment Applications Processors Data Sheet	Provides information about electrical characteristics, hardware design considerations, and ordering information	

Table 2. Related documentation*...continued*

Documents	Description	Link / how to obtain
i.MX 8XLite Industrial Applications Processors Data Sheet		
i.MX 8QM / i.MX 8QXP / i.MX 8DXL Hardware Developer's Guide	This purpose of this document is to help hardware engineers design and test their i.MX 8QM/8 QXP/8DXL processor-based designs. It provides information about board layout recommendations and design checklists to ensure first-pass success and avoid board bring-up problems.	
i.MX 8DXL Errata	Mask set errata to mask 0P23B	
MCIMX8DXL-WEVK design files	Board schematics, assembly layout	
i.MX Linux User's Guide	This document describes how to build and install the i.MX Linux OS BSP (where BSP stands for board support package) on the i.MX platform. It also covers special i.MX features and how to use them. The document also provides the steps to run the i.MX platform, including board DIP switch settings, and instructions on configuring and using the U-Boot boot loader.	

1.3 Kit contents

The table below lists the items included in the MCIMX8DXL-WEVK hardware kit.

Item	Description
Board	MCIMX8DXL-WEVK
AC power cord	IEC cable assembly with locking system for IEC C14 inlet, US version, 1.83 m
SD card	16 GB SD card
Power supply	12 V AC/DC, 11.5 A, level VI power supply, with 4-pin DIN output type
Worldwide adapter	Hardware accessory, universal adapter
Wi-Fi card	Wi-Fi card with Wi-Fi 6, 802.11 a/b/g/n, Bluetooth 5.2 BR/EDR/LE, SDIO 3.0 interface, SDR104 at 208 MHz, NXP 88W9098 chip
Fastner/screw	Fastner, screw M2.5x4 machine PHP SS
USB Type-C cable	USB 3.0 Type-C male to Type-A male cable assembly for serial download

1.4 Block diagram

The figure below shows the MCIMX8DXL-WEVK block diagram.

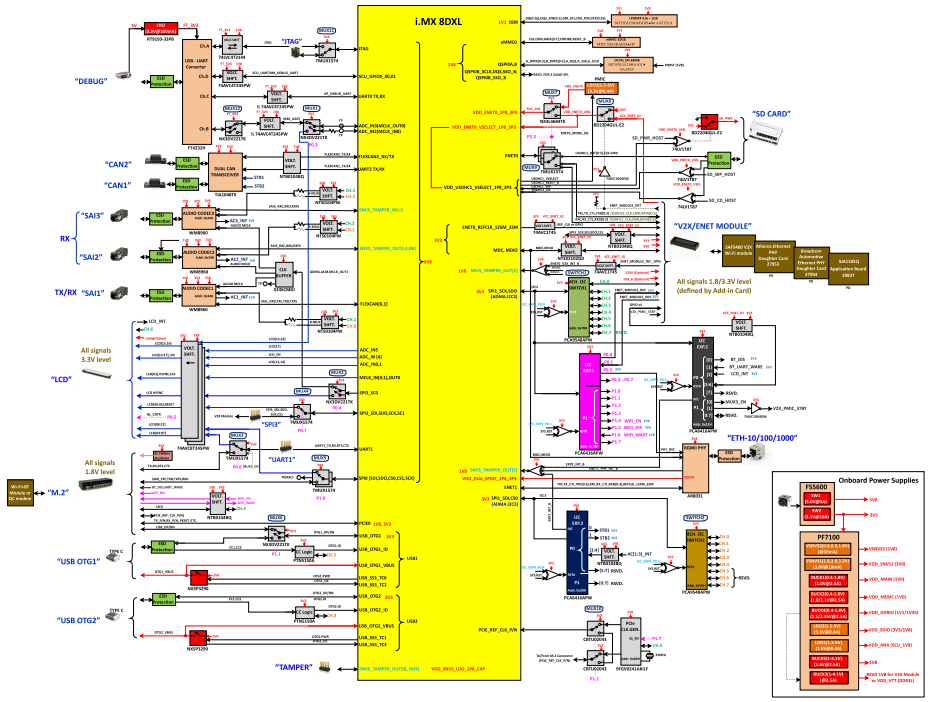

Figure 1. MCIMX8DXL-WEVK block diagram

1.5 Board features

The table below lists the features of the MCIMX8DXL-WEVK board.

Table 3. MCIMX8DXL-WEVK features

Board feature	Processor feature used	Description
Processor		NXP i.MX 8DualXLite processor (PIMX8DL1AVNFZAB), with two Arm Cortex-A35 cores each running at 1.2 GHz and one Arm Cortex-M4F core running at 264 MHz frequency. ***Note:*** *For details on MIMX8UD7DVP10SA, see i.MX 8DualXLite/8Solo XLite Applications Processor Reference Manual.*
LPDDR4	DDR controller and PHY	1 GB LPDDR4 SDRAM with 16-bit data bus and 4.266 Gbit/s data rate
Octal flash	Two FlexSPI controllers, QSPI0A and QSPI0B	512 Mbit octal SPI NOR flash memory with maximum frequency 200 MHz and operating voltage 1.8 V
eMMC	USDHC0 controller	32 GB NAND flash eMMC memory with 8-bit data bus
SD card	USDHC1 controller	SD card connector
V2X/Ethernet	ENET0, USDHC1, USDHC2, SPI2, and SNVS_TAMPER controllers	V2X/Ethernet socket for adding a V2X/Ethernet extension board
Gigabit Ethernet	ENET1 controller	An RGMII Ethernet PHY terminating at an RJ45 Gigabit Ethernet (10/100/1000 Mbit/s) connector
USB	USB_OTG1 and USB_OTG2 controllers	USB_OTG1 controller is connected to a USB 3.2 Gen 2 Type-C connector. USB_OTG2 controller is connected to another USB 3.2 Gen 2 Type-C connector or M.2 connector.

Table 3. MCIMX8DXL-WEVK features*...continued*

Board feature	Processor feature used	Description
CAN	FlexCAN1 and FlexCAN2 controllers	A high-speed dual CAN transceiver terminating at two DB9 female CAN connectors
UART	UART0 and UART1 controllers	UART0 controller is connected to the debug USB host via a USB to UART/MPSSE bridge. UART1 controller is connected to UART1 connector and M.2 connector (software-controlled).
SPI	SPI2 and SPI3 controllers	SPI2 controller is connected to a V2X/Ethernet socket. SPI3 controller is connected to SPI3 connector (software-controlled).
LCD	LCDIF controller	LCD connector with a TFT touch screen module
SAI	SAI0, SAI1, SAI2, and SAI3 controllers	SAI0 controller is connected to M.2 connector. Each of the SAI1, SAI2, and SAI3 controllers is connected to an audio codec terminating at an audio jack.
M.2	USB_OTG1, SAI0, UART1, PCIE0, PCIE_IOB controllers	M.2 Key-E mini card connector
I/O expander		Five input/output expanders for remote I/O expansion via the I2C-bus interface
I2C	I2C2, I2C3, and PMIC_I2C controllers	I2C2, I2C3, and PMIC_I2C buses for processor; FTB bus for debug USB host (via USB to UART/MPSSE bridge)
Board control and debug		A USB to UART/MPSSE bridge (connected to host computer through a USB micro-B connector), DIP switch, and JTAG header for board control and debug
Power		The board gets powered from external 12 V DC supply through a DIN connector. It has a PMIC device for managing board power. It provides six power monitors for power and energy measurement.
Clock		Six crystal oscillators and one two-output PCIe clock generator

1.6 Board pictures

The figure below shows the top-side view of the MCIMX8DXL-WEVK board, with connectors highlighted.

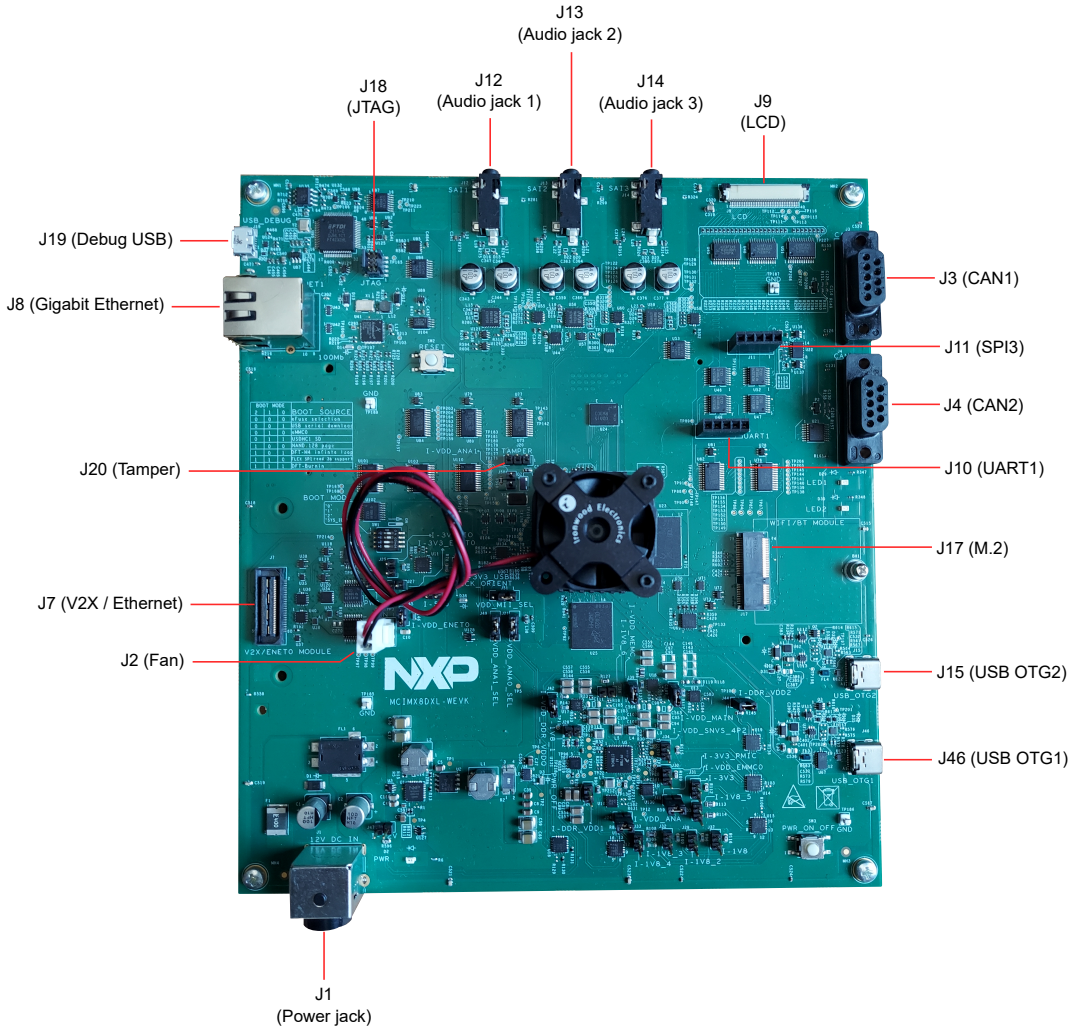

Figure 2. MCIMX8DXL-WEVK connectors (top-side view)

The figure below shows the bottom-side view of the MCIMX8DXL-WEVK board, with one connector highlighted.

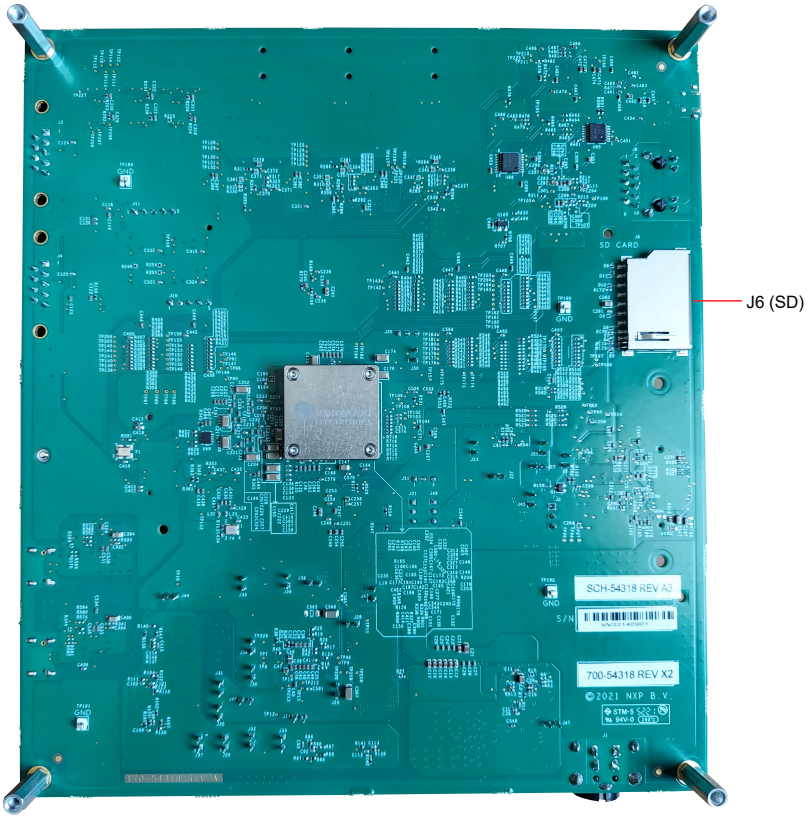

Figure 3. MCIMX8DXL-WEVK connectors (bottom-side view)

The figure below shows the board jumpers highlighted.

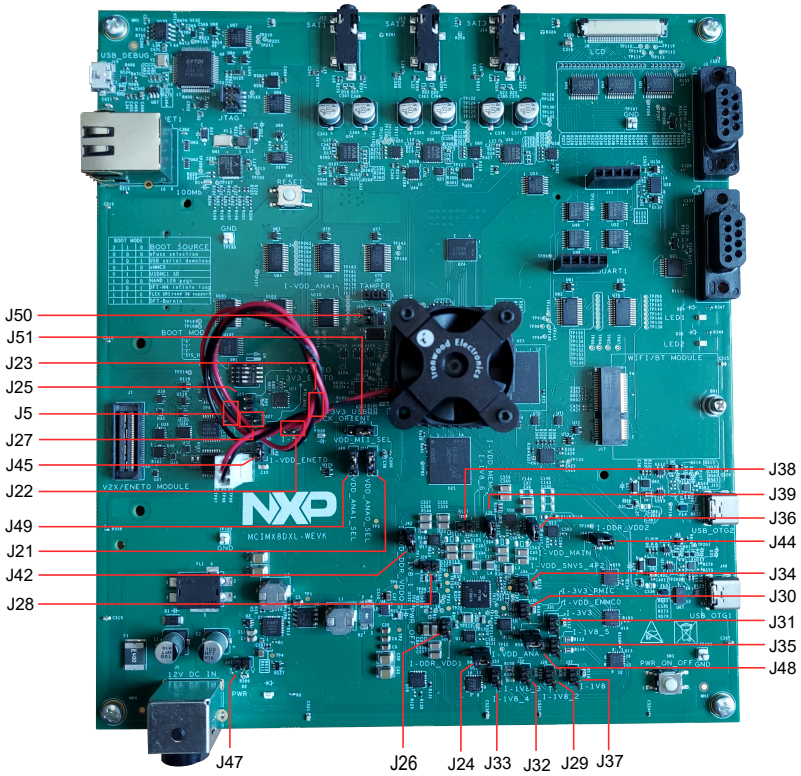

Figure 4. MCIMX8DXL-WEVK jumpers

The figure below shows the push buttons, DIP switch, and LEDs of the board highlighted.

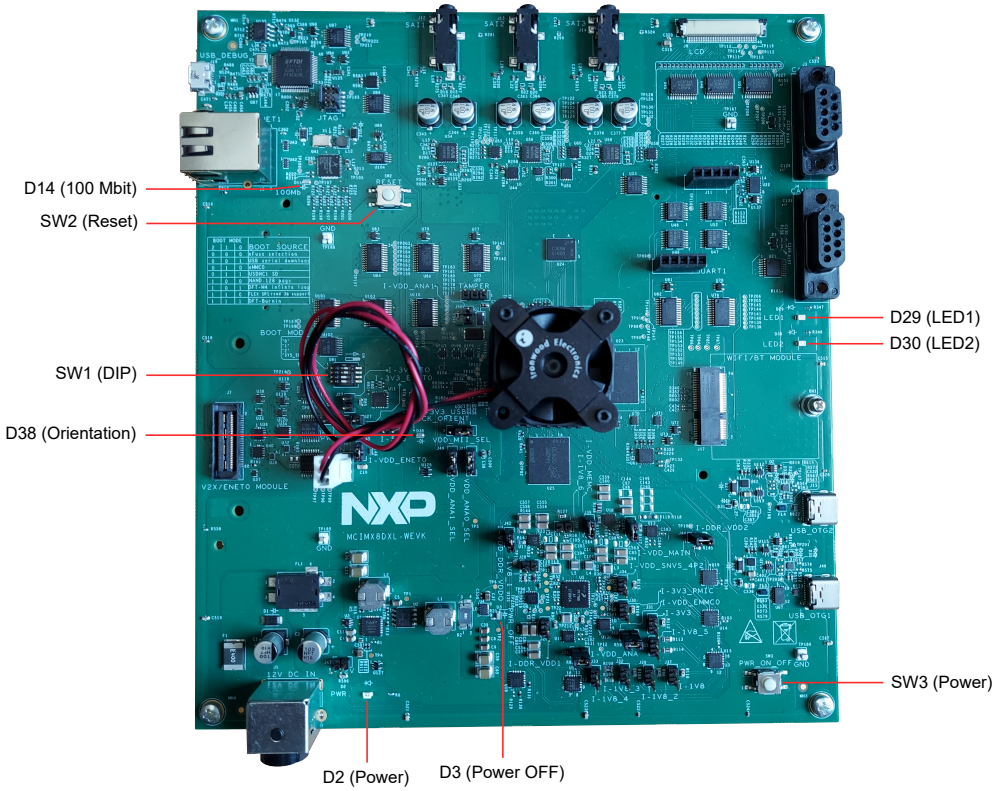

Figure 5. MCIMX8DXL-WEVK push buttons, DIP switch, and LEDs

1.7 Connectors

The table below describes the connectors of the MCIMX8DXL-WEVK board. The connectors are shown in Figure 2 and Figure 3.

Table 4. MCIMX8DXL-WEVK connectors

Part identifier	PCB label	Connector type	Description	Reference section
J1	12V DC IN	4-pin DIN connector	DC power jack	Section 2.2
J6	SD CARD	SD card receptacle	SD card slot	Section 2.7
J7	V2X/ENET0 MODULE	2x30-pin connector	V2X/Ethernet socket	Section 2.8
J8	ENET1	RJ45 connector	Gigabit Ethernet connector	Section 2.9
J46	USB_OTG1	USB 3.2 Gen 2 Type-C connector	USB OTG1 connector	Section 2.10
J15	USB_OTG2		USB OTG2 connector	
J3	CAN1	DB9 female connector	CAN1 connector	Section 2.11
J4	CAN2		CAN2 connector	
J10	UART1	5-position receptacle	UART1 connector	Section 2.12
J11	SPI3	5-position receptacle	SPI3 connector	Section 2.13
J9	LCD	40-pin connector	LCD connector	Section 2.14
J12	SAI1	5-pin audio jack	Input/output jack for audio codec 1	Section 2.15

Table 4. MCIMX8DXL-WEVK connectors*...continued*

Part identifier	PCB label	Connector type	Description	Reference section
J13	SAI2		Input/output jack for audio codec 2	
J14	SAI3		Input/output jack for audio codec 3	
J17	WIFI/BT MODULE	75-pin M.2 connector	M.2 Key-E mini card connector	Section 2.16
J19	USB_DEBUG	USB 2.0 micro-B connector	Debug USB connector	Section 2.19.3
J18	JTAG	2x5-pin header	JTAG header	Section 2.19.4
J2	FAN	1x3-pin header	Fan header with lock	For more information on these connectors, see MCIMX8DXL-WEVK schematics
J20	TAMPER	1x3-pin header	Allows remote tamper detection of the processor	

1.8 Jumpers

The table below describes the jumpers of the MCIMX8DXL-WEVK board. The jumpers are shown in Figure 4.

Table 5. MCIMX8DXL-WEVK jumpers

Part identifier	PCB label	Jumper type	Description	Reference section
J22	I-5V0	1x2-pin header	5V0 supply current measurement disable jumper: • Open (default setting): 5V0 supply current is measured by onboard power monitor U11 • Shorted: Current measurement is disabled for 5V0 supply	Section 2.2.1
J23	I-3V3_USB	1x2-pin header	3V3_USB supply current measurement disable jumper: • Open (default setting): 3V3_USB supply current is measured by onboard power monitor U11 • Shorted: Current measurement is disabled for 3V3_USB supply	
J25	I-3V3_IO	1x2-pin header	3V3_IO supply current measurement disable jumper: • Open (default setting): 3V3_IO supply current is measured by onboard power monitor U11 • Shorted: Current measurement is disabled for 3V3_IO supply	
J27	I-3V3_ENET0	1x2-pin header	VDD_ENET0_VSEL- supply current measurement disable jumper: • Open (default setting): VDD_ENET0_VSEL- supply current is measured by onboard power monitor U11	

Table 5. MCIMX8DXL-WEVK jumpers*...continued*

Part identifier	PCB label	Jumper type	Description	Reference section
			• Shorted: Current measurement is disabled for VDD_ENET0_ VSEL- supply	
J24	I-VDD_ANA	1x2-pin header	VDD_ANA supply current measurement disable jumper: • Open: VDD_ANA supply current is measured by onboard power monitor U12 • Shorted (default setting): Current measurement is disabled for VDD_ANA supply	
J26	I-DDR_VDD1	1x2-pin header	DDR_VDD1 supply current measurement disable jumper: • Open (default setting): DDR_ VDD1 supply current is measured by onboard power monitor U12 • Shorted: Current measurement is disabled for DDR_VDD1 supply	
J28	I-1V8_1	1x2-pin header	1V8_1 supply current measurement disable jumper: • Open (default setting): 1V8_1 supply current is measured by onboard power monitor U12 • Shorted: Current measurement is disabled for 1V8_1 supply	
J29	I-1V8_2	1x2-pin header	1V8_2 supply current measurement disable jumper: • Open (default setting): 1V8_2 supply current is measured by onboard power monitor U12 • Shorted: Current measurement is disabled for 1V8_2 supply	
J30	I-3V3_PMIC	1x2-pin header	3V3_PMIC supply current measurement disable jumper: • Open (default setting): 3 V3_PMIC supply current is measured by onboard power monitor U14 • Shorted: Current measurement is disabled for 3V3_PMIC supply	
J31	I-3V3	1x2-pin header	3V3 supply current measurement disable jumper: • Open (default setting): 3V3 supply current is measured by onboard power monitor U14 • Shorted: Current measurement is disabled for 3V3 supply	

Table 5. MCIMX8DXL-WEVK jumpers*...continued*

Part identifier	PCB label	Jumper type	Description	Reference section
J34	I-VDD_SNVS_4P2	1x2-pin header	VDD_SNVS1 supply current measurement disable jumper: • Open (default setting): VDD_SNVS1 supply current is measured by onboard power monitor U14 • Shorted: Current measurement is disabled for VDD_SNVS1 supply	
J36	I-VDD_MAIN	1x2-pin header	VDD_MAIN supply current measurement disable jumper: • Open: VDD_MAIN supply current is measured by onboard power monitor U14 • Shorted (default setting): Current measurement is disabled for VDD_MAIN supply	
J32	I-1V8_3	1x2-pin header	1V8_3 supply current measurement disable jumper: • Open (default setting): 1V8_3 supply current is measured by onboard power monitor U15 • Shorted: Current measurement is disabled for 1V8_3 supply	
J33	I-1V8_4	1x2-pin header	1V8_4 supply current measurement disable jumper: • Open (default setting): 1V8_4 supply current is measured by onboard power monitor U15 • Shorted: Current measurement is disabled for 1V8_4 supply	
J35	I-1V8_5	1x2-pin header	1V8_5 supply current measurement disable jumper: • Open (default setting): 1V8_5 supply current is measured by onboard power monitor U15 • Shorted: Current measurement is disabled for 1V8_5 supply	
J37	I-1V8	1x2-pin header	1V8 supply current measurement disable jumper: • Open (default setting): 1V8 supply current is measured by onboard power monitor U15 • Shorted: Current measurement is disabled for 1V8 supply	
J38	I-1V8_6	1x2-pin header	1V8_6 supply current measurement disable jumper: • Open (default setting): 1V8_6 supply current is measured by onboard power monitor U18	

Table 5. MCIMX8DXL-WEVK jumpers*...continued*

Part identifier	PCB label	Jumper type	Description	Reference section
			• Shorted: Current measurement is disabled for 1V8_6 supply	
J50	I-VDD_ANA1	1x2-pin header	Processor VDD_ANA1_1 P8 power domain current measurement disable jumper: • Open (default setting): Processor VDD_ANA1_1 P8 power domain current is measured by onboard power monitor U18 • Shorted: Current measurement is disabled for VDD_ANA1_1P8 power domain of the processor	
J48	I-VDD_EMMC0	1x2-pin header	Processor VDD_EMMC0_1 P8_3P3 power domain current measurement disable jumper: • Open: Processor VDD_EMMC0_1P8_3P3 power domain current is measured by onboard power monitor U18 • Shorted (default setting): Current measurement is disabled for VDD_EMMC0_1 P8_3P3 power domain of the processor	
J47	I-12V	1x2-pin header	12V0 supply current measurement disable jumper: • Open (default setting): 12V0 supply current is measured by onboard power monitor U18 • Shorted: Current measurement is disabled for 12V0 supply	
J39	I-VDD_MEMC	1x2-pin header	VDD_MEMC supply current measurement disable jumper: • Open: VDD_MEMC supply current is measured by onboard power monitor U19 • Shorted (default setting): Current measurement is disabled for VDD_MEMC supply	
J42	I-VDD_DDR_VDDQ	1x2-pin header	VDD_DDR_VDDQ supply current measurement disable jumper: • Open: VDD_DDR_VDDQ supply current is measured by onboard power monitor U19 • Shorted (default setting): Current measurement is disabled for VDD_DDR_VDDQ supply	
J44	I-DDR_VDD2	1x2-pin header	DDR_VDD2 supply current measurement disable jumper:	

Table 5. MCIMX8DXL-WEVK jumpers*...continued*

Part identifier	PCB label	Jumper type	Description	Reference section
			• Open: DDR_VDD2 supply current is measured by onboard power monitor U19 • Shorted (default setting): Current measurement is disabled for DDR_VDD2 supply	
J45	I-VDD_ENET0	1x2-pin header	VDD_ENET0 supply current measurement disable jumper: • Open: VDD_ENET0 supply current is measured by onboard power monitor U19 • Shorted (default setting): Current measurement is disabled for VDD_ENET0 supply	
J21	VDD_ANA0_SEL	1x3-pin header	Processor VDD_ANA0_1P8 source power supply selection jumper: • Pins 1-2 shorted (default setting): Processor analog supply VDD_ANA0_1P8 gets powered from VDD_ANA supply • Pins 2-3 shorted: VDD_ANA0_1P8 gets powered from 1V8_1 supply	For more information on these jumpers, see MCIMX8DXL-WEVK schematics
J49	VDD_ANA1_SEL	1x3-pin header	Processor VDD_ANA1_1P8 source power supply selection jumper: • Pins 1-2 shorted (default setting): Processor analog supply VDD_ANA1_1P8 gets powered from VDD_ANA supply • Pins 2-3 shorted: VDD_ANA1_1P8 gets powered from 1V8_1 supply	
J51	VDD_MII_SEL	1x3-pin header	MDC/MDIO voltage selection jumper: • 1-2 shorted (default setting): Use this jumper setting if module connected to V2X/ENET0 socket uses 3.3 V for MDC/MDIO signal pair • 2-3 shorted: Use this jumper setting if the connected module provides MDC/MDIO voltage	
J5	PWR_TEST	1x2-pin header	Force enable onboard power supplies jumper: • Open (default setting): If the processor was installed with correct orientation during assembly, then onboard power supplies are enabled during	

Table 5. MCIMX8DXL-WEVK jumpers*...continued*

Part identifier	PCB label	Jumper type	Description	Reference section
			power-on; otherwise, onboard power supplies are disabled during power-on • Shorted: Onboard power supplies are enabled during power-on, irrespective of processor orientation. This jumper setting allows to test onboard power supplies before installing the processor during board manufacturing. ***CAUTION:*** *Do not short jumper J5 if the processor is installed on the board. Shorting this jumper with processor installed may cause unrecoverable damage to the processor.*	

1.9 Push buttons

The table below describes the push buttons of the MCIMX8DXL-WEVK board. The push buttons are shown in Figure 5.

Table 6. MCIMX8DXL-WEVK push buttons

Part identifier	PCB label	Button name	Description
SW2	RESET	Reset button	Pressing this button resets the system and begins a boot sequence
SW3	PWR_ON_OFF	Power ON/OFF button	To turn ON power, press and hold this button for 0.5 seconds. To turn OFF power, press and hold the button for 5 seconds.

1.10 DIP switch

The MCIMX8DXL-WEVK board has a dual inline package (DIP) switch SW1, which has a set of four switches: SW1[1:4].

SW1[1:3] are used for selecting boot mode and they are connected to the i.MX 8DXL processor pins SCU_BOOT_MODE[0:2], respectively.

SW1[4] is used for controlling system ID memory write protection and it is connected to the debug USB host through the I2C-bus interface of the USB to UART/MPSSE bridge.

For each switch within the DIP switch:

- "OFF" setting corresponds to 0
- "ON" setting corresponds to 1

The table below describes the DIP switch settings. The DIP switch is shown in Figure 5.

Table 7. DIP switch settings

Switches	Supported function	Description
SW1[1:3]	Boot mode selection	SW1[3:1] (SW_BOOT_MODE[2:0]): • 000: Processor internal eFuse (default setting)

Table 7. DIP switch settings*...continued*

Switches	Supported function	Description
		• 001: USB serial download (processor can download a program image from a USB connection) • 010: EMMC0 • 011: USDHC1: SD card • 100: NAND, 128 pages • 101: Reserved • 110: FlexSPI • 111: Reserved
SW1[4]	System ID memory write protection control	• 0: Both read and write operations are allowed into system ID memory U104 (default setting) • 1: System ID memory is write-protected, only read operation is allowed

Note: *For more details on i.MX 8DXL boot modes and boot mode configuration, see "System Boot" chapter of i.MX 8DualXLite/8SoloXLite Applications Processor Reference Manual.*

1.11 LEDs

The MCIMX8DXL-WEVK board provides six light-emitting diodes (LEDs) for monitoring system functions, such as power-on, reset, and board faults. The information collected from LEDs can be used for debugging purposes.

The table below describes the MCIMX8DXL-WEVK LEDs. The LEDs are shown in Figure 5.

Table 8. MCIMX8DXL-WEVK LEDs

Part identifier	PCB label	LED color	Associated function	Description (when LED is ON)
D2	PWR	Green	Board power ON status	Board is powered ON
D3	PWR_OFF	Red	Board power OFF status	Board is powered OFF
D38	CHECK_ ORIENT	Red	Processor orientation error	The processor is rotated by 90°, 180°, or 270° from pin 1 orientation. To protect the processor, board and processor power supplies have been shut down.
D14	100Mb	Red	100 Mbit/s Ethernet link connection error	100 Mbit/s Ethernet link connection is active from RGMII PHY transceiver; 1000 Mbit/s (1 Gbit/s) Ethernet link connection is disabled
D29	LED1	Green	User LED 1	
D30	LED2	Green	User LED 2	

2 Functional description

This section describes the features and functions of the MCIMX8DXL-WEVK board.

Note: *For details of the i.MX 8DXL processor features, see i.MX 8DualXLite/8SoloXLite Applications Processor Reference Manual.*

2.1 Processor

The i.MX 8DualXLite (8DXL) applications processor is a member of the i.MX 8 family. This series of applications processors is focused on offering powerful solutions and multiple possibilities of development on projects with advanced graphics and safety-critical applications. More specifically, the i.MX 8DXL is a device that targets the automotive and industrial market segments and offers the possibility of a wide variety of embedded applications.

The chip has a flexible architecture allowing both high performance and low power consumption. It features two Arm Cortex-A35 cores, in addition to one Arm Cortex-M4F general-purpose core. The device includes V2X capabilities, as well as TSN networking and telematics.

For more information about the i.MX 8DXL processor, see the *i.MX 8DualXLite/8SoloXLite Applications Processor Reference Manual* and *i.MX 8XLite Automotive and Infotainment Applications Processors Data Sheet*.

2.2 Power supply

The MCIMX8DXL-WEVK board has the following primary power supplies:

- External 12 V DC power supply through 4-pin DIN connector J1
- External 5 V DC power supply through USB micro-B connector J19

These primary power supplies are used to produce secondary power supplies on the board to power the board components, including the i.MX 8DXL processor, power regulators, clock generator, LPDDR4 memory, octal flash memory, eMMC memory, V2X/Ethernet socket, Gigabit Ethernet PHY, CAN transceiver, LCD connector, audio codecs, M.2 connector, USB to UART/MPSSE bridge, JTAG header, DIP switch, and LEDs.

The figure below shows the MCIMX8DXL-WEVK power supply diagram.

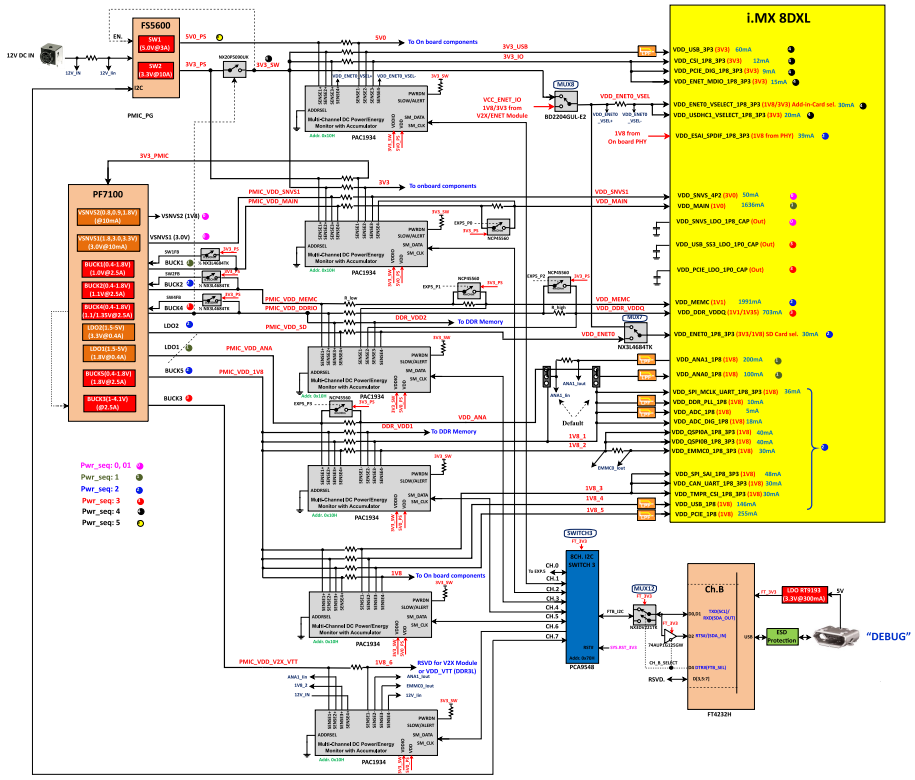

Figure 6. Power supply diagram

The table below describes the MCIMX8DXL-WEVK power supplies.

Table 9. MCIMX8DXL-WEVK power supplies

Power source	Manufacturer and part number	Power supply	Description
External 12 V DC supply through 4-pin DIN connector J1		12V0 (12 V)	• Supplies power to i.MX 8DXL processor, fan header J2, and power regulator U1 • Alternative 12 V power for V2X/Ethernet socket
Power regulator U1	NXP MFS5600 AMMA7ES	SW1: 5V0_PS (5 V)	• Supplies LDO2 power to PMIC • Produces 5V0 supply
		SW2: 3V3_PS (3.3 V)	• Supplies power to LEDs (D2 and D3), MUX13 (U102), PMIC loopback switches (U130 and U131), and power switches (U10, U13, U16, and U17) • Produces 3V3_PMIC supply • Produces 3V3_SW supply
From 5V0_PS supply		5V0 (5 V)	• Supplies power to LCD connector (J9) and programmable-current USB switches (U62 and U65) • Supplies 5 V power to CAN transceiver, V2X/ Ethernet socket, and audio codecs 1, 2, and 3
From 3V3_PS supply		3V3_PMIC (3.3 V)	Supplies SW1, SW2, SW3, SW4, SW5, LDO1, and VIN power to PMIC
From 3V3_PS supply through power switch U4		3V3_SW (3.3 V)	• Supplies 3.3 V power to MUX8 U39 • Produces 3V3 supply • Produces 3V3_USB supply

Table 9. MCIMX8DXL-WEVK power supplies*...continued*

Power source	Manufacturer and part number	Power supply	Description
			• Produces 3V3_IO supply • One of the source power supplies for VDD_ENET0_VSEL+ supply • One of the source power supplies for VDD_ENET0_VSEL- supply
From 3V3_SW supply		3V3 (3.3 V)	• Supplies power to M.2 connector, EXPANDER1 (U80), EXPANDER2 (U84), EXPANDER3 (U82), EXPANDER4 (U110), MUX1 (U44), MUX2 (U50), MUX3 (U49), MUX4 (U52), MUX5 (U46 and U47), MUX6 (U67), MUX7 (U34), MUX9 (U26, U29, and U31), MUX11 (U86), SWITCH1 (U75), SWITCH2 (U76), voltage translators (U21, U30, U35, U36, U40, U45, U48, U51, U55, U68, and U74), inverter ICs (U38, U73, U112, U128, U136, and U137), logic gates (U72, U77, U78, U79, U81, U83, U113, and U116), configuration channel logic chips (U114 and U117), differential 2:1 switches (U70 and U71), power switch (U32), and 2:1 switch (U134) • Supplies 3.3 V power to eMMC memory, CAN transceiver, Gigabit Ethernet PHY, V2X/Ethernet socket, and audio codecs 1, 2, and 3 • 3V3 supply is filtered to produce AVDD33 power for Gigabit Ethernet PHY • 3V3 supply is filtered to produce VBUS power for programmable-current USB switches U62 and U65
From 3V3_SW supply		3V3_USB (3.3 V)	Supplies 3.3 V power to i.MX 8DXL USB
From 3V3_SW supply		3V3_IO (3.3 V)	Supplies 3.3 V power to i.MX 8DXL ENET0, uSDHC, SPI1, and PCIe
From pin 57 of V2X/ ENET0 socket (J7)		VCC_ENET_IO (3.3/1.8 V)	• Supplies power to voltage translators U35, U36, U37, and U40 • Supplies 3.3/1.8 V power to MUX8 U39 • Another source power supply for VDD_ENET0_VSEL+ supply • Alternative power supply for voltage translator U30
From 3V3_SW supply or VCC_ ENET_IO supply		VDD_ENET0_VSEL+ (3.3/1.8 V)	Another source power supply for VDD_ENET0_VSEL- supply
From 3V3_SW supply or VDD_ ENET0_VSEL+ supply		VDD_ENET0_VSEL- (3.3/1.8 V)	• Supplies power to logic gates U118, U119, and U120 • Supplies another 3.3 V power to i.MX 8DXL ENET0
Power management integrated circuit (PMIC) U5	NXP PPF7100 BVMA1ES	SW1: PMIC_VDD_ MAIN (1 V at 2.5 A)	Produces VDD_MAIN supply
		SW2: PMIC_VDD_ MEMC (1.1 V at 2.5 A)	Produces VDD_MEMC supply

Table 9. MCIMX8DXL-WEVK power supplies*...continued*

Power source	Manufacturer and part number	Power supply	Description
		SW3: PMIC_VDD_V2X_VTT (1.8 V at 2.5 A)	Produces 1V8_6 supply
		SW4: PMIC_VDD_DDRIO (1.1 V at 2.5 A)	• Produces VDD_DDR_VDDQ supply • Produces DDR_VDD2 supply
		SW5: PMIC_VDD_1V8 (1.8 V at 2.5 A)	• Produces DDR_VDD1 supply • Produces 1V8_1 supply • Produces 1V8_2 supply • Produces 1V8_3 supply • Produces 1V8_4 supply • Produces 1V8_5 supply • Produces 1V8 supply
		LDO1: PMIC_VDD_ANA (1.8 V at 0.4 A)	Produces VDD_ANA supply
		LDO2: PMIC_VDD_SD (3.3/1.8 V at 0.4 A)	Produces VDD_ENET0 supply
		VSNVS1: PMIC_VDD_SNVS1 (3 V at 10 mA)	Produces VDD_SNVS1 supply
		VSNVS2: PMIC_VDD_SNVS2 (1.8 V at 10 mA)	Supplies power to voltage translators (U125 and U132), logic gates (U106 and U108), buffer / line driver (U107), and inverter IC (U109)
From PMIC_VDD_MAIN supply		VDD_MAIN (1 V at 2.5 A)	Supplies power to VDD_MAIN power domain of the i.MX 8DXL processor
From PMIC_VDD_MEMC supply		VDD_MEMC (1.1 V at 2.5 A)	Supplies power to VDD_MEMC power domain of the i.MX 8DXL processor
From PMIC_VDD_V2X_VTT supply		1V8_6 (1.8 V at 2.5 A)	Alternative 1.8 V power for V2X/Ethernet socket
From PMIC_VDD_DDRIO supply		VDD_DDR_VDDQ (1.1 V at 2.5 A)	Supplies power to VDD_DDR_VDDQ power domain of the i.MX 8DXL processor
From PMIC_VDD_DDRIO supply		DDR_VDD2 (1.1 V at 2.5 A)	Supplies VDD2 and VDDQ power to LPDDR4 memory
From PMIC_VDD_1V8 supply		DDR_VDD1 (1.8 V at 2.5 A)	Supplies VDD1 power to LPDDR4 memory
From PMIC_VDD_1V8 supply		1V8_1 (1.8 V at 2.5 A)	• Supplies power to i.MX 8DXL ENET1, UART0/LCDIF, UART1, SPI3, and MCLK • Supplies power to VDD_DDR_PLL power domain of the i.MX 8DXL processor • Alternative supply for VDD_ANA0_1P8 and VDD_ANA1_1P8 power domains of the i.MX 8DXL processor
From PMIC_VDD_1V8 supply		1V8_2 (1.8 V at 2.5 A)	• Supplies power to octal flash memory and i.MX 8DXL QSPI and eMMC • Supplies 1.8 V power to eMMC memory

Table 9. MCIMX8DXL-WEVK power supplies*...continued*

Power source	Manufacturer and part number	Power supply	Description
From PMIC_VDD_1 V8 supply		1V8_3 (1.8 V at 2.5 A)	Supplies power to i.MX 8DXL SNVS, FlexCAN, UART0, and SPI0
From PMIC_VDD_1 V8 supply		1V8_4 (1.8 V at 2.5 A)	Supplies 1.8 V power to i.MX 8DXL USB
From PMIC_VDD_1 V8 supply		1V8_5 (1.8 V at 2.5 A)	Supplies 1.8 V power to i.MX 8DXL PCIe
From PMIC_VDD_1 V8 supply		1V8 (1.8 V at 2.5 A)	• Supplies power to PCIe clock generator (U69), clock buffer (U57), logic gates (U121 and U126), voltage translator/buffer (U85), and voltage translators (U21, U37, U45, U48, U51, U53, U55, U58, U60, U68, U74, and U96) • Supplies 1.8 V power to audio codecs 1, 2, and 3
From PMIC_VDD_ ANA supply		VDD_ANA (1.8 V at 0.4 A)	• Supplies power to JTAG header (J18), voltage translator (U97), buffer / line driver (U92), and inverter IC (U127) • Supplies 1.8 V power to DIP switch SW1 and EXPANDER4 U110 • Supplies power to VDD_ANA0_1P8 and VDD_ ANA1_1P8 power domains of the i.MX 8DXL processor
From PMIC_VDD_ SD supply		VDD_ENET0 (3.3/1. 8 V at 0.4 A)	Supplies 3.3/1.8 V power to MUX7 U34
From PMIC_VDD_ SNVS1 supply		VDD_SNVS1 (3 V at 10 mA)	• Supplies power to processor reset IC U105 • Supplies power to VDD_SNVS power domain of the i.MX 8DXL processor
External 5 V DC supply through USB micro-B connector J19		DBG_5V0 (5 V)	• Supplies VDD power to power monitors U11, U12, U14, U15, U18, and U19 • Filtered DBG_5V0 power is supplied to LDO regulator U87 to produce FT_3V3 supply
LDO regulator U87	Richtek RT9193	FT_3V3 (3.3 V)	• Supplies power to system ID memory, EXPANDER5 (U101), MUX12 (U95), SWITCH3 (U103), voltage translator/buffer (U85), voltage translators (U96, U97, U125, and U132), buffers / line drivers (U89 and U129), and inverter IC (U98) • Supplies 3.3 V power to DIP switch SW1 and USB to UART/MPSSE bridge • Supplies VDD_I/O power to power monitors U11, U12, U14, U15, U18, and U19
From pin 49 of USB to UART/MPSSE bridge (U90)		FT_1V8 (1.8 V)	• Supplies power to buffer / line driver U94 • Supplies 1.8 V power to USB to UART/MPSSE bridge

The figure below shows the MCIMX8DXL-WEVK power-up sequence.

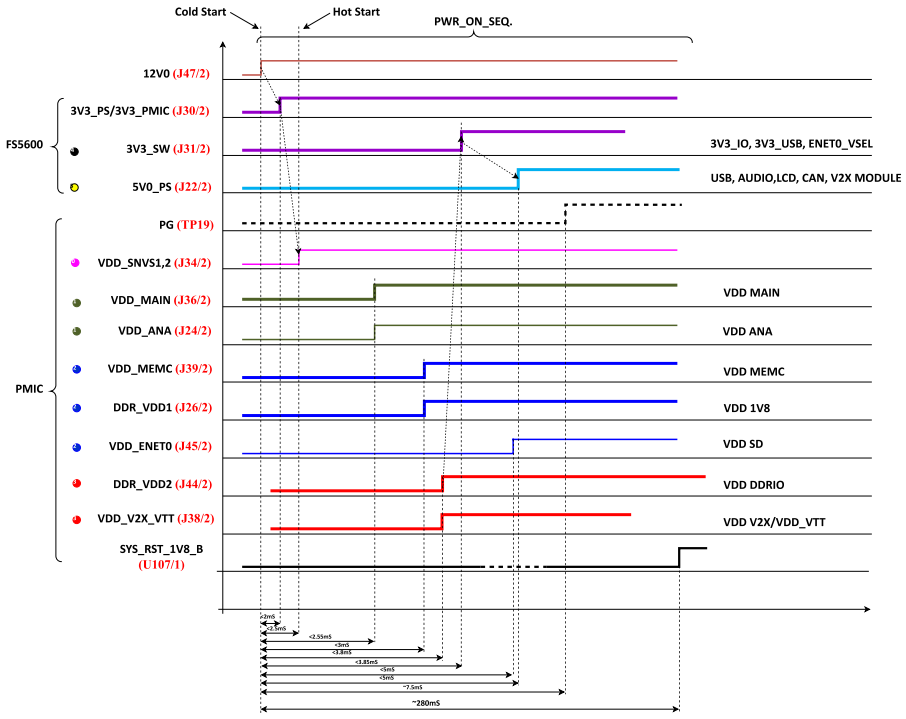

Figure 7. Power supply sequence

2.2.1 Current measurement

The MCIMX8DXL-WEVK board provides the following six quad-channel power monitors for onboard current/power measurement:

- U11
- U12
- U14
- U15
- U18
- U19

Each power monitor is a PAC1934T-I/JQ device from Microchip Technology.

The table below lists the power supplies that can be measured by the power monitors. For each measurable power supply, current measurement can be disabled using a 2-pin jumper. To reduce voltage drop during power-on, current measurement is disabled for some of the power supplies, by default.

Table 10. Measurable power supplies

Power monitor	Measurable power supply	Current sense resistors	Current measurement disable jumper	Default jumper setting
U11	5V0	R76	J22	Open
	3V3_USB	R78	J23	Open
	3V3_IO	R85	J25	Open
	VDD_ENET0_VSEL-	R91	J27	Open

Table 10. Measurable power supplies*...continued*

Power monitor	Measurable power supply	Current sense resistors	Current measurement disable jumper	Default jumper setting
U12	VDD_ANA	R82	J24	Shorted
	DDR_VDD1	R90	J26	Open
	1V8_1	R92 and R93	J28	Open
	1V8_2	R96	J29	Open
U14	3V3_PMIC	R109	J30	Open
	3V3	R112	J31	Open
	VDD_SNVS1	R115	J34	Open
	VDD_MAIN	R117, R118, and R119	J36	Shorted
U15	1V8_3	R100	J32	Open
	1V8_4	R108 and R105	J33	Open
	1V8_5	R113 and R114	J35	Open
	1V8	R116	J37	Open
U18	1V8_6	R127	J38	Open
	Processor VDD_ ANA1_1P8 power domain	R598	J50	Open
	Processor VDD_ EMMC0_1P8_3P3 power domain	R597	J48	Shorted
	12V0	R596	J47	Open
U19	VDD_MEMC	R135 and R136	J39	Shorted
	VDD_DDR_VDDQ	R143 and R144	J42	Shorted
	DDR_VDD2	R145	J44	Shorted
	VDD_ENET0	R146	J45	Shorted

2.2.2 Power measurement applications

You can use the following two applications to acquire real-time power data from the board. Both the applications are available for download at GitHub.

- BCU software: A command-line tool, designed to control boards/platforms that support remote control and power measurement. It provides functions such as on/off key operation, board reset, setting boot mode, JTAG debug, and power measurement through the USB debug port.
- PMT software: A GUI-based tool, with features similar to BCU. With additional GUI feature, it also allows real-time profiling of power supplies, such as graphical monitoring of power, voltage, and current.

The sampling rate achieved on BCU is higher than on PMT due to the GUI processing on PMT.

- Due to the higher sampling rate, BCU is used for power acquisition where fine live monitoring is not the primary purpose. For example, remote acquisition.
- Due to enhanced GUI, PMT is used for live power monitoring activities during system design, debug phases, and also post-processing analysis.

Power acquisitions made using BCU can be imported into PMT for post-processing analysis to combine the benefits of both applications, that is higher sampling resolution of BCU, and enhanced visibility of power supply activities of PMT.

For more information about BCU and PMT, see the BCU release note in GitHub and *i.MX Power Measurement Tool Application Note* (AN13119).

2.3 Clocks

The MCIMX8DXL-WEVK board provides all the clocks required for the processor and peripheral interfaces. The following table summarizes the specifications of each clock and the component that provides it.

Table 11. MCIMX8DXL-WEVK clocks

Clock generator	Manufacturer and part number	Clock	Frequency	Destination
Quartz crystal X1		ATH_[XTLI, XTLO]	25 MHz	Gigabit Ethernet PHY
Crystal oscillator Y1		BT_OSC_32KHZ	32.768 kHz	M.2 connector
Quartz crystal Y2		FT_[OSCI, OSCO]	12 MHz	USB to UART/MPSSE bridge
Quartz crystal Y3		24M_[XTALI, XTALO]	24 MHz	i.MX 8DXL processor
Quartz crystal QZ1		RTC_[XTALI, XTALO]	32.768 kHz	i.MX 8DXL processor (RTC)
Quartz crystal Y4		PCIE_XTAL_[X1, X2]	25 MHz	PCIe clock generator U69
i.MX 8DXL processor U20	NXP PIMX8DL1 AVNFZAB	PCIE_REF_CLK_[P, N]	100 MHz	If the value of the PCI_CLK_SEL signal from EXPANDER1 is 1, then the processor provides reference clock to M.2 module or vice versa. If the value of the PCI_CLK_SEL signal is 0, then PCIe clock generator U69 provides reference clock to the processor and M.2 module.
Clock generator U69	Renesas 9FGV0241 AKILF	REFCLK1_[P, N]	100 MHz	
		REFCLK2_[P, N]	100 MHz	

2.4 LPDDR4 memory

The MCIMX8DXL-WEVK board has a Low-Power Double Data Rate Gen4 (LPDDR4) memory chip, which is connected to the DDR interface of the i.MX 8DXL processor. The table below describes the LPDDR4 memory.

Table 12. LPDDR4 memory

Part identifier	Manufacturer and part number	Description
U23	Micron Technology MT53D512M16D1 DS-046 AAT ES:D	1 GB (8 Gbit) LPDDR4 synchronous dynamic random-access memory (SDRAM) with 16-bit data bus and 4266 MT/s data rate. With the i.MX 8DXL processor, the LPDDR4 memory runs at 2400 MT/s.

2.5 Octal flash memory

The MCIMX8DXL-WEVK board has an octal flash memory chip, which is connected to two FlexSPI controllers of the i.MX 8DXL processor. The table below describes the octal flash memory.

Table 13. Octal flash memory

Processor controllers	Octal flash memory		
	Part identifier	Manufacturer and part number	Description
QSPI0A and QSPI0B	U24	Micron Technology MT35 XU512ABA1G12-0AAT	512 Mbit (64 Mbit x 8) octal serial peripheral interface (SPI) NOR flash memory with maximum frequency 200 MHz and operating voltage 1.8 V

2.6 eMMC memory

The MCIMX8DXL-WEVK board has an Embedded Multimedia Card (eMMC) memory chip, which is connected to one of the three USDHC controllers of the i.MX 8DXL processor that supports eMMC 5.1 devices: USDHC0. The table below describes the eMMC memory.

Table 14. eMMC memory

Processor controller	eMMC memory		
	Part identifier	Manufacturer and part number	Description
USDHC0	U25	Micron Technology MTFC32 GAPALGT-AIT	32 GB NAND flash eMMC memory with 8-bit data bus

2.7 SD card connector

The MCIMX8DXL-WEVK board provides a secure digital (SD) connector for inserting an SD card. The SD connector is connected to one of the three USDHC controllers of the i.MX 8DXL processor that supports SD devices: USDHC1. USDHC1 and USDHC2 signals are multiplexed with ENET0 signals on the processor.

The figure below shows the MCIMX8DXL-WEVK SD implementation diagram.

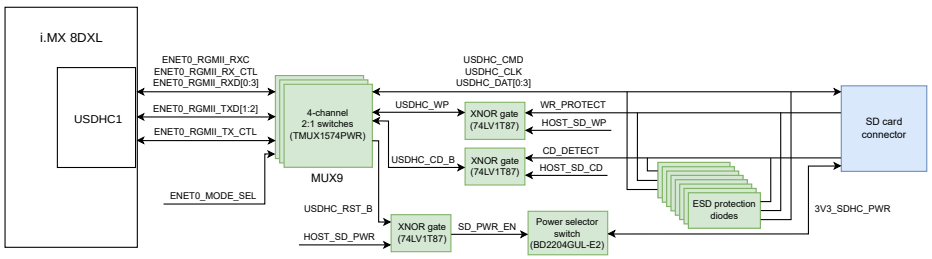

Figure 8. SD diagram

The table below details the SD connections.

Table 15. SD connections

Processor controller	Peripheral devices		
	Part identifiers	Manufacturer and part number	Description
USDHC1	U26, U29, and U31	Texas Instruments TMUX1574PWR	A set of three 4-channel, 2:1 mux/demux switches, referred as *MUX9*, which drives signals between the processor and SD connector or V2X/Ethernet socket
	U118, U119, and U120	Nexperia 74LV1T87	Three two-input XNOR gates. U118 and U119 drive write-protect and card-detect signals, respectively, from SD connector to MUX9. U120 is used to

Table 15. SD connections...*continued*

Processor controller	Peripheral devices		
	Part identifiers	Manufacturer and part number	Description
			enable/disable power selector switch for SD connector.
	U32	Rohm Semiconductor BD2204GUL-E2	Power supply selector switch for SD connector
	J6		SD connector for housing an SD card. Electrostatic discharge (ESD) diodes are used to protect the signals to/from the SD card against discharges.

Based on the value of the ENET0_MODE_SEL signal from EXPANDER1, MUX7 and MUX9 drive either SD card signals or V2X module signals (Dual-USDHC mode). For more information, see Section 2.17.

2.8 V2X/Ethernet socket

The MCIMX8DXL-WEVK board has a 2x30-pin vehicle-to-everything (V2X) / Ethernet socket J7 for plugging a V2X/Ethernet module.

The V2X/Ethernet socket is connected to ENET0, USDHC1, USDHC2, SPI2, and SNVS_TAMPER controllers of the i.MX 8DXL processor. USDHC1 and USDHC2 signals are multiplexed with ENET0 controller signals on the processor. SPI2 signals are multiplexed with USDHC1 controller signals on the processor.

Based on the value of the ENET0_MODE_SEL signal from EXPANDER1, MUX7 and MUX9 drive either SD card signals or V2X module signals (Dual-USDHC mode). For more information, see Section 2.17.

The table below provides pinout details of the V2X/Ethernet socket.

Table 16. V2X/Ethernet socket pinout

Pin numbers	Signal name	Connection details
4	ENET0_REFCLK_V2X_GPIO	Connected to the ENET0 controller of the i.MX 8DXL processor
48	ENET0_MODULE_MDIO	
50	ENET0_MODULE_MDC	
5	ENET0_MODULE_DET_B	Goes to MUX8 as a select signal to select one of its two inputs
7	ENET0_SPI2_SDO	Connected to the SPI2 controller of the i.MX 8DXL processor
9	ENET0_SPI2_SCK	
13	ENET0_SPI2_CS0	
31	ENET0_SPI2_SDI	
8	USDHC2_DAT3 (RGMII_TXD3)	Connected to the USDHC1 and USDHC2 controllers of the i.MX 8DXL processor
10	USDHC2_DAT2 (RGMII_TXD2)	
14	USDHC2_DAT1 (RGMII_TXD1)	
16	USDHC2_DAT0 (RGMII_TXD0)	
20	USDHC2_CLK	
24	USDHC2_CMD (RGMII_TX_CTL)	
28	USDHC1_CMD (RGMII_RX_CTL)	

Table 16. V2X/Ethernet socket pinout*...continued*

Pin numbers	Signal name	Connection details
32	USDHC1_CLK (RGMII_RXC)	
36	USDHC1_DAT0 (RGMII_RXD0)	
38	USDHC1_DAT1 (RGMII_RXD1)	
42	USDHC1_DAT2 (RGMII_RXD2)	
44	USDHC1_DAT3 (RGMII_RXD3)	
19	ENET0_MODULE_GPIO_1	Connected to EXPANDER2
23	ENET0_MODULE_GPIO_2	
27	ENET0_MODULE_GPIO_3	
37	ENET0_MODULE_GPIO_4	
58	V2X_PMIC_STBY_B	
43	ENET0_MODULE_INH	Connected to EXPANDER1
60	ENET0_RST_B	
52	SW1_CH0_SDA	Connected to SWITCH1
54	SW1_CH0_SCL	
56	ENET0_MODULE_INT_B_1PPS	Connected to the SNVS_TAMPER controller of the i.MX 8DXL processor
57	VCC_ENET_IO	Pin 57 of the V2X/Ethernet socket produces VCC_ENET_IO supply based on the ENET0_MODULE_DET_B signal from pin 5 of the socket, as follows: • If ENET0_MODULE_DET_B = 1, then VCC_ENET_IO = 3.3 V • If ENET0_MODULE_DET_B = 0, then VCC_ENET_IO = 1.8 V VCC_ENET_IO supply is one of the source power supplies for VDD_ENET0_VSEL+ supply. Therefore, VDD_ENET0_VSEL+ supply also depends on the ENET0_MODULE_DET_B signal, similar to VCC_ENET_IO supply.
15		Terminated at test point (CS1)
35		Terminated at test point (PRI SAF5400 GPIO2_11 / RGMII_RXDV / RMII_CRS_DV)
41		Terminated at test point (PRI SAF5400 REF_CLK1)
47		Terminated at test point (PRI SAF5400 MDC)
49		Terminated at test point (PRI SAF5400 MDIO)
1, 3		Connected to 3V3 supply
51, 55		Connected to 5V0 / 1V8_6 supply
59		Connected to 5V0 / 12V0 supply
2, 6, 11, 12, 17, 18, 21, 22, 25, 26, 29, 30, 33, 34, 39, 40, 45, 46, 53		Connected to GND

The table below lists the V2X/Ethernet modules/boards from NXP that are supported on the V2X/Ethernet socket.

Table 17. Supported V2X/Ethernet modules

Part number / how to obtain	Description
Contact NXP FAE or sales representative	V2X Wi-Fi module based on NXP SAF5400 modem
SJA1105Q-EVB	Application board based on NXP SJA1105Q Ethernet switch
IMXAI2ETH-ATH	Daughter card based on Atheros Ethernet PHY
IMXAI2ETH-BRC	Daughter card based on Broadcom automotive Ethernet PHY

2.9 Gigabit Ethernet interface

The Gigabit Ethernet interface of the MCIMX8DXL-WEVK board is implemented through an RGMII PHY transceiver that is routed to an RJ45 Gigabit Ethernet connector on the board. The PHY transceiver drives Ethernet signals between ENET1 controller of the i.MX 8DXL processor and Ethernet connector.

The figure below shows the Gigabit Ethernet diagram.

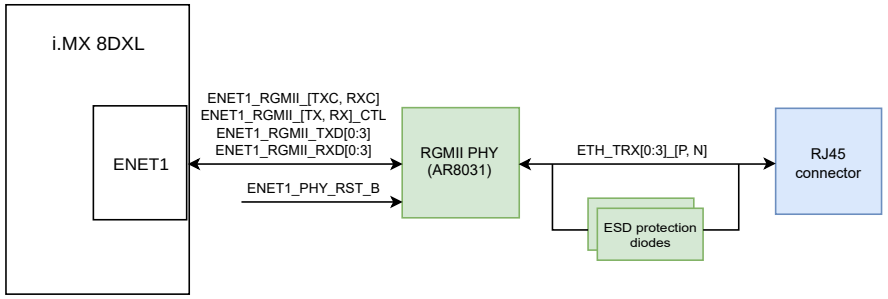

Figure 9. Gigabit Ethernet diagram

The table below details the connections between the processor and Gigabit Ethernet connector.

Table 18. Gigabit Ethernet connections

Processor controller	Peripheral devices		
	Part identifiers	Manufacturer and part number	Description
ENET1	U41	Qualcomm AR8031	RGMII PHY transceiver for driving Ethernet signals between ENET1 controller of the processor and Gigabit Ethernet connector. The ENET1_PHY_RST_B signal from EXPANDER1 is used to reset the PHY transceiver.
	U42 and U43	Nexperia IP4292CZ10-TBR	Two electrostatic discharge (ESD) diodes are placed between the PHY transceiver and Ethernet connector for protecting the signals against discharges
	J8		RJ45 Gigabit Ethernet (10/100/1000 Mbit/s) connector for connecting an Ethernet cable

2.10 USB interface

The i.MX 8DXL processor has two Universal Serial Bus (USB) 2.0 On-The-Go (OTG) controllers, USB_OTG1 and USB_OTG2, which provide host and device functionality with support for OTG. On the MCIMX8DXL-WEVK board, the USB_OTG1 controller is connected to a USB 3.2 Gen 2 Type-C connector or USB interface of the M.2 connector. The USB_OTG2 controller is connected to another USB 3.2 Gen 2 Type-C connector present on the board.

The figure below shows the USB OTG1 connection diagram.

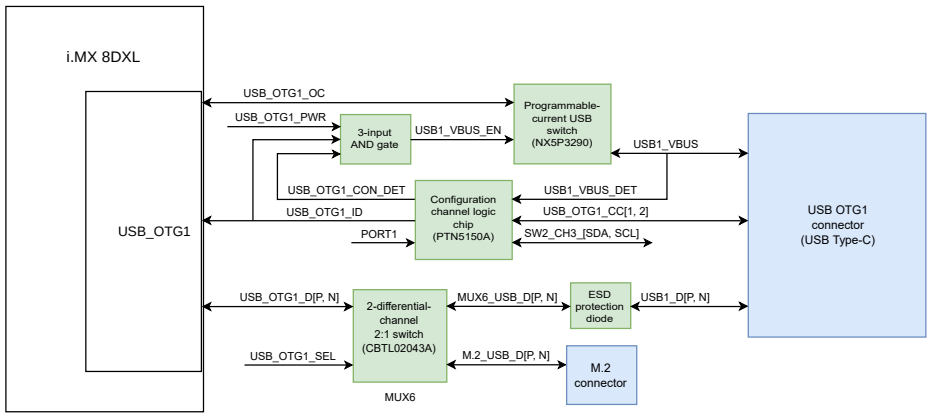

Figure 10. USB OTG1 diagram

The table below details the connections between the processor and USB OTG1 connector.

Table 19. USB OTG1 connections

Processor controller	Peripheral devices		
	Part identifier	Manufacturer and part number	Description
USB_OTG1	U67	NXP CBTL02043A	2-differential-channel, 2:1 mux/demux switch (MUX6), which drives a pair of differential data signals between the processor and USB OTG1 connector or M.2 connector. It selects USB OTG1 signals or M.2 USB signals based on the value of the USB_OTG1_SEL signal from EXPANDER1. An electrostatic discharge (ESD) diode (U123) is placed between MUX6 and USB OTG1 connector for protecting the signals against discharges.
	U117	NXP PTN5150A	Configuration channel (CC) logic chip for USB Type-C applications with CC control logic detection and indication functions. It controls the mode (Host or Device) for the USB OTG1 connector when a USB Type-C cable is attached.
	U116	Nexperia 74AUP1G11GW	3-input AND gate for enabling/disabling programmable-current USB switch
	U65	NXP NX5P3290	Programmable-current USB switch for producing VBUS power when USB OTG1 connector operates in Device mode. In Host mode, USB OTG1 connector produces VBUS power. The USB switch is powered from 5 V power supply. It sends power fault indications (through USB_OTG1_OC signal) to the processor if current consumption for the connected USB device exceeds the maximum allowed limit of 3.3 A.

Table 19. USB OTG1 connections...*continued*

Processor controller	Peripheral devices		
	Part identifier	Manufacturer and part number	Description
	J46	JAE Electronics DX07 S024JJ2R1300	USB 3.2 Gen 2 Type-C connector that allows external connection using a USB Type-C cable
	J17		M.2 connector. For more details, see Section 2.16.

The figure below shows the USB OTG2 connection diagram.

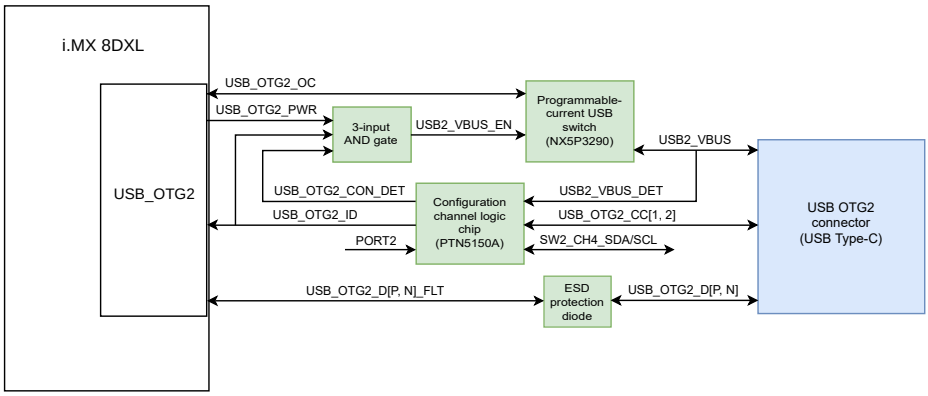

Figure 11. USB OTG2 diagram

The table below details the connections between the processor and USB OTG2 connector.

Table 20. USB OTG2 connections

Processor controller	Peripheral devices		
	Part identifier	Manufacturer and part number	Description
USB_OTG2	U122	Nexperia PRTR5V0U2F	ESD diode for protecting a pair of USB differential data signals between the USB_OTG2 controller of the processor and USB OTG2 connector
	U114	NXP PTN5150A	CC logic chip for USB Type-C applications with CC control logic detection and indication functions. It controls the mode (Host or Device) for the USB OTG2 connector when a USB Type-C cable is attached.
	U113	Nexperia 74AUP1G11GW	3-input AND gate for enabling/disabling programmable-current USB switch
	U62	NXP NX5P3290	Programmable-current USB switch for producing VBUS power when USB OTG2 connector operates in Device mode. In Host mode, USB OTG2 connector produces VBUS power. The USB switch is powered from 5 V power supply. It sends power fault indications (through USB_OTG2_OC signal) to the processor if current consumption for the connected USB device exceeds the maximum allowed limit of 3.3 A.
	J15	JAE Electronics DX07 S024JJ2R1300	USB 3.2 Gen 2 Type-C connector that allows external connection using a USB Type-C cable

USB OTG1 connector mode depends on the PORT pin setting (PORT1 input signal) of CC logic chip U117. Similarly, USB OTG2 connector mode depends on the PORT pin setting (PORT2 input signal) of CC logic chip U114. The table below explains USB OTG1/OTG2 connector modes.

Table 21. USB OTG1/OTG2 connector modes

U117/U114 PORT pin setting	USB OTG1/OTG2 connector mode	Description
PORT pin is connected to 3V3 (VDD) via a 10 kΩ resistor	Downstream-Facing Port (DFP) mode	The USB OTG1/OTG2 connector operates in Host mode. When a USB Type-C cable is attached, it provides power over VBUS.
PORT pin is connected to GND via a 10 kΩ resistor	Upstream-Facing Port (UFP) mode	The USB OTG1/OTG2 connector operates in Device mode. When a USB Type-C cable is attached, it consumes power from VBUS.
PORT pin is left floating	Dual-Role Power (DRP) mode	The USB OTG1/OTG2 connector operates in Host or Device mode

The USB_OTG[1, 2]_CON_DET signal is an input/output signal that acts as an input signal (I2C address signal) to the corresponding CC logic chip or as an output signal (device/cable detect signal) from the corresponding CC logic chip to the processor. It also impacts the PORT[1, 2] signal. The table below explains the working of the USB_OTG[1, 2]_CON_DET signal.

Table 22. USB_OTG[1, 2]_CON_DET signal functions

Signal position	Signal function	CC logic chip mode	CC logic chip I2C address	Impact on PORT[1, 2] signal
Signal is pulled up 3V3 (VDD) through a 10 kΩ resistor	Acts as an input signal to the corresponding CC logic chip, indicates its I2C address	I2C mode	0x7A	PORT[1, 2] input signal to the corresponding CC logic chip can be latched only during power-on
Signal is pulled down to GND through a 10 kΩ resistor			0x3A	
Signal is at midpoint (left floating)	Acts as an output signal from the corresponding CC logic chip, signals to the processor if any device/cable is attached to USB OTG1/OTG2 connector	Non-I2C mode	Not applicable	PORT[1, 2] input signal to the corresponding CC logic chip can be changed dynamically

Note: *For more details on the PTN5150A pin assignments, see PTN5150A Product Data Sheet at NXP website.*

2.11 CAN interface

The Controller Area Network (CAN) interface of the MCIMX8DXL-WEVK board is implemented through a dual CAN transceiver that is routed to two DB9 female connectors on the board via two CAN buses. Each CAN bus is a physical two-wire bus.

On the processor side, the CAN transceiver is connected to FlexCAN1 and FlexCAN2 controllers of the i.MX 8DXL processor. FlexCAN1 signals are multiplexed with UART2 signals on the processor.

The CAN transceiver writes the input data from the processor FlexCAN controllers to the CAN bus lines and sends the output data read from the CAN bus lines to the processor controllers.

The figure below shows the MCIMX8DXL-WEVK CAN diagram.

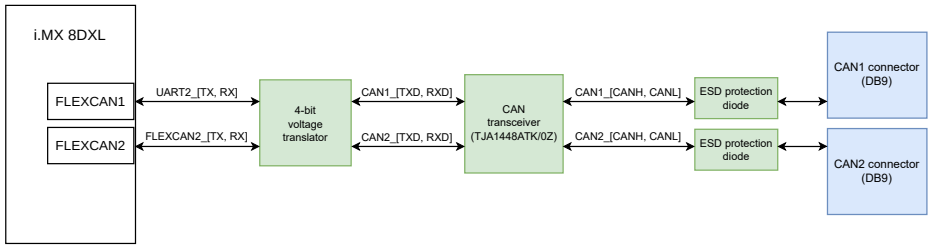

Figure 12. CAN diagram

The table below details the MCIMX8DXL-WEVK CAN connections.

Table 23. MCIMX8DXL-WEVK CAN connections

Processor controllers	Peripheral devices		
	Part identifier	Manufacturer and part number	Description
FLEXCAN1 and FLEXCAN2	U21	Nexperia 74AVC4T245 PW	A 4-bit voltage translator that shifts voltage levels of signals between the processor and CAN transceiver from 1.8 V to 3.3 V and vice versa
	U22	NXP TJA1448ATK/0Z	A high-speed dual CAN transceiver with Standby mode that converts and sends digital data from the processor to the CAN bus lines as analog data, and converts and sends analog data from CAN bus lines to the processor as digital data
	J3 (connected to FLEXCAN1)		A DB9 female CAN connector that allows external CAN connection with the CAN bus. An electrostatic discharge (ESD) diode is used to protect the CAN signals to/from the CAN connector against discharges.
	J4 (connected to FLEXCAN2)		

The STB1 and STB2 signals from EXPANDER3 are used to control Standby mode operation of the two transceivers within the TJA1448ATK/0Z CAN transceiver.

2.12 UART interface

The MCIMX8DXL-WEVK board supports connections with two Universal Asynchronous Receiver/Transmitter (UART) controllers of the i.MX 8DXL processor: UART0 and UART1. UART0 controller is connected to the debug USB host via a USB to UART/MPSSE bridge. UART1 controller is connected to a UART connector or UART interface of an M.2 connector.

UART1 signals are multiplexed with LCDIF controller signals on the i.MX 8DXL processor. For more details, see Section 2.14.

The figure below shows the MCIMX8DXL-WEVK UART diagram.

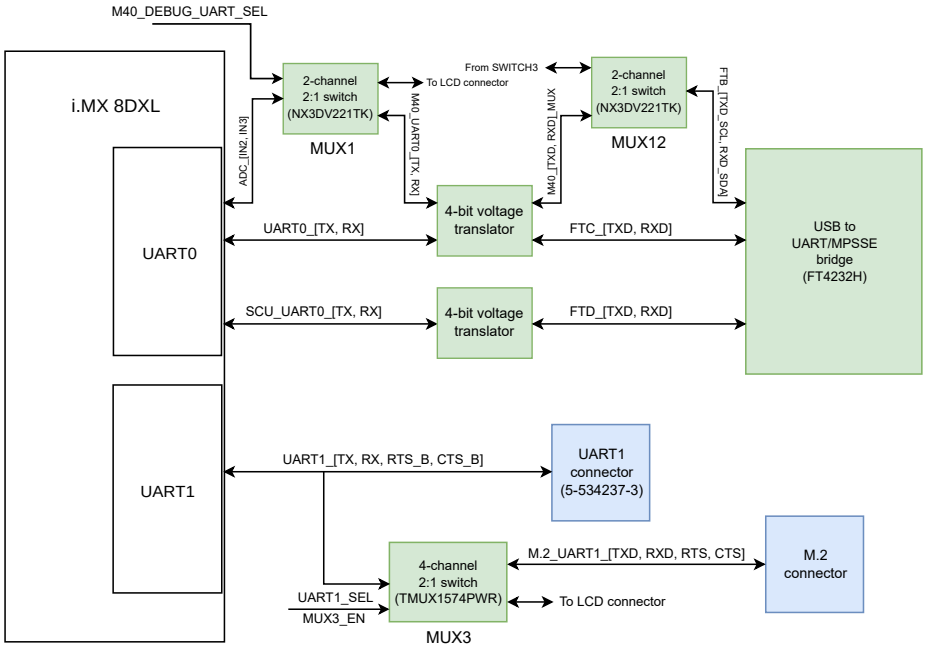

Figure 13. UART diagram

The table below details the UART connections.

Table 24. UART connections

Processor controller	Peripheral devices		
	Part identifier	Manufacturer and part number	Description
UART0	U44	NXP NX3DV221TK	A 2-channel, 2:1 mux/demux switch (referred as MUX1), which drives signals between the processor and USB to UART/MPSSE bridge (through MUX12) or LCD connector. It selects M40 UART signals (from the bridge) or LCD signals based on the value of the M40_DEBUG_UART_SEL signal from EXPANDER1.
	U95		A 2-channel, 2:1 mux/demux switch (referred as MUX12), which drives signals between the USB to UART/MPSSE bridge and i.MX 8DXL processor (through MUX1) or SWITCH3
	U96	Nexperia 74AVC4T245PW	A 4-bit voltage translator that shifts voltage levels of signals between the processor/MUX1 and USB to UART/MPSSE bridge / MUX12 from 1.8 V to 3.3 V and vice versa
	U97		A 4-bit voltage translator that shifts voltage levels of signals between the processor and USB to UART/MPSSE bridge from 1.8 V to 3.3 V and vice versa
	U90	FTDI FT4232H	USB to UART/MPSSE bridge. For more details, see Section 2.19.
UART1	U49	Texas Instruments TMUX1574PWR	A 4-channel, 2:1 mux/demux switch (referred as MUX3), which drives signals between the processor and M.2 connector or LCD connector. It selects M.2 UART signals or LCD signals based on the value of the UART1_SEL signal

Table 24. UART connections...*continued*

Processor controller	Peripheral devices		
	Part identifier	Manufacturer and part number	Description
			from EXPANDER1. MUX3 is disabled, by default. It can be enabled using the MUX3_EN signal from EXPANDER2.
	J10	TE Connectivity 5-534237-3	5-position receptacle (UART1 connector) for external UART connection. Its pinout details are given below: • 1: UART1_TX • 2: UART1_RX • 3: GND • 4: UART1_CTS_B • 5: UART1_RTS_B
	J17		M.2 connector. For more details, see Section 2.16.

2.13 SPI interface

The MCIMX8DXL-WEVK board supports connections with SPI2 and SPI3 controllers of the i.MX 8DXL processor. SPI2 is connected to V2X/Ethernet socket. SPI2 signals are multiplexed with USDHC1 controller signals on the i.MX 8DXL processor.

SPI3 is connected to a SPI connector on the board. SPI3 signals are multiplexed with LCDIF controller signals on the i.MX 8DXL processor. The board uses a mux/demux device for muxing/demuxing the SPI3 and LCDIF signals on the board. For more details, see Section 2.14.

The figure below shows the MCIMX8DXL-WEVK SPI diagram.

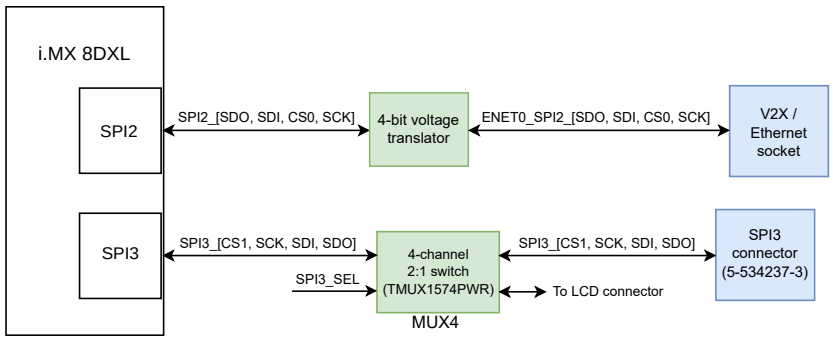

Figure 14. SPI diagram

The table below details the SPI connections.

Table 25. SPI connections

Processor controller	Peripheral devices		
	Part identifier	Manufacturer and part number	Description
SPI2	U36	NXP NTB0104BQ	A 4-bit voltage translator that shifts voltage levels of signals between the processor and V2X/Ethernet socket from 3.3 V to 3.3 V / 1.8 V and vice versa
	J7		V2X/Ethernet socket. For more details, see Section 2.8.

Table 25. SPI connections*...continued*

Processor controller	Peripheral devices		
	Part identifier	Manufacturer and part number	Description
SPI3	U52	Texas Instruments TMUX1574PWR	A 4-channel, 2:1 mux/demux switch (referred as MUX4), which drives signals between the processor and SPI3 connector J11 or LCD connector. It selects SPI3 signals or LCD signals based on the value of the SPI3_SEL signal from EXPANDER1.
	J11		5-position receptacle (SPI3 connector) for external SPI connection. Its pinout details are given below: • 1: SPI3_CS1 • 2: SPI3_SCK • 3: GND • 4: SPI3_SDI • 5: SPI3_SDO

2.14 LCD interface

The i.MX 8DXL processor has an enhanced Liquid Crystal Display Interface (LCDIF) controller that can drive a wide range of display devices varying in size and capability. The MCIMX8DXL-WEVK board provides an LCD connector along with a thin film transistor (TFT) touch screen module for communicating with the LCDIF controller of the i.MX 8DXL processor.

The LCDIF controller signals are multiplexed with other controller signals on the processor. The MCIMX8DXL-WEVK board uses mux/demux devices for muxing/demuxing signals to achieve different functionality from the same set of signals. The table below lists the mux/demux devices used in the LCD interface of the board, and indicates the processor controllers whose signals are muxed/demuxed by the mux/demux devices.

Table 26. Mux/demux devices used in LCD interface

Mux/demux device	Processor controllers
MUX1	UART0 and LCDIF
MUX2	Audio clock mux (ACM) and LCDIF
MUX3	UART1 and LCDIF
MUX4	SPI3 and LCDIF
MUX5	SAI0 and LCDIF

The figure below shows the MCIMX8DXL-WEVK LCD diagram.

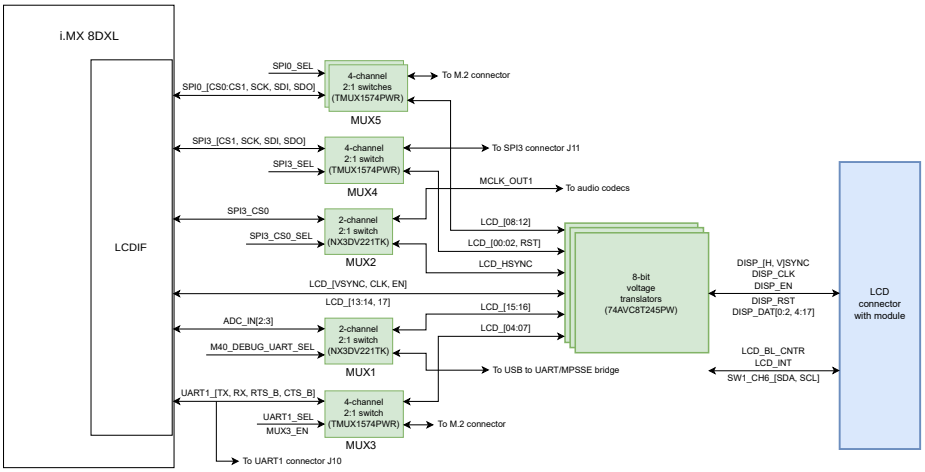

Figure 15. LCD diagram

The table below details the connections between the processor and LCD connector/module.

Table 27. LCD connections

Processor controller	Peripheral devices		
	Part identifiers	Manufacturer and part number	Description
LCDIF	U44	NXP NX3DV221 TK	A 2-channel, 2:1 mux/demux switch (referred as MUX1), which drives signals between the processor and USB to UART/MPSSE bridge (through MUX12) or LCD connector. It selects M40 UART signals (from the bridge) or LCD signals based on the value of the M40_DEBUG_UART_SEL signal from EXPANDER1.
	U50		A 2-channel, 2:1 mux/demux switch (referred as MUX2), which drives signals between the processor and audio codecs or LCD connector. It selects audio codec clock signal or LCD HSYNC signal based on the value of the SPI3_CS0_SEL signal from EXPANDER1.
	U49	Texas Instruments TMUX1574PWR	A 4-channel, 2:1 mux/demux switch (referred as MUX3), which drives signals between the processor and M.2 connector or LCD connector. It selects M.2 UART signals or LCD signals based on the value of the UART1_SEL signal from EXPANDER1. MUX3 is disabled, by default. It can be enabled using the MUX3_EN signal from EXPANDER2.
	U52		A 4-channel, 2:1 mux/demux switch (referred as MUX4), which drives signals between the processor and SPI3 connector J11 or LCD connector. It selects SPI3 signals or LCD signals based on the value of the SPI3_SEL signal from EXPANDER1.
	U46 and U47		A pair of 4-channel, 2:1 mux/demux switches (referred as MUX5), which drives signals between the processor and M.2 connector or LCD connector. It selects M.2 SAI0 signals or LCD signals based on the value of the SPI0_SEL signal from EXPANDER1.
	U45, U48, and U51	Nexperia 74AVC8 T245PW	A set of three 8-bit voltage translators that shifts voltage levels of signals between the processor and LCD connector from 1.8 V to 3.3 V and vice versa

Table 27. LCD connections...*continued*

Processor controller	Peripheral devices		
	Part identifiers	Manufacturer and part number	Description
	J9	Cvilux Corporation CF2033SF	0.5 mm pitch, zero insertion force (ZIF) side entry LCD connector. It houses a WKS Technology WKS101WX001-WCT TFT touch screen module having 10" size, 5 V at 600 mA, 1280x800 pixel.

2.15 Serial audio interface

The i.MX 8DXL processor has four Serial Audio Interface (SAI) controllers: SAI0, SAI1, SAI2, and SAI3. The MCIMX8DXL-WEVK board supports all of them. On the board, the SAI0 controller is connected to the I2S interface of the M.2 connector. Each of the SAI1, SAI2, and SAI3 controllers is connected to an audio codec. Audio codecs are used for encoding/decoding audio data. Each audio codec is connected to an audio jack for audio input/output.

On the processor, signals of the four SAI controllers are multiplexed with signals of other processor controllers, as follows:

- SAI0 signals are multiplexed with LCDIF signals
- SAI1 signals are multiplexed with FLEXCAN0 and FLEXCAN1 signals
- SAI2 and SAI3 signals are multiplexed with SNVS_TAMPER signals

The figure below shows the MCIMX8DXL-WEVK serial audio interface diagram.

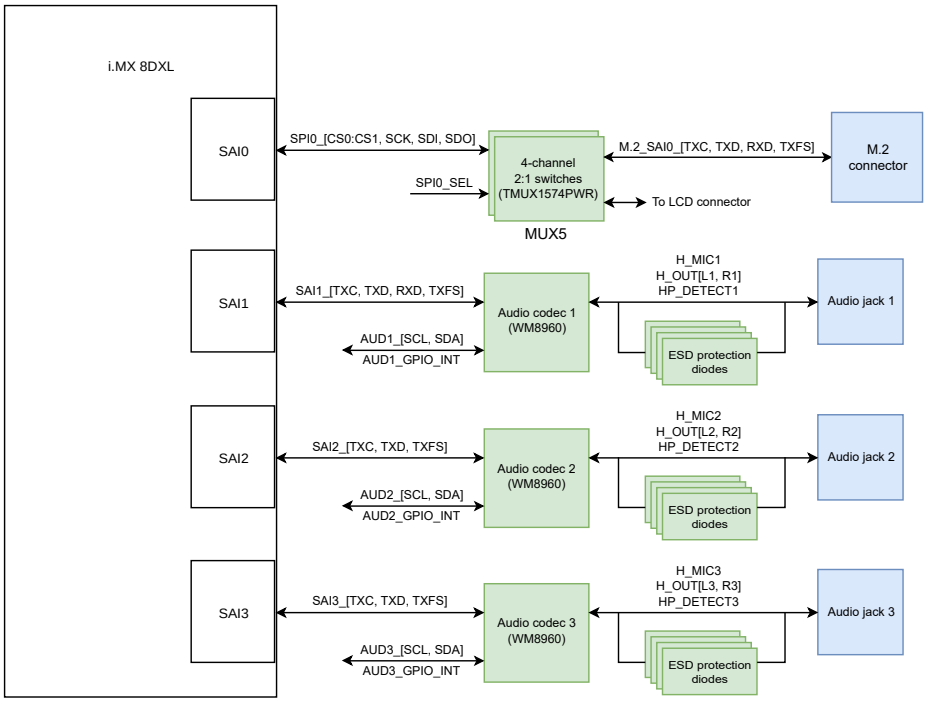

Figure 16. SAI diagram

The table below details the serial audio interface connections in the MCIMX8DXL-WEVK board.

Table 28. SAI connections

Processor controller	Peripheral devices		
	Part identifiers	Manufacturer and part number	Description
SAI0	U46 and U47	Texas Instruments TMUX1574PWR	A pair of 4-channel, 2:1 mux/demux switches (referred as MUX5), which drives signals between the processor and M.2 connector or LCD connector. It selects M.2 SAI0 signals or LCD signals based on the value of the SPI0_SEL signal from EXPANDER1.
	J17		M.2 connector. For more details, see Section 2.16.
SAI1, SAI2, and SAI3	U54 (connected to SAI1)	Cirrus Logic WM8960	Stereo audio codec that supports 24-bit I2S data and 48 kHz sampling rate. The audio codec: • Encodes analog audio received from the audio jack as digital signals and sends them to the processor • Decodes digital signals received from the processor into analog audio and sends it to the audio jack
	U56 (connected to SAI2)		
	U59 (connected to SAI3)		
	J12 (connected to SAI1)		5-pin audio jack that provides analog input/output to the audio codec. It receives/sends audio data between the onboard audio codec and an external audio source. Electrostatic discharge (ESD) diodes are placed between the audio codec and audio jack for protecting the signals against discharges.
	J13 (connected to SAI2)		
	J14 (connected to SAI3)		

2.16 M.2 connector

The MCIMX8DXL-WEVK board has a 75-pin, M.2 Key-E mini card connector J17 for plugging a Wi-Fi + Bluetooth card or Qualcomm modem. The M.2 mini card connector supports UART, USB, PCIe, I2C, I2S, and GPIO connections.

The M.2 connector is connected to USB_OTG1, SAI0, UART1, PCIE0, and PCIE_IOB controllers of the i.MX 8DXL processor. SAI0 and UART1 signals are multiplexed with LCDIF controller signals on the i.MX 8DXL processor.

The table below explains the M.2 connector pinout.

Table 29. M.2 connector pinout

Pin numbers	Signal name	Connection details
3	M.2_USB_DP	Connected to MUX6 (U67), which drives a pair of differential data signals between the processor and USB OTG1 connector or M.2 connector. It selects USB OTG1 signals or M.2 USB signals based on the value of the USB_OTG1_SEL signal from EXPANDER1.
5	M.2_USB_DN	
6	LED1	Connected to D29 LED (LED1)
16	LED2	Connected to D30 LED (LED2)
8	M.2_SAI0_TXC	Connected to MUX5 (U46, U47), which drives signals between the processor and M.2 connector or LCD connector. It selects M.2 SAI0 signals or LCD signals based on the value of the SPI0_SEL signal from EXPANDER1.
10	M.2_SAI0_TXFS	
12	M.2_SAI0_RXD	
14	M.2_SAI0_TXD	

Table 29. M.2 connector pinout*...continued*

Pin numbers	Signal name	Connection details
20	BT_UART_WAKE_B	Connected to EXPANDER2 (U84), which is a 16-bit, I2C-bus input/output expander
54	BT_DIS_B	
21	M.2_WIFI_WAKE_B	Connected to EXPANDER1 (U80), which is a 16-bit, I2C-bus input/output expander
23	M.2_WIFI_EN	
56	WIFI_DIS_B	
22	M.2_UART1_RXD	Connected to MUX3 (U49), which drives signals between the processor and M.2 connector or LCD connector. It selects M.2 UART signals or LCD signals based on the value of the UART1_SEL signal from EXPANDER1. MUX3 is disabled, by default. It can be enabled using the MUX3_EN signal from EXPANDER2.
32	M.2_UART1_TXD	
34	M.2_UART1_CTS	
36	M.2_UART1_RTS	
35	M.2_PCIE0_TX_P	Connected to the PCIE0 controller of the i.MX 8DXL processor
37	M.2_PCIE0_TX_N	
41	M.2_PCIE0_RX_P	
43	M.2_PCIE0_RX_N	
52	PCIE_CTRL_PERST_B	
55	PCIE_CTRL_WAKE_B	
47	PCIE_CONN_REFCLK_P	Differential PCIe reference clock. If the value of the PCI_CLK_SEL signal from EXPANDER1 is 1, then the processor provides reference clock to M.2 module or vice versa. If the value of the PCI_CLK_SEL signal is 0, then PCIe clock generator U69 provides reference clock to the processor and M.2 module.
49	PCIE_CONN_REFCLK_N	
50	BT_OSC_32KHZ	32.768 kHz clock input from Y1 crystal oscillator
53	M2_CLKREQ_B	Clock feedback to clock generator U69
58	M.2_I2C_SDA	Connected to SWITCH1 (U75), which is an 8-channel I2C-bus switch for I2C2 bus
60	M.2_I2C_SCL	
2, 4, 72, 74		Connected to 3V3 supply
1, 7, 18, 33, 39, 45, 51, 57, 63, 69, 75		Connected to GND
9, 11, 13, 15, 17, 19, 24, 25, 26, 27, 28, 29, 30, 31, 38, 40, 42, 44, 46, 48, 59, 61, 62, 64, 65, 66, 67, 68, 70, 71, 73		Not connected

A Wi-Fi + Bluetooth card is provided with the MCIMX8DXL-WEVK board kit. The card has been tested by NXP on the M.2 connector of the board. The table below describes the Wi-Fi + Bluetooth card. For more information on the card, see https://www.embeddedartists.com/products/1xl-m-2-module/.

Table 30. Wi-Fi + Bluetooth card

Feature	Description
Manufacturer	Embedded Artists AB
Part number	EAR00387

Table 30. Wi-Fi + Bluetooth card*...continued*

Feature	Description
Module	Murata LBEE5ZZ1XL (also known as 1XL)
Chipset	NXP 88W9098
WLAN standards	802.11a/b/g/n/ac/ax 2x2 MU-MIMO, Wi-Fi 6
Bluetooth standards	5.2 BR/EDR/LE

2.17 I2C-bus I/O expanders

The MCIMX8DXL-WEVK board provides five 16-bit general-purpose input/output expanders that support remote I/O expansion via the I2C-bus interface.

The table below describes the MCIMX8DXL-WEVK I/O expanders.

Table 31. I/O expanders

Part identifier	Manufacturer and part number	Expander name	Purpose
U80	NXP PCA6416APW	EXPANDER1	Support remote I/O expansion for the i.MX 8DXL processor
U84		EXPANDER2	
U82		EXPANDER3	
U110		EXPANDER4	
U101		EXPANDER5	Supports remote I/O expansion for the debug USB host via USB to UART/MPSSE bridge (U90)

The table below describes EXPANDER1.

Table 32. EXPANDER1

Port number	Signal	Direction	Description
P0_0	ENET0_MODULE_RST_B	To V2X module	• 0: Resets V2X module • 1 (default value): Does nothing
P0_1	ENET0_MODULE_INH	From V2X module	• 0: Does nothing • 1 (default value): Informs the processor that V2X module operation has been stopped (inhibited) for some reasons
P0_2	ENET1_PHY_RST_B	To AR8031 PHY	• 0: Resets AR8031 PHY • 1 (default value): Does nothing
P0_3	M40_DEBUG_UART_SEL	To MUX1	• 0: Selects LCD signals at MUX1 • 1 (default value): Selects M40 UART signals (from USB to UART/MPSSE bridge) at MUX1
P0_4	SPI3_CS0_SEL	To MUX2	• 0: Selects LCD HSYNC signal at MUX2 • 1 (default value): Selects audio codec clock signal at MUX2
P0_5	LCD_BL_CNTR	To LCD module	• 0: Does nothing • 1 (default value): Controls LCD backlight
P0_6	UART1_SEL	To MUX3	• 0: Selects LCD signals at MUX3

Table 32. EXPANDER1*...continued*

Port number	Signal	Direction	Description
			• 1 (default value): Selects M.2 UART signals at MUX3
P0_7	SPI3_SEL	To MUX4	• 0: Selects LCD signals at MUX4 • 1 (default value): Selects SPI3 signals at MUX4
P1_0	SPI0_SEL	To MUX5	• 0: Selects LCD signals at MUX5 • 1 (default value): Selects M.2 SAI0 signals at MUX5
P1_1	USB_OTG1_SEL	To MUX6	• 0: Selects M.2 USB signals at MUX6 • 1 (default value): Selects USB OTG1 signals at MUX6
P1_2	PCI_CLK_SEL	To 2:1 switches U70 and U71	• 0: PCIe clock generator U69 provides reference clock to the processor and M.2 module • 1 (default value): The processor provides reference clock to M.2 module or vice versa
P1_3	ENET0_MODE_SEL	To MUX7 and MUX9	• 0: Selects V2X module signals (Dual-USDHC mode) at MUX7 and MUX9 • 1 (default value): Selects SD card signals at MUX7 and MUX9
P1_4	WIFI_EN	To M.2 module	• 0: Does nothing • 1 (default value): Enables Wi-Fi submodule of M.2 module
P1_5	WIFI_DIS_B	To M.2 module	• 0: Disables Wi-Fi submodule of M.2 module • 1 (default value): Does nothing
P1_6	WIFI_WAKE_B	From M.2 module	• 0: Notifies the processor that Wi-Fi submodule of M.2 module has come out of Deep-Sleep mode • 1 (default value): Does nothing
P1_7	SS_CNTRL	To PCIe clock generator U69	• 0 (default value): Clocks from PCIe clock generator U69 are spread-spectrum modulated • 1: Clocks from PCIe clock generator U69 are fixed

The table below describes EXPANDER2.

Table 33. EXPANDER2

Port number	Signal	Direction	Description
P0_0	BT_DIS_B	To M.2 module	• 0: Disables Bluetooth submodule of M.2 module • 1 (default value): Does nothing
P0_1	BT_UART_WAKE_B	From M.2 module	• 0: Notifies the processor that UART submodule of M.2 module has come out of Deep-Sleep mode • 1 (default value): Does nothing

Table 33. EXPANDER2*...continued*

Port number	Signal	Direction	Description
P0_2	LCD_INT	From LCD module	• 0: Interrupt handling is ON for LCD module • 1 (default value): Interrupt handling is OFF for LCD module
P0_3	ENET0_AUX_GPIO1	Bidirectional	User-defined
P0_4	ENET0_AUX_GPIO2	Bidirectional	
P0_5	ENET0_AUX_GPIO3	Bidirectional	
P0_6	ENET0_AUX_GPIO4	Bidirectional	
P0_7		Reserved	
P1_0	MUX3_EN	To MUX3	• 0: Disables MUX3 • 1 (default value): Enables MUX3
P1_1	V2X_PMIC_STBY	To V2X module	• 0: Enables Standby mode of V2X module PMIC • 1 (default value): Disables Standby mode of V2X module PMIC (enables Normal mode)
P1_2	EXP2_P1_2	Reserved	
P1_3	EXP2_P1_3		
P1_4	EXP2_P1_4		
P1_5	EXP2_P1_5		
P1_6	EXP2_P1_6		
P1_7	EXP2_P1_7		
INT_B	EXP2_INT_B	To i.MX 8DXL processor	• 0: Interrupt handling is ON for EXPANDER2 • 1 (default value): Interrupt handling is OFF for EXPANDER2

The table below describes EXPANDER3.

Table 34. EXPANDER3

Port number	Signal	Direction	Description
P0_0	STB1	CAN transceiver	• 0: Enables Standby mode of first transceiver within CAN transceiver • 1 (default value): Disables Standby mode of first transceiver within CAN transceiver (enables Normal mode)
P0_1	STB2		• 0: Enables Standby mode of second transceiver within CAN transceiver • 1 (default value): Disables Standby mode of second transceiver within CAN transceiver (enables Normal mode)
P0_2	AUD1_INT	From audio codec 1	• 0: Interrupt handling is OFF for audio codec 1 • 1 (default value): Interrupt handling is ON for audio codec 1

Table 34. EXPANDER3*...continued*

Port number	Signal	Direction	Description
P0_3	AUD2_INT	From audio codec 2	• 0: Interrupt handling is OFF for audio codec 2 • 1 (default value): Interrupt handling is ON for audio codec 2
P0_4	AUD3_INT	From audio codec 3	• 0: Interrupt handling is OFF for audio codec 3 • 1 (default value): Interrupt handling is ON for audio codec 3
P0_5	EXP3_P0_5	Reserved	
P0_6	EXP3_P0_6		
P0_7	EXP3_P0_7		
P1_0	EXP3_P1_0		
P1_1	EXP3_P1_1		
P1_2	EXP3_P1_2		
P1_3	EXP3_P1_3		
P1_4	EXP3_P1_4		
P1_5	EXP3_P1_5		
P1_6	EXP3_P1_6		
P1_7	EXP3_P1_7		
INT_B	EXP3_INT_B	To i.MX 8DXL processor	• 0: Interrupt handling is ON for EXPANDER3 • 1 (default value): Interrupt handling is OFF for EXPANDER3

The table below describes EXPANDER4.

Table 35. EXPANDER4

Port number	Signal	Direction	Description
P0_0	I2C_EXP4_P0.0	To SWITCH1 U75	• 0: Resets SWITCH1 • 1 (default value): Does nothing
P0_1	I2C_EXP4_P0.1	To EXPANDER1	• 0: Resets EXPANDER1 • 1 (default value): Does nothing
P0_2	I2C_EXP4_P0.2	To EXPANDER2	• 0: Resets EXPANDER2 • 1 (default value): Does nothing
P0_3	I2C_EXP4_P0.3	To SWITCH2 U76	• 0: Resets SWITCH2 • 1 (default value): Does nothing
P0_4	I2C_EXP4_P0.4	To EXPANDER3	• 0: Resets EXPANDER3 • 1 (default value): Does nothing
P0_5	I2C_EXP4_P0.5	To 2:1 switch U134	• 0: Selects V2X module signals at U134 • 1 (default value): Selects AR8031 PHY signals at U134
P0_6	EXP4_P0_6	Reserved	
P0_7	EXP4_P0_7		

Table 35. EXPANDER4*...continued*

Port number	Signal	Direction	Description
P1_0	EXP4_P1_0		
P1_1	EXP4_P1_1		
P1_2	EXP4_P1_2		
P1_3	EXP4_P1_3		
P1_4	EXP4_P1_4		
P1_5	EXP4_P1_5		
P1_6	EXP4_P1_6		
P1_7	EXP4_P1_7		

The table below describes EXPANDER5, which allows to reconfigure the board by debug USB host, via USB to UART/MPSSE bridge (U90).

Table 36. EXPANDER5

Port number	Signal	Direction	Description
P0_0	HOST_BOOT_MODE0	To MUX13	HOST_BOOT_MODE[2:0] (boot mode selection): • 000: Processor internal eFuse (default setting) • 001: USB serial download (processor can download a program image from a USB connection) • 010: EMMC0 • 011: USDHC1: SD card • 100: NAND, 128 pages • 101: Reserved • 110: FlexSPI • 111: Reserved
P0_1	HOST_BOOT_MODE1		
P0_2	HOST_BOOT_MODE2		
P0_3	HOST_SD_PWR	To SD card	• 0: Disables SD card power • 1 (default value): Enables SD card power
P0_4	HOST_SD_WP	To i.MX 8DXL processor	• 0: Notifies the processor that write-protection is not enabled for SD card • 1 (default value): Notifies the processor that write-protection is enabled for SD card
P0_5	HOST_SD_CD		• 0: Notifies the processor that SD card is not detected in the SD card slot • 1 (default value): Notifies the processor that SD card is present in the SD card slot
P0_6	EXP5_P0_6	Reserved	
P0_7	EXP5_P0_7		
P1_0	VDD_MAIN_I_SW	To 2:1 switch U130	• 0: PMIC switch for PMIC_VDD_MAIN supply gets local feedback • 1 (default value): PMIC switch for PMIC_VDD_MAIN supply gets feedback from another board device
P1_1	VDD_MEMC_I_SW		• 0: PMIC switch for PMIC_VDD_MEMC supply gets local feedback

Table 36. EXPANDER5*...continued*

Port number	Signal	Direction	Description
			• 1 (default value): PMIC switch for PMIC_ VDD_MEMC supply gets feedback from another board device
P1_2	VDD_DDRIO_I_SW	To 2:1 switch U131	• 0: PMIC switch for PMIC_VDD_DDRIO supply gets local feedback • 1 (default value): PMIC switch for PMIC_ VDD_DDRIO supply gets feedback from another board device
P1_3	VDD_ANA_I_SW	To power switch U10	• 0: Power switch U10 is disabled • 1 (default value): Power switch U10 is enabled
P1_4	EXP5_P1_4	Reserved	
P1_5	EXP5_P1_5		
P1_6	TEST_MODE_SELECT	To i.MX 8DXL processor	• 0: i.MX 8DXL processor Test mode is selected • 1 (default value): i.MX 8DXL processor Test mode is not selected
P1_7	BOOT_SRC_SEL	To MUX13	• 0: Processor boot mode is controlled by debug USB host via USB to UART/MPSSE bridge (U90) • 1 (default value): Processor boot mode is controlled by DIP switch SW1

2.18 I2C-bus interface

The Inter-Integrated Circuit (I2C) protocol is a serial bus protocol that allows multiple peripheral devices to communicate to one or more master devices with a pair of control and data signals. In the MCIMX8DXL-WEVK board, I2C-bus interface is implemented through I2C buses from two I2C masters, as described in the table below.

Table 37. I2C buses in MCIMX8DXL-WEVK board

I2C master	I2C buses
i.MX 8DXL processor (PIMX8DL1AVNFZAB)	I2C2, I2C3, and PMIC_I2C
Debug USB host (via USB to UART/MPSSE bridge)	FTB

To manage large number of I2C devices, the MCIMX8DXL-WEVK board uses three I2C-bus switches. The board also uses five input/output expanders to provide remote input/output expansion for the I2C masters via the I2C-bus interface.

The tables below show the MCIMX8DXL-WEVK I2C-bus device mapping.

Table 38. I2C2, I2C3, and PMIC_I2C bus device mapping

I2C-bus	I2C channel	I2C address	Device	Description
(All)			PIMX8DL1AVNFZAB (U20)	Processor, which acts as I2C master
I2C2		0x70	PCA9548APW (U75) (SWITCH1)	8-channel I2C-bus switch for I2C2 bus
	SW1_CH0		V2X/ENET0 module	Board/module placed in V2X/Ethernet socket J7

Table 38. I2C2, I2C3, and PMIC_I2C bus device mapping*...continued*

I2C-bus	I2C channel	I2C address	Device	Description
	SW1_CH1		WM8960 (U54)	Audio codec 1
	SW1_CH2		WM8960 (U56)	Audio codec 2
	SW1_CH3		WM8960 (U59)	Audio codec 3
	SW1_CH4		M.2 module	Board/module placed in M.2 connector J17
	SW1_CH5		9FGV0241AKILF (U69)	PCIe clock generator
	SW1_CH6		WKS101WX001-WCT TFT touch screen module	LCD module placed in LCD connector J9
		0x20	PCA6416APW (U80) (EXPANDER1)	16-bit, I2C-bus input/output expander
		0x21	PCA6416APW (U84) (EXPANDER2)	
I2C3		0x70	PCA9548APW (U76) (SWITCH2)	8-channel I2C-bus switch for I2C3 bus
	SW2_CH0		WM8960 (U54)	Audio codec 1 (alternative I2C control signals)
	SW2_CH1		WM8960 (U56)	Audio codec 2 (alternative I2C control signals)
	SW2_CH2		WM8960 (U59)	Audio codec 3 (alternative I2C control signals)
	SW2_CH3	0x7A/0x3A	USB Type-C cable	Cable connected to USB OTG1 connector
	SW2_CH4	0x7A/0x3A	USB Type-C cable	Cable connected to USB OTG2 connector
		0x20	PCA6416APW (U82) (EXPANDER3)	16-bit, I2C-bus input/output expander
PMIC_I2C		0x20	PCA6416APW (U110) (EXPANDER4)	16-bit, I2C-bus input/output expander
		0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, 0x0F	PPF7100BVMA1ES (U5)	7-channel power management integrated circuit (PMIC)

Table 39. FTB I2C-bus device mapping

I2C bus	I2C channel	I2C address	Device	Description
FTB			Debug USB host	Host computer (acting as I2C master) connected to the board through USB micro-B connector J19. I2C-bus implementation is done via USB to UART/MPSSE bridge U90.
		0x70	PCA9548APW (U103) (SWITCH3)	8-channel I2C-bus switch for FTB I2C bus

Table 39. FTB I2C-bus device mapping*...continued*

I2C bus	I2C channel	I2C address	Device	Description
	SW3_CH0	0x20	PCA6416APW (U101) (EXPANDER5)	16-bit, I2C-bus input/output expander
	SW3_CH1	0x10	PAC1934T-I/JQ (U11)	Power monitor for monitoring 5V0, 3 V3_USB, 3V3_IO, and VDD_ENET0_ VSEL- power supplies
	SW3_CH2	0x10	PAC1934T-I/JQ (U14)	Power monitor for monitoring 3V3_ PMIC, 3V3, VDD_SNVS1, and VDD_ MAIN power supplies
	SW3_CH3	0x10	PAC1934T-I/JQ (U19)	Power monitor for monitoring VDD_ MEMC, VDD_DDR_VDDQ, DDR_ VDD2, and VDD_ENET0 power supplies
	SW3_CH4	0x10	PAC1934T-I/JQ (U12)	Power monitor for monitoring VDD_ ANA, DDR_VDD1, 1V8_1, and 1V8_2 power supplies
	SW3_CH5	0x10	PAC1934T-I/JQ (U15)	Power monitor for monitoring 1V8_3, 1V8_4, 1V8_5, and 1V8 power supplies
	SW3_CH6	0x10	PAC1934T-I/JQ (U18)	Power monitor for monitoring 1V8_6 and 12V0 power supplies and VDD_ ANA1_1P8 and VDD_EMMC0_1P8_3 P3 processor power domains
	SW3_CH7	0x18, 0x19, 0x1A, 0x1B, 0x1C, 0x1D, 0x1E, 0x1F	MFS5600AMMA7ES (U1)	Power regulator that produces 5V0_PS and 3V3_PS supplies on the board
		0x57	AT24C02C-XHM-B (U104)	2 kbit serial-I2C EEPROM with write-protect option. It serves as system ID memory and stores board information, such as board ID and revision, processor ID and revision, and board serial number.

2.19 Board control and debug interface

The MCIMX8DXL-WEVK board uses a USB to UART / multi-protocol synchronous serial engine (MPSSE) device (FTDI FT4232H) U90 for board control and debug. The figure below shows the board control and debug diagram.

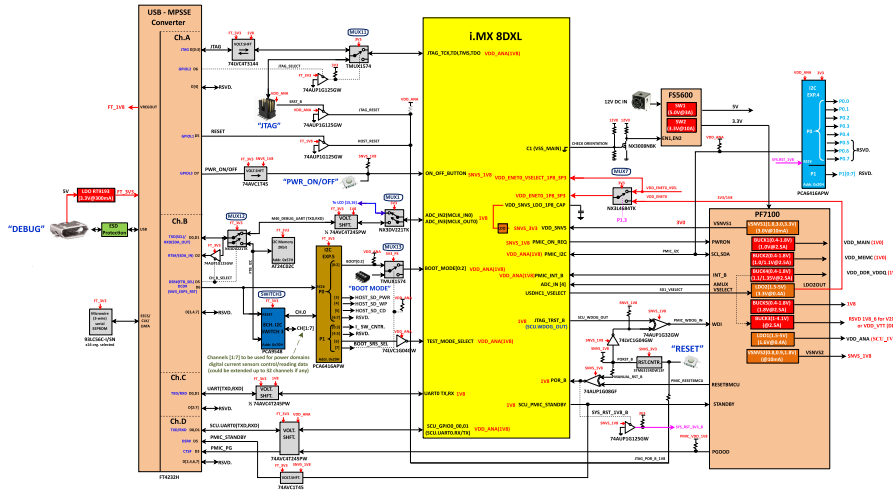

Figure 17. Board control and debug diagram

The USB to UART/MPSSE device acts as a bridge to enable communication between the host computer and i.MX 8DXL processor. The USB to UART/MPSSE bridge is connected to a USB micro-B connector J19, which serves as debug USB connector on the board. A USB cable can be used to connect the board to the host computer.

The USB to UART/MPSSE bridge has four UART channels (A, B, C, and D) that allow USB to UART connections or USB to MPSSE connections (through protocols, such as JTAG, I2C, or SPI). One or both of channels A and B can be configured as MPSSE ports.

The table below describes how each channel of the bridge can be used on the MCIMX8DXL-WEVK board.

Table 40. USB to UART/MPSSE bridge channel connections

Channel	Description
A	Provides a remote JTAG debugging option for i.MX 8DXL processor system. Another remote JTAG debugging option for i.MX 8DXL processor system is provided by the JTAG header J18. For more details, see Section 2.19.4.
B	Can be used as UART debug port for debugging the Arm Cortex-M4 core of the i.MX 8DXL processor. It can also be used as I2C port for controlling/managing peripheral devices, such as power monitors, power regulator U1, and system ID memory (see Section 2.18). This channel can also be used for remote boot mode control.
C	Can be used as UART debug port for debugging the Arm Cortex-A35 core of the processor
D	Connected to the UART controller of the processor that is associated with the system controller unit (SCU) of the processor

The Board Control Utilities (BCU) software supports board control features, debugging via open-OCD, and also power monitoring. For more details, see https://github.com/NXPmicro/bcu.

The Power Measurement Tool (PMT) also provides board control features and power monitoring with graphical interface. For more details, see AN13119, i.MX Power Measurement Tool.

2.19.1 System ID memory

The MCIMX8DXL-WEVK board has a 2 kbit serial-I2C electrically erasable programmable read-only memory (EEPROM) with the following details:

- Part identifier: U104

- Manufacturer and part number: Microchip Technology AT24C02C-XHM-B

The EEPROM serves as the system ID memory and stores the following board information:

- Board ID and revision
- Processor ID and revision
- PMIC ID and revision
- Number of measurable power supplies on the board
- Board serial number (user-defined)

Before a board is used for the first time, the system ID memory of the board must be programmed correctly. The system ID memory of a board is initially programmed during manufacturing. However, if an error occurs in the future, then the memory can be reset to its manufacturing settings.

The table below shows useful information about the board that is stored in the system ID memory. The "Data" column indicates manufacturing settings as per the current revision of the MCIMX8DXL-WEVK board. These settings may change in a future revision of the board.

Table 41. System ID memory manufacturing settings

Setting	Value	Comments
`BOARD_ID`	NXP i.MX8DXL WEVK Board	Ensure that `BOARD_ID` and `BOARD_REV` are set properly in the PMT `yaml` configuration file. In BCU, provide the correct `[-brev=]` value in the command if you are not using the default revision value. ***Note:*** *`BOARD_REV` may have a different value for your board based on your board revision.*
`BOARD_REV`	A3	
`SOC_ID`	i.MX8DXL	This setting is related to the `[-board=]` option in BCU and it cannot be changed manually
`SOC_REV`	A0	In BCU, provide the correct `[-srev=]` value in the command if you are not using the default revision value. ***Note:*** *`SOC_REV` may have a different value for your board based on the processor revision.*
`PMIC_ID`	PPF7100 BVMA1ES	These settings are related to the `[-board=]` option in BCU and they cannot be changed manually
`PMIC_REV`	N/A	
`NBR_PWR_RAILS`	15	
`BOARD_SN`	24 (example)	Board-specific serial number. It is user-defined and can be set to a value in the range 1~65535.

The BCU or PMT software can detect the type of board connected to the host computer by reading the system ID memory of the board. You can use the BCU or PMT software to update the system ID memory of a board. For example, you can set a new value for the board-specific serial number (`BOARD_SN`).

For more information about the BCU and PMT software, see Section 2.2.2. For detailed instructions on how to configure the system ID memory, see the BCU documentation in GitHub and *i.MX Power Measurement Tool Application Note* (document AN13119).

2.19.2 Boot modes

In the MCIMX8DXL-WEVK board, a boot mode can be selected through DIP switch SW1. For more details on the boot modes and boot mode selection, see Section 1.10.

2.19.3 Debug USB connector

The MCIMX8DXL-WEVK board provides a USB 2.0 micro-B connector (debug USB connector) J19, which allows connection with the host computer for debugging the board.

The debug USB connector is connected to the `USBDP` and `USBDM` pins of FT4232H (USB to UART/MPSSE bridge) via PRTR5V0U2F, which is an ultra-low capacitance electrostatic discharge (ESD) protection device.

2.19.4 JTAG header

The MCIMX8DXL-WEVK board provides a 2x5-pin Samtec FTSH-105-01-L-DV-K header (J18) for allowing JTAG debugging of the board using a remote debugger. The table below shows the JTAG header pinout.

Table 42. JTAG header pinout

Pin number	Signal	Description
1	JTAG_VTREF	Power supply (VDD_ANA)
2	CON_JTAG_TMS	Test access point (TAP) machine state
4	CON_JTAG_TCK	TAP clock
6	CON_JTAG_TDO	TAP data out
8	CON_JTAG_TDI	TAP data in
10	JTAG_SRST_B	System reset
9	JTAG_TRST_B_CONN	Test point
7	GND (RTCK)	Ground
3, 5	GND	

2.20 Board errata

None

3 Revision history

The table below summarizes the revisions to this document.

Table 43. Revision history

Revision	Date	Topic cross-reference	Change description
1	10 March 2023	Section 2.16	Added a link, https://www.embeddedartists.com/products/1xl-m-2-module/
0	29 July 2022		Initial NDA release

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