# LVPECL LVDS HCSL and CML Clock Transformation

Pericom Clock IC Application Engineering

## 1. Introduction

Today all electronic bus is in serial connectivity and clock timing goes to differential clock too in most system designs. Differential clock can transmit much longer PCB trace because its signal reference is to its + and – ones than CMOS clock which needs Vcc or VDD and GND as its reference. Differential + and – clocks cancel each other in common mode voltage plus its relative smaller voltage swing dramatically reduces system clocks' EMI headache than before.

The most used differential clocks are LVPECL, LVDS, HCSL and CML that Pericom Clock IC family has them all. This application note is to provide those drivers basic structure, explanation, and practical useful techniques on how to interface each other between driver and receiver termination.

### Contents



## 2. LVPECL LVDS HCSL and CML Driver

The Figure 1. diagram shows LVPECL, LVDS, HCSL and CML(AC) voltage levels vs. CMOS clock. The CML(AC) is listed because CML is always used in AC coupling and its DC voltage level is much related with its Vcc supply.

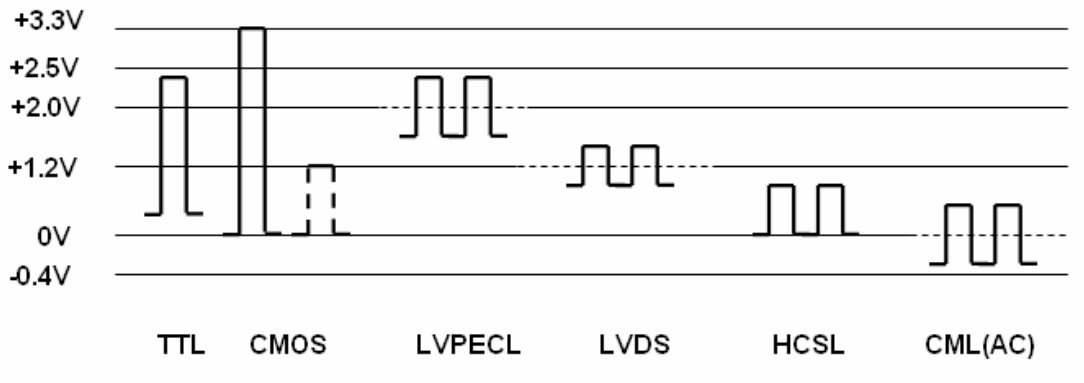


**Figure 1. LVPECL LVDS HCSL and CML voltage levels**

## 2.1 LVPECL Driver and Termination

Figure 2. shows the LVPECL(Low Voltage Positive Emitter-Coupled Logic) driver's datasheet specification diagram to generate about 0.7V swing differential clock. Single end clock swing is about 2V+/-400mV with +/-100mV variation from vendor to vendor.

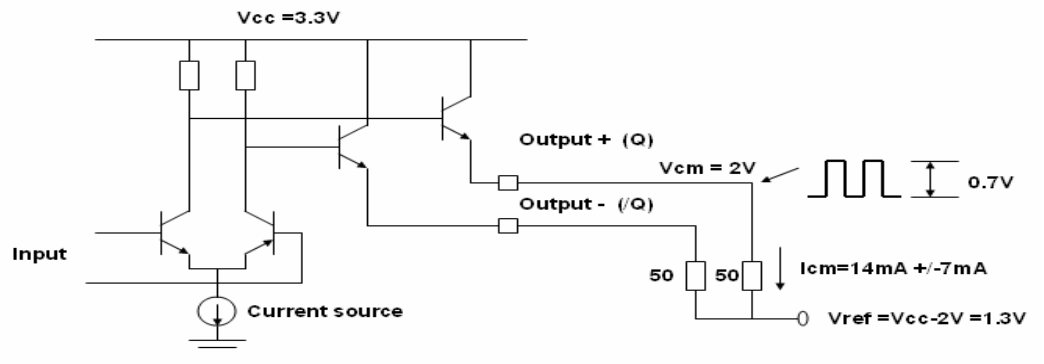


**Figure 2. LVPECL driver termination in Vcc-2V reference voltage**

But practical LVPECL application uses 150 ohm pull-down and 100 ohm cross at the receive end termination as Figure 3. shows, which is the equivalent as the Figure 2. termination load. In this way, LVPECL can be used in either DC or AC coupling drive.

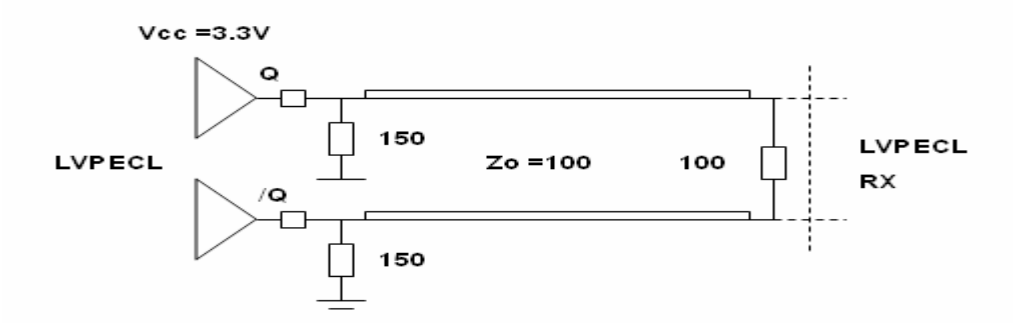


**Figure 3. LVPECL driver popular practical use termination**

## 2.2 LVDS Driver and Termination

LVDS(Low Voltage Differential Signal) driver is the push and pull driver which does not need the pull-down resistor at the TX side as Figure 4. shows. It only needs 100 ohm cross or the equivalent differential termination. It means the coupling can be DC or AC coupling directly.

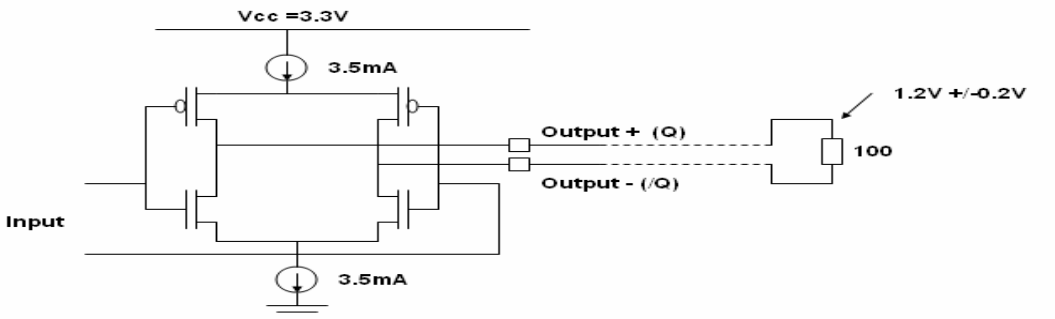


**Figure 4. LVDS driver termination in 100 ohm cross**

## 2.3 HCSL Driver and Termination

HCSL is Intel defined differential clock for PCIe reference clock. It needs driver source termination in serial 33 ohm and 50 ohm pull-down. The receive side is to drive high impedance termination with 2 pF emulation. The signal specification is based on the 10 in. +2pF load, as shown in Figure 5. This driver has I_ref pin to connect a 475 ohm to GND as the driver reference current.

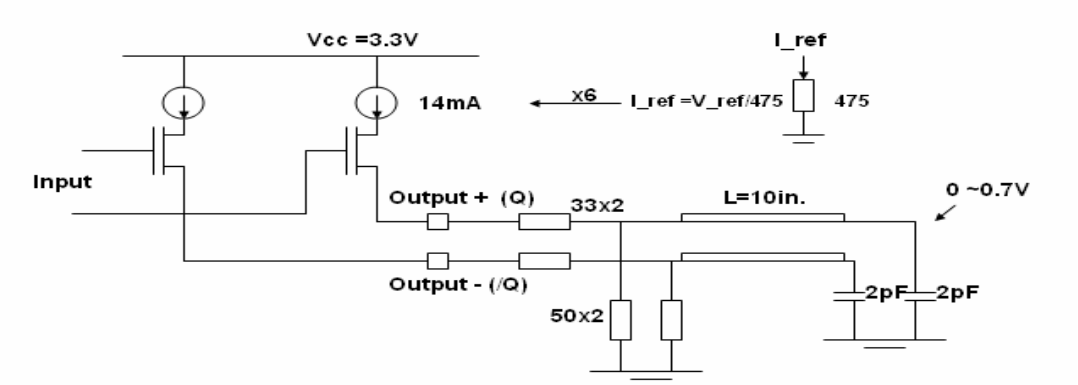


**Figure 5. HCSL driver in serial 33 and 50 pull-down termination**

## 2.4 CML Driver and Termination

CML(Current Mode Logic) is 50 ohm output drive and 50 ohm receive. It uses AC coupling in applications, such as ASIC data link and HDMI all use CML driver. Today more ASIC reference clock input specifies CML signal input too. So its DC level variation according to its Vcc supply as in the Figure 6. is not so important

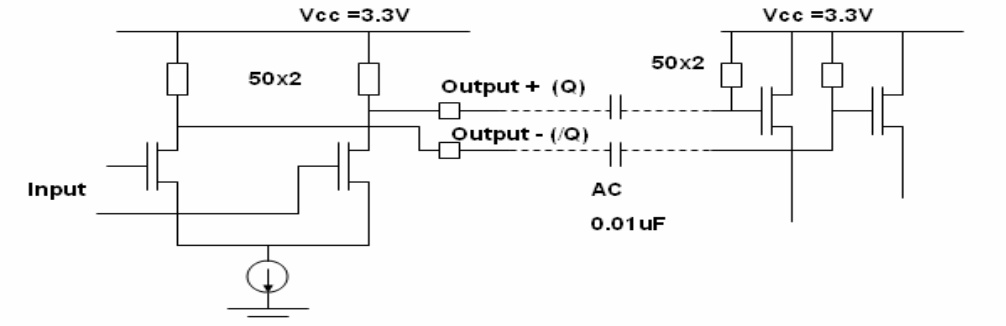


**Figure 6. CML driver and receiver diagram**

## 3. LVPECL LVDS HCSL and CML Transformation

Although those 4 type clocks have their own driver circuit structure, but they always can drive in DC or AC coupling if the receiver is the same type. But the real applications very often meet transformation termination between them in available clocks. The following Table 1. list the matrix of clock type transformation guide that suggests AC coupling is always preferred if driver and receiver are not in the same type.

**Table 1. LVPECL LVDS HCSL and CML transformation Guide**

| Drive \ Receive | LVPECL | LVDS | HCSL | CML |
|---|---|---|---|---|
| **LVPECL** | DC, AC Coupling | DC, AC Coupling | AC coupling | AC coupling |
| **LVDS** | DC, AC Coupling | DC, AC Coupling | AC coupling | AC coupling |
| **HCSL** | AC coupling | AC coupling | DC, (AC) (1) coupling | AC coupling |
| **CML** | AC coupling | AC coupling | AC coupling | DC, AC Coupling |

It is worth to note that differential receiver always has vary wide Vcm (common mode voltage) working range since it receive clock differentially such as Pericom most differential clock ICs can directly DC receive LVPECL, LVDS, HCSL drive as datasheet indicates. If the clock has internal bias, then can receive AC drive clock without external bias circuit by check datasheet.

### 3.1 LVPECL AC Drive ASIC Example

To isolate the different clock driver type DC level influence, many ASIC providers such as Broadcom and Freescale etc. suggest LVPECL AC coupling drive reference clock input as in Figure 7. and 8. One more note that they do not need external 100 cross termination if ASIC already has one inside the IC. But layout the cross 100 ohm in is fine for later board bring up. The double termination can do ASIC input clock swing in case needed.

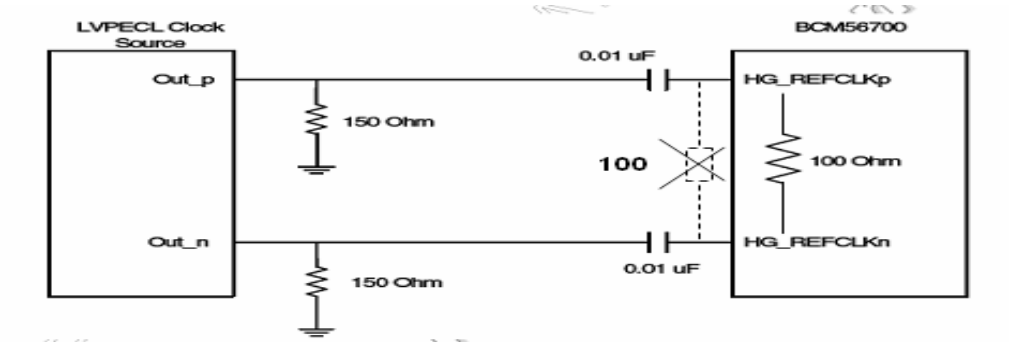


**Figure 7. Broadcom ASIC AC coupling receive LVPECL**

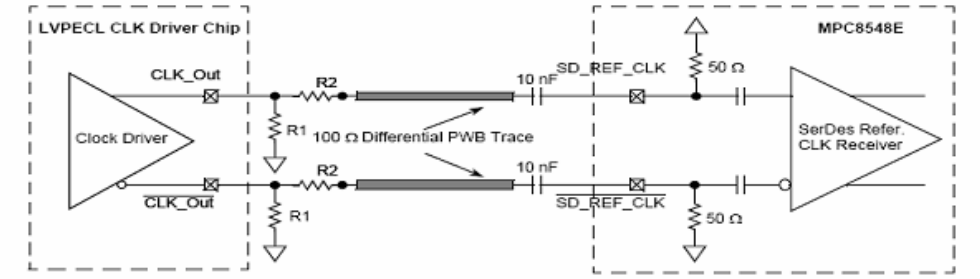


**Figure 8. Freescale CPU AC receive LVPECL clock**

But Freescale CUP PCIe and SGMII can accept HSCL DC coupling drive as shown in Figure 9. It is normal that HCSL drive 50 ohm termination will see half voltage swig drop vs. it drive high impedance by its original definition. It has no performance influence since the receiver has enough gain, normally =>200mV is enough.

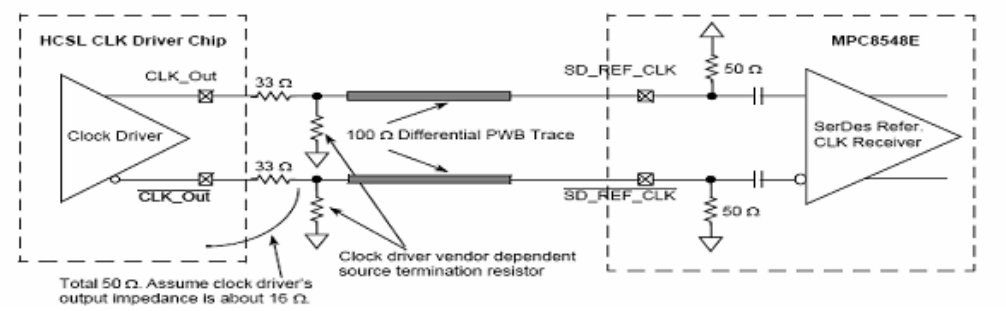


**Figure 9. Freescale CUP DC receive HCSL clock**

## 3.2 LVPECL LVDS and CML Drive HCSL

It is a straight forward optimal drive HCSL by using AC coupling of LVPECL, LVDS, and CML drivers, which uses 470/60 Thevenin termination for both HCSL DC bias recover and 50 ohm termination functions.

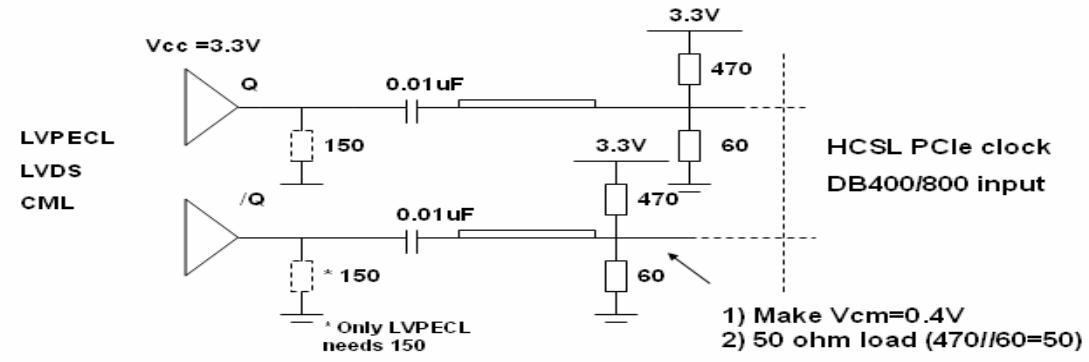


**Figure 10. LVPECL LVDS and CML Drive HCSL Input**

### 3.3 HCSL Drive LVPECL LVDS and CML

HCSL drives LVPECL and LVDS needs DC recover bias to their bias level. If ASIC can accept AC LVPECL and LVDS input, then the external bias is not needed. So HCSL can always drive CML input in AC coupling. As we mentioned before, that HCSL drive 50 ohm equivalent load will get ½ its voltage swing drop, which is normal in applications without any performance decay since those receivers have enough input voltage swing tolerance.

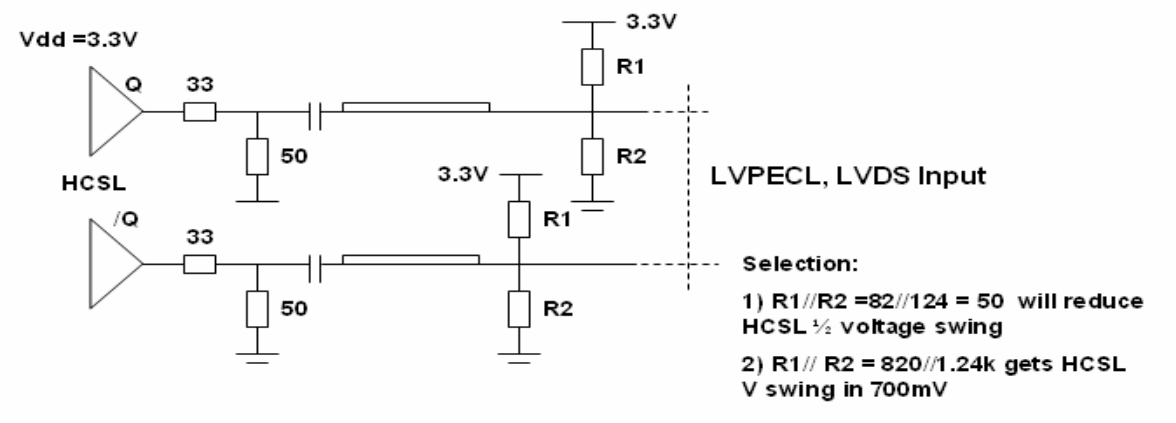


**Figure 11. HCSL Drive LVPECL and LVDS Input**

### 3.4 CMOS Drive Differential Input

CMOS clock voltage has full voltage swing to its supply, for example VDD=3.3V and 2.5V have 3.3V and 2.5V clock voltage swing respectively. When use CMOS clock to drive differential input, one of the diff input needs Thenvenin bias as shown in Figure 12. For example, R1=R2=1k (bias V= 1.65V) for 3.3V CMOS drive; R1=1.6k, R2=1k (bias V= 1.26V) for 2.5V CMOS clock drive to make the bias in 1/2 of CMOS voltage swing that is the best edge drive noise margin range.

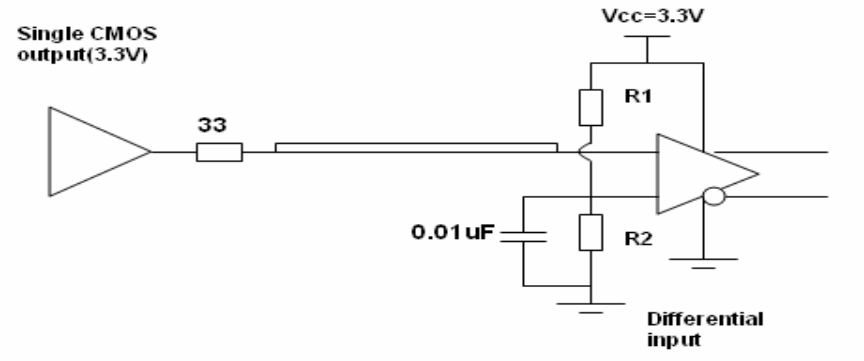


**Figure 12. HCSL Drive LVPECL and LVDS Input**

## 4. Pericom New 1.5GHz Differential Clock IC

.

Pericom is the major differential clock ICs supplier in the world. Its new PI6C49S1510 differential clock IC family can reach max. working frequency in 1.5GHz which provide supper margin for general Ethernet clocks 125MHz, 156.25MHz, and 312.5MHz or higher frequency clock applications as well as lower frequencies too.

PI6C49S1510 can set LVPECL, LVDS, and HCSL output in the same chip. Many big companies already qualify and design in this product for the coming popular 10GE and 40GE applications.

http://www.pericom.com/assets/Datasheets/PI6C49S1510.pdf
http://www.pericom.com/products/clocks/clock-ic/?input-type=Differential#tab-finder
http://www.pericom.com/products/clocks/hiflex-clock/

## Contact Information

Please contact Pericom regional sales reprehensive or franchised distributor at the company web:
http://www.pericom.com/
Pericom Clock IC marketing group
Phone: +1-408-435-0800