AN13164

iMX8MP PCIe Bandwith Analysis

Rev. 0 — February 24, 2021 Application Note

Contents

1 Introduction

The i.MX 8M Plus family focuses on Machine Learning (ML) and vision, advanced multimedia, and industrial IoT with high reliability. It is built to meet the needs of Smart Home, Building, City and Industry 4.0 applications.

PCI Express technology provides a high-speed scalable solution for reliable data transport. The PCIe IP of i.MX 8M Plus provides PCI Express Gen 3.0 x1 functionality.

2 Purpose

This document presents various usage scenarios for PCIe on the i.MX 8M Plus to provide a more clear understanding of the cases where near Gen3 x1 line rate bandwidth (8 Gbits/s) can be achieved after protocol overhead.

3 Acronyms and Abbreviations

Table 1. Acronyms and abbreviations

Acronyms and abbreviations	Description
PCIe	Peripheral Component Interconnect (PCI) Express
RC	Root Complex
EP	End Point
DMA	Direct Memory Access
DUT	Device Under Test
TLP	Transaction Layer Packet
MWr	Memory Write
MRd	Memory Read

4 Overview

4.1 Software environment

Linux BSP release 5.4.70_2.3.0 (GA for i.MX 8M Plus) was used to obtain the results presented in this document. The test procedure is based on the standard Linux PCI test.

The PCIe DMA benchmarking procedure made use of the new EP framework introduced starting with the 5.4.y release line. The 5.4.70 release includes fine tuning of the PCIe PHY registers, that allows to avoid bandwith impact due to the signal quality of the connection in test system hardware.

4.2 Hardware setup

The measurements were performed in two scenarios:

- i.MX 8M Plus - End Point ↔ i.MX 8M Plus – Root Complex
- i.MX 8M Plus - End Point ↔ i.MX 8QuadMax – Root Complex

In both cases the boards were connected using a PCIe M2 connector board.

Both i.MX 8M Plus and i.MX 8QuadMax are PCIe 3.0 capable.

5 Results

Table 2 presents the performance results obtained when transferring a buffer size of 8MB. The data is transferred using DMA.

Table 2. Performance results

EP (PCIe DMA transfer initiator)	Data Transfer Type related to i.MX 8M Plus	RC	Avg. Throughput (MB/s)
i.MX 8M Plus	READ FROM (i.MX 8M Plus EP Outbound MRd)	i.MX 8QuadMax	753
i.MX 8M Plus	WRITE TO (i.MX 8M Plus EP Outbound MWr)	i.MX 8QuadMax	809
i.MX 8QuadMax	READ FROM (i.MX 8M Plus RC Inbound MRd)	i.MX 8M Plus	793
i.MX 8QuadMax	WRITE TO (i.MX 8M Plus RC Inbound MWr)	i.MX 8M Plus	480
i.MX 8M Plus	READ FROM (i.MX 8M DUT-DUT)	i.MX 8M Plus	768
i.MX 8M Plus	WRITE TO (i.MX 8M DUT-DUT)	i.MX 8M Plus	441

Figure 1, Figure 2, and Figure 3 present how the throughput scales for various amounts of data being transferred.

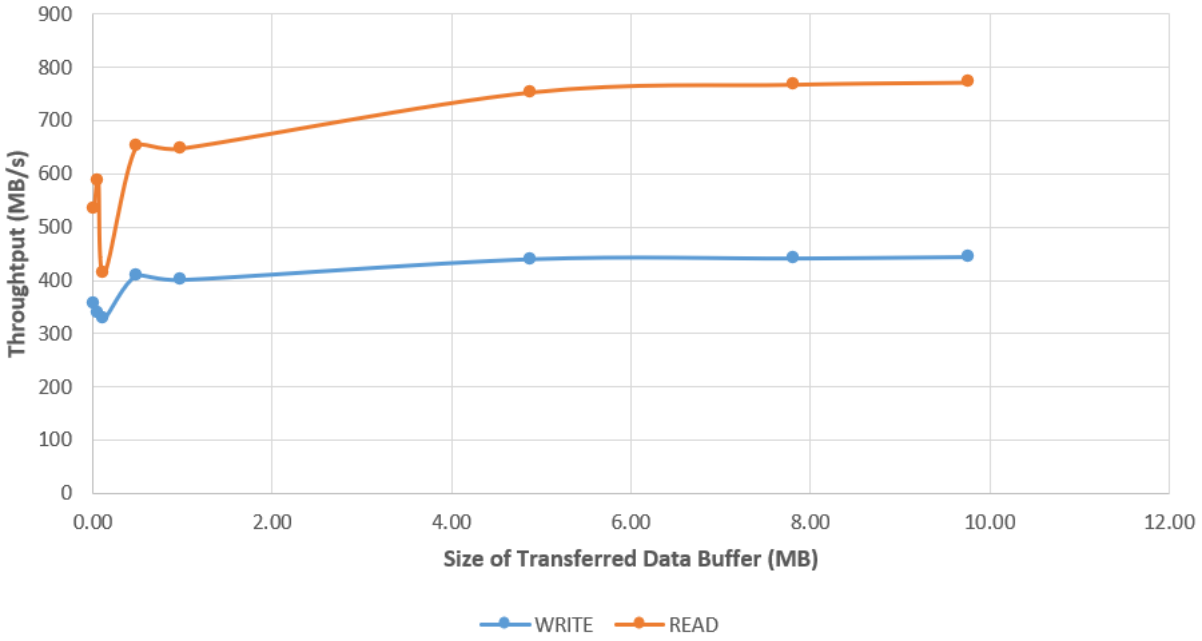

Figure 1. i.MX 8MP PCIe DUT-DUT Throughput Analysis
8MP - EP (DMA transfer initiator); 8MP - RC

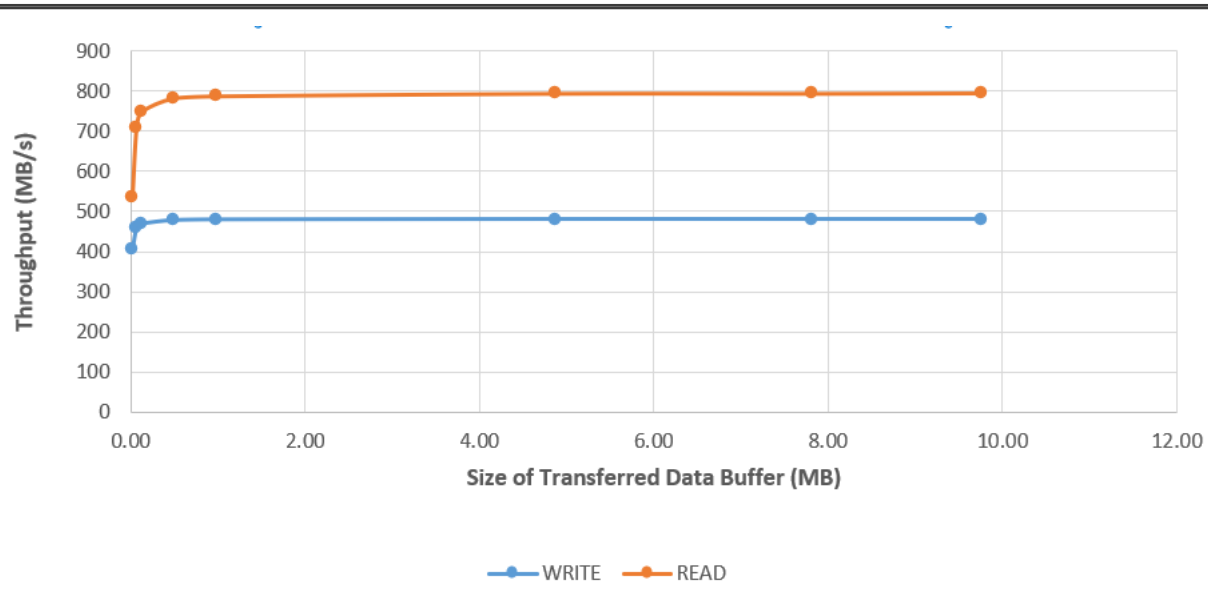

Figure 2. i.MX 8MP PCIe RC Inbound Throughput Analysis
8QM - EP (DMA transfer initiator); 8MP - RC

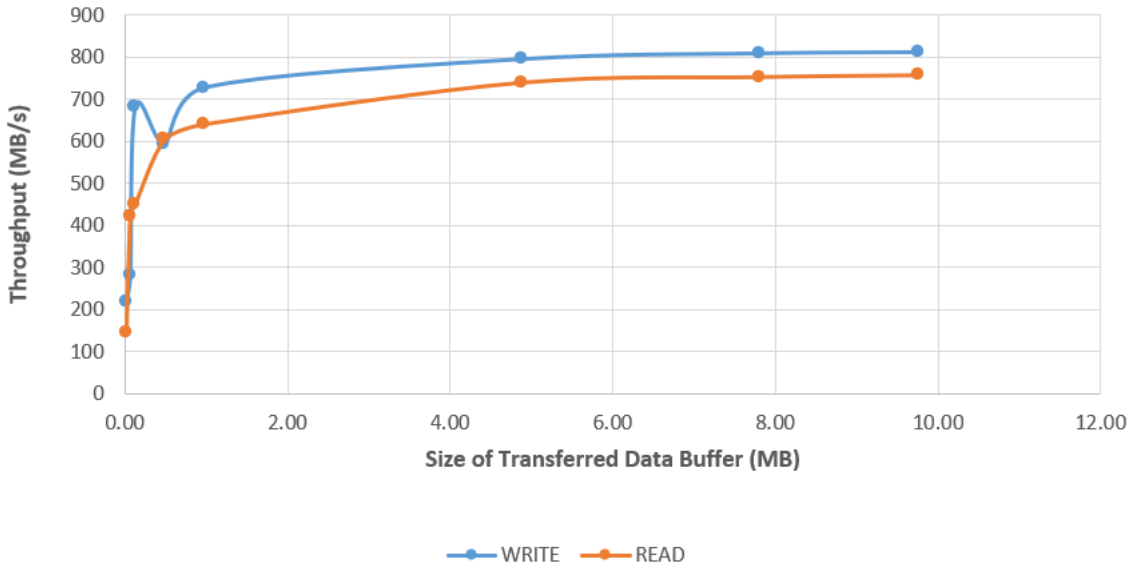

Figure 3. i.MX 8MP PCIe EP Outbound Throughput Analysis
8MP - EP (DMA transfer initiator); 8QM - RC

6 Results analysis

As shown in Table 2, one can notice that while in some cases the bandwidth fits Gen 3 expectations, in other cases it is limited to the performance slightly better than the realistic Gen2 throughput.

This is due to an i.MX 8M Plus limitation decribed below.

When the outstanding inbound write data transfer size exceeds 400 Bytes, the number of inbound MWr TLP transactions that the i.MX 8M Plus PCIe Controller can support is up to the combination of 12 headers and 400 bytes of data payload. This remains true as long as neither is exceeded.

NOTE

This limitation can also be noticed on i.MX 8M Mini and i.MX 8M Quad regardless of the PCIe Gen X.

Higher performance can be obtained to achieve the same goal by having the i.MX 8M Plus issue outbound MRd transactions instead of using inbound MWr.

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