i.MX23 Reference Schematics

Rev. C

Revision History

REV. A - 7/1/2009

- Original Release

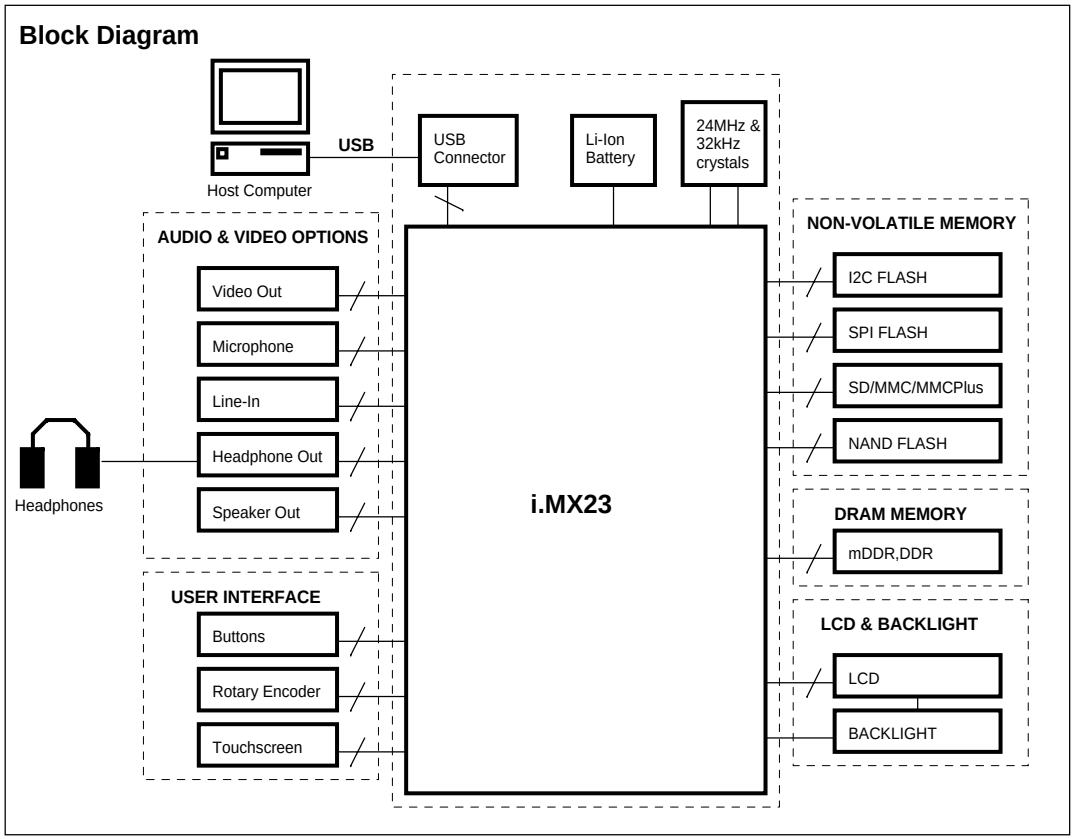
REV. B - 8/12/2009

- Added 128QFP Package
- Added external speaker amplifier option.

REV. C - 2/12/2010

- Added i.MX23 5V Only, No Li-Ion Battery Configuration
- Clarified operation and limitations of RESET circuitry when powered from 5V or from li-ion battery.
- Added guidance on selection of mDDR or DDR1 device.

Block Diagram



NOTE: These schematics are subject to change.

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Drawing Title: i.MX23 REFERENCE SCHEMATICS

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i.MX23 EXAMPLE COMPONENTS

DCDC Inductor

For best battery life, the DCDC inductor should have a low DC resistance. The current rating of the inductor should be higher than the measured peak current through the inductor, which will be application-specific. The inductor value is recommended to be between 4.7uH and 15uH.

Note that inductors with a higher DC resistance may be used, but may impact battery life

Reference Designator	Description	Manufacturer	Manufacturer Part Number
L1	15uH, 900mA, 213mOhm RDC	Sumida	CDRH3D28NP-150N
L1	10uH, 690mA, 18mOhm RDC	Panasonic	ELL4LM100M
L1	15uH, 500mA, 520mOhm RDC	Nantong Meda (MEDAFA)	MAH 32-150

DCDC Output Capacitors

The C1, C8, and C14 output capacitors should have an ESR less than 400mOhms. Ceramic capacitors are recommended (Y5V capacitors should not be used for C1, C8, or C14).

Reference Designator	Description	Manufacturer	Manufacturer Part Number
C1,C8,C14	33uF, X5R, 6.3V , Ceramic Capacitor	Murata	GRM32DR60J336ME19L

32kHz Crystal

Reference Designator	Description	Manufacturer	Manufacturer Part Number
Y2	32kHz 20ppm Crystal	Seiko	VT200FA-6PF20PPM
Y2	32kHz 20ppm Crystal	Seiko	SSPT7FA-7PF20PPM

24MHz Crystal

Reference Designator	Description	Manufacturer	Manufacturer Part Number
Y1	24MHz 30ppm Crystal	Jing Feng	24.000MHz Jing Feng Crystal 2x6mm cylinder, +/- 30ppm, CL = 10pF

USB Ferrites and ESD Protection

Reference Designator	Description	Recommended Manufacturer	Manufacturer Part Number
L22	Ferrite, DCR < 100mOhm, 68 ohms @ 100MHz, 1A	Steward	MI0603J680R-10
L50	Ferrite, DCR < 400mOhm, 1500 ohms @ 100MHz, 400mA	Steward	HZ0805D152R-10
D2	ESD Protection Diode	ON Semi.	NZL6V8AXV3T1

Audio Input / Output Ferrites

Reference Designator	Description	Recommended Manufacturer	Manufacturer Part Number
L4, L5, L6, L7, L8, L9, L19, L20, L21	Ferrite, DCR < 400mOhm, 1500 ohms @ 100MHz	Steward	HZ0805D152R-10

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Page Title: RECOMMENDED COMPONENTS

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i.MX233 169-Pin Package
Li-Ion Battery or 5V Powered Configuration

The i.MX233 should use ceramics + 100 mOhm series resistors or low-ESR tantalums for both the VDD4P2 and the LI-ION BATTERY supplies to prevent a battery charger oscillation issue.

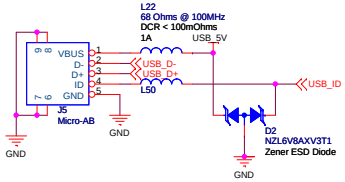
USB 2.0 Connector

Route USB D+ and D- according to the High Speed USB2.0 Design Guidelines. D+ and D- should have a 90 ohm differential trace impedance and the PCB should have a 20 mil minimum spacing between the USB data lines (D+ and D-) and other signal lines.

In order to maximize ESD immunity, the industrial design plastics should expose the USB Connector as little as possible.

The L22 ferrite is recommended for ESD immunity. Note that any ferrite in series with the USB_5V supply should have a low DCR (<100mOhms).

The D2 Zener Diode is strongly recommended to protect the VDD5V pin of the i.MX23 from damaging overvoltage conditions that can result from USB cable attachments or from ESD events.

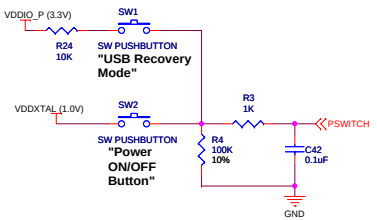


For applications that support cable-based detection of Host or Device modes.

USB_ID >> SSP1_DETECT

POWER & RECOVERY BUTTONS

Note that button SW1 could be assigned to another function as well during normal, non-recovery operation.



RESET CIRCUIT

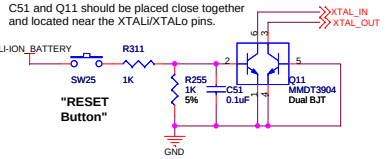
Pressing the RESET button in the circuit shown below will cause a full system reset (i.e., the i.MX processor will reset and all the i.MX DCDC output rails will be pulled to ground) if the following conditions are true:

1) The i.MX is being powered from a Li-Ion battery
2) No 5V source is present on the i.MX VDD5V pin

If a 5V source is present on the VDD5V pin, pressing the RESET button will still cause a i.MX processor reset, but the VDDIO, VDDA, VDDM, and VDDD supply rails will not be pulled to ground.

Note: A dual BJT is recommended to provide equal capacitive loading to both XTALi and XTALo. If a single BJT is used on XTALi, the xtal load capacitor values should be adjusted to account for the BJT loading (typically ~5pF).

C51 and Q11 should be placed close together and located near the XTALi/XTALo pins.



Note: C15, C30 and C31 should be located close to the i.MX device.

XTAL must be close to the i.MX233

XTAL must be close to the i.MX233

Consult XTAL datasheet for recommended load capacitor values.

NOTE: Use double vias for these VDDIO_EMI pinsand place the bypass capacitors as close as possible - one for ball L6 and one for balls L8 / L10.

i.MX233
169-BGA

IMPORTANT LAYOUT DESIGN NOTES

1) The crystals should be placed as close as possible to the i.MX device.

2) For best USB jitter performance, the VDDXTAL capacitor and the crystal load capacitors should NOT connect to the ground plane near the DRAM bus routing and grounds. These ground connections should preferably be close to the VAG bypass capacitor.

3) All DCDC input & output capacitors should be located close to the i.MX device.

IMPORTANT CRYSTAL DESIGN NOTES

Consult crystal manufacturer datasheet for recommended load capacitor values (typically 10-18pF).

Cload = [(C26*C27) / (C26+C27)] + Cstray

where Cstray = stray PCB capacitance, typically 4 - 6 pF

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Drawing Title: **i.MX23 REFERENCE SCHEMATICS**

Page Title: **i.MX233 169-BGA**

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i.MX233 169-Pin Package
5V Only Configuration (No Li-Ion Battery)

This schematic shows an application running off of 5V always, with no Li-Ion battery. The primary differences in this schematic compared to the Li-Ion battery case are:

1) The connection of the i.MX's PMU VDD4P2, BATT, and DCDC_BATT pins.
2) The RESET circuit.
3) The POWER button circuit (or lack thereof).

OPTIONAL RTC BACKUP

D19, R327, R238, and SC1 are optional components that may be added if the application requires the RTC to remain powered even if 5V power is lost.

To use this circuit, populate D19, R327, and SC1, and remove R329.

Value of SuperCap required will be determined by amount of time required to power RTC without 5V present and the RTC current (typically ~13uA for the 32kHz).

D19 BAT30 Schottky DNP-RTC
R258 0.100 Ohm
C66 33uF Ceramic
C67 1uF
C68 0.1uF
R327 200 DNP-RTC
SC1 SuperCap 4.5V DNP-RTC
R329 1K
R330 1K

The i.MX233 should use ceramics + 100 mOhm series resistors or low-ESR tantalums for the VDD4P2 supply.

C2 0.01uF
C3 0.1uF
C4 1uF
C1 33uF
C43 0.01uF
C45 0.1uF
C44 1uF
C50 33uF
C9 0.01uF
C10 0.1uF
C11 1uF
C8 33uF
L1 15uH
C46 0.1uF
C48 0.1uF
C7 1uF
C12 0.1uF
C13 0.1uF
C5 0.1uF
C6 0.1uF

NOTE: Use double vias for these VDDIO_EMI pinsand place the bypass capacitors as close as possible - one for ball L6 and one for balls L8 / L10.

POWER & RECOVERY BUTTONS

There is no need for a POWER button in a 5V only configuration. If a 5V source is present on the VDD5V pin, the i.MX device will automatically power up. There is also no way to power down the i.MX PMU's outputs (VDDIO, VDDA, VDDM, & VDDD) if a 5V source is present on the VDD5V pin. If true power down is required, it is recommended to add a switch to the 5V source.

Note that button SW1 could be assigned to another function as well during normal, non-recovery operation.

VDDIO_P (3.3V) — SW1 SW PUSHBUTTON "USB Recovery Mode" — R3 1K — PSWITCH
R24 10K
R4 100K 10%
C42 0.1uF

OPTIONAL USB5V / WALL 5V MUX CIRCUIT

WALL_5V — D20 MBR160M-40 Schottky — 5V
USB_5V
Q28 Si2305
R255 1M

OPTIONAL RESET CIRCUIT

SW25 "RESET Button"
Q27 Si2305
R311 1K
C51 0.1uF
R255 1M

Pressing the RESET button in the circuit shown above will cause a full system reset (i.e., the i.MX processor will reset and all the i.MX DCDC output rails will be pulled to ground).

If not used, short the VDD5V net to the USB5V net.

VDD5V — C129 0.1uF — C130 4.7uF — R256 1 Ohm — USB_D+ / USB_D-

U1 i.MX233 -169BGA

VDDA (1.8V): C18 0.1uF, C19 1uF
VDDXTAL (1.0V): C25 0.1uF, C16 1uF
LI-ION_BATTERY
SPKR+ / SPKR-
HP_R / HP_L
HP_VGND
LINE_IN_R / LINE_IN_L
MIC
VDAC1

LRADC0 / TEMP / MICBIAS
LRADC1 / TEMP / MICBIAS
LRADC2 / TOUCH_X+ / LINE2_INL
LRADC3 / TOUCH_Y+ / LINE2_INR
LRADC4 / TOUCH_X-
LRADC5 / TOUCH_Y-

PSWITCH
SERIAL_JTAG — R2 100K 10%

XTAL_IN / XTAL_OUT — Y1 24.000MHz — C26 XPF — C27 XPF
XTAL must be close to the i.MX233

Y2 32.768kHz 30ppm — C28 XPF — C29 XPF
Consult XTAL datasheet for recommended load capacitor values.

i.MX233 169-BGA

GPMI_D00 / LCD_D08 / SSP2_DATA0
GPMI_D01 / LCD_D09 / SSP2_DATA1
GPMI_D02 / LCD_D10 / SSP2_DATA2
GPMI_D03 / LCD_D11 / SSP2_DATA3
GPMI_D04 / LCD_D12 / SSP2_DATA4
GPMI_D05 / LCD_D13 / SSP2_DATA5
GPMI_D06 / LCD_D14 / SSP2_DATA6
GPMI_D07 / LCD_D15 / SSP2_DATA7
GPMI_D08 / LCD_D18 / SSP1_DATA4
GPMI_D09 / LCD_D19 / SSP1_DATA5
GPMI_D10 / LCD_D20 / SSP1_DATA6
GPMI_D11 / LCD_D21 / SSP1_DATA7
GPMI_D12 / LCD_D22
GPMI_D13 / LCD_D23
GPMI_D14 / UART2_RX
GPMI_D15 / UART2_TX / GPMI_CE3n

GPMI_CE0n
GPMI_CE1n
GPMI_CE2n
GPMI_RDY0 / SSP2_DETECT
GPMI_RDY1 / SSP2_CMD
GPMI_RDY2
GPMI_RDY3
GPMI_WRn / SSP2_SCK
GPMI_RDn
GPMI_WPn
GPMI_CLE / LCD_D16
GPMI_ALE / LCD_D17

SSP1_DETECT / GPMI_CE3n / USB_ID
SSP1_DATA2 / I2C_SDA
SSP1_DATA1 / I2C_SCL
SSP1_DATA0 / SPI_MISO
SSP1_CMD / SPI_MOSI
SSP1_SCK
SSP1_DATA3 / SPI_SS

LCD_D00
LCD_D01
LCD_D02
LCD_D03
LCD_D04
LCD_D05
LCD_D06
LCD_D07
LCD_D08 / SAIF2_D0
LCD_D09 / SAIF1_D0
LCD_D10 / SAIF_BITCLK
LCD_D11 / SAIF_LRCLK
LCD_D12 / SAIF2_D1
LCD_D13 / SAIF2_D2
LCD_D14 / SAIF1_D2
LCD_D15 / SAIF1_D1
LCD_D16 / SAIF1_ALTBITCLK
LCD_D17

LCD_CS
LCD_RS / LCD_CCIRCLK
LCD_RESET / GPMI_CE3n
LCD_WR_E
LCD_ENABLE / I2C_SCL
LCD_HSYNC / I2C_SDA
LCD_VSYNC / LCD_BUSY
LCD_DOTCLK / GPMI_RDY3

PWM0 / ROTARYA / UARTDBG_RX
PWM1 / ROTARYB / UARTDBG_TX
PWM2 / GPMI_RDY3
PWM3 / UART1_CTS
PWM4 / UART1_RTS

ROTARYB / UART2_CTS / GPMI_CE3n
ROTARYA / UART2_RTS / SPDIF

I2C_SDA / GPMI_CE2n / UART1_RX
I2C_SCL / GPMI_RDY2 / UART1_TX

UART1_RX / SSP1_DATA6
UART1_TX / SSP1_DATA7
UART1_CTS / SSP1_DATA4
UART1_RTS / SSP1_DATA5

EM_D00 … EM_D15
EM_A00 … EM_A12
EM_CE0n … EM_CE1n
EM_DQM0 … EM_DQM1
EM_DQS0 … EM_DQS1
EM_CLK … EM_CLKn
EM_BA0 … EM_BA1
EM_RASn
EM_CASn
EM_WEn
EM_CKE

USB 2.0 Connector

Route USB D+ and D- according to the High Speed USB2.0 Design Guidelines. D+ and D- should have a 90 ohm differential trace impedance and the PCB should have a 20 mil minimum spacing between the USB data lines (D+ and D-) and other signal lines.

In order to maximize ESD immunity, the industrial design plastics should expose the USB Connector as little as possible.

The L22 ferrite is recommended for ESD immunity. Note that any ferrite in series with the USB_5V supply should have a low DCR (<100mOhms).

The D2 Zener Diode is strongly recommended to protect the VDD5V pin of the i.MX23 from damaging overvoltage conditions that can result from USB cable attachments or from ESD events.

L22 68 Ohms @ 100MHz DCR < 100mOhms 1A — USB_5V
J5 Micro-AB — USB_D- / USB_D+ / USB_ID / GND
L50
D2 NZL6V8AXV3T1 Zener ESD Diode

For applications that support cable-based detection of Host or Device modes.
USB_ID — SSP1_DETECT

IMPORTANT LAYOUT DESIGN NOTES

1) The crystals should be placed as close as possible to the i.MX device.

2) For best USB jitter performance, the VDDXTAL capacitor and the crystal load capacitors should NOT connect to the ground plane near the DRAM bus routing and grounds. These ground connections should preferably be close to the VAG bypass capacitor.

3) All DCDC input & output capacitors should be located close to the i.MX device.

IMPORTANT CRYSTAL DESIGN NOTES

Consult crystal manufacturer datasheet for recommended load capacitor values (typically 10-18pF).

Cload = [(C26*C27) / (C26+C27)] + Cstray

where Cstray = stray PCB capacitance, typically 4 - 6 pF

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Drawing Title: i.MX23 REFERENCE SCHEMATICS
Page Title: i.MX233 169-BGA 5V Only
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i.MX233 128-Pin LQFP Package
Li-Ion Battery or 5V Powered Configuration

The i.MX233 should use ceramics + 100 mOhm series resistors or low-ESR tantalums for both the VDD4P2 and the LI-ION BATTERY supplies to prevent a battery charger oscillation issue.

Note: C15, C30 and C31 should be located close to the i.MX device.

USB 2.0 Connector

Route USB D+ and D- according to the High Speed USB2.0 Design Guidelines. D+ and D- should have a 90 ohm differential trace impedance and the PCB should have a 20 mil minimum spacing between the USB data lines (D+ and D-) and other signal lines.

In order to maximize ESD immunity, the industrial design plastics should expose the USB Connector as little as possible.

The L22 ferrite is recommended for ESD immunity. Note that any ferrite in series with the USB_5V supply should have a low DCR (<100mOhms).

The D2 Zener Diode is strongly recommended to protect the VDD5V pin of the i.MX23 from damaging overvoltage conditions that can result from USB cable attachments or from ESD events.

For applications that support cable-based detection of Host or Device modes.

USB_ID >> SSP1_DETECT

POWER & RECOVERY BUTTONS

Note that button SW1 could be assigned to another function as well during normal, non-recovery operation.

RESET CIRCUIT

Pressing the RESET button in the circuit shown below will cause a full system reset (i.e., the i.MX processor will reset and all the i.MX DCDC output rails will be pulled to ground) if the following conditions are true:

1) The i.MX is being powered from a Li-Ion battery
2) No 5V source is present on the i.MX VDD5V pin

If a 5V source is present on the VDD5V pin, pressing the RESET button will still cause a i.MX processor reset, but the VDDIO, VDDA, VDDM, and VDDD supply rails will not be pulled to ground.

Note: A dual BJT is recommended to provide equal capacitive loading to both XTALi and XTALo. If a single BJT is used on XTALi, the xtal load capacitor values should be adjusted to account for the BJT loading (typically ~5pF).

C51 and Q11 should be placed close together and located near the XTALi/XTALo pins.

XTAL must be close to the i.MX233

Consult XTAL datasheet for recommended load capacitor values.

i.MX233
128-QFP

IMPORTANT LAYOUT DESIGN NOTES

1) The crystals should be placed as close as possible to the i.MX device.

2) For best USB jitter performance, the VDDXTAL capacitor and the crystal load capacitors should NOT connect to the ground plane near the DRAM bus routing and grounds. These ground connections should preferably be close to the VAG bypass capacitor.

3) All DCDC input & output capacitors should be located close to the i.MX device.

IMPORTANT CRYSTAL DESIGN NOTES

Consult crystal manufacturer datasheet for recommended load capacitor values (typically 10-18pF).

Cload = [(C26*C27) / (C26+C27)] + Cstray

where Cstray = stray PCB capacitance, typically 4 - 6 pF

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Drawing Title: i.MX23 REFERENCE SCHEMATICS

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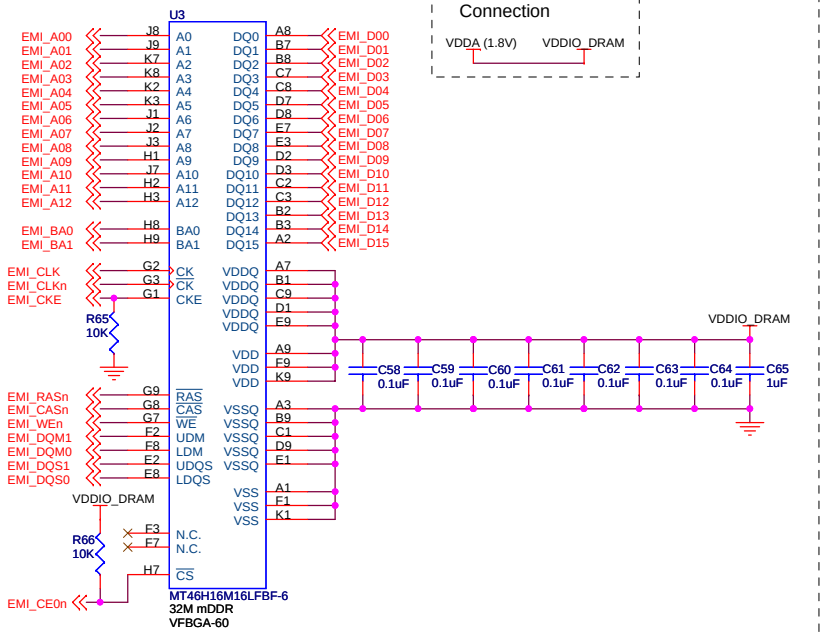
1.8V Mobile DDR

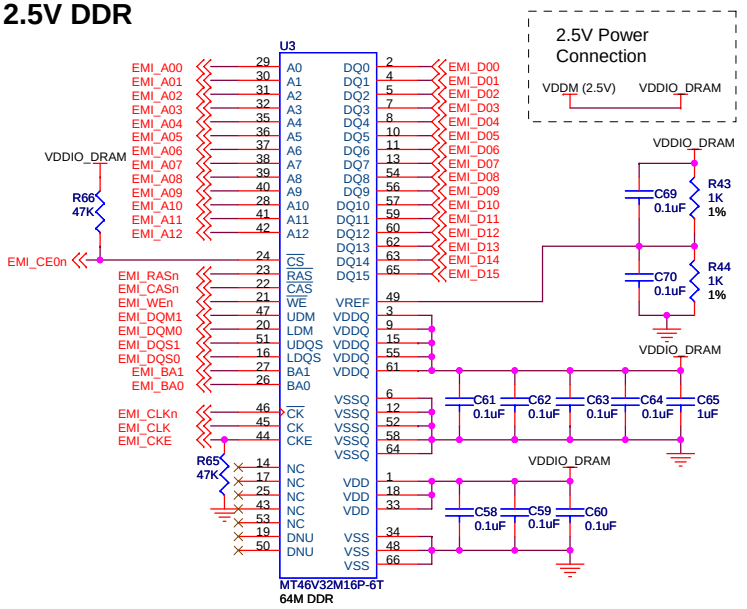


mDDR Recommendations

- Maximum Capacity: 64MB per chip enable. This limitation is because most (if not all) of DRAMs > 64MB require 14 row bits and the i.MX23 supports 13 row bits maximum.
- The 128QFP has 1 chip enable for a maximum capacity of 64MB and the 169BGA has 2 chip enables for a maximum capacity of 128MB (requires use of 2 x 64MB DDR devices).
- x16 data bus
- For best performance, the mDDR should support the maximum i.MX23 DRAM clock frequency (~160MHz) with CAS Latency = 3

Reference Designator	Description	Manufacturer	Manufacturer Part Number
U3	1.8V, 32MB, x16, 166MHz mDDR	Micron	MT46H16M16LFBF-6

2.5V DDR



DDR1 Recommendations

- Maximum Capacity: 64MB per chip enable. This limitation is because most (if not all) of DRAMs > 64MB require 14 row bits and the i.MX23 supports 13 row bits maximum.
- The 128QFP has 1 chip enable for a maximum capacity of 64MB and the 169BGA has 2 chip enables for a maximum capacity of 128MB (requires use of 2 x 64MB DDR devices).
- x16 data bus
- For best performance, the DDR1 should support the maximum i.MX23 DRAM clock frequency (~150MHz) with CAS Latency = 2.5

Reference Designator	Description	Manufacturer	Manufacturer Part Number
U3	2.5V, 64MB, x16, 166MHz DDR1	Micron	MT46V32M16P-6T

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Drawing Title: **i.MX23 REFERENCE SCHEMATICS**

Page Title: **DRAM**

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NAND FLASH

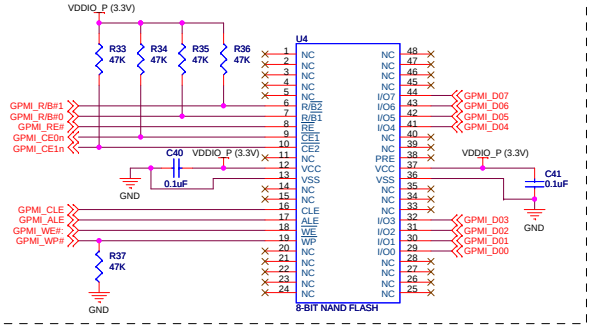
Important Design Notes

1) The WP# pull-down resistor is required to protect the flash memory from inadvertent writes during power transitions.
2) All CE# and R/B# pins require pull up resistors. Note that the i.MX23 has integrated CE# and R/B# pull-up resistors that must be enabled by OTP.
3) The circuits below show dual-CE NAND flash. If using a single-CE NAND flash, change pins 6 and 10 to NO CONNECT.

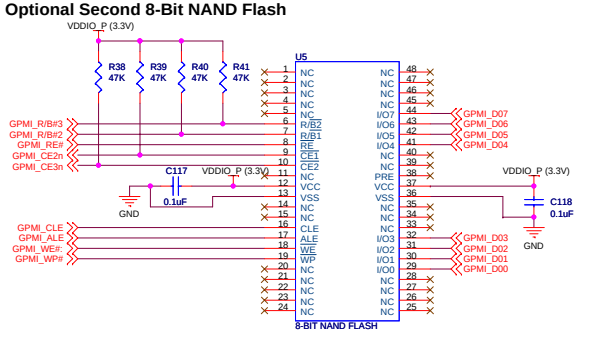
GPMI_CE3n Pin Assignment Options

On Page Net Name	i.MX23 Pin Assignment	
GPMI_CE3n	GPMI_D15	Option 1: BSP Default
GPMI_CE3n	ROTARYB	Option 2
GPMI_CE3n	LCD_RESET	Option 3
GPMI_CE3n	SSP1_DETECT	Option 4

8-Bit NAND Flash



Optional Second 8-Bit NAND Flash



SD/MMC/MMCPlus

SD/MMC/MMCPlus Pin Assignment Options

Option 1: SSP1 (BSP Default Configuration)

On Page Net Name	i.MX23 Pin Assignment
SSP_CMD	SSP1_CMD
SSP_SCK	SSP1_SCK
SSP_DATA0	SSP1_DATA0
SSP_DATA1	SSP1_DATA1
SSP_DATA2	SSP1_DATA2
SSP_DATA3	SSP1_DATA3
SSP_DATA4	GPMI_D08
SSP_DATA5	GPMI_D09
SSP_DATA6	GPMI_D10
SSP_DATA7	GPMI_D11
SSP_DETECT	SSP1_DETECT

Option 2: SSP1 (Alternate Configuration)

On Page Net Name	i.MX23 Pin Assignment
SSP_CMD	SSP1_CMD
SSP_SCK	SSP1_SCK
SSP_DATA0	SSP1_DATA0
SSP_DATA1	SSP1_DATA1
SSP_DATA2	SSP1_DATA2
SSP_DATA3	SSP1_DATA3
SSP_DATA4	UART1_CTS
SSP_DATA5	UART1_RTS
SSP_DATA6	UART1_RX
SSP_DATA7	UART1_TX
SSP_DETECT	SSP1_DETECT

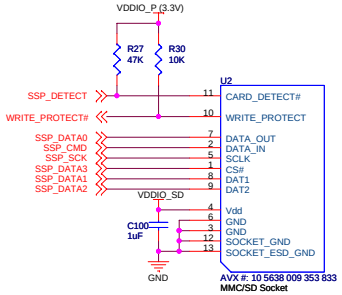
Option 3: SSP2

On Page Net Name	i.MX23 Pin Assignment
SSP_CMD	GPMI_R/B#1
SSP_SCK	GPMI_WE#:
SSP_DATA0	GPMI_D00
SSP_DATA1	GPMI_D01
SSP_DATA2	GPMI_D02
SSP_DATA3	GPMI_D03
SSP_DATA4	GPMI_D04
SSP_DATA5	GPMI_D05
SSP_DATA6	GPMI_D06
SSP_DATA7	GPMI_D07
SSP_DETECT	GPMI_R/B#0

Important Design Notes

1) The SD/MMC socket should have an integrated, normally-open, mechanical CARD DETECT switch.
2) The i.MX23 has integrated pull up resistors for the SD/MMC DATA and CMD signals that must be enabled by setting a register.

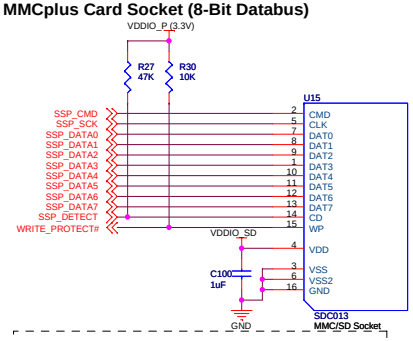
SD / MMC Card Socket (4-Bit Databus)



WRITE_PROTECT# refers to the user-selectable slide switch on SD/MMC cards. This support is optional and can be assigned to any free GPIO pin (not just PWM4).

PWM4 <<>> WRITE_PROTECT#

MMCplus Card Socket (8-Bit Databus)



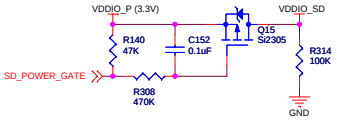
WRITE_PROTECT# refers to the user-selectable slide switch on SD/MMC cards. This support is optional and can be assigned to any free GPIO pin (not just PWM4).

PWM4 <<>> WRITE_PROTECT#

Required Power Switch for Removable SD/MMC Media

This circuitry gates power to the SD/MMC/MMCPlus socket. This ensures reliable operation with some SD/MMC/MMCPlus cards that require large amounts of current at insertion.

At start-up, SD_POWER_GATE is high and VDDIO_SD is unpowered. When CARD_DETECT goes low due to card insertion, firmware will drive SD_POWER_GATE low to connect VDDIO_P to VDDIO_SD. After waiting 30 msec to allow the VDDIO_SD supply to stabilize, the firmware will enable the internal SSP_DATA and SSP_CMD pull-up resistors and begin communicating with the SD/MMC card. When the card is removed and CARD_DETECT goes high, SD_POWER_GATE will be driven high again.

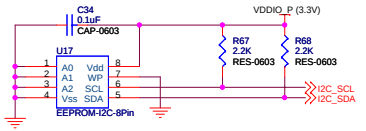


If the application does not need to boot from the SSP port, the SD_POWER_GATE function can be assigned to any free GPIO pin (not just PWM3). However, if the SD/MMC/MMCPlus device is the boot device, SD_POWER_GATE must be driven by the ROM, which supports only 3 OTP-selectable options: PWM0, LCD_DOTCLK, or PWM3.

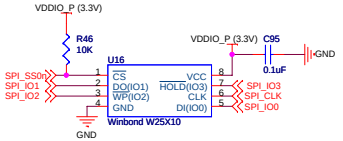
PWM3 <<>> SD_POWER_GATE

I2C EEPROM

Use Microchip 24LCxx-I/P or Equivalent



SPI FLASH



Reference Designator	Description	Manufacturer	Manufacturer Part Number
U16	SPI Flash, 3.0V	Winbond	W25X10

SPI Flash Pin Assignment Options

Option 1: SSP1

On Page Net Name	i.MX23 Pin Assignment
SPI_SS0n	SSP1_DATA3
SPI_CLK	SSP1_SCK
SPI_IO0	SSP1_CMD
SPI_IO1	SSP1_DATA0
SPI_IO2	SSP1_DATA1
SPI_IO3	SSP1_DATA2
SPI_SS1n	SSP1_DATA4
SPI_SS2n	SSP1_DATA5

Option 2: SSP2

On Page Net Name	i.MX23 Pin Assignment
SPI_SS0n	GPMI_D03
SPI_CLK	GPMI_WE#:
SPI_IO0	GPMI_R/B#1
SPI_IO1	GPMI_D00
SPI_IO2	GPMI_D01
SPI_IO3	GPMI_D02
SPI_SS1n	GPMI_D04
SPI_SS2n	GPMI_D05

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Page Title: NON-VOLATILE MEMORY OPTIONS

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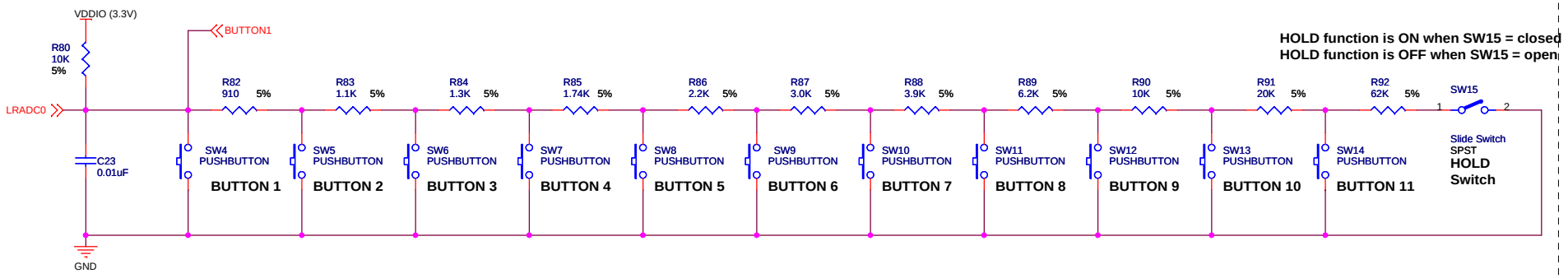
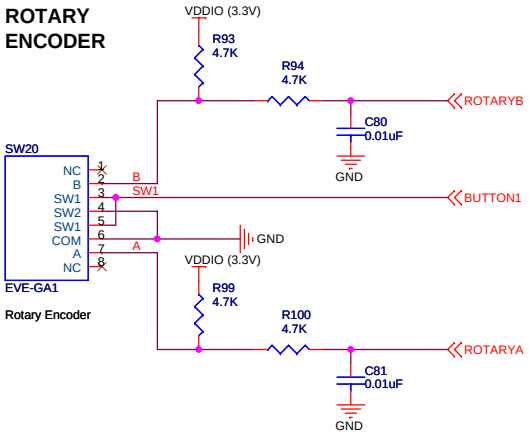
BUTTONS

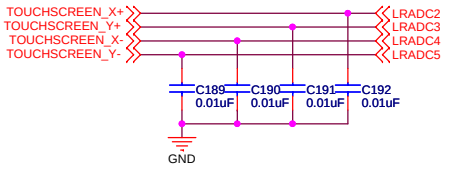


HOLD function is ON when SW15 = closed
HOLD function is OFF when SW15 = open

ROTARY ENCODER



RESISTIVE TOUCHSCREEN / TOUCHPANEL



NOTE: If using a device with an impedance greater than a few kOhms (such as a Touchpanel), the C189-C192 filter capacitors on the LRADC channels may be reduced to 5pF. These smaller capacitors reduce the settling time, which reduces the amount of time the processor must wait to take an accurate reading.
These filter capacitors should be placed close to the i.MX23.

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Page Title:
USER INTERFACE

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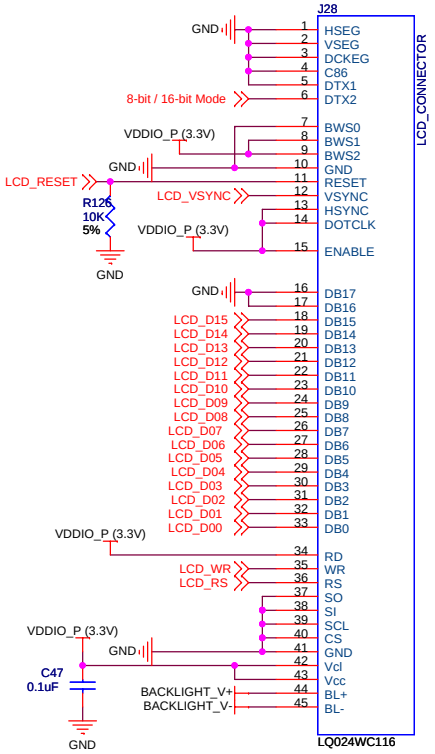
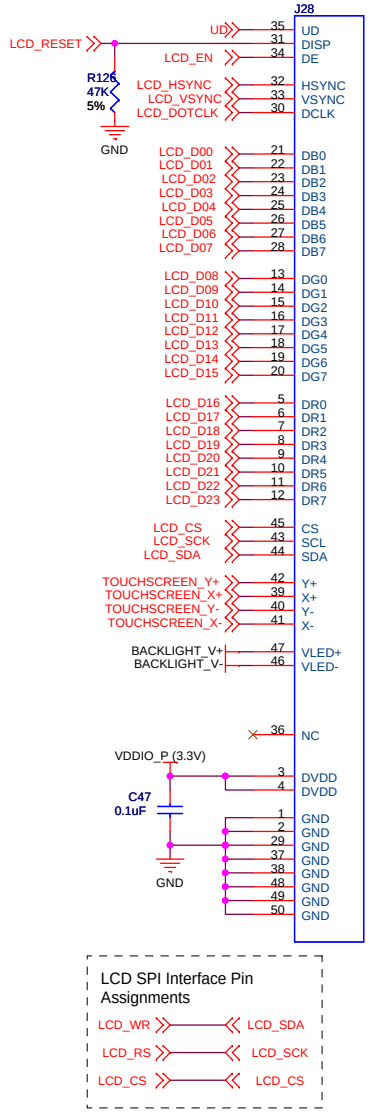
LCD & LED DISPLAY OPTIONS

LCD (8-bit or 16-bit 8080 System Mode)

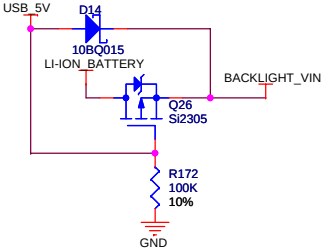


LCD (24-bit DOTCLK Mode)



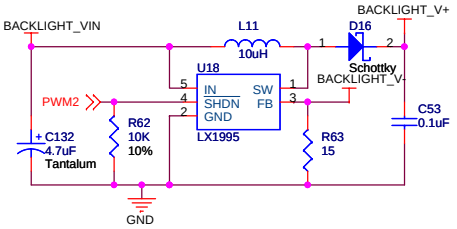
LCD SPI Interface Pin Assignments

Recommended Backlight Power Selection



External Backlight Boost Circuit

Backlight should have 3 or more LEDs in series. If the backlight has fewer than 3 LEDs, the backlight may draw power even if the player is powered off.



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Page Title: **LCD**

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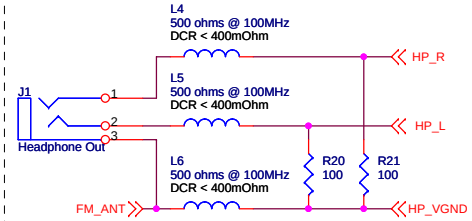
i.MX23 HEADPHONE-OUT OPTIONS

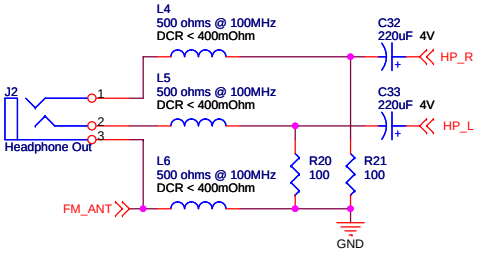
OPTION 1: Direct Drive Headphone Jack (Recommended)

NOTE:
- FM_ANT is the antenna for designs with an FM Tuner
- L4, L5, L6 should be as close as possible to the headphone jack.



OPTION 2: AC-Coupled Headphone Jack

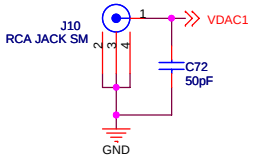
NOTE:
- FM_ANT is the antenna for designs with an FM Tuner
- L4, L5, L6 should be as close as possible to the headphone jack.



i.MX23 VIDEO OUT

Single or Double Termination

The VIDEO_DAC ground should be routed as a star connection to the VAG capacitor.

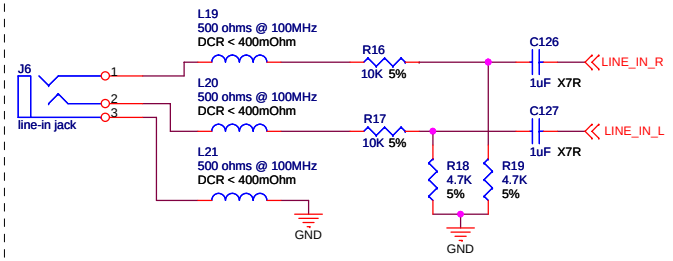


i.MX23 AUDIO-IN OPTIONS

LINE-IN JACK

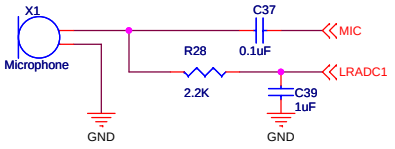
NOTE: The LRADC2 and LRADC3 pins can be configured as an additional LINE IN.

NOTE: For lowest low-frequency distortion, use of X7R 1uF capacitors instead of X5R.



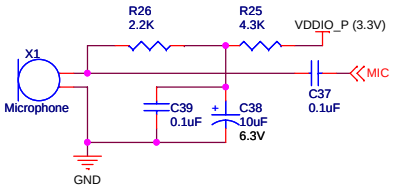
MICROPHONE OPTION 1: LRADC1 bias

Using the LRADC MIC_Bias improves power consumption, since the MIC_Bias can be disabled when not being used.



MICROPHONE OPTION 2: VDDIO bias

For lowest background noise, the VDDIO_P connection to R25 should be routed as a star connection to the 33uF VDDIO_P capacitor. In particular, the VDDIO_P supply for mic bias should be isolated from the VDDIO_P supply for the SD/MMC socket, as SD/MMC card accesses can create supply noise that can show up on the microphone input.

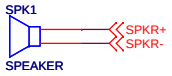


i.MX23 SPEAKER OPTIONS

OPTION 1: Integrated Speaker Amplifier

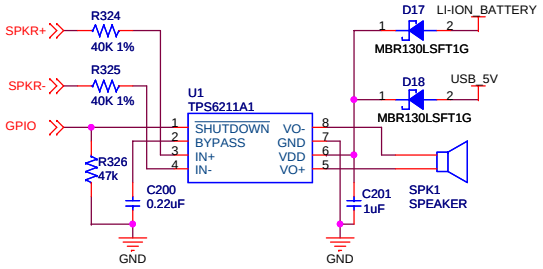
For maximum output power, all speaker power and output pins (VDDS, VSSA5, SPKR+, and SPKR-) should be routed with very wide trace widths to minimize resistive loss.

Recommended speaker impedance is 4 ohms or greater.



IMPORTANT: Because speaker usage causes a large amount of on-chip power dissipation, it is important to understand and follow the guidelines in the "Thermal Conditions" section of the "Characteristics and Specifications" chapter of i.MX23 Reference Manual. If thermal conditions cannot be met, an external speaker amplifier should be used.

OPTION 2: External Speaker Amplifier



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Page Title: **AUDIO & VIDEO OPTIONS**

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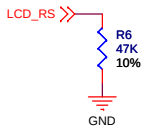
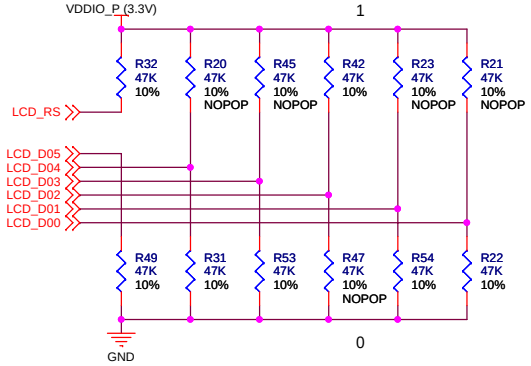
i.MX233 Bootmode Resistor Selection

Option 1: OTP



This mode requires that the appropriate boot mode be written into the OTP boot mode register.

Option 2: Resistor



LCD_D05 = ETM Enable Bit:
Low = ETM disabled
High = ETM enabled

	LCD DATA			
BOOT MODE	**03**	**02**	**01**	**00**
USB	0	0	0	0
I2C Master	0	0	0	1
SPI Flash 1 Master	0	0	1	0
SPI Flash 2 Master	0	0	1	1
NAND	0	1	0	0
DEBUG	0	1	1	0
SD/MMC 1	1	0	0	1
SD/MMC 2	1	0	1	0

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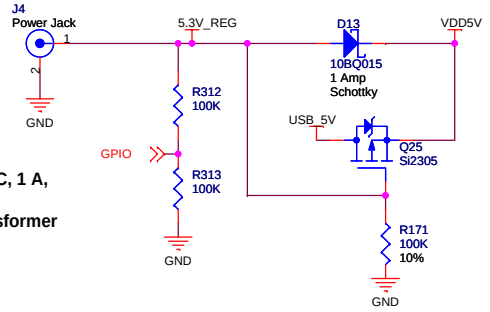
MISC. CIRCUITS

OPTIONAL: Wall Power + USB Power Switch

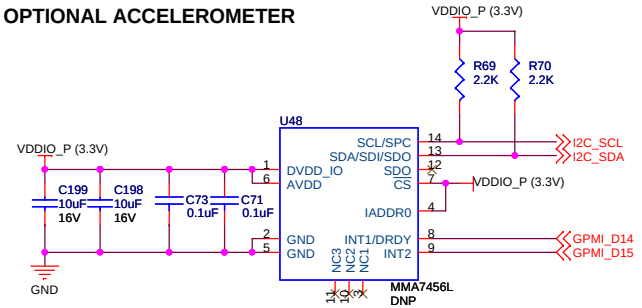
This circuit allows the i.MX23 to power from an external wall power supply. In the case where wall power and USB power are both connected, power will come from the wall power supply. Note that a GPIO and some firmware support may be required to help the i.MX23 differentiate between USB5V and wall power.

To implement this circuit, remove the direct USB_5V connection on the i.MX23 VDD5V pin, and connect the USB_5V line through a FET as shown.

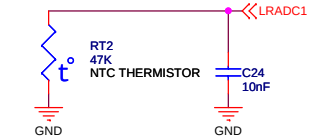
Note that the 5V wall power supply may need to be slightly higher than 5.0V to ensure that it is always higher than the USB_5V supply and thus always supplying power. Use of 5.2V or 5.3V for the wall power supply is ideal.



OPTIONAL ACCELEROMETER

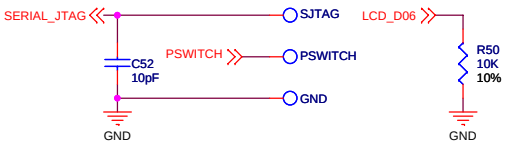


OPTIONAL TEMPERATURE SENSE

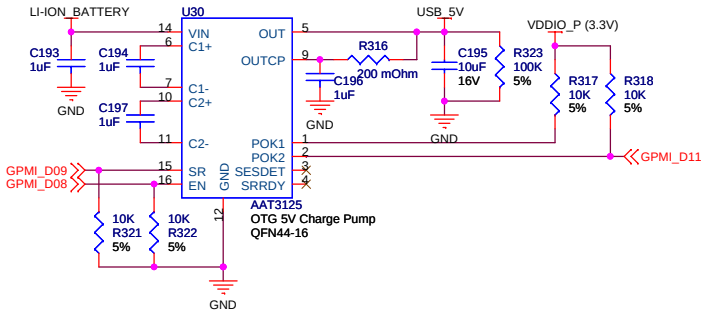


OPTIONAL SERIAL JTAG PORT CONNECTIONS

In order to allow debugging on a i.MX23-based device, it is recommended to add 3 testpoints as shown below. In addition, there are other changes that may be required to support debugging:
1) It may also be necessary to add a 10pF capacitor to GND on the SERIAL_JTAG line to reliably debug.
2) The C42 0.1uF capacitor on PSWITCH may need to be moved to the other side of the R3, 1K resistor.



OPTIONAL 5V CHARGE PUMP FOR USB HOST APPLICATIONS



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Page Title: **OPTIONAL CIRCUITS**

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