MIMXRT1170HDUG

Hardware Development Guide for the MIMXRT1160/1170 Processor

Rev. 2 — 09/2021

User Guide

Contents

1 Introduction

This document's purpose is to help hardware engineers design and test their MIMXRT1170 processor-based designs. It provides information about board layout recommendations and design checklists to ensure first-pass success and avoid board bring-up problems. This guide is released along with the relevant device-specific hardware documentation such as data sheets, reference manuals, and application notes available on nxp.com.

NOTE

RT1160 shares the same design with RT1170, so engineers can also use this document for RT1160.

2 Background

The i.MX RT1170 is a new processor family featuring NXP's advanced implementation of the high performance Arm® Cortex®-M7 Core and power efficient Arm Cortex-M4 core. It provides high CPU performance and real-time response.

The i.MX RT1170 has 2 MB of on-chip RAM in total, including a 512 KB RAM which can be flexibly configured as Tightly-Coupled Memory (TCM) or general purpose On-Chip RAM (OCRAM). The i.MX RT1170 integrates advanced power management module with DC-DC and LDOs that reduce complexity of external power supply and simplify power sequencing.

It provides various memory interfaces, including SDRAM, Raw NAND FLASH, NOR FLASH, SD/eMMC, Quad SPI, Hyper RAM/Flash. It also provides a wide range of other interfaces for connecting external peripherals, such as WLAN, BluetoothR, GPS, displays, and camera sensors. Like other i.MX processors, i.MX RT1170 also has rich audio and video features, including MIPI CSI/DSI, LCD display, graphics accelerator, camera interface, S/PDIF, and I^2S audio interface.

The i.MX RT1170 applications processor can be used in areas such as industrial HMI, IoT, high-end audio appliance, low-end instrument cluster, Point-of-Sale(PoS), motor control, and home appliances.

3 Power supply

For power supply voltage specifications, refer to the Operating Ranges table in the device data sheets. See Table 1 and Table 2 for power supply decoupling recommendations.

NOTE

The Figure 1 in this section is applicable to RT1170 silicon and these tables do not include the on-chip LDO output specification, which can be found in the device data sheet.

Table 1. Processor supply capacitors when on-chip DCDC regulators are used

Power rail	0.1 µF[1]	0.22 µF[1]	1 µF[1]	2.2 µF[1]	4.7 µF[1]	22 µF[1]	Notes
DCDC_IN	1				1	1	Place 0402 under balls M5, N5, place 0603 as close as possible to the processor.
DCDC_ANA				1			Place under ball M7
DCDC_ANA_SENSE	1						Place under ball M6
DCDC_DIG				1		1	Place 0402 under ball K8, place 0603 as close as possible to the processor.
DCDC_DIG_SENSE	1						Place under ball L7
VDDA_1P8_IN	1						Place under ball M11
VDD_SOC_IN_X	1		2		2	1	Place 0402 under balls H8, H10, J8, J10, K10, place 0603 as close as possible to the processor.
VDD_LPSR_IN					1		Place under ball R12
VDD_LPSR_ANA					1		Place under ball P12
VDD_LPSR_DIG				1			Place under ball P11
VDD_SNVS_IN			1				Place under ball U12
VDD_SNVS_ANA				1			Place under ball U14
VDD_SNVS_DIG		1					Place under ball T14
VDD_USB_1P8			1				Place under ball H12, isolate from 1V8 source with series ferrite bead (120-ohm@100MHz)
VDD_USB_3P3			1				Place under ball G12, isolate from 3V3 source with series ferrite bead (120-ohm@100MHz)
VDDA_ADC_1P8			1				Place under ball K15
VDDA_ADC_3P3			1				Place under ball J13
VDDA_1P0				1			Place under ball N11
VDD_MIPI_1P8			1				Place under ball F9, isolate from 1V8 source with series ferrite bead (120-ohm@100MHz)
VDD_MIPI_1P0			1				Place under ball F10, power source is on-chip LDO regulator VDDA_1P0
NVCC_SD1				1			Place under ball D14
NVCC_SD2				1			Place under ball G13
NVCC_EMC1_X				1	1		Place 2.2 µF under balls F6, F7

Table continues on the next page...

Table 1. Processor supply capacitors when on-chip DCDC regulators are used (continued)

Power rail	0.1 µF[1]	0.22 µF[1]	1 µF[1]	2.2 µF[1]	4.7 µF[1]	22 µF[1]	Notes
NVCC_EMC2_X				1	1		Place 2.2 µF under balls H6, J6
NVCC_GPIO				1	1		Place 2.2 µF under ball M12
NVCC_DISP1				1			Place under ball D12
NVCC_DISP2				1			Place under ball E7
NVCC_LPSR				1			Place under ball P7
NVCC_SNVS	1						Place under ball U11
ADC_VREFH				1			Place under ball G16
USB1_VBUS			1				Place under ball D17
USB2_VBUS			1				Place under ball D16

1. 0.1, 0.22, 1, 2.2, 4.7 µF are size 0402, type X5R. 22 uF is size 0603, type X5R.

Table 2. Processor supply capacitors when external PMIC or regulators utilized (on-chip DCDC regulators not used)

Power rail	0.1 µF[1]	0.22 µF[1]	1 µF[1]	2.2 µF[1]	4.7 µF[1]	22 µF[1]	Notes
VDD_SOC_IN_x			2		3	1	Place 0402 under balls H8, J8, J9, J10, K10
VDD_LPSR_IN					1		Place under ball R12
VDD_LPSR_ANA					1		Place under ball P12
VDD_LPSR_DIG				1			Place under ball P11
VDDA_ADC_3P3	1		1				Place 1 µF under ball J13, place 0.1 µF near J13, isolate from 3V3 source with series ferrite bead (120-ohm@100MHz)
ADC_VREFH				1			Place under ball G16
VDDA_ADC_1P8			1		1		Place 1 µF under ball K15, place 4.7 µF near K15, isolate from 1V8 source with series ferrite bead (120-ohm@100MHz)
VDDA_1P8_IN	1						Place under ball M11
VDDA_1P0				1			Place under ball N11
VDD_SNVS_IN			1				Place under ball U12
VDD_SNVS_ANA				1			Place under ball U14
VDD_SNVS_DIG		1					Place under ball T14
NVCC_SNVS	1						Place under ball U11
NVCC_LPSR				1			Place under ball P7
NVCC_GPIO				1	1		Place 2.2 µF under ball M12

Table continues on the next page...

Table 2. Processor supply capacitors when external PMIC or regulators utilized (on-chip DCDC regulators not used) (continued)

Power rail	0.1 µF[1]	0.22 µF[1]	1 µF[1]	2.2 µF[1]	4.7 µF[1]	22 µF[1]	Notes
NVCC_SD1				1			Place under ball D14
NVCC_SD2				1			Place under ball G13
NVCC_DISP1				1			Place under ball D12
NVCC_DISP2				1			Place under ball E7
NVCC_EMC1_X				1	1		Place under balls F7, G6
NVCC_EMC2_X				1	1		Place under balls H6, J6
VDD_MIPI_1P8			1				Place under ball F9, isolate from 1V8 source with series ferrite bead (120-ohm@100MHz)
VDD_MIPI_1P0			1				Place under ball F10, power source is on-chip LDO regulator VDDA_1P0
VDD_USB_1P8			1				Place under ball H12, isolate from 1V8 source with series ferrite bead (120-ohm@100MHz)
VDD_USB_3P3			1				Place under ball G12, isolate from 3V3 source with series ferrite bead (120-ohm@100MHz)
USB1_VBUS			1				Place under ball D17
USB2_VBUS			1				Place under ball D16

1. 0.1 µF, 0.22 µF, 1 µF, 2.2 µF, and 4.7 µF are size 0402 and 22 µF is size 0805. Type X6S is used for automotive cluster and extended temperature range.

Table 3. Power supply and SNVS domain signals

Item	Recommendation	Description
1. Power sequence	Comply with the power-up/power-down sequence guidelines (as described in the data sheet) to guarantee a reliable operation of the device.	Any deviation from these sequences may result in these situations: • Excessive current during the power-up phase • Prevention of the device from booting • Irreversible damage to the processor (worst-case scenario)
2. SNVS domain signals	Do not overload the coin cell backup power rail VDD_SNVS_IN. Note that these I/Os are associated with VDD_SNVS_IN (most inputs have on-chip pull resistors and do not require external resistors):	Concerning i.MX RT1170: • The chip internal LDO VDD_SNVS_ANA output power capacity is 1 mA and should be tied together with NVCC_SNVS.

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Table 3. Power supply and SNVS domain signals (continued)

Item	Recommendation	Description
	• PMIC_STBY_REQ—configurable output • PMIC_ON_REQ—push-pull output • TEST_MODE—on-chip pull-down • POR—on-chip pull-up • WAKEUP—the GPIO that wakes the SoC up in the SNVS mode • GPIO_SNVS_XX—on-chip pull-down	• Be careful to use SNVS signals to drive external load as the SNVS GPIO drive is quite low, refer to the i.MX RT1170 data sheet for details. • By default, the functionality of GPIO_SNVS_XX pin is determined by the part number. Tamper function is available only on tamper-enabled parts, and GPIO is the only available function on parts which do not support tamper. The MUX_MODE must be configured to select the function in both cases. • The GPIO_SNVS_XX pins will automatically switch to tamper function in the SNVS mode even on the part where GPIO function is supported. For more details, refer to ERR051122. • Access delay occurs on the GPIO_SNVS_xx signals due to the module's 32 kHz clock source.
3. Power ripple	Maximum ripple voltage limitation.	The common limitation for the ripple noise shall be less than 5 % Vp-p of the supply voltage average value. The related power rails affected are VDD_XXX, VDD_XXX_IN, VDDA_1P0, VDD_XXX_ANA, VDD_XXX_DIG.
4. Supply currents	Maximum supply currents comply with maximum supply currents in data sheet	Concerning i.MX RT1170: • The DCDC_DIG_X output power capacity is 850 mA and DCDC_ANA_X output power capacity is 150 mA. • Do not use DCDC_ANA_X to drive load higher than 150mA. • For frequencies higher than 600 MHz and up to 800 MHz, refer to the CM7 power source guideline table in the i.MX RT1170 data sheet for automotive products.

Power Sequence Requirements:

- For power supply sequencing requirements, refer to Section 8 of the i.MX RT1170 data sheet.

The power control logic of the IMXRT1170 EVK board is shown in the following figure:

- It will power up SNVS first, then PMIC_REQ_ON will be asserted to enable external DC/DC to power up other power domains.
- ON/OFF button is used to switch PMIC_REQ_ON to control power modes.
- RESET button and WDOG output are used to reset the system power.

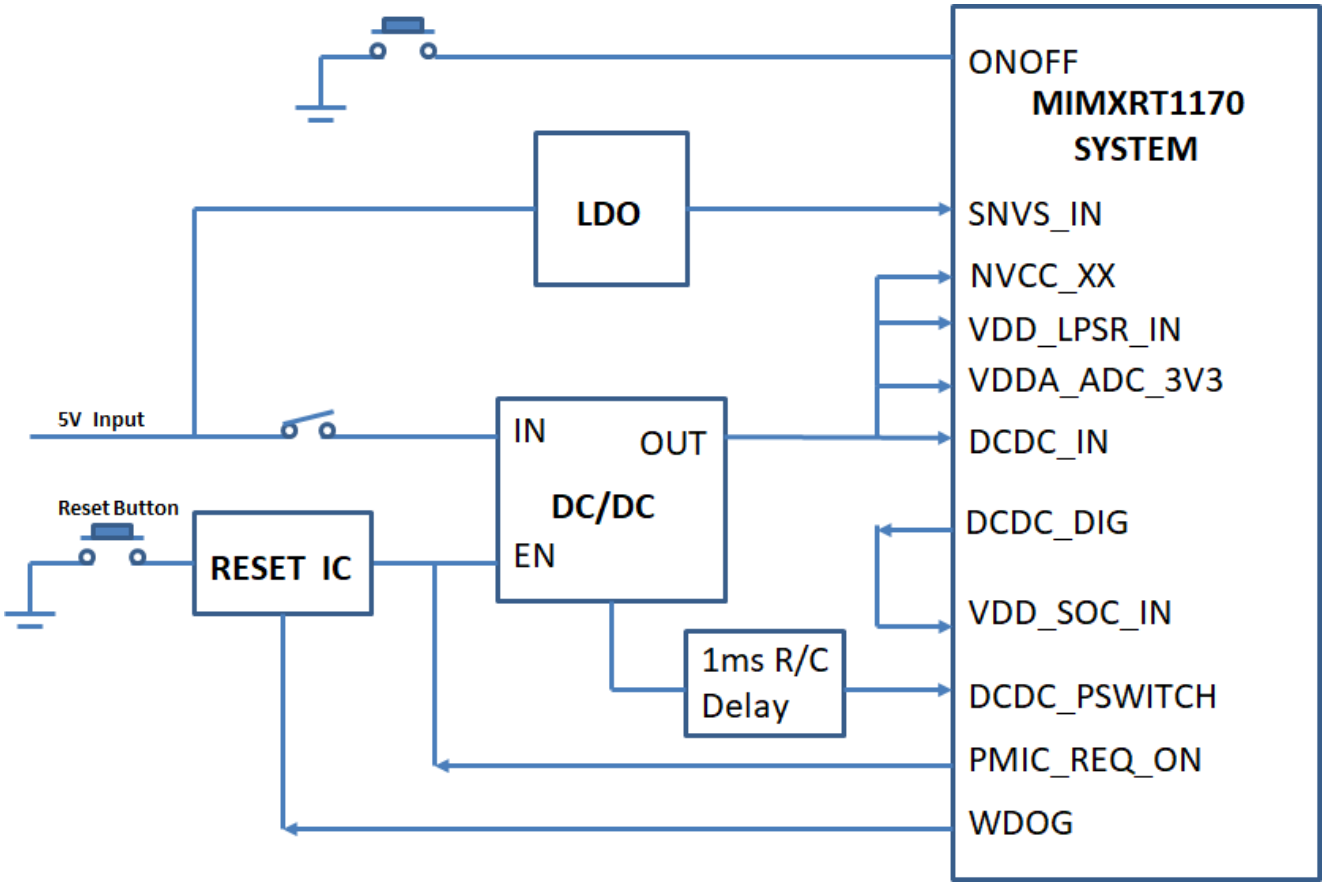

Figure 1. Power control diagram

3.1 On-chip DC/DC module

The internal DC/DC of RT1170 has two outputs, one output (VDD_DIG) typical 0.7 V~1.15 V, another output (VDD_ANA) typical 1.8 V and its switching frequency is about 1.5 MHz.

The DC/DC requires external inductor and capacitors, the illustration is as below Figure 3, please pay attention to the below items:

- The recommended value for the external inductor is about 4.7 μH with the saturation current > 1.5 A and ESR < 0.1 Ω.
- The external bulk capacitor total is about 66 μF, this includes all the capacitors used on DCDC_DIG_X and VDD_SOC_IN.
- DCDC_PSWITCH should delay 1 ms with respect to DCDC_IN to guarantee that DCDC_IN is stable before the DC/DC starts up.
- If you want to bypass the internal DC/DC, DCDC_PSWITCH and DCDC_MODE must be tied to the ground, others signals such as DCDC_IN, DCDC_LP, DCDC_LN, DCDC_ANA, DCDC_ANA_SENSE, DCDC_DIG, and DCDC_DIG_SENSE can be floating.
- Try to keep the DC/DC current loop as small as possible to avoid EMI issues.

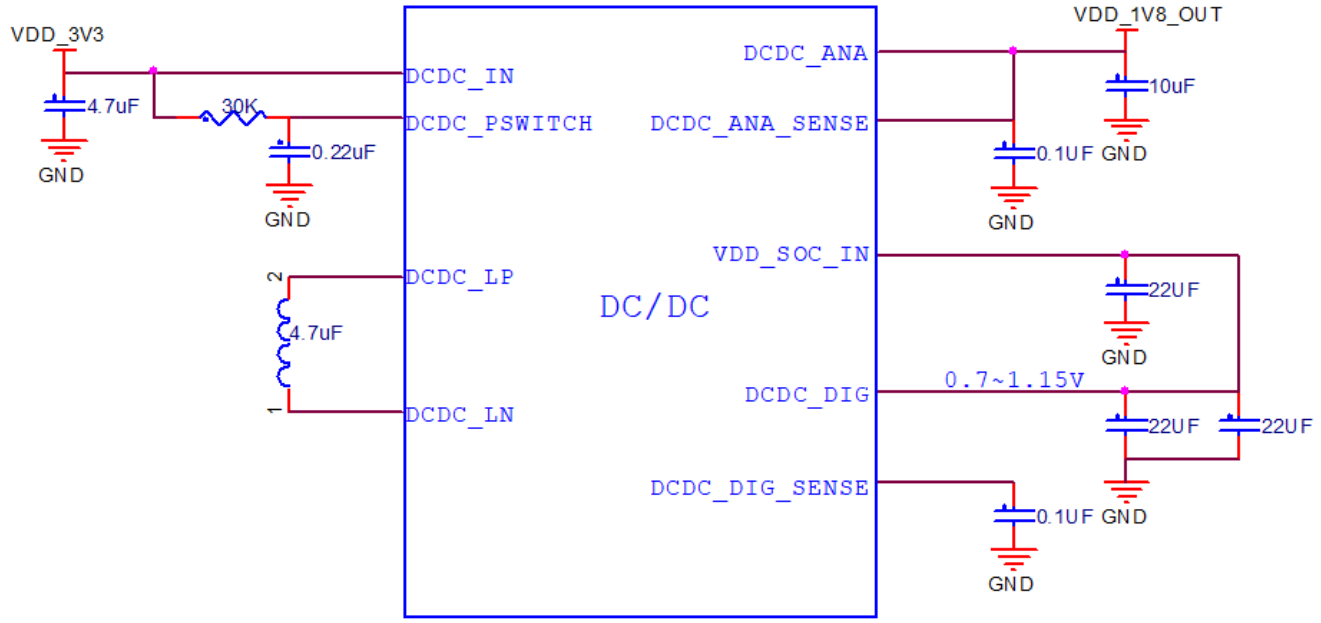

Figure 2. DC/DC function diagram

NOTE

The processor's on-chip DC-DC regulator is suitable for consumer and industrial applications up to 105 degrees C. For automotive applications, contact your NXP representative.

4 Clocks

See Table 4 for the clock configuration. The 32.768-kHz and 24-MHz oscillators are used for the EVK design. For RT1170, it is necessary to use 32.768-kHz and 24-MHz crystals for the hardware design.

Table 4. Clocks' configurations

Signal name	Recommended connections	Description
1.RTC_XTALI/RTC_XTALO	For the precision 32.768-kHz oscillator, connect a crystal between RTC_XTALI and RTC_XTALO. Choose a crystal with a maximum ESR (Equivalent Series Resistance) of 100 k and follow the manufacturer's recommendation for the loading capacitance. Do not use an external biasing resistor because the bias circuit is on the chip.	To hit the exact oscillation frequency, the board capacitors must be reduced to account for the board and chip parasitics. The integrated oscillation amplifier is self-biasing, but relatively weak. Care must be taken to limit the parasitic leakage from RTC_XTALI and RTC_XTALO to either the power or the ground (>100 M). This de-biases the amplifier and reduces the start-up margin.
	For the external kHz source (if feeding an external clock into the device), RTC_XTALI can be driven DC-coupled with RTC_XTALO floating or driven by a complimentary signal.	If you want to feed an external low-frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The logic level

Table continues on the next page...

Table 4. Clocks' configurations (continued)

Signal name	Recommended connections	Description
		of this forcing clock must not exceed the VDD_SNVS_DIG level and the frequency shall be <100 kHz under the typical conditions.
	An on-chip loose-tolerance ring oscillator of approximately 40 kHz is available. If RTC_XTALI is tied to GND and RTC_XTALO is floating, the on-chip oscillator is engaged automatically.	When a high-accuracy real-time clock is not required, the system may use the on-chip 40-kHz oscillator. The tolerance is ±50 %. The ring oscillator starts faster than the external crystal and is used until the external crystal reaches a stable oscillation. The ring oscillator also starts automatically if no clock is detected at RTC_XTALI at any time.
2. XTALI/XTALO	For the precision 24-MHz oscillator, connect a fundamental-mode crystal between XTALI and XTALO. An typical 80 ESR crystal rated for a maximum drive level of 250 μW is acceptable. Alternately, a typical 50 ESR crystal rated for a maximum drive level of 200 μW may be used. For the RT1170 24-MHz OSCILLATOR, the smaller the ESR, the better the startup and power consumption. To use the high-power mode, populate the 1-Mohm resistor between XTALI and XTALO.	The SDK software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24-MHz oscillator is available in the system. In this case, please refer to section of Bypass Configuration (24 MHz) from the reference manual. For the bypass mode pin connection, the external bypass clock can be put in from EXTAL pin, at the same time, XTALO can be used as other functions. The logic level of this forcing clock must not exceed the VDD_LPSR_ANA level. If this clock is used as a reference for the USB and Ethernet, then there are strict frequency tolerance and jitter requirements. The +-50 ppm accuracy is required for the Ethernet while the +-100 ppm accuracy is required for the USB. See the OSC24M chapter and the relevant interface specification chapters for details.
3.CLK1_P/CLK1_N	Internal use only	These pins are used for NXP internal testing. The CLK1_P and CLK1_N pair should be left floating.

5 Debugging and programming

This section provides the JTAG interface summary and recommendations for using the JTAG, SWD debug, and Serial downloader I/O.

NOTE

By default, the RT1170 silicon can use both SWD and JTAG modes using the Arm stitching sequence. For the RT1170EVK board, it defaults to use the SWD debug without any board modification. If you want to use the JTAG debug, solder out R187, R208, R195, and R78, because some JTAG signals are multiplexed with other functions.

The MIMXRT1170-EVK also features a FreeLink circuit, which makes it easier to debug without an external debugger.

Table 5. JTAG interface summary

JTAG signals	I/O type	On-chip termination[1]	External termination
JTAG_TCK	Input	Pull-down	Not required;
JTAG_TMS	Input	Pull-up	Not required; can use 10 kΩ pull-up
JTAG_TDI	Input	Pull-up	Not required; can use 10 kΩ pull-up
JTAG_TDO	3-state output	None	Do not use pullup or pull-down
JTAG_TRSTB	Input	Pull-up	Not required; can use 10 kΩ pull-up
JTAG_MOD	Input	Pull-down	Use 4.7 kΩ pull-down or tie to GND

1. For on-chip termination values, refer to Section 8 of the data sheet.

Table 6. JTAG recommendation

Signals	Recommendation	Description
1. JTAG_TDO	Do not add external pull-up or pull-down resistors on JTAG_TDO.	See Table 5 for a summary of the JTAG interface. This I/O has an on-chip keeper circuit which avoids a floating condition.
2. JTAG signals other than JTAG_TDO and JTAG_MOD	Ensure that the on-chip pull-up/pull-down configuration is followed if external resistors are used with the JTAG signals (except for JTAG_TDO). For example, do not use an external pull-down on an input that has an on-chip pull-up.	External resistors can be used with all JTAG signals except for JTAG_TDO, but they are not required. See Table 5 for a summary of the JTAG interface.
3. JTAG_MOD	JTAG_MOD is called SJC_MOD in some documents. Both names refer to the same signal. JTAG_MOD shall be externally connected to GND for normal operation in a system. The termination to GND through an external pull-down resistor is allowed. Use a 4.7-kΩ resistor.	When JTAG_MOD is low, the JTAG interface is configured for a common software debug, adding all the system TAPs to the chain. When JTAG_MOD is low, the JTAG interface is also configured to a mode compliant with the IEEE 1149.1 standard.

Table 7. SWD recommendation

Signals	Recommendation	Description
1. SWD_DIO	Same practice as JTAG_TMS	On the RT1170EVK board, the SWD debug port is used by default. There is also a low-cost on-board Freelink debugger using the SWD port.
2. SWD_CLK	Same practice as JTAG_CLK	

The ROM's Serial Downloader mode provides a means to download a program image to the chip over USB or UART serial connection. In this mode, typically a host PC can communicate to the ROM bootloader using serial download protocol. NXP's ROM flashloader also uses these same serial connections. It is strongly recommended for all boards to make at least one of the serial downloader ports (USB1 or UART1) available to be able to make use of NXP's image and fuse programming enablement.

Table 8. Serial downloader I/Os table

Signals	Recommendation	Description
1.UART1 2. USB1	The serial downloader provides a means to download a program image to the chip over the USB and UART serial connections. In this mode, the ROM programs the WDOG1 for a time-out specified by the fuse WDOG time-out select (see the Fusemap chapter for details) if the WDOG_ENABLE eFuse is 1 and continuously polls for the USB and UART connection. If no activity is found on the USB OTG1 and UART1 and the watchdog timer expires, the Arm core is reset.	The ROM polls for the UART1 and USB1 activity circularly until the ROM gets 0x5A, 0xA6 from the UART RXD or first HID report from the USB bus. When an active connection port is found, the ROM uses it for the PC downloading.

6 Boot, reset, and miscellaneous

See Table 9 for the boot, reset, and miscellaneous configurations, such as ON/OFF, TEST_MODE, NC pins, and other.

Table 9. Boot configuration

Item	Recommendation	Description
1. BOOT_CFG[11:0]	The BOOT_CFG signals are required for a proper functionality and operation and shall not be left floating during development if BOOT_CFG fuses and BT_FUSE_SEL are not configured.	See the “System Boot” chapter in your chip reference manual for the correct boot configuration. Note that an incorrect setting may result in an improper boot sequence.
2. BOOT_MODE[1:0]	For logic 0: • Tie to GND through 100K external resistor For logic 1: • Tie to the NVCC_LPSR power domain through a 4.7K external resistor	BOOT_MODE1 and BOOT_MODE0 each have on-chip pull-down devices with a nominal value of 35 kΩ. When the on-chip fuses determine the boot configuration, both boot mode inputs can be disconnected.
3. BOOT_CFG and BOOT_MODE signals multiplexed with RGMII signals	As the BOOT_CFG pins are multiplexed with RGMII signals, recommend to add 22K isolation resistors to avoid malfunction. For BOOT_MODE pins, suggest to add 4.7K isolation resistors.	Please refer to the EVK design for reference and try to avoid signal stubs in layout.

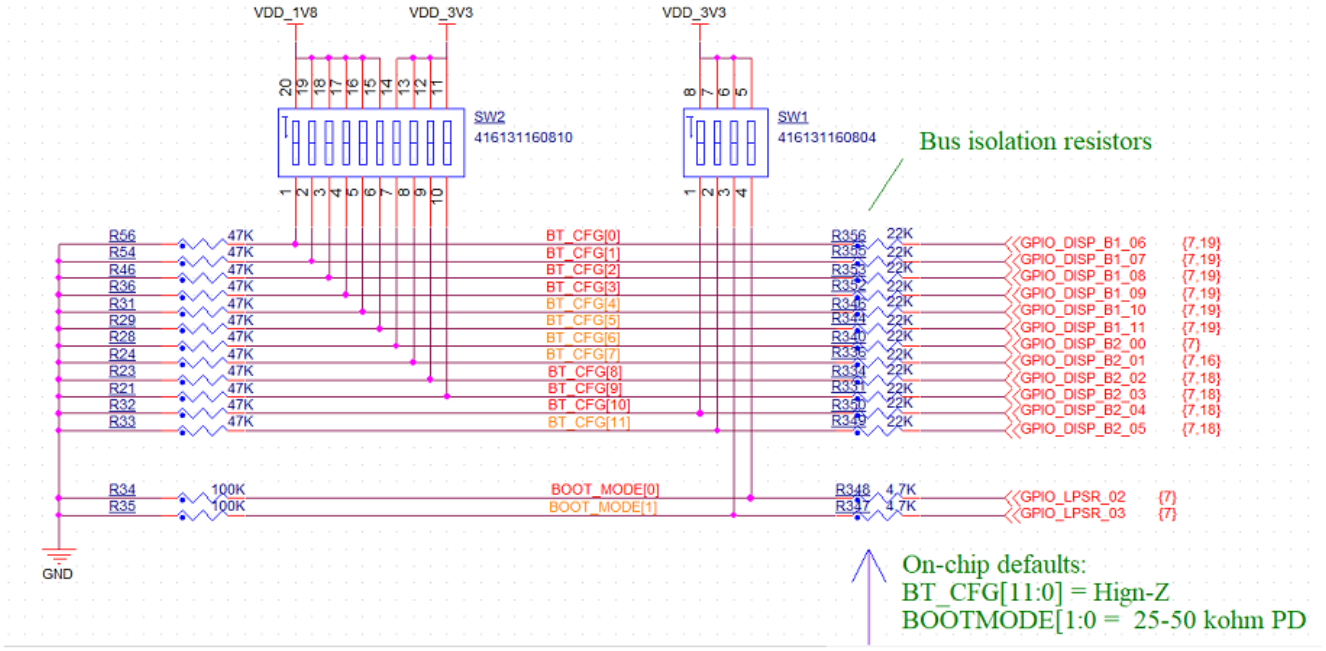

Figure 3. Boot mode setting

Table 10. Reset and miscellaneous recommendations

Item	Recommendation	Description
1. POR_B	The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the i.MX RT1170 Reference Manual (IMXRT1170RM) for further details and to ensure that all necessary requirements are being met.	See the “System Boot” chapter in your chip reference manual for the correct boot configuration. Note that an incorrect setting may result from an improper boot sequence. POR_B signal has internal 100K pull up to SNVS domain, should pull up to VDD_SNVS_ANA if need to add external pull up resistor, otherwise it will cause additional leakage during SNVS mode. It's recommended to add the external reset IC to the circuit to guarantee POR_B is properly processed during power up/down, please refer to the EVK design for details. Note: 1. As the Low DCDC_IN detection threshold is 2.6 V, the reset IC's reset threshold must be higher than 2.6 V, then the whole chip is reset before the internal DCDC module reset to guarantee the chip safety during power down. 2. For power on reset, on any conditions ones need to make sure the voltage on

Table continues on the next page...

Table 10. Reset and miscellaneous recommendations (continued)

Item	Recommendation	Description
		DCDC_PSWITCH PIN is below 0.5 V before power up.
2. ON/OFF	For portable applications, the ON/OFF input may be connected to the ON/OFF SPST push-button. The on-chip debouncing is provided, and this input has an on-chip pullup. If not used, ON/OFF can be a no-connect. A 4.7-kΩ to 10-kΩ series resistor can be used when the current drain is critical.	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF.
3. TEST_MODE	The TEST_MODE input is internally connected to an on-chip pull-down device. You may either float this signal or tie it to GND.	This input is reserved for NXP manufacturing use.

Table 11. ROM Bootloader Peripheral PinMux

Peripheral	Instance	Port (IO function)	PAD	Mode	Note
LPUART	1	LPUART1_TX	GPIO_AD_24	ALT0	Can be used for serial downloader mode Refer to Serial Downloader in Reference Manual for more information.
		LPUART1_RX	GPIO_AD_25	ALT0	
LPSPI	1	LPSPI1_SCK	GPIO_AD_28	ALT0	Serial NOR/EEPROM connected to one of the LPSPI ports can be used as a recovery device. Refer to Recovery devices in Reference Manual for more information. Note: recovery device boot is disabled by default. Fuses must be blown to enable and configure this option.
		LPSPI1_PCS0	GPIO_AD_29	ALT0	
		LPSPI1_SDO	GPIO_AD_30	ALT0	
		LPSPI1_SDI	GPIO_AD_31	ALT0	
	2	LPSPI2_SCK	GPIO_SD_B2_07	ALT6	
		LPSPI2_PCS0	GPIO_SD_B2_08	ALT6	
		LPSPI2_SDO	GPIO_SD_B2_09	ALT6	
		LPSPI2_SDI	GPIO_SD_B2_10	ALT6	
	3	LPSPI3_SCK	GPIO_DISP_B1_04	ALT9	
		LPSPI3_PCS0	GPIO_DISP_B1_07	ALT9	
		LPSPI3_SDO	GPIO_DISP_B1_06	ALT9	
		LPSPI3_SDI	GPIO_DISP_B1_05	ALT9	
	4	LPSPI4_SCK	GPIO_DISP_B2_12	ALT9	
		LPSPI4_PCS0	GPIO_DISP_B2_15	ALT9	
		LPSPI4_SDO	GPIO_DISP_B2_14	ALT9	

Table continues on the next page...

Table 11. ROM Bootloader Peripheral PinMux (continued)

Peripheral	Instance	Port (IO function)	PAD	Mode	Note
		LPSPI4_SDI	GPIO_DISP_B2_13	ALT9	
SEMC NAND	N/A	SEMC_DATA00	GPIO_EMC_B1_00	ALT0	Parallel NAND flash connected to the SEMC is a primary boot option. Refer to Parallel NAND flash Boot over SEMC in Reference Manual for more information.
		SEMC_DATA01	GPIO_EMC_B1_01	ALT0	
		SEMC_DATA02	GPIO_EMC_B1_02	ALT0	
		SEMC_DATA03	GPIO_EMC_B1_03	ALT0	
		SEMC_DATA04	GPIO_EMC_B1_04	ALT0	
		SEMC_DATA05	GPIO_EMC_B1_05	ALT0	
		SEMC_DATA06	GPIO_EMC_B1_06	ALT0	
		SEMC_DATA07	GPIO_EMC_B1_07	ALT0	
		SEMC_DATA08	GPIO_EMC_B1_30	ALT0	
		SEMC_DATA09	GPIO_EMC_B1_31	ALT0	
		SEMC_DATA10	GPIO_EMC_B1_32	ALT0	
		SEMC_DATA11	GPIO_EMC_B1_33	ALT0	
		SEMC_DATA12	GPIO_EMC_B1_34	ALT0	
		SEMC_DATA13	GPIO_EMC_B1_35	ALT0	
		SEMC_DATA14	GPIO_EMC_B1_36	ALT0	
		SEMC_DATA15	GPIO_EMC_B1_37	ALT0	
		SEMC_ADDR09	GPIO_EMC_B1_18	ALT0	
		SEMC_ADDR11	GPIO_EMC_B1_19	ALT0	
		SEMC_ADDR12	GPIO_EMC_B1_20	ALT0	
		SEMC_BA1	GPIO_EMC_B1_22	ALT0	
		SEMC_CSX0	GPIO_EMC_B1_41	ALT0	
uSDHC	1	USDHC1_CD_B	GPIO_AD_32	ALT4	eMMC/MMC or SD/eSD connected to one of the USDHC ports is a primary boot option. Refere to Expansion device in Reference Manual for more information.
		USDHC1_WP	GPIO_AD_33	ALT4	
		USDHC1_VSELECT	GPIO_AD_34	ALT4	
		USDHC1_RESET_B	GPIO_AD_35	ALT4	
		USDHC1_CMD	GPIO_SD_B1_00	ALT0	
		USDHC1_CLK	GPIO_SD_B1_01	ALT0	
		USDHC1_DATA0	GPIO_SD_B1_02	ALT0	
		USDHC1_DATA1	GPIO_SD_B1_03	ALT0	
		USDHC1_DATA2	GPIO_SD_B1_04	ALT0	
		USDHC1_DATA3	GPIO_SD_B1_05	ALT0	

Table continues on the next page...

Table 11. ROM Bootloader Peripheral PinMux (continued)

Peripheral	Instance	Port (IO function)	PAD	Mode	Note
	2	USDHC2_CD_B	GPIO_AD_26	ALT11	
		USDHC2_WP	GPIO_AD_27	ALT11	
		USDHC2_VSELECT	GPIO_AD_28	ALT11	
		USDHC2_DATA3	GPIO_SD_B2_00	ALT0	
		USDHC2_DATA2	GPIO_SD_B2_01	ALT0	
		USDHC2_DATA1	GPIO_SD_B2_02	ALT0	
		USDHC2_DATA0	GPIO_SD_B2_03	ALT0	
		USDHC2_CLK	GPIO_SD_B2_04	ALT0	
		USDHC2_CMD	GPIO_SD_B2_05	ALT0	
		USDHC2_RESET_B	GPIO_SD_B2_06	ALT0	
		USDHC2_DATA4	GPIO_SD_B2_08	ALT0	
		USDHC2_DATA5	GPIO_SD_B2_09	ALT0	
		USDHC2_DATA6	GPIO_SD_B2_10	ALT0	
		USDHC2_DATA7	GPIO_SD_B2_11	ALT0	
FlexSPI1	1	FLEXSPI1_B_DATA3	GPIO_SD_B2_00	ALT1	QSPI memory attached to FlexSPI is a primary boot option. Refer to Serial NOR Flash Boot via FlexSPI in Reference Manual for more information. The ROM will read the 512-byte FlexSPI NOR configuration parameters described in FlexSPI Serial NOR Flash Boot Operation Reference Manual using the non-italicized pins. Note: These pins are a secondary pinout option for FlexSPI serial NOR flash boot
		FLEXSPI1_B_DATA2	GPIO_SD_B2_01	ALT1	
		FLEXSPI1_B_DATA1	GPIO_SD_B2_02	ALT1	
		FLEXSPI1_B_DATA0	GPIO_SD_B2_03	ALT1	
		FLEXSPI1_B_SCLK	GPIO_SD_B2_04	ALT1	
		FLEXSPI1_B_DQS	GPIO_SD_B1_05	ALT8	
		FLEXSPI1_B_SS0_B	GPIO_SD_B1_04	ALT8	
		FLEXSPI1_B_SS1_B	GPIO_SD_B1_03	ALT9	
		FLEXSPI1_A_DQS	GPIO_SD_B2_05	ALT1	
		FLEXSPI1_A_SS0_B	GPIO_SD_B2_06	ALT1	
		FLEXSPI1_A_SS1_B	GPIO_SD_B1_02	ALT9	
		FLEXSPI1_A_SCLK	GPIO_SD_B2_07	ALT1	
		FLEXSPI1_A_DATA0	GPIO_SD_B2_08	ALT1	
		FLEXSPI1_A_DATA1	GPIO_SD_B2_09	ALT1	

Table continues on the next page...

Table 11. ROM Bootloader Peripheral PinMux (continued)

Peripheral	Instance	Port (IO function)	PAD	Mode	Note
		FLEXSPI1_A_DATA2	GPIO_SD_B2_10	ALT1	
		FLEXSPI1_A_DATA3	GPIO_SD_B2_11	ALT1	
		FLEXSPI1_A_DQS	GPIO_EMC_B2_18	ALT6	Second option
FlexSPI2 (QSPI / HyperFLASH)	2	FLEXSPI2_B_DATA7	GPIO_EMC_B1_41	ALT4	Octal serial NOR flash memory attached to FlexSPI is a primary boot option. Refer to Serial NOR Flash Boot via FlexSPI in Reference Manual for more information. The ROM will read the 512-byte FlexSPI NOR configuration parameters described in FlexSPI Serial NOR Flash Boot Operation in Reference Manual using the non-italicized pins For 8-bit wide memories the FLEXSPI_B_DATA[3:0] pins are combined with the FLEXSPI_A_DATA[3:0] lines to get the full 8-bit port. Note: ROM can configure the italicized signals based on the FlexSPI NOR configuration parameters provided.
		FLEXSPI2_B_DATA6	GPIO_EMC_B2_00	ALT4	
		FLEXSPI2_B_DATA5	GPIO_EMC_B2_01	ALT4	
		FLEXSPI2_B_DATA4	GPIO_EMC_B2_02	ALT4	
		FLEXSPI2_B_DATA3	GPIO_EMC_B2_03	ALT4	
		FLEXSPI2_B_DATA2	GPIO_EMC_B2_04	ALT4	
		FLEXSPI2_B_DATA1	GPIO_EMC_B2_05	ALT4	
		FLEXSPI2_B_DATA0	GPIO_EMC_B2_06	ALT4	
		FLEXSPI2_B_DQS	GPIO_EMC_B2_07	ALT4	
		FLEXSPI2_B_SS0_B	GPIO_EMC_B2_08	ALT4	
		FLEXSPI2_B_SCLK	GPIO_EMC_B2_09	ALT4	
		FLEXSPI2_A_SCLK	GPIO_EMC_B2_10	ALT4	
		FLEXSPI2_A_SS0_B	GPIO_EMC_B2_11	ALT4	
		FLEXSPI2_A_DQS	GPIO_EMC_B2_12	ALT4	
		FLEXSPI2_A_DATA0	GPIO_EMC_B2_13	ALT4	
		FLEXSPI2_A_DATA1	GPIO_EMC_B2_14	ALT4	
		FLEXSPI2_A_DATA2	GPIO_EMC_B2_15	ALT4	
		FLEXSPI2_A_DATA3	GPIO_EMC_B2_16	ALT4	
		FLEXSPI2_A_DATA4	GPIO_EMC_B2_17	ALT4	

Table continues on the next page...

Table 11. ROM Bootloader Peripheral PinMux (continued)

Peripheral	Instance	Port (IO function)	PAD	Mode	Note
		FLEXSPI2_A_DATA5	GPIO_EMC_B2_18	ALT4	
		FLEXSPI2_A_DATA6	GPIO_EMC_B2_19	ALT4	
		FLEXSPI2_A_DATA7	GPIO_EMC_B2_20	ALT4	
		GPIO_MUX2_IO08	GPIO_EMC_B1_40	ALT5	Second option
		GPIO_MUX4_IO03	GPIO_SD_B1_00	ALT5	FlexSPI Reset
		SEMC_ADDR09	GPIO_EMC_18	ALT0	
		SEMC_ADDR11	GPIO_EMC_19	ALT0	
		SEMC_ADDR12	GPIO_EMC_20	ALT0	
		SEMC_BA1	GPIO_EMC_22	ALT0	
		SEMC_RDY	GPIO_EMC_40	ALT0	
		SEMC_CSX0	GPIO_EMC_41	ALT0	
		SEMC_CSX1	GPIO_B0_00	ALT6	
		SEMC_CSX2	GPIO_B0_01	ALT6	
		SEMC_CSX3	GPIO_B0_02	ALT6	
		SEMC_ADDR08	GPIO_EMC_17	ALT0	
FlexSPIN OR Flash-QSPI	1	FLEXSPI_B_DATA3	GPIO_SD_B1_00	ALT1	QSPI memory attached to FlexSPI is a primary boot option. Refer to Serial NOR Flash Boot via FlexSPI in Reference Manual for more information.The ROM will read the 512-byte FlexSPI described in FlexSPI Serial NOR Flash Boot Operation in Reference Manual using the non italicized pins. Note: ROM can configure the italicized signals based on the FlexSPI NOR configuration parameters provided.
		FLEXSPI_B_DATA2	GPIO_SD_B1_01	ALT1	
		FLEXSPI_B_DATA1	GPIO_SD_B1_02	ALT1	
		FLEXSPI_B_DA TA0	GPIO_SD_B1_03	ALT1	
		FLEXSPI_B_SCLK	GPIO_SD_B1_01	ALT1	
		FLEXSPI_B_DQS	GPIO_SD_B0_05	ALT4	
		FLEXSPI_B_SS0_B	GPIO_SD_B0_04	ALT4	
		FLEXSPI_B_SS1_B	GPIO_SD_B0_01	ALT6	
		FLEXSPI_A_DQS	GPIO_SD_B1_05	ALT1	
		FLEXSPI_A_SS0_B	GPIO_SD_B1_06	ALT1	
		FLEXSPI_A_SS1_B	GPIO_SD_B0_00	ALT6	
		FLEXSPI_A_SCLK	GPIO_SD_B1_07	ALT1	
		FLEXSPI_A_DATA0	GPIO_SD_B1_08	ALT1	
		FLEXSPI_A_DATA1	GPIO_SD_B1_09	ALT1	
		FLEXSPI_A_DATA2	GPIO_SD_B1_10	ALT1	

Table continues on the next page...

Table 11. ROM Bootloader Peripheral PinMux (continued)

Peripheral	Instance	Port (IO function)	PAD	Mode	Note
		FLEXSPI_A_DATA3	GPIO_SD_B1_11	ALT1	
FlexSPIN OR-QSPI-2nd Option	1	FLEXSPI_A_SS0_B	GPIO_AD_B1_15	ALT0	QSPI memory attached to FlexSPI is a primary boot option. Refer to Serial NOR Flash Boot via FlexSPI in Reference Manual for more information. The ROM will read the 512-byte FlexSPI NOR configuration parameters described in FlexSPI Serial NOR Flash Boot Operation Reference Manual using the non-italicized pins. Note: These pins are a secondary pinout option for FlexSPI serial NOR flash boot.
		FLEXSPI_A_SCLK	GPIO_AD_B1_14	ALT0	
		FLEXSPI_A_DQS	GPIO_AD_B1_09	ALT0	
		FLEXSPI_A_DATA0	GPIO_AD_B1_13	ALT0	
		FLEXSPI_A_DATA1	GPIO_AD_B1_12	ALT0	
		FLEXSPI_A_DATA2	GPIO_AD_B1_11	ALT0	
		FLEXSPI_A_DATA3	GPIO_AD_B1_10	ALT0	
Fle xSPIN OR Flash-Octal	1	FLEXSPI_B_DATA3	GPIO_SD_B1_00	ALT1	Octal serial NOR flash memory attached to FlexSPI is a primary boot option. Refer to Serial NOR Flash Boot via FlexSPI in Reference Manual for more information. The ROM will read the 512-byte FlexSPI NOR configuration parameters described in FlexSPI Serial NOR Flash Boot Operation in Reference Manual using the non-italicized pins For 8-bit wide memories the FLEXSPI_B_DATA[3:0] pins are combined with the FLEXSPI_A_DATA[3:0] lines to get the full 8-bit port. FlexSPI NOR configuration parameters provided.
		FLEXSPI_B_DATA2	GPIO_SD_B 1_01	ALT1	
		FLEXSPI_B_DATA1	GPIO_SD_B1_02	ALT1	
		FLEXSPI_B_DATA0	GPIO_SD_B1_03	ALT1	
		FLEXSPI_B_SCLK	GPIO_SD_B1_01	ALT1	
		FLEXSPI_B_DQS	GPIO_SD_B0_05	ALT4	
		FLEXSPI_B_SS0_B	GPIO_SD_B0_04	ALT4	
		FLEXSPI_B_SS1_B	GPIO_SD_B0_01	ALT6	
		FLEXSPI_A_DQS	GPIO_SD_B1_05	ALT1	
		FLEXSPI_A_SS0_B	GPIO_SD_B1_06	ALT1	
		FLEXSPI_A_SS1_B	GPIO_SD_B0_00	ALT6	
		FLEXSPI_A_SCLK	GPIO_SD_B1_07	ALT1	
		FLEXSPI_A_DATA0	GPIO_SD_B1_08	ALT1	
		FLEXSPI_A_DATA1	GPIO_SD_B1_09	ALT1	
		FLEXSPI_A_DATA2	GPIO_SD_B1_10	ALT1	
		FLEXSPI_A_DATA3	GPIO_SD_B1_11	ALT1	
FlexSPI NAND Flash	1	FLEXSPI_A_DQS	GPIO_SD_B1_05	ALT1	Serial NAND memory attached to FlexSPI is a primary boot option. Refer to Serial NAND Flash Boot over FlexSPI in Reference Manual for more information.
		FLEXSPI_A_SS0_B	GPIO_SD_B1_06	ALT1	
		FLEXSPI_A_SCLK	GPIO_SD_B1_07	ALT1	
		FLEXSPI_A_DATA0	GPIO_SD_B1_08	ALT1	
		FLEXSPI_A_DATA1	GPIO_SD_B1_09	ALT1	
		FLEXSPI_A_DATA2	GPIO_SD_B1_10	ALT1	

Table continues on the next page...

Table 11. ROM Bootloader Peripheral PinMux (continued)

Peripheral	Instance	Port (IO function)	PAD	Mode	Note
		FLEXSPI_A_DATA3	GPIO_SD_B1_11	ALT1	
FlexSPI RESET		GPIO1_IO29	GPIO_AD_B1_13	ALT5	

NOTE

ROM does not support boot from FLEXSPI_B port directly. ROM always seeks a valid Flash Configuration Block from the FLEXSPI_A port and then re-configures the FLEXSPI controller using the valid parameters in the block read-out. This reconfiguration can include, but is not limited to, FLEXSPI_B port support.

7 Layout recommendations

7.1 Stackup

A high-speed design requires a good stackup to have the right impedance for the critical traces.

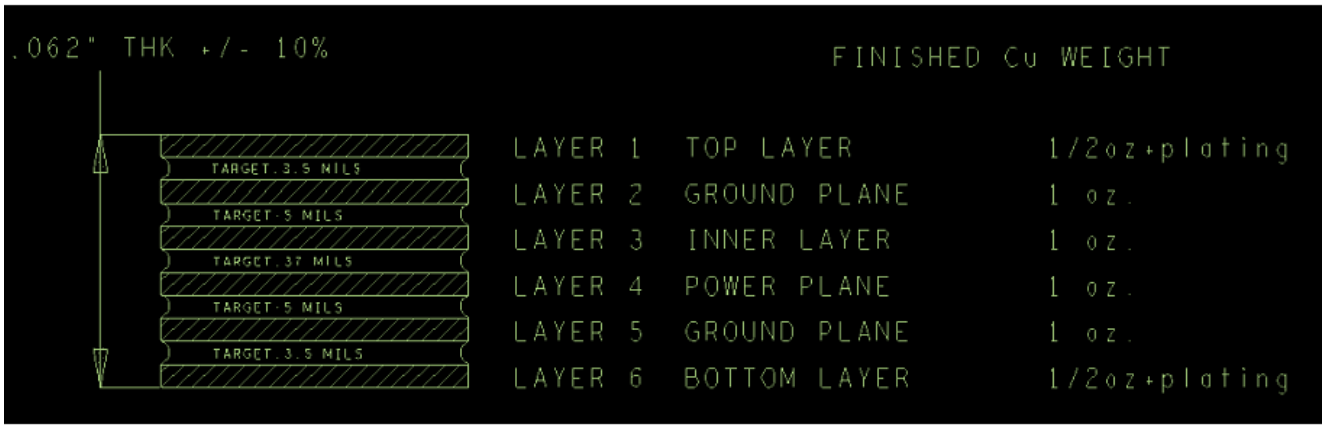

Figure 4. IMXRT1170EVK stackup

The constraints for the trace width depend on many factors, such as the board stackup and the associated dielectric and copper thickness, required impedance, and required current (for power traces). The stackup also determines the constraints for routing and spacing. Consider the following when designing the stackup and selecting the material for your board:

- The board stackup is critical for the high-speed signal quality.
- Preplan the impedance of the critical traces.
- The high-speed signals must have reference planes on adjacent layers to minimize crosstalk.
- The NXP reference design equals Isola FR4.
- The NXP validation boards equal Isola FR4.
- The recommended stackup is six layers, with the layer stack shown in Figure 4.The left- hand image shows the detail provided by NXP inside the fabrication detail as a part of the Gerber files. The right-hand side shows the solution suggested by the PCB fabrication company for the requirements. Figure 5 shows the IMXRT1170EVK PCB stackup implementation:

Layers	Single Ended		Differential			Differential		
	Trace Width (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing 'Airgap' (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing 'Airgap' (Mils)	Impedance (Ohms)
L1	5.00	50	4.2	6.00	100	4.70	5.00	90
L3	5.00	50						
L6	5.00	50				4.70	5.00	90

Figure 5. IMXRT1170EVK stackup implementation

7.2 Placement of bulk and decoupling capacitors

Place the small decoupling capacitors and the larger bulk capacitors on the bottom side of the CPU. The 0402 decoupling capacitors and the 0603 bulk capacitors must be placed as close as possible to the power balls. Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure the high-speed transient current demand of the processor. The correct via size, trace width, and trace space are critical to preserve the adequate routing space. The recommended geometry is as follows:

- For the BGA constraint area:
  - The via type is 18/8 mils, the trace width is 4 mils, and the trace space is 3.79 mils.
- For the default area (except for the BGA):
  - The via type is 18/8 mils, the trace width is 7 mils, and the trace space is 7 mils.
  - The preferred BGA power-decoupling design layout is available at www.nxp.com.
  - Use the NXP design strategy for power and decoupling.

7.3 FlexSPI

FlexSPI is a flexible SPI (Serial Peripheral Interface) host controller which supports two SPI channels and up to 4 external devices. Each channel supports Single/Dual/Quad/ Octal mode data transfer (1/2/4/8 bidirectional data lines). FlexSPI is the most commonly used external memory.

Please refer to section FlexSPI parameters from the datasheet, there are several sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally
  - (FlexSPIn_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the
  - DQS pad (FlexSPIn_MCR0[RXCLKSRC] = 0x1)
- Read strobe provided by memory device and input from DQS pad
  - (FlexSPIn_MCR0[RXCLKSRC] = 0x3)

So for QSPI Flash without a DQS provided by the memory, only the option of FlexSPIn_MCR0[RXCLKSRC] = 0x1 can achieve 133 MHz SDR R/W speed, and FlexSPI_DQS pin should be left floating.

For Octal Flash where a DQS signal is provided by the memory, need to use the option of FlexSPIn_MCR0[RXCLKSRC] = 0x3 which can achieve 166 MHz DDR R/W, in such case FlexSPI_DQS pin should be connected to the flash directly.

7.4 SDRAM

The SDRAM interface (running at up to 200 MHz) is one of the critical interfaces for the chip routing. The controlled impedance for the single-ended traces must be 50 Ω. Ideally, route all signals at the same length as the EVK board. See the IMXRT1170-EVK layout to route all signals at the same length (±50 mils).

The SDRAM routing must be separated into two groups: data and address/control. See the EVK layout to separate all SDRAM signals into two groups:

- SEMC_DQS signal line should be left floating.
- All data lines and DM[x]
- All address lines and control lines

RT1170EVK is a 6-layer board design, both routing groups refer to the GND plane for the impedance control. One group is routed at the top layer (the reference plane is the second layer), while the other group is routed at the bottom layer (the reference plane is the fifth layer).

7.5 USB

Use these recommendations for the USB:

- Route the DP and DM differential pair first.
- Route the DP and DM signals on the top (or bottom) layer of the board.
- The trace width and spacing of the DP and DM signals must meet the differential impedance requirement of 90 Ω.
- Route the traces over the continuous planes (power and ground):
  - They must not pass over any power/GND plane slots or anti-etch.
  - When placing the connectors, make sure that the ground plane clearouts around each pin have ground continuity between all pins.
- Maintain the parallelism (skew-matched) between DP and DM, and match the overall differential length difference to less than 5 mils.
- Maintain the symmetric routing for each differential pair.
- Do not route the DP and DM traces under the oscillators or parallel to the clock traces (and/or data buses).
- Minimize the lengths of the high-speed signals that run parallel to the DP and DM pair.
- Keep the DP and DM traces as short as possible.
- Route the DP and DM signals with a minimum amount of corners. Use 45-degree turns instead of 90-degree turns.
- Avoid layer changes (vias) on the DP and DM signals. Do not create stubs or branches.
- Provide the ground return vias within a 50-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- When the USB signals are not used, it is recommended to follow Unused pins recommendation.

7.6 Ethernet

RT1170 has two ethernet controllers, one is 10M/100M ethernet controller with support for IEEE1588 and the other one is gigabit ethernet controller with support for AVB/TSN. For the RGMII port, the layout is quite critical and below are the guidelines.

- To ensure correct RGMII function, the length of PCB trace should be less than 15cm with a 5pf loading to comply with maximum 1ns delay regulation and the total trace loading (5pf input loading included) should be within 15pf.

- Clock and other high-speed traces must be as short as possible, it's necessary to have a GND plane under these traces.
- RXC and TXC are high-speed (125MHz) signals; Keep a 20mil space between clock and data signals.
- Match each RGMII TX and RX (RXC/RXD/RXCTL/RXDV) group trace length to within +/-50mil.
- Route the RGMII traces at 50ohm impedance, and make sure those traces are routed over an unbroken GND reference ground plane.
- For the RXC signal from the PHY, place R/C close to the PHY (less than 500 mils) and adjust the R/C value to tune the timing.

7.7 High-speed signal routing recommendations

The following list provides recommendations for routing the traces for high-speed signals. Note that the propagation delay and the impedance control must match to have a correct communication with the devices.

- The high-speed signals (SDRAM, RMII, RGMII, USB, Display, Hyperflash, SD card) must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in the reference planes. Review the via voids to ensure that they do not create splits (space out vias).
- Provide ground return vias within a 100-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- A solid GND plane must be directly under the crystal-associated components, and traces.
- The clocks or strobes that are on the same layer need at least 2.5× spacing from the adjacent traces (2.5× height from the reference plane) to reduce crosstalk.
- All synchronous modules must have the bus length matching and relative clock length control.
- For the SD module interfaces:
  - Match the data, clock, and CMD trace lengths (length delta depends on the bus rates).
  - Follow similar SDRAM rules for data, address, and control as for the SD module interfaces.
- For the RT1170 FlexSPI module to support QSPI flash, FlexSPI_DQS pin should be kept floating to achieve high-speed access.

7.8 Unused pins recommendation

Table 12. Recommended connections for unused analog interfaces

Module	Ball Name	Recommendations if Unused
32 kHz OSC	RTC_XTALI, RTC_XTALO	Not connected It is recommended that RTC_XTALI ties to GND if external crystal is not connected.
ADC	ADC_VREFH	10 kΩ resistor to ground
	VDDA_ADC_1P8	10 kΩ resistor to ground
	VDDA_ADC_3P3	10 kΩ resistor to ground
CCM	CLK1_N, CLK1_P	Not connected
DAC	DAC_OUT	Not connected
MIPI	VDD_MIPI_1P0	For lowest leakage, 10 kΩ resistor to ground. For possible easier layout but higher leakage, tie directly to power (inductors and capacitors are

Table continues on the next page...

Table 12. Recommended connections for unused analog interfaces (continued)

Module	Ball Name	Recommendations if Unused
		not required). Leakage is typically 45 µA but could be a few hundred µA at high temperature.
	VDD_MIPI_1P8	For lowest leakage, 10 kΩ resistor to ground. For possible easier layout but higher leakage, tie directly to power (inductors and capacitors are not required). Leakage is typically 45 µA but could be a few hundred µA at high temperature.
	MIPI_DSI_CKN, MIPI_DSI_CKP, MIPI_DSI_DN0, MIPI_DSI_DP0, MIPI_DSI_DN1, MIPI_DSI_DP1	Not connected
	MIPI_CSI_CKN, MIPI_CSI_CKP, MIPI_CSI_DN0, MIPI_CSI_DP0, MIPI_CSI_DN1, MIPI_CSI_DP1	Not connected
DCDC	DCDC_IN, DCDC_IN_Q, DCDC_DIG, DCDC_ANA	Not connected
	DCDC_DIG_SEANSE, DCDC_ANA_SENSE, DCDC_LP, DCDC_LN	Not connected
	DCDC_PSWITCH, DCDC_MODE	To ground
USB	USB1_DN, USB1_DP, USB1_VBUS, USB2_DN, USB2_DP, USB2_VBUS	Not connected
	VDD_USB_1P8	Tie directly to power; capacitors are not required.
	VDD_USB_3P3	Tie directly to power; capacitors are not required.
SYS OSC	XTALI, XTALO	Not connected

NOTE

For unused digital IO, suggest to tie low or configure it to pull down.

8 Related resources

- i.MX RT1170 Crossover Processors Data Sheet for Consumer Products (document IMXRT1170CEC)
- i.MX RT1170 Crossover Processors Data Sheet for Industrial Products (document IMXRT1170IEC)
- i.MX RT1170 Crossover Processors Data Sheet for Automotive Products (document IMXRT1170AEC)

9 Revision history

The following table summarizes the changes done to this document since the initial release.

Table 13. Revision history

Revision number	Date	Substantive changes
2	09/2021	• Updated the document title from "Hardware Development Guide for the MIMXRT1170 Processors" to "Hardware Development Guide for the MIMXRT1160/1170 Processors" • Added a note to provide support on RT1160 in the Introduction section • In the Power supply section, — Removed the table "Power domains" — Updated the power rail values and notes in Table 1 "Processor supply capacitors when on-chip DCDC regulators are used" — Added Table 2 "Processor supply capacitors when external PMIC or regulators utilized (on-chip DCDC regulators not used)" — Renamed the table from "Power sequence and recommendations" to "Power supply and SNVS domain signals" and updated the description of SNVS domain signals in Table 3 "Power supply and SNVS domain signals" — Removed the figure "Power up and power down sequences" — Updated power sequence requirements • Updated the on-chip termination values and added a footnote in Table 5 "JTAG interface summary" • Updated the description of JTAG_TDO in Table 6 "JTAG recommendation" • Removed an item "For the RT1170 SEMC module to support SDRAM, SEMC_DQS pin (GPIO_EMC_B1_39) should be kept floating to achieve high-speed access" from the High-speed signal routing recommendations section • In the Unused pins recommendation section, — Renamed the column "Pad Name" to "Ball Name" — Updated the recommendation values of MIPI and USB modules — Added a note • Added the Related resources section
1	03/2021	Minor updates in Power supply, On-chip DC/DC module, and Table 6.
0	11/2020	Initial public release

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