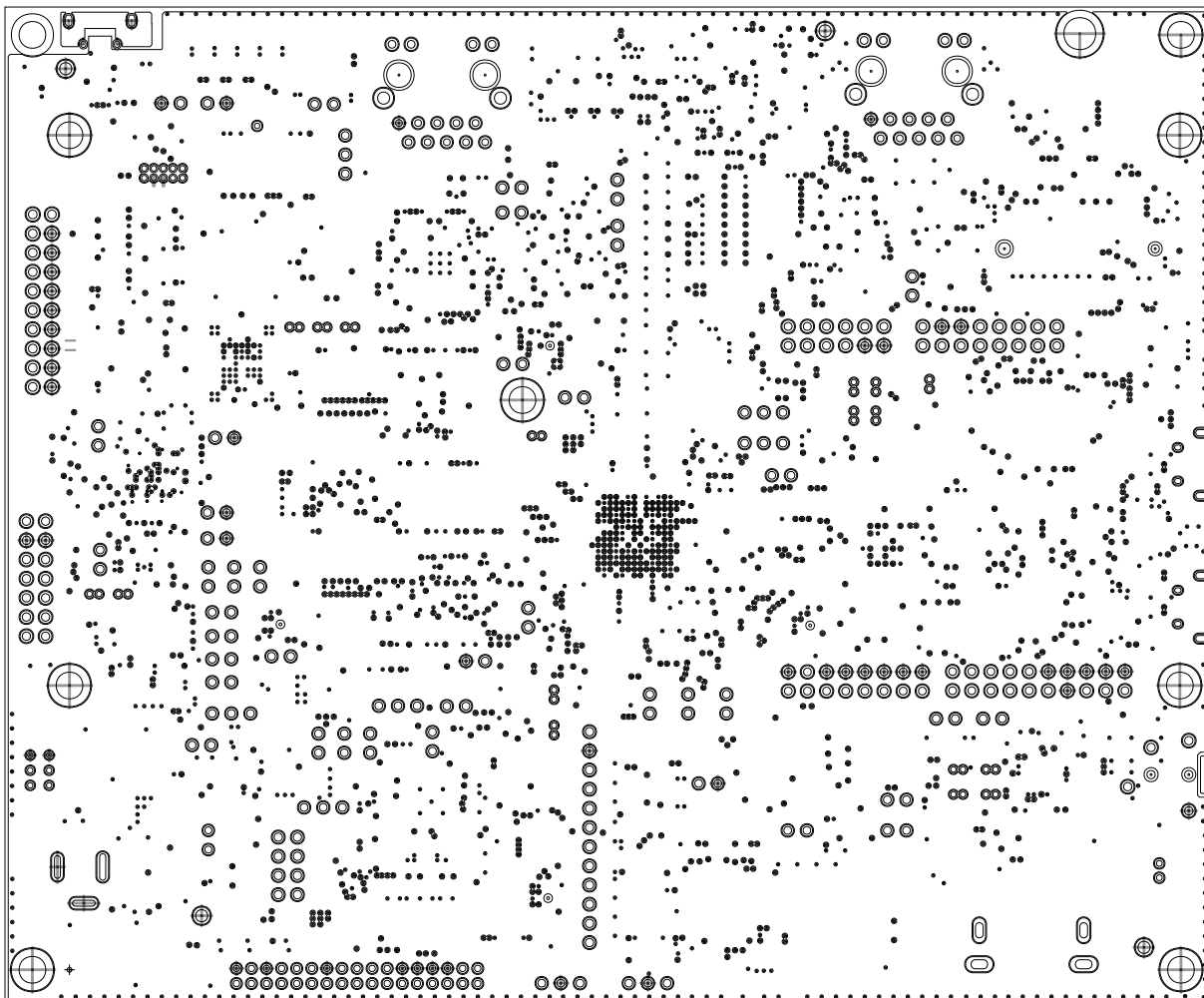


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SHEET 6 OF 12	FILM L3_INT_1	DATE 10-28-22	NUMBER 170-55139 REV C1



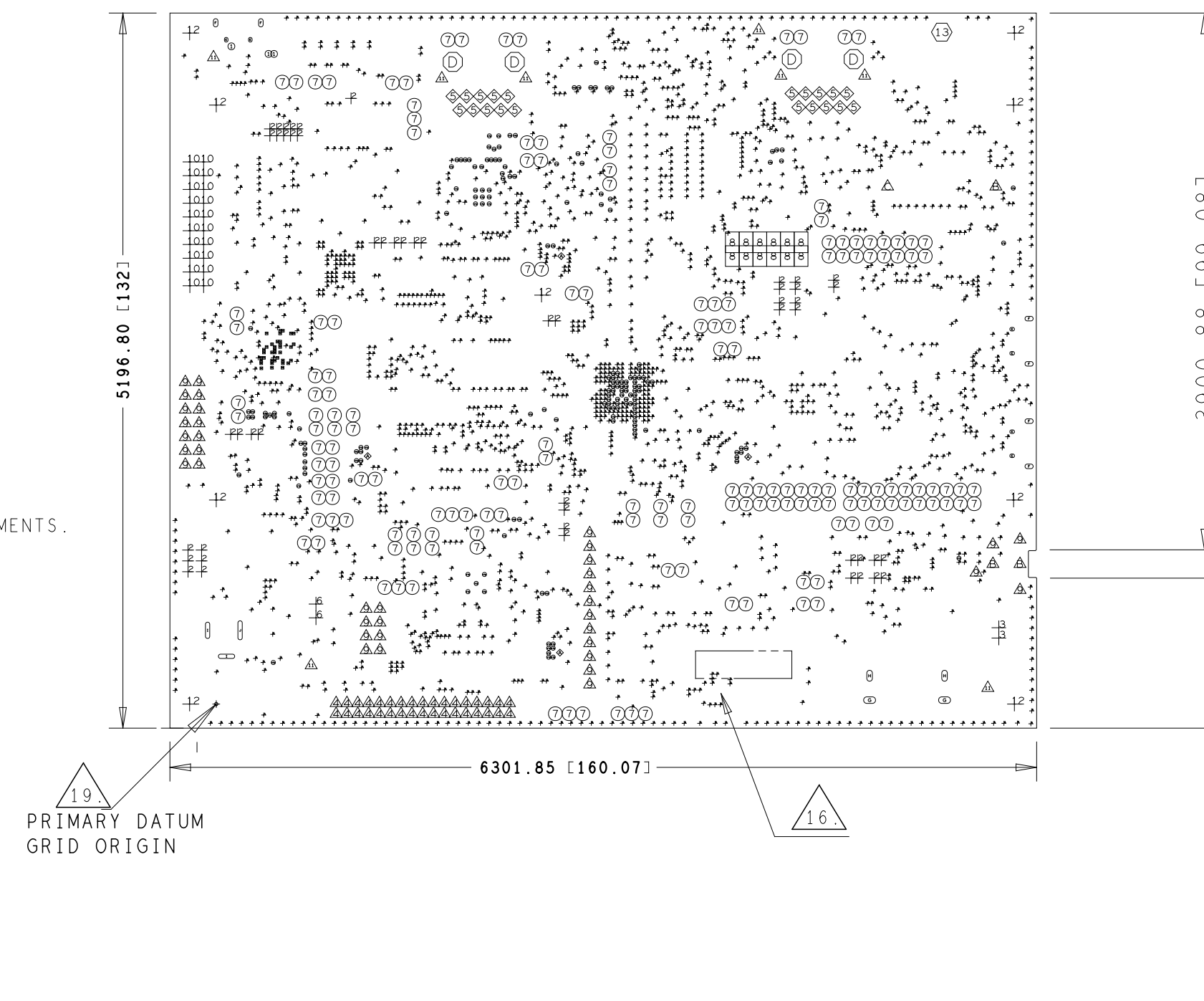
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SHEET 5 OF 12	FILM L2_GND_1	DATE 10-28-22	NUMBER 170-55139 REV C1

NOTES (UNLESS OTHERWISE SPECIFIED):

- THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).
- THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
- BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98  
T<sub>g</sub> - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.  
T<sub>d</sub> - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
- COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
- CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'
- MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .003"/.004"
- PLATING FINISH: A. BOTH SIDES ENIG; TO MEET THE REQUIREMENTS OF IPC-4552 (LATEST REVISION).
- FAB VENDOR IS NOT ALLOWED TO USE ODB FOR FABRICATION. CAN BE USED ONLY FOR REFERENCE.
- SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION). GREEN COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP. TYPE: LPI OR EQUIVALENT.  
A. LOCATION = +/- .002" OF PLATED PADS.  
B. DIAMETER OR SIZE = +/- .002 OF ORIGINAL DATA
- SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.
- ELECTRICAL TEST - 100% IPCD356. PCB FABRICATOR TO PERFORM A NET COMPARE AGAINST THE IPCD356 NETLIST PROVIDED BY NXP.
- PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
- DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS. UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.
- TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
- TWO SOLDER SAMPLES TO BE PROVIDED.
- SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN. MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
- THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (Pb)
- THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
- ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.
- FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
- THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS. KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.
- THIS BOARD USES VIA-IN-PAD: SEE FAB\_VIAFILL.ART  
A. ALL VIAS USING X.1 DRILL SIZES ARE TO BE FILLED WITH NON-CONDUCTIVE VIA FILL. LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.  
B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.  
C. DIMPLE OR PROTRUSION ON VIA-IN-PADS MUST BE NO GREATER THAN .001".

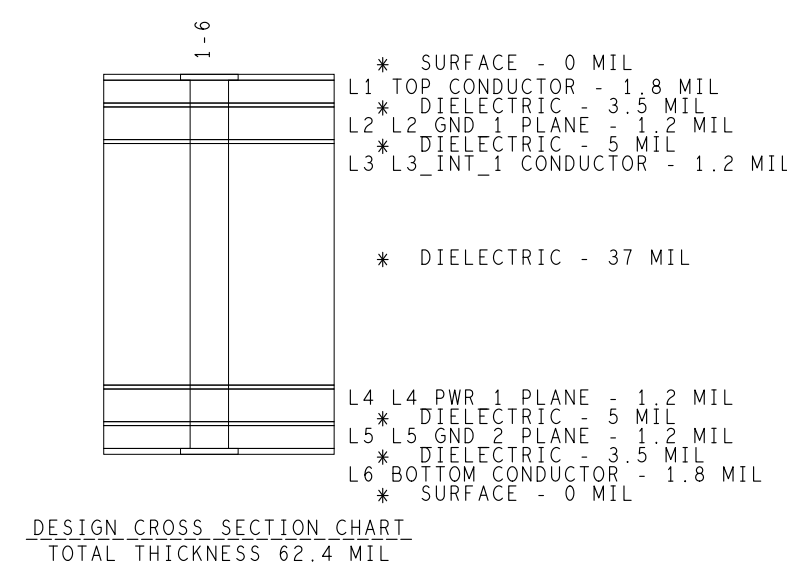
REVISIONS						
ZONE	REV	DESCRIPTION	DATE	APPROVED		
				DE	PE	CAD
	A	ORIGINAL RELEASE	04-12-22	A.L.	L.P.	A.Z.
	B	UPDATED	08-17-22	A.L.	L.P.	A.Z.
	C1	UPDATED	10-28-22	A.L.	L.P.	A.Z.

DRILL CHART: TOP to BOTTOM					
ALL UNITS ARE IN MILS					
FIGURE	FINISHED SIZE	TOLERANCE	DRILL	PLATED	QTY
⊕	8.0	+0.0/-8.0		PLATED	2279
⊕	8.1	+0.0/-8.1		PLATED	171
⊕	8.1	+0.0/-8.1		PLATED	36
⊕	10.0	+0.0/-10.0		PLATED	3
⊕	28.0	+3.0/-3.0		PLATED	51
⊕	30.0	+3.0/-3.0		PLATED	2
⊕	33.0	+2.0/-2.0		PLATED	34
⊕	35.0	+2.0/-2.0		PLATED	20
⊕	36.0	+3.0/-3.0		PLATED	2
⊕	40.0	+3.0/-3.0		PLATED	166
⊕	41.0	+3.0/-3.0		PLATED	12
⊕	43.0	+3.0/-3.0		PLATED	38
⊕	45.0	+3.0/-3.0		PLATED	20
⊕	63.0	+3.0/-3.0		PLATED	8
⊕	139.0	+3.0/-3.0		PLATED	9
⊕	166.0	+3.0/-3.0		PLATED	1
⊕	15.0	+2.0/-2.0		NON-PLATED	4
⊕	43.0	+2.0/-2.0		NON-PLATED	3
⊕	63.0	+2.0/-2.0		NON-PLATED	1
⊕	128.0	+2.0/-2.0		NON-PLATED	4
⊕	34.0x26.0	+3.0/-3.0		PLATED	4
⊕	34.0x26.0	+3.0/-3.0		PLATED	2
⊕	59.0x33.0	+3.0/-3.0		PLATED	2
⊕	59.0x33.0	+3.0/-3.0		PLATED	4
⊕	79.0x40.0	+2.0/-2.0		PLATED	2
⊕	86.61x47.24	+2.0/-2.0		PLATED	2
⊕	118.0x31.0	+2.0/-2.0		PLATED	1
⊕	118.0x31.0	+2.0/-2.0		PLATED	1
⊕	137.8x31.5	+2.0/-2.0		PLATED	1



DETAIL B  
IMPEDANCE REQUIREMENTS  
IMPEDANCE TOLERANCE IS 10%

LAYERS	SE			DIFF					
	TRACE WIDTH	IMPEDANCE	TRACE WIDTH	TRACE SPACING	IMPEDANCE	TRACE WIDTH	TRACE SPACING	IMPEDANCE	REFERENCE LAYER
L1_PS	5.00	50.00	4.70	5.00	90.00	4.20	6.00	100.00	2
L3_INT_1	5.00	50.00	4.70	5.00	90.00	4.20	6.00	100.00	2,4
L6_SS	5.00	50.00	4.70	5.00	90.00	4.20	6.00	100.00	5



DETAIL A  
LAYER STACKUP  
SCALE: NONE

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE:  
DECIMALS .XX .01  
ANGLES 0-30°  
XXX .005

RMS ALL MACHINED SURFACES. BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS.  
UNDERLINED DIM. NOT TO SCALE. THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

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PART NO.  
170-55139

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NXP SEMICONDUCTORS

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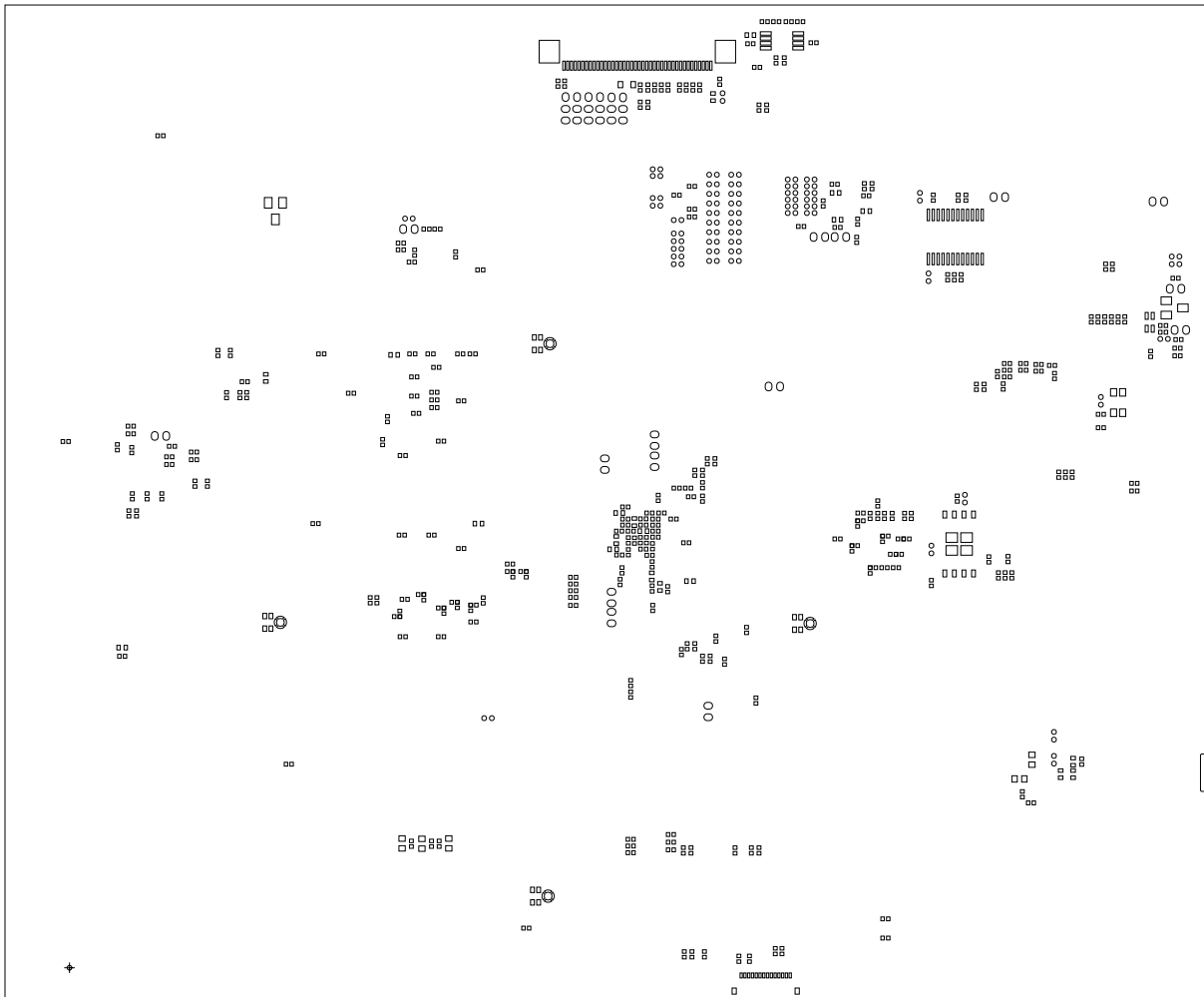
APPROVALS  
DRAWN: Aison Zhou  
CHECKED: Leo Pan  
DESIGN ENGINEER: Albert Li

DATE  
08-17-22  
08-17-22  
08-17-22

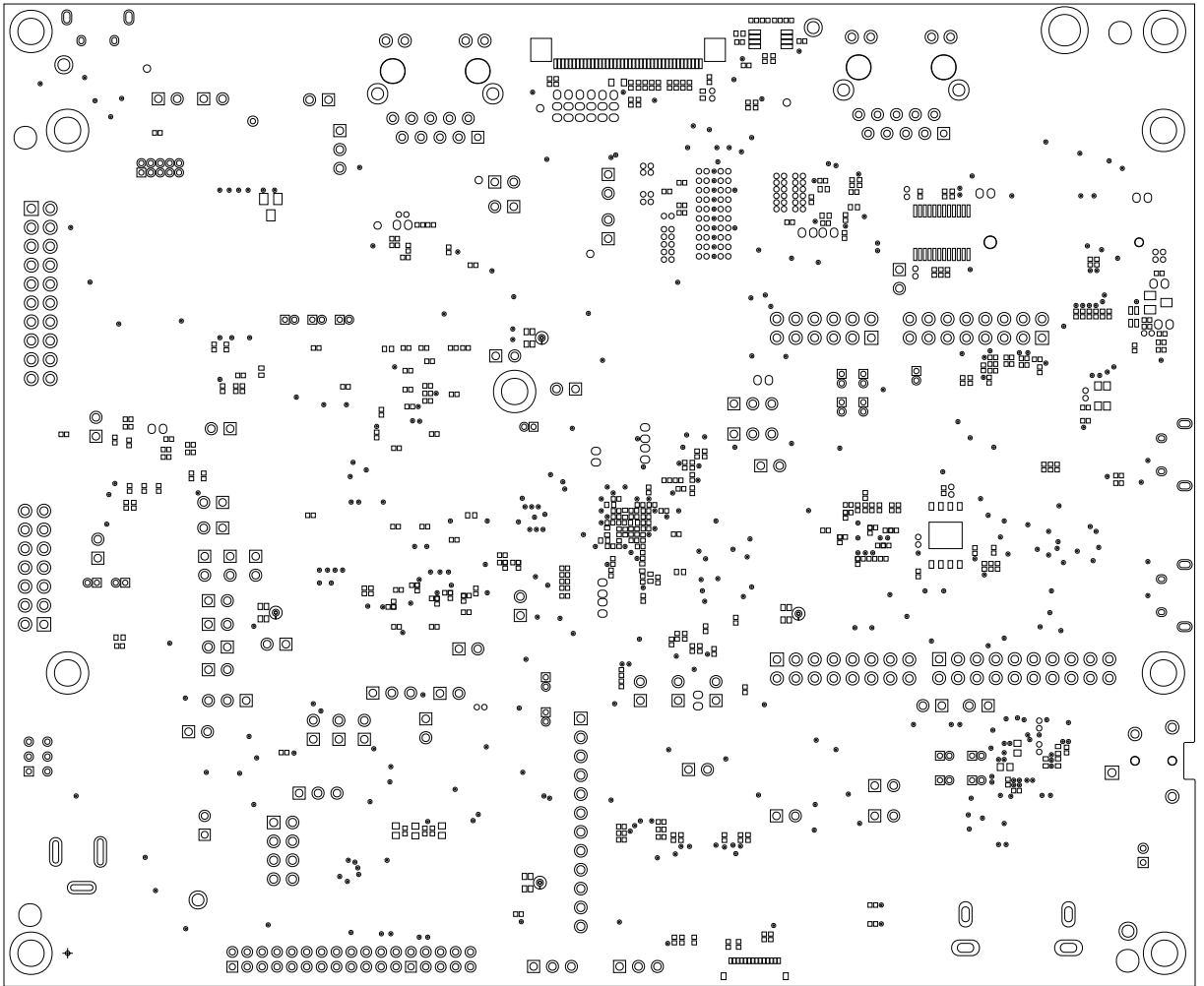
TITLE:  
PRINTED WIRING BOARD  
MIMXRT1170-EVKB

SIZE: D  
CAD FILE NAME: LAY-55139  
DWG. NO.: FAB-55139  
REV: B

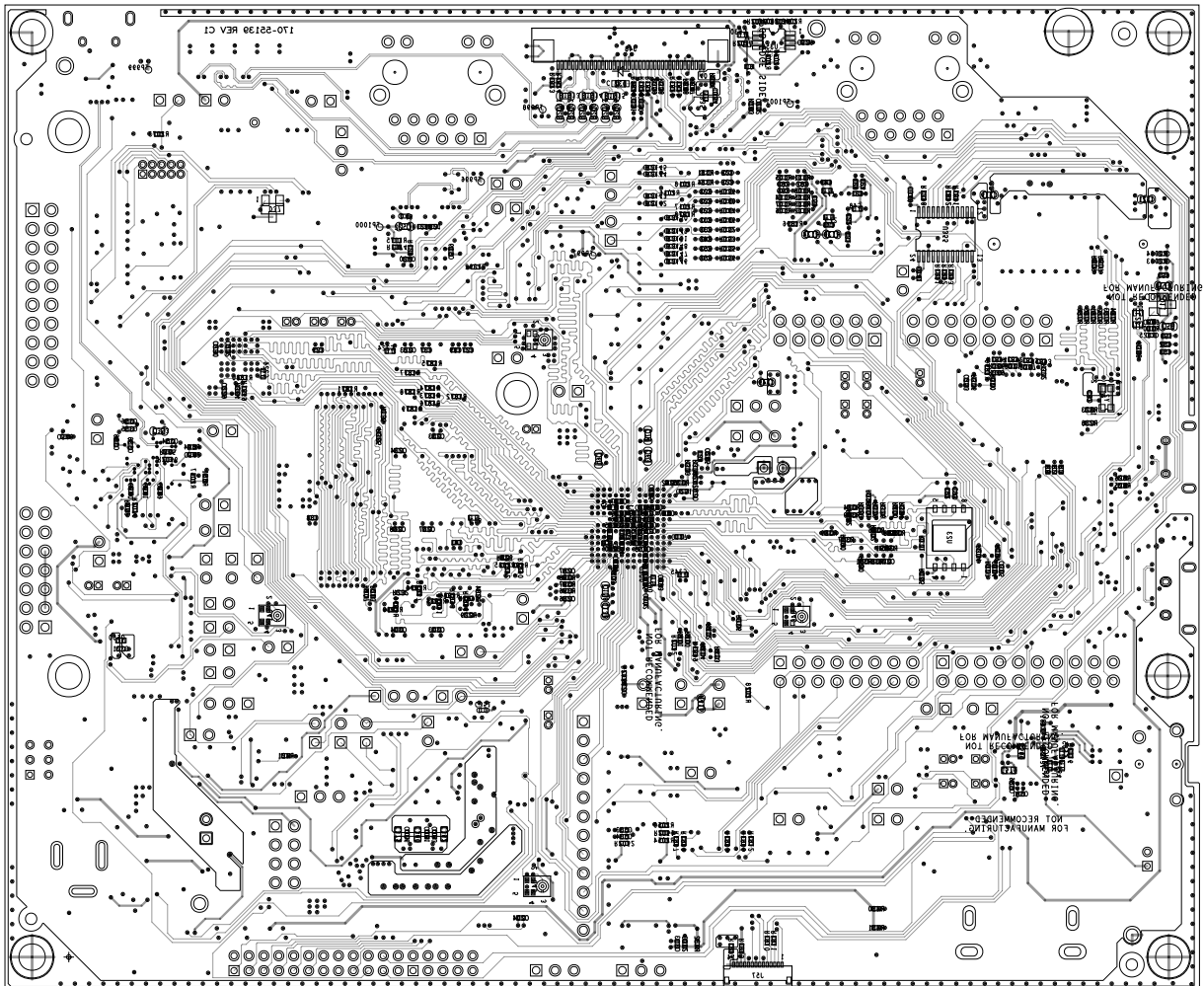
SCALE: 1/1  
DO NOT SCALE DRAWING  
SHEET: 1 OF 2



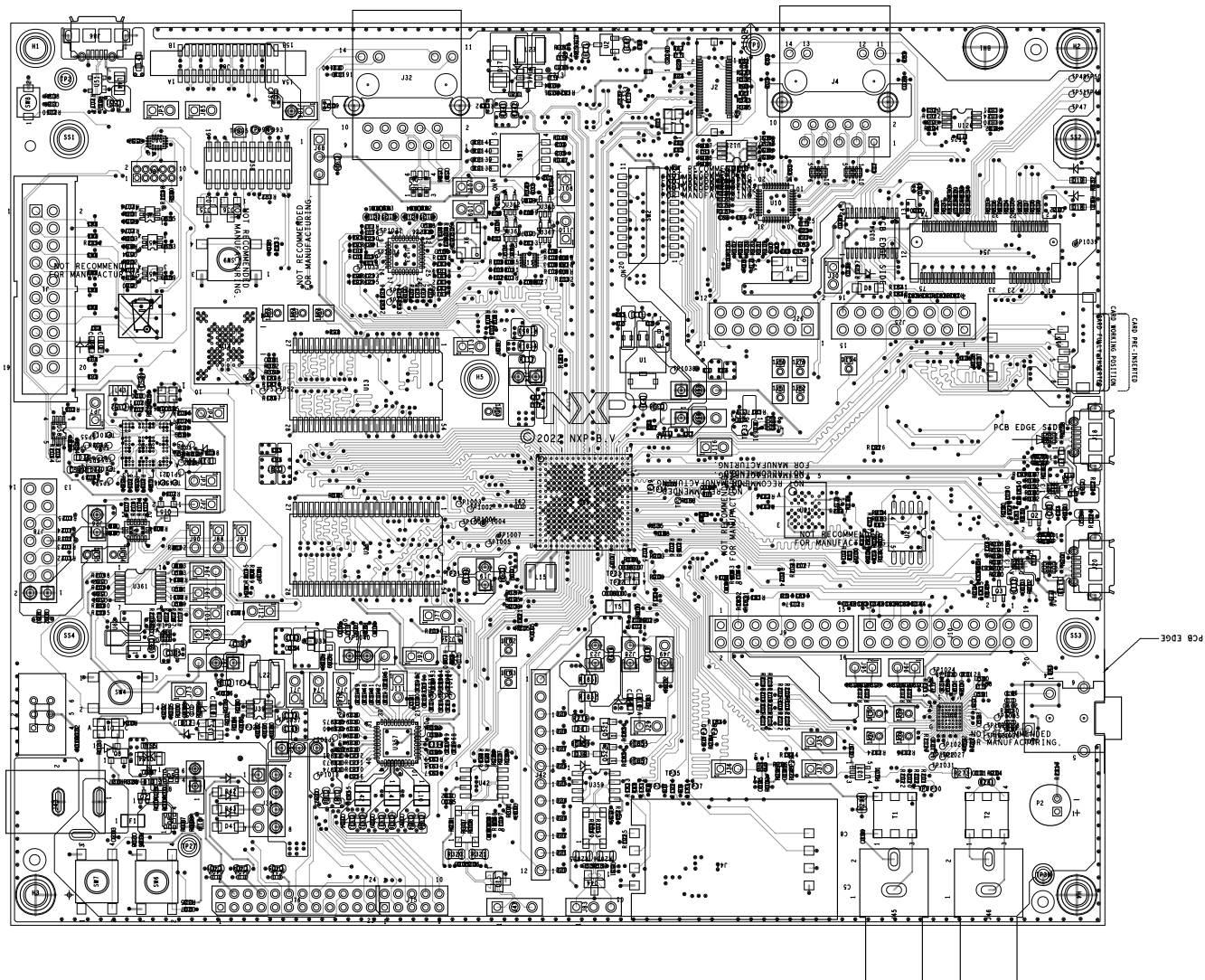
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SHEET 12 OF 12	FILM SECONDARY PASTEMASK	DATE 10-28-22	NUMBER 170-55139 REV C1



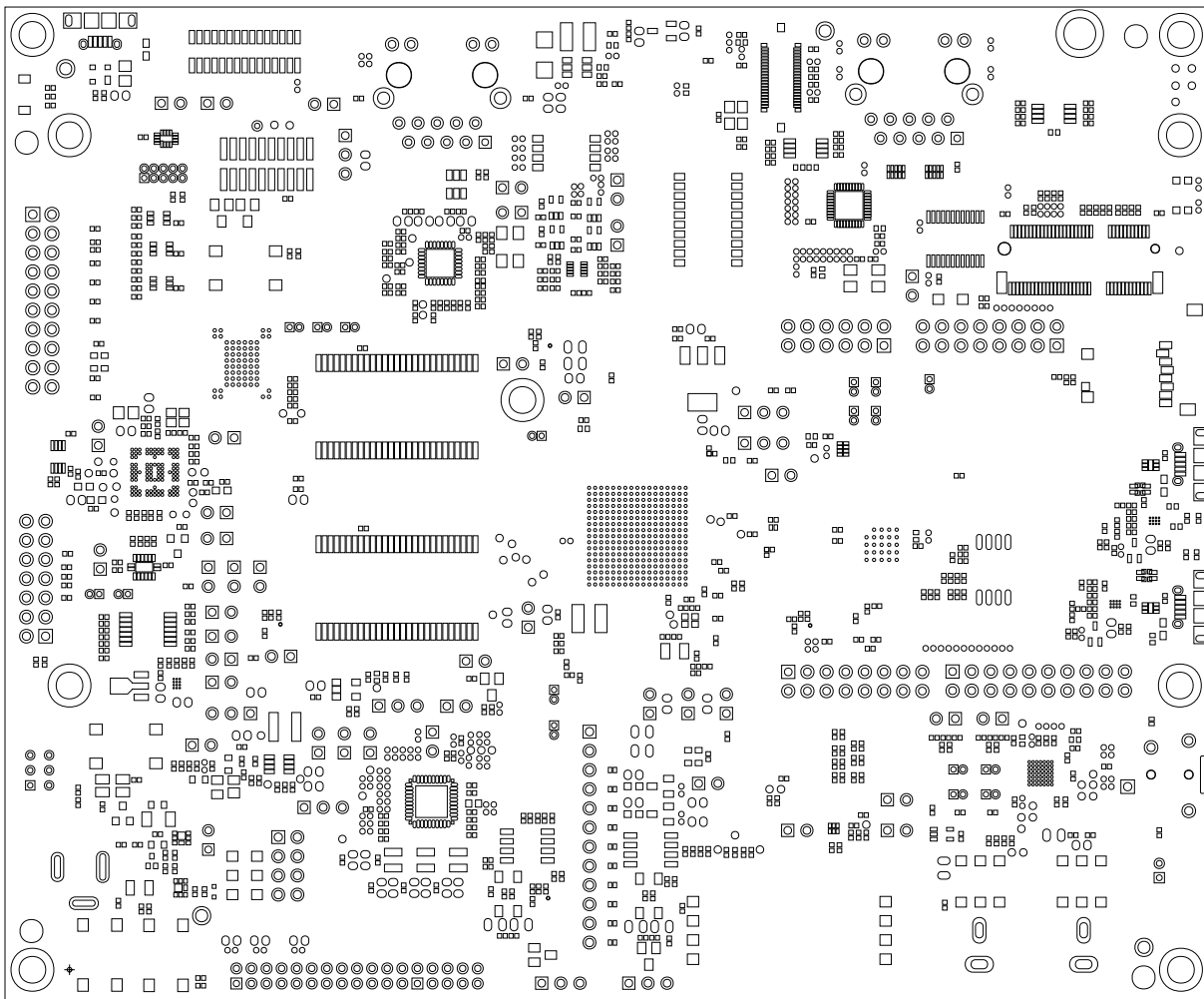
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SHEET 11 OF 12	FILM SECONDARY SOLDMASK	DATE 10-28-22	NUMBER 170-55139 REV C1



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SHEET 9 OF 12	FILM L6_SS	DATE 10-28-22	NUMBER 170-55139 REV C1

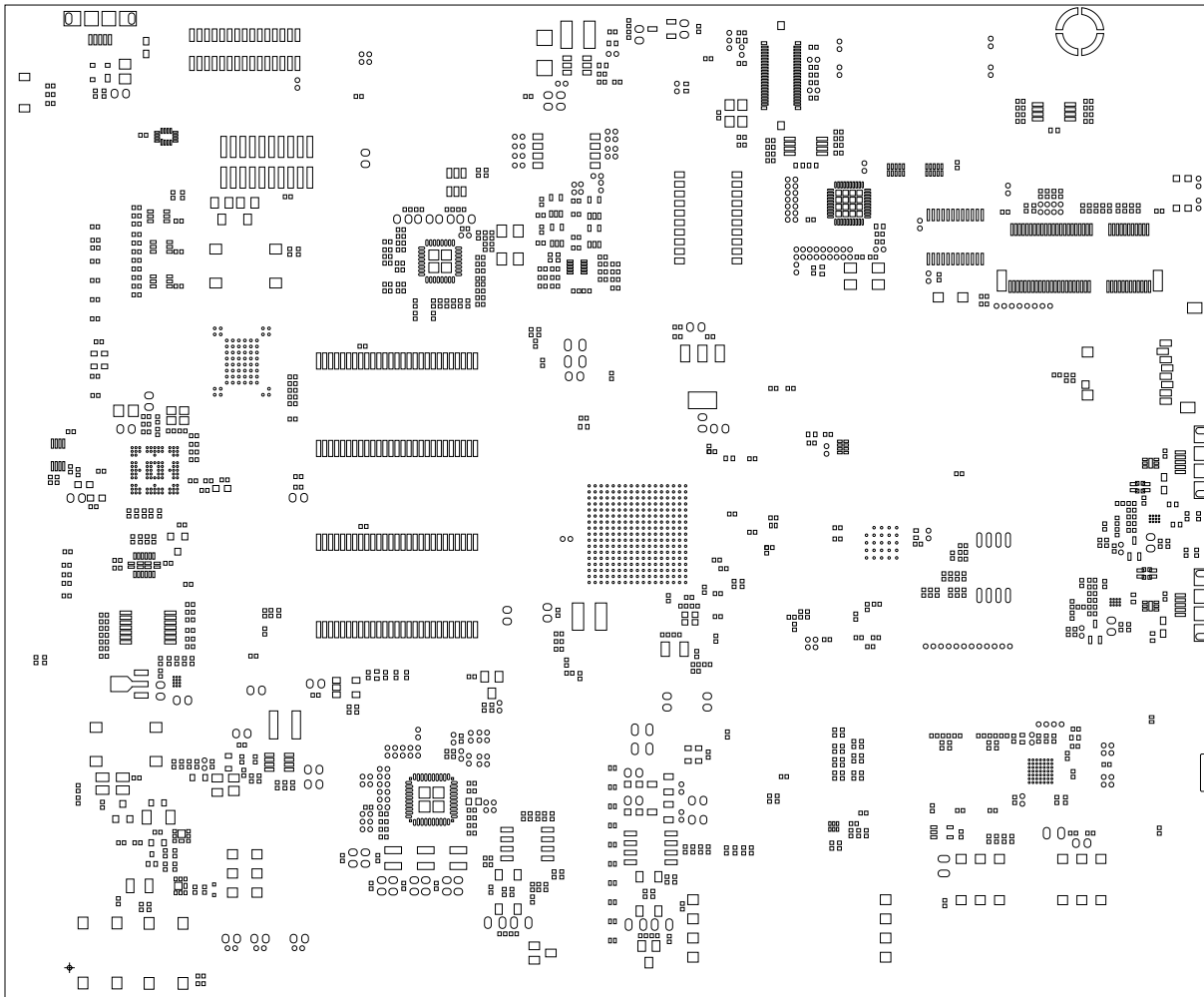


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SHEET 4 OF 12	FILM L1_PS	DATE 10-28-22	NUMBER 170-55139 REV C1

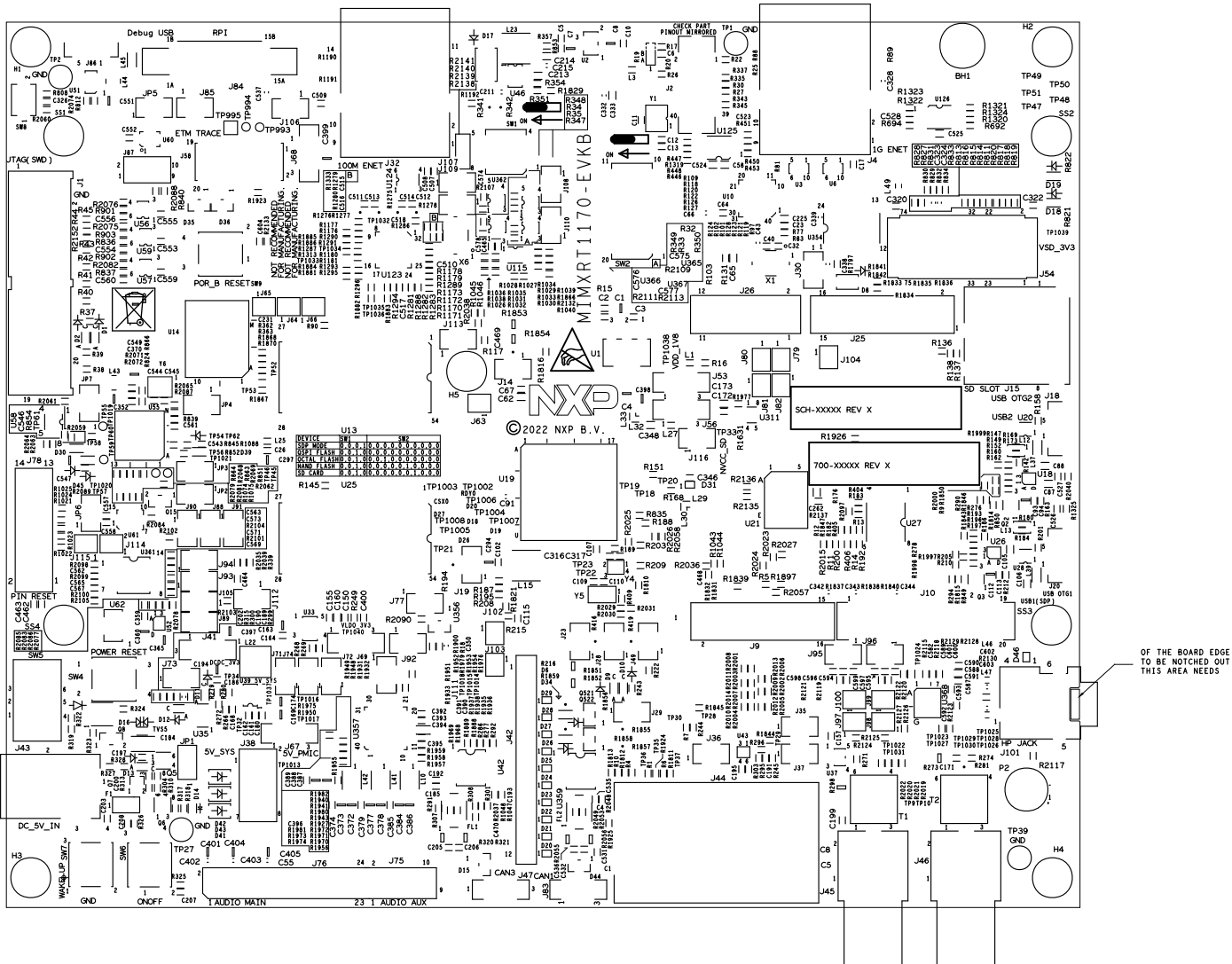


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SHEET 2 OF 12	FILM PRIMARY SOLDMASK	DATE 10-28-22	NUMBER 170-55139 REV C1

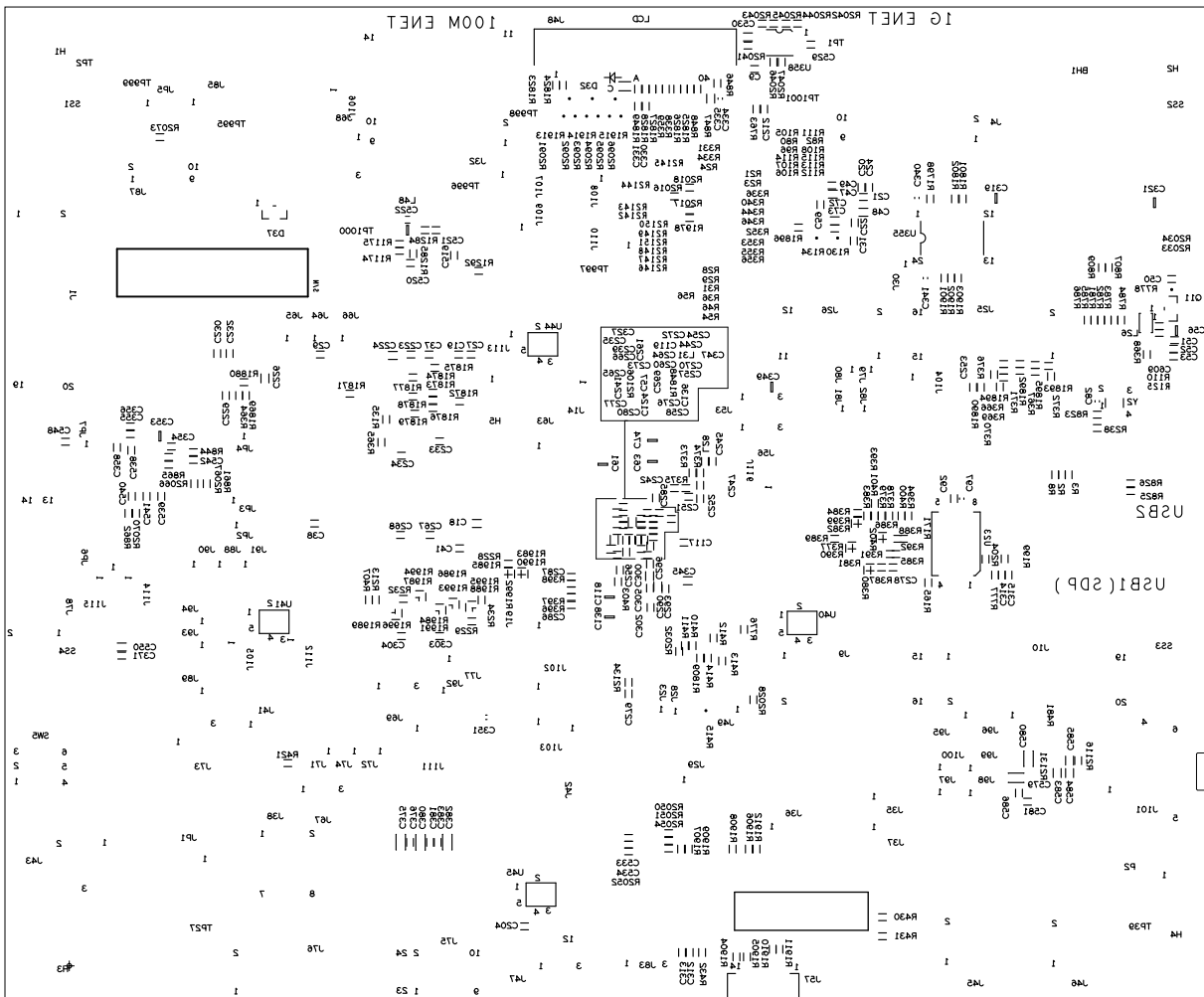




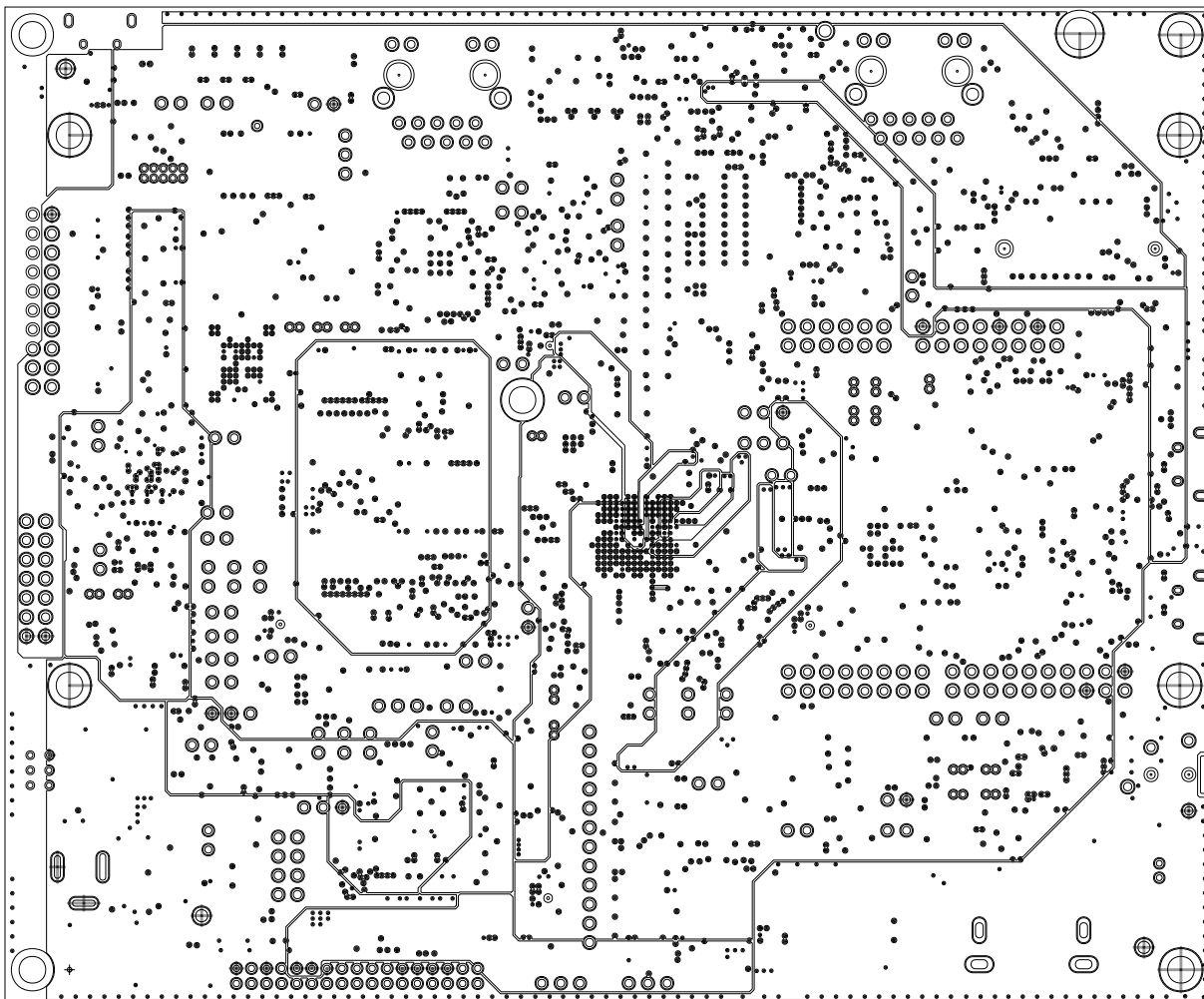
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SHEET 3 OF 12	FILM PRIMARY PASTEMASK	DATE 10-28-22	NUMBER 170-55139 REV C1



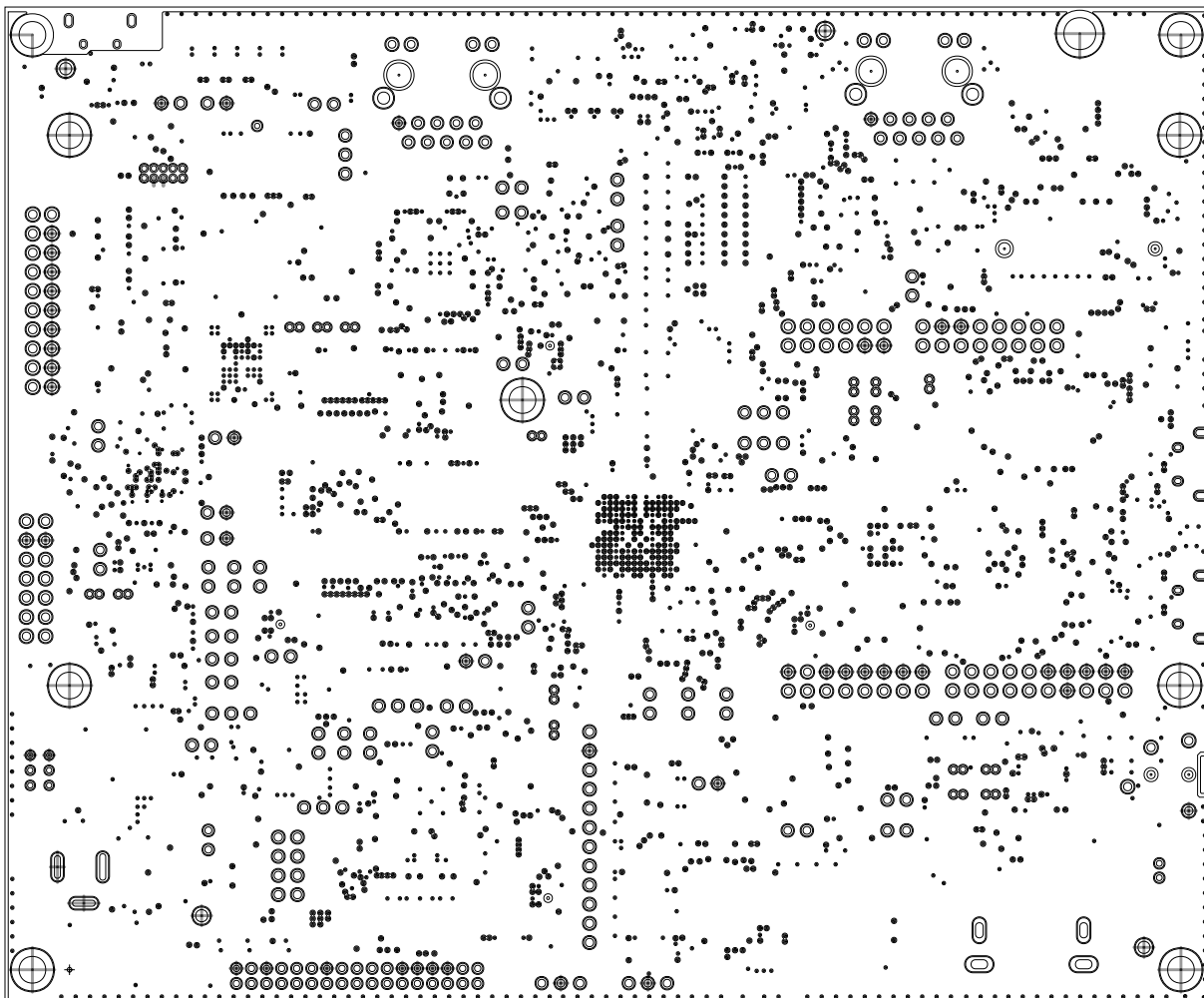
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SHEET 1 OF 12	FILM PRIMARY SILKSCREEN	DATE 10-28-22
	NUMBER 170-55139	REV C1



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SHEET 10 OF 12	FILM SECONDARY SILKSCREEN	DATE 10-28-22	NUMBER 170-55139 REV C1



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SHEET 7 OF 12	FILM L4_PWR_1	DATE 10-28-22	NUMBER 170-55139 REV C1



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SHEET 8 OF 12	FILM L5_GND_2	DATE 10-28-22	NUMBER 170-55139 REV C1

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NOTES (UNLESS OTHERWISE SPECIFIED):

REVISIONS						
ZONE	REV	DESCRIPTION	DATE	APPROVED		
				DE	PE	CAD
	A	ORIGINAL RELEASE	04-12-22	A.L.	L.P.	A.Z.
	B	UPDATED	08-17-22	A.L.	L.P.	A.Z.
	C1	UPDATED	10-28-22	A.L.	L.P.	A.Z.

THIS FAB VIAFILL.ART SHOWS LOCATIONS OF VIA-IN-PAD TO BE FILLED



D

D

C

C

B

B

A

A

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7

6

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3

2

1

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES  
 TOLERANCES ARE:  
 DECIMALS ANGLES  
 .XX .01 0-30°  
 .XXX .005  
 ✓ RMS ALL MACHINED SURFACES.  
 BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS.  
 UNDERLINED DIM. NOT TO SCALE. THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

PART NO. 170-55139		THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCEDURE OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP.		NXP SEMICONDUCTORS 6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA	
<input type="checkbox"/> COMPANY PUBLIC <input checked="" type="checkbox"/> COMPANY INTERNAL <input type="checkbox"/> COMPANY CONFIDENTIAL		APPROVALS DRAWN: <u>Atson Zhou</u> 08-17-22 CHECKED: <u>Leo Pan</u> 08-17-22 DESIGN ENGINEER: <u>Albert Li</u> 08-17-22		TITLE: PRINTED WIRING BOARD MIMXRT1170-EVKB	
SIZE: D	CAD FILE NAME: LAY-55139	DWG. NO.: FAB-55139	REV: B	SCALE: 1/1 DO NOT SCALE DRAWING SHEET 1 OF 2	