IMX8HWDG

i.MX8 QM / i.MX8 QXP / i.MX 8DXL Hardware Developer's Guide

Rev. 2.6 — 20 March 2023 **User guide**

Document information

Information	Content
Keywords	i.MX8 QM, i.MX8 QXP, i.MX 8DXL
Abstract	This document's purpose is to help hardware engineers design and test their i.MX 8 series processor-based designs. It provides information on board layout recommendations, design checklists to ensure first-pass success and ways to avoid board bring-up problems.

1 Overview

This document's purpose is to help hardware engineers design and test their i.MX 8 series processor-based designs. It provides information on board layout recommendations, design checklists to ensure first-pass success and ways to avoid board bring-up problems.

Engineers are expected to have a working understanding of board layouts and common board hardware terminology.

This guide is released along with relevant device-specific hardware documentation such as datasheets, reference manuals, and application notes available at nxp.com.

1.1 Devices supported

This Hardware Developer's Guide currently supports the i.MX8 QM (29 x 29 mm package), i.MX8 QXP (21 x 21 mm and 17x17 mm package), and i.MX8 DXL (15 x 15 mm package) processors.

1.2 Essential reference

This guide is intended as a companion to the i.MX 8 series chip reference manuals and data sheets. For the reflow profile and thermal limits during soldering, see *General Soldering Temperature Process Guidelines* (document AN3300). These documents are available at nxp.com.

1.3 Suggested reading

This section lists additional reading that provides background for the information in this manual as well as general information about the architecture.

1.3.1 General information

The following documentation provides useful information about the Arm® processor architecture and computer architecture in general.

- For information about the Arm Cortex®-A35 processor, see: https://www.arm.com/products/processors/cortex-a/cortex-a35-processor.php
- For information about the Arm Cortex-A53 processor, see: https://www.arm.com/products/processors/cortex-a/cortex-a53-processor.php
- For information about the Arm Cortex-A72 processor, see: https://www.arm.com/products/processors/cortex-a/cortex-a72-processor.php
- For information about the Arm Cortex-M4F processor, see: https://www.arm.com/products/processors/cortex-m/cortex-m4-processor.php
- **Computer Architecture: A Quantitative Approach** (Fourth Edition) - by John L. Hennessy and David A. Patterson
- **Computer Organization and Design: The Hardware/Software Interface** (Second Edition), by David A. Patterson and John L. Hennessy

The following documentation provides useful information about high-speed board design:

- **Right the First Time- A Practical Handbook on High Speed PCB and System Design - Volumes I & II** - Lee W. Ritchey (Speeding Edge) - ISBN 0-9741936- 0-72
- **Signal and Power Integrity Simplified** (Second Edition) - Eric Bogatin (Prentice Hall)- ISBN 0-13-703502-0
- **High Speed Digital Design- A Handbook of Black Magic** - Howard W. Johnson & Martin Graham (Prentice Hall) - ISBN 0-13-395724-1

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- **High Speed Signal Propagation- Advanced Black Magic** - Howard W. Johnson & Martin Graham - (Prentice Hall) - ISBN 0-13-084408-X
- **High Speed Digital System Design- A handbook of Interconnect Theory and Practice** - Hall, Hall and McCall (Wiley Interscience 2000) - ISBN 0-36090-2
- **Signal Integrity Issues and Printed Circuit Design** - Doug Brooks (Prentice Hall) ISBN 0-13-141884-X
- **PCB Design for Real-World EMI Control** - Bruce R. Archambeault (Kluwer Academic Publishers Group) - ISBN 1-4020-7130-2
- **Digital Design for Interference Specifications** - A Practical Handbook for EMI Suppression -David L. Terrell & R. Kenneth Keenan (Newnes Publishing) - ISBN 0-7506-7282-X
- **Electromagnetic Compatibility Engineering**- Henry Ott (First Edition - John Wiley and Sons) - ISBN 0-471-85068-3
- **Introduction to Electromagnetic Compatibility** - Clayton R. Paul (John Wiley and Sons) - ISBN 978-0-470-18930-6
- **Grounding & Shielding Techniques** - Ralph Morrison (Fifth Edition - John Wiley & Sons) - ISBN 0-471-24518-6
- **EMC for Product Engineers** - Tim Williams (Newnes Publishing) - ISBN 0-7506- 2466-3

1.4 Related documentation

NXP documentation is available from the sources listed on the back page of this guide.

Additional literature is published as new NXP products become available. For a current list of documentation, see nxp.com.

1.5 Conventions

This document uses the following notational conventions:

`Courier` Used to indicate commands, command parameters, code examples, and file and directory names.

Italics indicates command or function parameters.

Bold Function names are written in bold.

cleared/set When a bit takes the value of zero, it is said to be cleared; when it takes a value of one, it is said to be set.

Mnemonics Instruction mnemonics are shown in lowercase bold. Book titles in text are set in italics.

sig_name Internal signals are written in all lowercase.

nnnn nnnnh Denotes a hexadecimal number.

0b Denotes a binary number.

rA, **r**B Instruction syntax used to identify a source GPR.

rD Instruction syntax used to identify a destination GPR.

REG[FIELD] Abbreviations for registers are shown in uppercase text. Specific bits, fields, or ranges appear in brackets. For example, MSR[LE] refers to the little-endian mode enable bit in the machine state register.

x In some contexts, such as signal encodings, an unitalicized “x” indicates a do not care.

x An italicized “*x*” indicates an alphanumeric variable.

n, m An italicized “*n*” indicates a numeric variable.

In this guide, notations for all logical, bit-wise, arithmetic, comparison, and assignment operations follow C Language conventions.

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1.6 Acronyms and abbreviations

Table 1 defines the acronyms and abbreviations used in this document.

Table 1. Definitions and acronyms

Acronym	Definition
Arm	Advanced RISC Machines processor architecture
BGA	Ball Grid Array package
BOM	Bill Of Materials
BSDL	Boundary Scan Description Language
CAN	Flexible Controller Area Network peripheral
CCM	Clock Controller Module
CSI	MIPI Camera Serial Interface
DDR	Dual Data Rate DRAM
DDR3L	Low-voltage DDR3 DRAM
DDRC	DDR Controller
DFP	Downstream Facing Port (USB Type-C)
DRP	Dual Role Port (USB Type-C)
ECSPI	Enhanced Configurable SPI peripheral
EIM	External Interface Module
ENET	10/100/1000 Mbps Ethernet MAC peripheral
EPIT	Enhanced Periodic Interrupt Timer peripheral
ESR	Equivalent Series Resistance
GND	Ground
GPC	General Power Controller
GPIO	General-Purpose Input/Output
HDCP	High-bandwidth Digital Content Protection
I^2C	Inter-integrated Circuit interface
IBIS	Input output Buffer Information Specification
IOMUX	i.MX8 chip-level I/O Multiplexing
JTAG	Joint Test Action Group
KPP	Keypad Port Peripheral
LDB	LVDS Display Bridge
LDO	Low Drop-Out regulator
LPCG	Low-Power Clock Gating
LPDDR4	Low-Power DDR4 DRAM
LVDS	Low-Voltage Differential Signaling
MLB	Media Local Bus
ODT	On-Die Termination

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Table 1. Definitions and acronyms*...continued*

Acronym	Definition
OTP	One-Time Programmable
PCB	Printed-Circuit Board
PCIe	PCI Express
PCISig	Peripheral Component Interconnect Special interest group
PDN	Power Distribution Network
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
PTH	Plated Through Hole PCB (no microvias)
RGMII	Reduced Gigabit Media Independent Interface (Ethernet)
RMII	Reduced Media Independent Interface (Ethernet)
ROM	Read-Only Memory
UFP	Upstream Facing Port (USB Type-C)

2 i.MX8 QM, QXP, and DXL design checklist

This document provides a design checklist for the i.MX8 QM (29 x 29 mm package), i.MX8 QXP (21 x 21 mm package), and i.MX8 DXL (15 x 15 mm package) processors. The design checklist tables contain recommendations for optimal design. Where appropriate, the checklist tables also provide an explanation of the recommendation so that users have a greater understanding of why certain techniques are recommended. All supplemental tables referenced by the checklist appear in sections following the design checklist tables.

2.1 Design checklist tables

Table 2. LPDDR4 recommendations (i.MX8 QM)

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. Connect the DDR_CHn_ZQ balls on the processor (balls AF44 and AF10) to individual 240 Ω, 1 % resistors to GND.	This is a reference used during DRAM output buffer driver calibration.
	2. The ZQ0 and ZQ1 balls on each LPDDR4 device should be connected through 240 Ω, 1 % resistors to the LPDDR4 VDD2 rail.	
	3. Place a 10 kΩ, 5 % resistor to the ground on the DRAM reset signal.	This ensures adherence to the JEDEC specification until the control is configured and starts driving the DDR.
	4. The DDR_CHn_VREF balls on the processor (balls U43 and U11) should be left unconnected.	The reference voltage generator is on the chip, so no external source is required.
	5. The QM balls DDR_CHn_DCF09 and DDR_CHx_DCF25 should be left unconnected. The ODT_CA balls on the LPDDR4 device should be connected directly to the LPDDR4 VDD2 rail.	DDR_CH(0:1)_DCF09 = T52, T2 DDR_CH(0:1)_DCF25 = AF52, AF2 LPDDR4 ODT on the i.MX8 QM is command-based, making the processor ODT_CA output balls unnecessary.
	6. The architecture for each chip inside the DRAM package must be x16.	The processor does not support the byte mode specified in JESD209-4C.

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Table 2. LPDDR4 recommendations (i.MX8 QM)*...continued*

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	7. The processor balls DDR_CHn_ATO (balls AF46/AF8), DDR_CHn_DTO0 (balls U45/U9), and DDR_CHn_DTO1 (balls T44/T10) should be left unconnected.	These are observability ports for manufacturing and they are not used otherwise.

Table 3. LPDDR4 recommendations (i.MX8 QXP)

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. Connect the DDR_ZQ ball on the processor (ball G9) to an external 240 Ω, 1 % resistor to GND.	This is a reference used during DRAM output buffer driver calibration.
	2. Connect the ZQ0/ZQ1 balls on the LPDDR4 device through 240 Ω, 1 % resistors to the VDD2 supply of the LPDDR4 device.	
	3. Place a 10 kΩ, 5 % resistor to the ground on the DRAM reset signal.	This ensures the adherence to the JEDEC specification until the control is configured and starts driving the DDR.
	4. The DDR_VREF ball (AD8) should be left unconnected.	The reference voltage generator is on the chip, so no external source is required.
	5. The QXP device balls DDR_DCF09 and DDR_DCF25 should be left unconnected. The ODT_CA balls on the LPDDR4 device should be connected directly to the LPDDR4 VDD2 rail.	DDR_DCF09 = ball AB6, DDR_DCF25 = ball K8 The LPDDR4 ODT on the i.MX8 QXP is command-based, making the processor ODT_CA output balls unnecessary.
	6. The architecture for each chip inside the DRAM package must be x16.	The processor does not support the byte mode specified in JESD209-4C.
	7. The processor balls DDR_ATO (ball AB8) and DDR_DTO0:1 (balls AC7, AE7) should be left unconnected.	These are observability ports for manufacturing and they are not used otherwise.

Table 4. LPDDR4 Recommendations (i.MX8 DXL)

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. Connect the DDR_ZQ ball on the processor (ball AJ7) to an external 240 Ω, 1 % resistor to GND.	This is a reference used during DRAM output buffer driver calibration.
	2. Connect the ZQ0/ZQ1 balls on the LPDDR4 device through 240 Ω, 1 % resistors to the VDD2 supply of the LPDDR4 device.	-
	3. Place a 10 kΩ, 5 % resistor to the ground on the DRAM reset signal.	This ensures the adherence to the JEDEC specification until the control is configured and starts driving the DDR.
	4. The DDR_VREF ball (AJ9) should be left unconnected.	The reference voltage generator is on the chip, so no external source is required.
	5. The DXL device ball DDR_DCF09 should be left unconnected. The ODT_CA balls on the LPDDR4 device should be connected directly to the LPDDR4 VDD2 rail.	DDR_DCF09 = ball A5 The LPDDR4 ODT on the i.MX8 DXL is command-based, making the processor ODT_CA output balls unnecessary.

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Table 4. LPDDR4 Recommendations (i.MX8 DXL)*...continued*

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	6. The architecture for a DRAM chip must be x16.	The processor does not support the byte mode specified in JESD209-4C.
	7. The processor balls DDR_ATO (ball AC7) and DDR_DTO0:1 (balls AG7, AG9) should be left unconnected.	These are observability ports for manufacturing and they are not used otherwise.

Table 5. I^2C recommendations

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. Verify the target I^2C interface clock rates.	The I^2C bus can only be operated as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I^2C port.
	2. Verify that there are no I^2C address conflicts on any of the I^2C buses utilized.	There are multiple I^2C ports available on the chip, so if a conflict exists, move one of the conflicting devices to a different I^2C bus. If this is not possible, use an I^2C bus switch (NXP part number PCA9646).
	3. Do not place more than one set of pull-up resistors on the I^2C lines.	This could result in excessive loading and potential incorrect operation. Choose the pull-up value commensurate with the bus speed being utilized.
	4. Ensure that the VCC rail powering the i.MX8 I^2C interface balls matches the supply voltage used for the pull-up resistors and the slave I^2C devices.	Prevent device damage or incorrect operation due to voltage mismatch.

Table 6. Debug recommendations – JTAG and UART

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. Do not use external pull-up or pull-down resistors on JTAG_TDO.	JTAG_TDO is configured with an on-chip keeper circuit such that the floating condition is actively eliminated if an external pull resistor is not present.
	2. Follow the recommendations for external pull-up and pull-down resistors given in Section 2.2.	-
	3. TEST_MODE_SELECT (ball BC49 on the QM, ball AE29 on the QXP, and ball AN29 on the DXL) should be connected to the ground.	This ball is for factory use only. This ball has an internal pull-down in case of i.MX8 DXL. An external connection to the ground is optional in case of i.MX8 DXL.

Table 7. Reset and on/off recommendations

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. The POR_B input must be asserted at powerup and remain asserted until the last power rail for the devices required for system boot is at its working voltage. This functionality is controlled by the PMIC (PF8100, PF8200, or PF7100).	A reset switch may be wired to the chip's POR_B, which is a cold-reset negative-logic input that resets all modules and logic in the IC. POR_B may be used in addition to internally generated power-on reset signal (logical AND, both internal and external signals are considered active low). While

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Table 7. Reset and on/off recommendations*...continued*

Checkbox	Recommendation	Explanation/Supplemental Recommendation
		POR_B is asserted (low) on the i.MX8, output PMIC_ON_REQ remains asserted (high).
	2. For portable applications, the ON_OFF_BUTTON input may be connected to an ON/OFF SPST pushbutton switch to the ground. On-chip debouncing is provided, and this input has an on-chip pullup. If not used, ON_OFF_BUTTON should be a no-connect.	A brief connection (0.5 sec < press < 4 sec) to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to the GND generates an interrupt (intended to initiate a software-controllable power-down). An approximately 5-second (or more) connection to GND causes a forced OFF.
	3. If PMIC_ON_REQ is not used, the pin should be left unconnected.	-

Table 8. i.MX8 QM power/decoupling recommendations

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. Comply with the power-up sequence guidelines, as described in the data sheet to guarantee reliable operation of the device.	Any deviation from these sequences may result in the following situations: • Excessive current during the power-up phase. • Prevention of the device from booting. • Irreversible damage to the processor (worst case scenario).
	2. Maximum ripple voltage requirements.	A common requirement for the ripple noise should be less than 5 % peak-to-peak of the supply voltage nominal value.
	3. The internal LDOs shown below should be decoupled with individual pairs of 2.2 µF caps: • VDD_HDMI_TX0_LDO_1P0_CAP • VDD_HDMI_RX0_LDO0_1P0_CAP • VDD_HDMI_RX0_LDO1_1P0_CAP • VDD_PCIE_LDO_1P0_CAP	Place at least one capacitor underneath the BGA package as close as possible to each LDO output (desired trace length < 50 mils). The HDMI RX LDO outputs should only be connected to the caps, while the others should be connected to the i.MX8 QM balls, as shown below: • VDD_HDMI_TX0_LDO_1P0_CAP 1. VDD_HDMI_TX0_1P0 • VDD_PCIE_LDO_1P0_CAP 1. VDD_PCIE0_1P0 2. VDD_PCIE1_1P0 3. VDD_PCIE_SATA0_1P0
	4. The VDD_USB_SS3_LDO_1P0_CAP internal LDO should be decoupled with three 2.2 µF caps.	Place two capacitors underneath the BGA package as close as possible to the LDO output (desired trace length < 50 mils). The other cap should be placed on the back side as close as possible to the other two capacitors. This LDO output should only drive: 1. VDD_USB_OTG1_1P0 2. VDD_USB_OTG2_1P0

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Table 9. i.MX8 QXP power/decoupling recommendations

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. Comply with the power-up sequence guidelines, as described in the data sheet to guarantee reliable operation of the device.	Any deviation from these sequences may result in the following situations: • Excessive current during the power-up phase. • Prevention of the device from booting. • Irreversible damage to the processor (worst case scenario).
	2. Maximum ripple voltage requirements.	A common requirement for the ripple noise should be less than 5 % peak-to-peak of the supply voltage nominal value.
	3. The VDD_PCIE_LDO_1P0_CAP internal LDO should be decoupled with a 2.2 μF cap and a 0.22 μF cap.	Place the 0.22 μF capacitor underneath the BGA package as close as possible to the LDO output (desired trace length < 50 mils).
	4. The VDD_USB_SS3_LDO_1P0_CAP internal LDO should be decoupled with a 2.2 μF cap and two 0.22 μF caps.	Place the 0.22 μF capacitors underneath the BGA package as close as possible to the LDO output (desired trace length < 50 mils). This LDO output should only drive VDD_USB_OTG1_1P0.

See the i.MX8QM LPDDR4 MEK layout for the recommended capacitor placement.

Table 10. i.MX8 DXL power/decoupling recommendations

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. Comply with the power-up sequence guidelines, as described in the datasheet to guarantee reliable operation of the device.	Any deviation from these sequences may result in the following situations: • Excessive current during the power-up phase. • Prevention of the device from booting. • Irreversible damage to the processor (worst-case scenario).
	2. Maximum ripple voltage requirements.	A common requirement for the ripple noise should be less than 5 % peak to peak of the supply voltage nominal value.
	3. The VDD_PCIE_LDO_1P0_CAP internal LDO should be decoupled with a 4.7 μF capacitor and a 0.22 μF capacitor.	Place the 0.22 μF capacitor underneath the BGA package and as close to the LDO output as possible (desired trace length < 50 mils).
	4. The VDD_USB_SS3_LDO_1P0_CAP internal LDO should be decoupled with a 2.2 μF capacitor and two 0.22 μF capacitors.	Place the 0.22 μF capacitors underneath the BGA package and as close to the LDO output as possible (desired trace length < 50 mils).
	5. VDD_TMPR_CSI_1P8_3P3 must be connected to different power supplies, depending on the use case.	Connect VDD_TMPR_CSI_1P8_3P3 to: • VDD_SNVS_LDO_1P8_CAP when tamper is used. • A 1.8 V or 3.3V I/O supply (depending on the I/O level needed) when the I/O is used for GPIO or SAI functions. When the I/O pins are not

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Table 10. i.MX8 DXL power/decoupling recommendations...*continued*

Checkbox	Recommendation	Explanation/Supplemental Recommendation
		used, VDD_TMPR_CSI_1P8_3P3 can be left unconnected.

Table 11. Capacitor recommendations to be placed near i.MX8 QM[2]

Checkbox	Supply	1 µF	2.2 µF	22 µF	100 µF	Notes
	VDD_DDR_CH0_VDDQ VDD_DDR_CH0_VDDQ_CKE		6	2	---	2.2 µF caps should be placed under the BGA package.
	VDD_DDR_CH0_VDDA_PLL_1P8		2			This rail should be sourced from the main 1.8 V rail through a 120 Ω ferrite bead.
	VDD_DDR_CH1_VDDQ VDD_DDR_CH1_VDDQ_CKE		6	2	---	2.2 µF caps should be placed under the BGA package.
	VDD_DDR_CH1_VDDA_PLL_1P8		2			This rail should be sourced from the main 1.8 V rail through a 120 Ω ferrite bead.
	VDD_A53		5	---	2	2.2 µF caps should be placed under the BGA package.
	VDD_A72		5	---	3	2.2 µF caps should be placed under the BGA package.
	VDD_GPU0		6	---	3	2.2 µF caps should be placed under the BGA package.
	VDD_GPU1		6	---	3	2.2 µF caps should be placed under the BGA package.
	VDD_MEMC		6	---	3	2.2 µF caps should be placed under the BGA package.
	VDD_MAIN		13	---	2	2.2 µF caps should be placed under the BGA package.
	VDD_LVDS0_1P0 VDD_LVDS1_1P0 VDD_MIPI_CSI0_1P0 VDD_MIPI_CSI1_1P0 VDD_MIPI_DSI0_1P0 VDD_MIPI_DSI1_1P0 VDD_MIPI_DSI0_PLL_1P0 VDD_MIPI_DSI1_PLL_1P0		5	1	---	These 8 balls are tied to the VDD_MAIN supply and filtered as shown (see the development platform schematic and Section 3.11).
	VDD_SCU_XTAL _1P8	---	---	---	---	Place a 0.22 µF cap under the BGA package.
	VDD_ANAn_1P8 VDD_SCU_1P8_n VDD_SCU_ANA_1P8 VDD_CP_1P8		6	---	---	2.2 µF caps should be placed under the BGA package.
	VDD_M1P8_CAP	---	1	---	---	Placed under the BGA package.
	VREFH_ADC VDD_ANA0_1P8_n VDD_ADC_1P8 VDD_MIPI_CSIn_1P8 VDD_MIPI_		8	---	2	These 19 balls are tied to the 1.8 V SMPS supply through dual 120 Ω ferrite beads and filtered as shown

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Table 11. Capacitor recommendations to be placed near i.MX8 QM[2] *...continued*

Checkbox	Supply	1 µF	2.2 µF	22 µF	100 µF	Notes
	DSIn_1P8 VDD_LVDSn_1 P8 VDD_MLB_1P8 (Note 4) VDD_PCIEn_PLL_1P8 VDD_PCIE_ SATA0_PLL_1P8 VDD_PCIE_IOB_ 1P8 VDD_PCIE_LDO_1P8 VDD_ USB_HSIC0_1P8 VDD_HDMI_ RX0_1P8 VDD_HDMI_TX0_1P8					(see the i.MX8QM LPDDR4 MEK schematic for illustration). Place the eight 2.2 µF caps under the BGA package.
	VDD_HDMI_TX0_1P0 VDD_ HDMI_TX0_ LDO_1P0_CAP		2	---	---	Balls AW15 and AV16 of the processor.
	VDD_HDMI_RX0_LDOn_ 1P0_CAP		4	---	---	Balls AU19 and AU21 of processor (2 x 2.2 µF per ball).
	VDD_PCIE_LDO_1P0_CAP VDD_PCIEn_1P0 VDD_PCIE_SATA0_1P0		2	---	---	Balls N29, M26, N25, and N24, respectively to the processor.
	VDD_USB_SS3_LDO_ 1P0_CAP VDD_USB_OTGn_1P0		3	---	---	Balls M30, M32, and N31, respectively to the processor. Place two caps under the BGA package.
	VDD_SNVS_4P2	---	---	---	---	Ball AT38, use 0.22 µF.
	VDD_SNVS_LDO_1P8_CAP	---	1	---	---	Ball AW39.
	VDD_USB_HSIC0_1P2		1	---	---	Ball V26.
	VDD_SIM0_1P8_3P3	1	---	---	---	Ball AK42.
	VDD_USDHC1_1P8_3P3_n	1	---	---	---	Balls M36 and N37.
	VDD_USDHC2_1P8_3P3_1	1	---	---	---	Ball M38.
	VDD_ENET0_1P8_2P5_3P3_n		1	---	---	Balls M40 and N39.
	VDD_ENET1_1P8_2P5_3P3	1	---	---	---	Ball T38.
	VDD_HDMI_RX0_VH_RX_3P3 VDD_USB_OTG1_3P3 VDD_USB_OTG2_3P3	2	1	---	---	These three balls should be filtered through a 120 Ω ferrite bead. Place the two 1 µF caps under the BGA package.
	VDD_ENET_MDIO_1P8_2P5_3P3	1	---	---	---	Ball N17 (if connected to the main 1.8 V or 3.3 V, this ball would fall into the digital power group below).
	VDD_EMMC0_1P8_3P3 VDD_PCIE_DIG_1P8_3P3 VDD_LVDS_DIG_1P8_3P3 VDD_MIPI_DSI_DIG_1P8_3P3 VDD_QSPI0_1P8_3P3 VDD_QSPI1A_1P8_3P3 VDD_MLB_DIG_1P8_3P3 (Note 5) VDD_M4_GPT_UART_1P8_3P3_n VDD_SPI_SAI_1P8_3P3_n VDD_ESAI0_MCLK_1P8_3P3_ n VDD_ESAI1_SPDIF_SPI_1P8_ 3P3 VDD_FLEXCAN_1P8_3P3 VDD_USDHC_VSELECT_1P8_3P3	Digital Power, see note				These power balls can be connected to either 1.8 V or 3.3 V, depending on the specific design. The exact number of caps on each rail (1.8 V or 3.3 V) will be dependent on the number of balls connected to that rail, but there should be a cap for every 1-2 balls and each ball should have a capacitor relatively close to it.

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Table 11. Capacitor recommendations to be placed near i.MX8 QM[2] *...continued*

Checkbox	Supply	1 µF	2.2 µF	22 µF	100 µF	Notes
Note 1: All capacitors in MEK use the X7S or X7R grades. Note 2: For PMIC capacitor recommendations, see the PMIC data sheet. Note 3: Recommended capacitor placement used in the NXP i.MX8QM MEK Customer Board. Note 4: MLB is not supported on this product. This MLB power rail may be tied to the power supply voltage indicated or terminated per the Hardware Developer's Guide and power supplies of unused functions. Note 5: MLB is not supported on this product. The MLB power rail must be tied to the power supply voltage indicated if other I/O functions are used as determined by the IOMUX selection. Alternately, terminate the MLB supply per the Hardware Developer's Guide and power supplies of unused functions.						

See the i.MX8QXP LPDDR4 MEK layout for recommended capacitor placement.

Table 12. Capacitor recommendations to be placed near i.MX8 QXP[2]

Checkbox	Supply	0.22 µF	1 µF	2.2 µF	10 µF	22 µF	Notes
	VDD_DDR_VDDQ	8	2	9	---	3	
	VDD_MAIN	---	---	12	6	4	
	VDD_A35	3	2	7	3	4	
	VDD_GPU			11	3	4	
	VDD_MIPI_1P0	---	---	1	---	---	These two balls (AD18 and AE19) are connected to the VDD_MAIN rail, so there are 13 2.2 µF caps on VDD_MAIN.
	VDD_ANA0_1P8	1	---	1	---	---	
	VDD_ANA1_1P8	1	---	1	---	---	Through LRC filter (see the development platform schematic).
	VDD_SNVS_4P2	2	---	---	---	---	
	VDD_SNVS_LDO_1P8_CAP	1	---	1	---	---	-
	VDD_CAN_UART_1P8_3P3	2	---	---	---	---	
	VDD_ESAI_SPDIF_1P8_2P5_3P3	2	---	---	---	---	
	VDD_SPI_SAI_1P8_3P3	2	---	---	---	---	
	VDD_SPI_MCLK_UART_1P8_3P3	2	---	---	---	---	
	VDD_ADC_DIG_1P8	2	---	---	---	---	
	VDD_ADC_1P8 ADC_VREFH	3	---		---	---	Supply through one 120 Ω ferrite bead.
	VDD_MIPI_1P8_n	2	---	1	---	---	Supply through one 120 Ω ferrite bead.
	VDD_MIPI_DSI_DIG_1P8_3P3	2	---	---	---	---	
	VDD_MIPI_CSI_DIG_1P8	2	---	---	---	---	
	VDD_TMPR_CSI_1P8_3P3	1	---	---	---	---	
	VDD_CSI_1P8_3P3	4	---	---	---	---	Supply through one 120 Ω ferrite bead.

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Table 12. Capacitor recommendations to be placed near i.MX8 QXP[2]...*continued*

Checkbox	Supply	0.22 µF	1 µF	2.2 µF	10 µF	22 µF	Notes
	VDD_DDR_PLL_1P8	1	1	---	1	---	Supply through one 120 Ω ferrite bead.
	VDD_USDHC1_1P8_3P3	1	---	---	---	---	2 x 0.1 uF or 1 x 0.22 uF.
	VDD_USDHC1_VSELECT_1P8_3P3	2	---	---	---	---	
	VDD_EMMC0_1P8_3P3	1	---	---	---	---	
	VDD_EMMC0_VSELECT_1P8_3P3	1	---	---	---	---	
	VDD_QSPI0A_1P8_3P3	2	---	---	---	---	
	VDD_QSPI0B_1P8_3P3	2	---	---	---	---	
	VDD_ENET0_VSELECT_ 1P8_2P5_3P3	1	---	---	---	---	
	VDD_ENET0_1P8_2P5_3P3	2	---	---	---	---	
	VDD_ENET_MDIO_1P8_3P3	2	---	1	---	---	
	VDD_PCIE_1P8	2	---	1	---	---	Supply through a 120 Ω ferrite bead.
	VDD_PCIE_LDO_1P0_CAP	1	---	1	---	---	
	VDD_PCIE_DIG_1P8_3P3	2	---	---	---	---	
	VDD_USB_SS3_LDO_1P0_ CAP VDD_USB_OTG_1P0	2	---	1	---	---	
	VDD_USB_1P8	2	---	1	---	---	Supply through one 120 Ω ferrite bead.
	VDD_USB_3P3	2	---	1	---	---	
Note 1: All capacitors in MEK use the X7S or X7R grades. Note 2: For PMIC capacitor recommendations, see the PMIC data sheet.							

Table 13. Capacitor recommendations to be placed near i.MX8 DXL[2]

Checkbox	Supply	0.22 µF	1 µF	2.2 µF	10 µF	22 µF	Notes
	VDD_DDR_VDDQ	4 (3*)	1*	4 (3*)	---	3	
	VDD_MAIN	---	---	13 (11*)	6	4	
	VDD_MEMC			12 (7*)	1	2	
	VDD_ANA0_1P8	1*	---	1	---	---	Through LRC filter (see the development platform schematic)
	VDD_ANA1_1P8	1*	---	1	---	---	Through LRC filter (see the development platform schematic)

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Table 13. Capacitor recommendations to be placed near i.MX8 DXL[2] *...continued*

Checkbox	Supply	0.22 µF	1 µF	2.2 µF	10 µF	22 µF	Notes
	VDD_SNVS_4P2	2*	---	---	---	---	
	VDD_SNVS_LDO_1P8_CAP	1*	---	1	---	---	
	VDD_CAN_UART_1P8_3P3	2 (1*)	---	---	---	---	
	VDD_ESAI_SPDIF_1P8_3P3	3 (2*)	---	---	---	---	
	VDD_SPI_SAI_1P8_3P3	2*	---	---	---	---	
	VDD_SPI_MCLK_UART_1P8_3P3	2*	---	---	---	---	
	VDD_ADC_DIG_1P8	2	---	---	---	---	
	VDD_ADC_1P8 ADC_VREFH	3*	---		---	---	Supply through one 120 Ω ferrite bead
	VDD_TMPR_CSI_1P8_3P3	1*	---	---	---	---	
	VDD_CSI_1P8_3P3	4 (1*)	---	---	---	---	Supply through one 120 Ω ferrite bead
	VDD_DDR_PLL_1P8	1*	1*	---	1	---	Supply through one 120 Ω ferrite bead
	VDD_USDHC1_VSELECT_1P8_3P3	2*	---	---	---	---	
	VDD_EMMC0_1P8_3P3	2*	---	---	---	---	
	VDD_QSPI0A_1P8_3P3	2*	---	---	---	---	
	VDD_QSPI0B_1P8_3P3	2 (1*)	---	---	---	---	
	VDD_ENET0_VSELECT_1P8_3P3	2	---	---	---	---	
	VDD_ENET0_1P8_3P3	2	---	---	---	---	
	VDD_ENET_MDIO_1P8_3P3	2	---	---	---	---	
	VDD_PCIE_1P8	2 (1*)	---	1	---	---	Supply through one 120 Ω ferrite bead
	VDD_PCIE_LDO_1P0_CAP	1*	---	1*	---	---	
	VDD_PCIE_DIG_1P8_3P3	2 (1*)	---	---	---	---	
	VDD_USB_SS3_LDO_1P0_CAP	2	---	1	---	---	
	VDD_USB_1P8	3	---	---	---	---	Supply through one 120 Ω ferrite bead

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Table 13. Capacitor recommendations to be placed near i.MX8 DXL[2] *...continued*

Checkbox	Supply	0.22 µF	1 µF	2.2 µF	10 µF	22 µF	Notes
	VDD_USB_3P3	2	---	1	---	---	Supply through one 120 Ω ferrite bead

* From total, place this amount under the chip. The rest can be placed around the chip.

Table 14. PCIe recommendations

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. The reference clock source should have a HCSL (High-Speed Current-Steering Logic) differential output. Resistors of approximately 50 Ω are required to terminate both traces to GND. Do not AC couple this clock. ***Note:*** *i.MX6 processors used LVDS outputs for the PCIe interface. The connection requirements are different for this SOC.*	The NXP development platform board design uses a Micrel DSC557 device. However, NXP does not recommend one supplier over another and it does not suggest that this is the only clock generator supplier. The particular device used should support all specifications (jitter, accuracy, and so on.) The internal PCIe reference clock is good for all standard PCIe applications. The clock may be connected to one or two external devices (depending on location). Use a buffer, distributor, or external clock reference for additional PCIe destinations. The internal PCIe reference clock is not spread spectrum capable. For EMC/EMI sensitive applications, it is recommended to use an external reference clock source.
	2. The default DFE setting may not be suitable for PCIe Gen2 -3.5dB TX de-emphasis in case of lossy channels.	For this case, NXP recommends a higher DFE setting with these modifications in the PCIe PHY registers: 1. Enable the override for the default behavior: force A1 Gain (reg241).A1_force = 1b1. 2. Set a suitable value in force A1 Gain (reg241).A1_init. NXP suggests a starting value of 0xB for jitter tolerance margin. Optimize this value for your design.
	3. The differential transmitters from the processor must be AC coupled. Use a 0.22 µF capacitor on both the PCIE_TXP and PCIE_TXN outputs.	The PCIe specification compliance requires AC coupling at each transmitter. The receiver must be DC coupled.
	4. The PCIE_REF_QR ball should be connected to ground through a 453 Ω, 1 % resistor.	This signal is ball E23 on the i.MX8 QM, ball F12 on the i.MX8 QXP, and ball G11 on the i.MX8 DXL.
	5. The PCIE_REXT ball should be connected to the PCIE0_PHY_PLL_REF_RETURN ball through an 845 Ω, 0.5 % resistor.	PCIE_REXT is ball D22 (QM), H12 (QXP), and G9 (DXL). PCIE_PHY_PLL_REF_RETURN is ball M28 (QM), ball G11 (QXP), and ball J11 (DXL). ***Note:*** *The i.MX8 processor packages route the PCIe RX and TX data pairs (including SATA) as 85 Ω differential impedance traces. NXP recommends routing PCB differential traces to match. See Section 3.7 for more details.*
	6. PCIE_SATA0_PHY_PLL_REF_RETURN, PCIE0_ PHY_PLL_REF_RETURN and PCIE1_PHY_PLL_REF_	See the i.MX8QM LPDDR4 MEK for the correct implementation.

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Table 14. PCIe recommendations*...continued*

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	RETURN should be connected to VDD_PCIE_1V8 by 0.22 µF capacitors (8QM).	
	7. PCIE0_PHY_PLL_REF_RETURN should be connected to VDD_PCIE_1V8 by 0.22 µF and 22 µF capacitors in case of 8QXP and by 0.47 µF and 47 µF capacitors in case of 8DXL.	See the i.MX8QXP LPDDR4 MEK/i.MX8DXL LPDDR4 EVK for the correct implementation.

Table 15. USB recommendations

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. To comply with the USB OTG specification, the VBUS supply to the OTG connector should default to off when the board powers up.	The processor should turn on VBUS if required.
	2. Connect a 499 Ω, 1 % resistor to ground on the USB_OTG2_REXT ball (ball E29 on QM and ball D14 on QXP.	
	3. Connect a 499 Ω, 1 % resistor to ground on the USB_SS3_REXT ball (ball E27 on QM, ball E13 on QXP).	Not applicable on DXL.
	4. If using USB1 OTG, connect USB_OTG1_VBUS (ball A39 on QM, ball H18 on QXP, and ball G17 on DXL) to the 5 V OTG connector VBUS.	If unused, leave VBUS unconnected.
	5. If using USB_OTG2, connect USB_OTG2_ VBUS via a resistive voltage divider to the VBUS pin of the connector such that the 5.5 V VBUS voltage is reduced to 3.3 V On QM (ball A35) and QXP (ball H16). On DXL, connect USB_OTG2_ VBUS (ball G13) to the 5 V OTG connector VBUS.	On QM and QXP, the OTG1 and OTG2 interfaces are implemented differently, and while the OTG1 VBUS ball is 5 V tolerant, the OTG2 VBUS ball is not. On DXL, both OTG VBUS balls are 5 V tolerant.
	6. Route all USB differential signals with 90 Ω differential impedance.	USB_OTG1 is not compatible with the SS interface.
	7. ESD protection should be implemented at the connector pins. Choose a low-capacitance device recommended for high-speed interfaces.	This will prevent potential damage to board components from ESD.

Table 16. HDMI recommendations (i.MX8 QM only)

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. Connect a 499 Ω, 1 % resistor to ground on the HDMI_RX0_REXT ball (ball BJ11).	
	2. Connect a 499 Ω, 1 % resistor to ground on the HDMI_TX0_REXT ball (ball BJ7).	
	3. Route all HDMI receive and transmit differential pairs with 100 Ω differential impedance.	
	4. To provide a DisplayPort output on the i.MX8 QM Display TX output, follow the implementation details in Section 3.13.	

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Table 16. HDMI recommendations (i.MX8 QM only)*...continued*

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	5. To provide an HDMI output on the i.MX8 QM Display TX output, follow the implementation details in Section 3.13.	
	6. The HDMI_TX0_CEC trace must be pulled up to the VCC_3V3 rail through a 27 k Ω resistor in series with a Schottky diode.	

Table 17. Oscillator/crystal recommendations

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. Connect a 32.768 KHz crystal between RTC_XTALI and RTC_XTALO.	For ESR selection, negative resistance / ESR and drive level must be considered at the same time. See the processor datasheet for the general crystal requirements. Follow the manufacturer's recommendation for loading capacitance. Use short traces between the crystal and the processor, with a ground plane under the crystal, load capacitors, and associated traces. Internal load capacitors should be used. See Section 3.9.3.
	2. Instead of a crystal, the i.MX8 QM/QXP/DXL 32.768 KHz can be driven with an external clock (oscillator) driven into the RTC_XTALI input (RTC_XTALO floated).	The voltage level of this driving clock should not exceed the voltage of the VDD_SNVS_LDO_1P8_CAP rail and the frequency should be <100 KHz under typical conditions. Do not exceed VDD_SNVS_LDO_1P8_CAP or damage/malfunction may occur. The RTC_XTALI signal should not be driven if the VDD_SNVS_CAP supply is off. This can lead to damage or malfunction. For the RTC_XTALI VIL and VIH voltage levels, see the latest i.MX8 QM, i.MX 8QXP, and i.MX 8DXL datasheet available at www.nxp.com.
	3. Connect a 24.00 MHz crystal between XTALI and XTALO.	For ESR selection, negative resistance / ESR and drive level must be considered at the same time. See the processor datasheet for the general crystal requirements. Internal load capacitors should be used. See Section 3.9.3.
	4. VSS_SCU_XTAL considerations	Follow the implementation of the associated development platform. If it is desired to further reduce oscillator noise, VSS_SCU_XTAL pins can be separated from VSS_MAIN. ***Note:*** *For 8DXL, the equivalent of VSS_SCU_XTAL is ball AL27.*

Table 18. SD card recommendations

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. If booting from SD card is needed, connect a 10 kΩ pull-up resistor to the uSDHC reset signal (8DXL).	The external pull-up resistor is needed to support booting from the SD card on 8DXL, because the ROM code (by default) enables internal pull-down on the reset pin. This is because the default function of the pin is ENET0_RMII_TX_CTL. The board initialization

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Table 18. SD card recommendations

Checkbox	Recommendation	Explanation/Supplemental Recommendation
		software should disable the internal pull-down to avoid power leakage.

Table 19. Tamper pin recommendations (i.MX 8DXL)

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	1. TAMPER_IN0-3 and TAMPER_OUT1-4 pins can only be configured as a group.	All the pins can be used either as tamper pins or as GPIO pins. Mixed configurations, where some of the pins serve as tamper pins and some of the pins serve as GPIOs, are not supported. When configured as GPIOs, the pins can only be used as inputs. See Table 8 for the associated power supply requirements and AN13365 for more details.

Table 20. SIM Card recommendations (i.MX 8QM)

Checkbox	Recommendation	Explanation/Supplemental Recommendation
	Connect a 20-kΩ pull-up resistor to VDD_SIM0_1P8_3P3 on SIM0_IO (ball AN45).	The on-chip pull-up resistor is too weak for the SIM. Ensure that the on-chip pull-up resistor is disabled when an external resistor is used. The SIM specification recommends a 20-kΩ pull-up resistor.

2.2 JTAG signal termination

Table 21 is a JTAG termination chart showing what terminations should be placed on PCB designs.

Table 21. Recommended JTAG board terminations

JTAG Signal	I/O Type	External Termination	Comment
JTAG_TCK	Input	10 kΩ pull-down	
JTAG_TMS	Input	10 kΩ pull-up	
JTAG_TDI	Input	10 kΩ pull-up	
JTAG_TDO	3-state output	None	
JTAG_TRSTB*	Input	10 kΩ pull-up	No connection from the JTAG to the processor.

* Not available on i.MX8 QXP and i.MX8 DXL

3 i.MX8 layout/routing recommendations

3.1 Introduction

This chapter provides recommendations to assist design engineers with the layout of i.MX8 QM, i.MX8 QXP, or i.MX8 DXL systems.

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3.2 Basic design recommendations

When using the Allegro design tool, it is recommended to use the schematic symbol and PCB footprint created by NXP. When not using the Allegro tool, use the Allegro footprint export feature (supported by many tools). If the export is not possible, create the footprint per the package dimensions outlined in the product data sheet.

The native Allegro layout and gerber files are available on www.nxp.com.

3.2.1 Placing decoupling capacitors

Place small decoupling and larger bulk capacitors on the bottom side of the PCB.

The 0201 or 0402 decoupling and 0603 (or larger) bulk capacitors should be mounted as close as possible to the power vias. The distance should be less than 50 mils. Additional bulk capacitors can be placed near the edge of the BGA via array. Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure high-speed transient current required by the processor. See the i.MX8 QM, i.MX8 QXP, and i.MX8 DXL development platform layouts for examples of the desired decoupling capacitor placement.

Correct via size is critical for preserving adequate routing space. The recommended geometry for the via and pads on an i.MX8 QM design is a metric 45r20 via (0.2 mm drill, 0.45 mm annular ring), while for i.MX8 QXP and i.MX8DXL designs, it is an imperial 18r10 via (10 mil drill, 18 mil annular ring). An 18r8 via may also be used.

The following list provides the main recommendations for choosing the correct decoupling scheme:

- Place the largest capacitance in the smallest package that the budget and manufacturing can support.
- For high-speed bypassing, select the required capacitance with the smallest package (for example, 0.1 μF, 0.22 μF, 1.0 μF, 2.2 μF, or even 4.7 μF in an 0201 package size).
- Minimize the trace length (inductance) to small caps.
- Series inductance cancels out capacitance.
- Tie caps to GND plane directly with a via.
- Place capacitors close to the power ball of the associated package from the schematic.
- A preferred BGA power decoupling design is available on the development platform board design available on www.nxp.com. Customers should use the NXP design strategy for power and decoupling.

Note: *NXP uses 0402 capacitors in its customer designs as an example for customers who may not be able to use 0201 components. Nevertheless, NXP recommends using 0201 capacitor where possible: 0201 capacitors have less package inductance and the number of capacitors placed underneath the processor can be increased.*

3.3 Stack-up recommendations

3.3.1 Stack-up recommendation (i.MX8 QM)

Due to the number of balls on the i.MX 8QM processor in the 29 mm x 29 mm package, it is recommended to use a minimum 12-layer PCB stack-up. Of the 12-layers on the PCB, a sufficient number of layers must be dedicated to power routing to ensure the IR drop target of 1 % for the i.MX8 QM CPU power rails is met.

The constraints for the trace width depend on a number of factors, such as the board stack-up and associated dielectric and copper thickness, required impedance, and required current (for power traces). The stack-up also determines the constraints for routing and spacing. Consider the following when designing the stack-up and selecting board material:

- Board stack-up is critical for high-speed signal quality.
- Preplanning impedance of critical traces is required.
- High-speed signals must have reference planes on adjacent layers to minimize crosstalk.

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- Use PCB materials that have good transmission qualities at high frequencies utilized by the i.MX8 QM interfaces. The NXP i.MX8 QM customer platform utilizes Megtron 6.

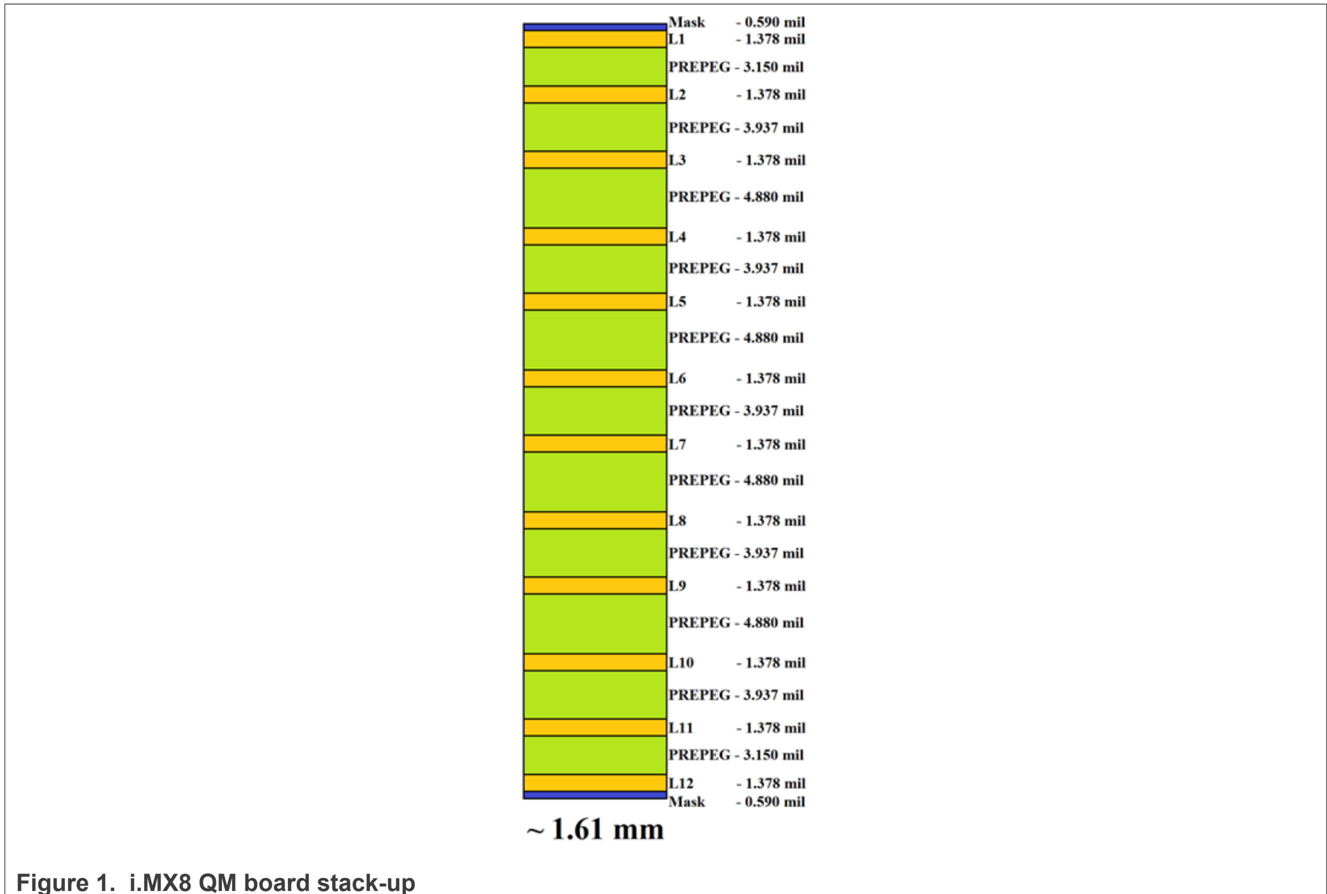

Figure 1. i.MX8 QM board stack-up

3.3.2 Stack-up recommendation (i.MX8 QXP)

For the i.MX 8QXP processor in the 21 mm x 21 mm package, it is recommended to use a minimum 8-layer PCB stack-up. Of the eight layers on the PCB, a sufficient number of layers must be dedicated to power routing to ensure that the IR drop target of 1 % for the i.MX8 QXP CPU power rails is met. The Cu foil thickness of the power routing layers may be increased to provide additional current carrying capacity.

Consider the following when designing the stack-up and selecting board material:

- Board stack-up is critical for high-speed signal quality.
- Preplanning impedance of critical traces is required.
- High-speed signals must have reference planes on adjacent layers to minimize crosstalk.
- Use PCB materials that have good transmission qualities at high frequencies utilized by the i.MX8 QXP interfaces. The NXP i.MX8 QXP customer platform utilizes TU-872SLK Sp.

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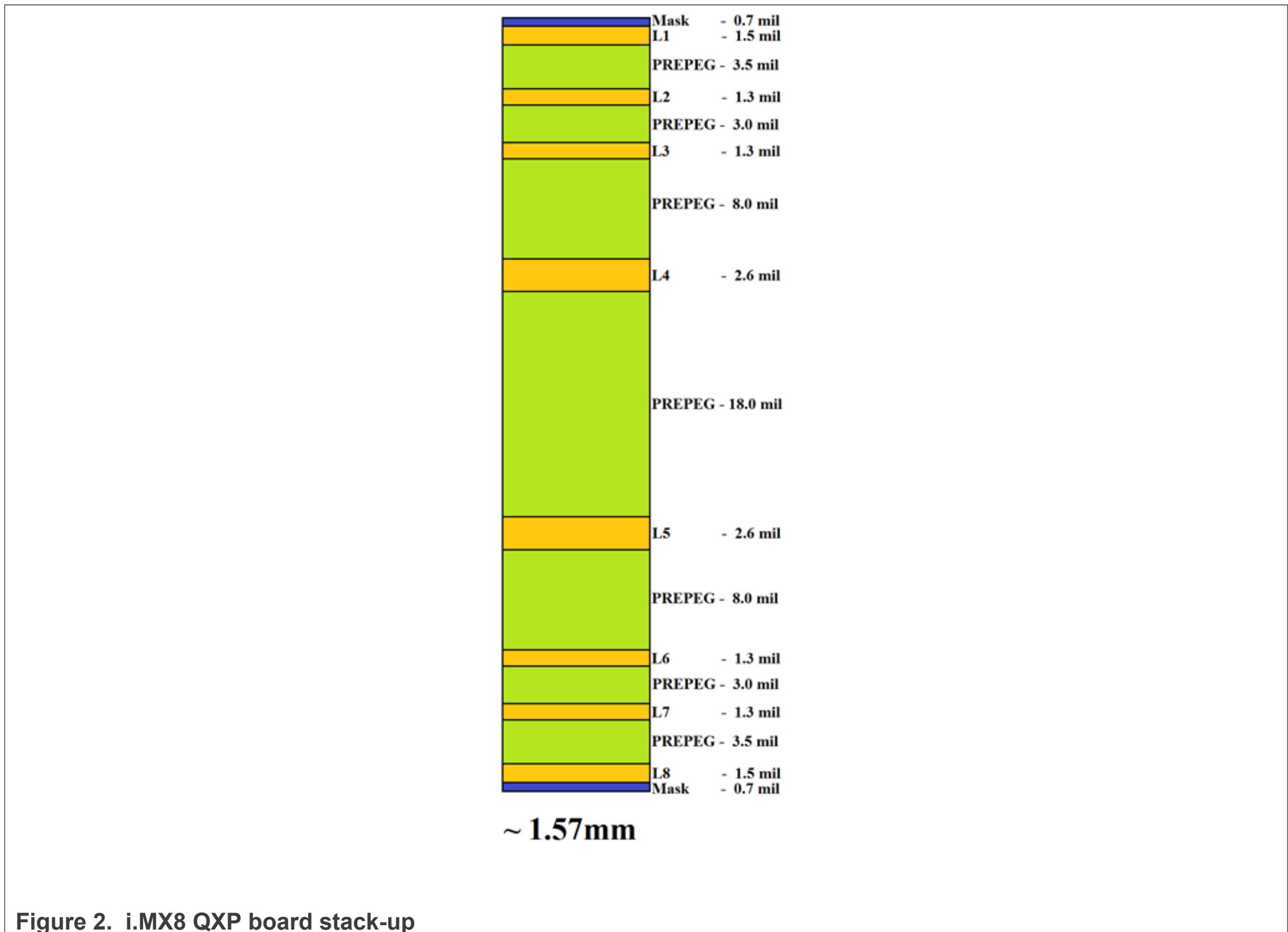

Figure 2. i.MX8 QXP board stack-up

3.3.3 Stack-up recommendation (i.MX8 DXL)

For the i.MX 8DXL processor in the 15 mm x 15 mm package, it is recommended to use at least an 8-layer PCB stack-up. Of the eight layers on the PCB, a sufficient number of layers must be dedicated to power routing to ensure that the IR drop target of 1 % for the i.MX8 DXL CPU power rails is met. The Cu foil thickness of the power-routing layers may be increased to provide additional current-carrying capacity.

Consider the following when designing the stack-up and selecting the board material:

- Board stack-up is critical for high-speed signal quality.
- Preplanning of impedance of critical traces is required.
- High-speed signals must have reference planes on adjacent layers to minimize cross-talk.
- Use PCB materials that have good transmission qualities at high frequencies utilized by the i.MX8 DXL interfaces. The NXP i.MX8 DXL customer platform utilizes Megtron 4.

Note: *The i.MX 8DXL LPDDR4 EVK board utilizes a 12-layer stack-up to support complex power-consumption measurements. For customer designs, the number of layers can be reduced to 8 and the i.MX8QXP MEK board stack-up can be used (see Figure 2).*

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3.4 DDR layout routing recommendations

3.4.1 DDR pin naming

The i.MX8 QXP processor can be used with either the LPDDR4 memory or the DDR3L memory. The i.MX8 DXL processor can be used with either the LPDDR4 memory or the DDR3L memory. The iMX8 QM processor can be used with the LPDDR4 memory. Because these memory types have different I/O signals, there are 33 generically named balls that have different functions, depending on the type of memory used. See Table 22 for the connectivity of these generic balls for DDR3L (QXP and DXL only) and LPDDR4 (QXP, DXL, and 8QM). This table represents all three processors, and the two columns shown in the "QM Ball #" field are the ball numbers for channel 0 and channel 1 balls, respectively.

Table 22. DDR3L/LPDDR4 connectivity

Ball Name	QXP Ball #	DXL Ball #	QM Ball #		DDR3L function (QXP)	DDR3L function (DXL)	LPDDR4 function (QM, QXP)	LPDDR4 function (DXL)
DDR_ DCF00	W1	N1	U47	U7	A5	A5	CA2_A	CA2_A
DDR_ DCF01	U3	J1	W47	W7	A6	A6	CA4_A	CA4_A
DDR_ DCF02	-----	-----	Y48	Y6	-----	-----	-----	-----
DDR_ DCF03	U1	J3	Y46	Y8	A7	A7	CA5_A	CA5_A
DDR_ DCF04	U7	A7	W43	W11	A8	A8	-----	-----
DDR_ DCF05	U5	M2	Y44	Y10	A9	A9	-----	-----
DDR_ DCF06	-----	-----	W45	W9	-----	-----	-----	-----
DDR_ DCF07	T2	Y2	W51	W3	RAS#	RAS#	-----	-----
DDR_ DCF08	AB4	N3	T48	T6	A3	A3	CA3_A	CA3_A
DDR_ DCF09	AB6	A5	T52	T2	ODT0	ODT0	-----	-----
DDR_ DCF10	AC5	R1	T50	T4	A1	A1	CS0_A	CS0_A
DDR_ DCF11	W3	W1	U51	U3	A0	A0	CA0_A	CA0_A
DDR_ DCF12	Y8	U3	U49	U5	A2	A2	CS1_A	CS1_A
DDR_ DCF13	-----	-----	T46	T8	-----	-----	-----	-----
DDR_ DCF14	Y2	T2	W53	W1	-----	-----	CKE0_A	CKE0_A
DDR_ DCF15	Y4	P2	Y52	Y2	-----	-----	CKE1_A	CKE1_A

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Table 22. DDR3L/LPDDR4 connectivity*...continued*

Ball Name	QXP Ball #	DXL Ball #	QM Ball #		DDR3L function (QXP)	DDR3L function (DXL)	LPDDR4 function (QM, QXP)	LPDDR4 function (DXL)
DDR_ DCF16	W7	U1	U53	U1	A4	A4	CA1_A	CA1_A
DDR_ DCF17	N3	B4	AC47	AC7	A12	A12	CA4_B	-----
DDR_ DCF18	L1	H2	AB48	AB6	RESET_N	RESET_N	RESET_N	RESET_N
DDR_ DCF19	N1	B6	AB46	AB8	A14	A14	CA5_B	-----
DDR_ DCF20	P4	B2	AC43	AC11	A15	A15	-----	-----
DDR_ DCF21	T8	V2	AE45	AE9	BA0	BA0	-----	-----
DDR_ DCF22	P2	A3	AC51	AC3	BA1	BA1	-----	-----
DDR_ DCF23	T4	F2	AC45	AC9	BA2	BA2	-----	-----
DDR_ DCF24	T6	E1	AB44	AB10	CAS#	CAS#	-----	-----
DDR_ DCF25	K8	-----	AF52	AF2	ODT1	-----	-----	-----
DDR_ DCF26	L7	G1	AE47	AE7	A13	A13	CA3_B	-----
DDR_ DCF27	K4	E3	AE51	AE3	A10	A10	CA0_B	-----
DDR_ DCF28	K6	J7	AF50	AF4	CS_N[0]	CS N[0]	CS0_B	-----
DDR_ DCF29	K2	-----	AE49	AE5	CS_N[1]	-----	CS1_B	-----
DDR_ DCF30	N7	L7	AC53	AC1	CKE0	CKE0	CKE0_B	-----
DDR_ DCF31	L5	-----	AB52	AB2	CKE1	-----	CKE1_B	-----
DDR_ DCF32	L3	C5	AE53	AE1	A11	A11	CA1_B	-----
DDR_ DCF33	P8	J9	AF48	AF6	WE#	WE#	CA2_B	-----

3.4.2 i.MX8 QM DDR package conductor lengths

When performing the required trace length matching for LPDDR4 routing, the bond wires within the i.MX8 QM package must be accounted for and included in the match calculation. The table below lists the lengths from each die I/O to the package ball, as well as the propagation/fly time from the die I/O to the package ball.

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Note: *The values for substrate lengths and delay time are determined by the CAD program used to design the package substrate. For simulation tools that use delay times as an input, the delay time numbers can be used, because they are more accurate. The customer must ensure that the simulation tool is properly set up for using delay times. The package trace lengths provided are exact, but no information is provided for the package substrate stack-up, so determining delay time directly from the trace length can only be done as an approximation. NXP has determined that using trace lengths with Cadence Allegro provides more consistent results.*

Table 23. i.MX8 QM DDR 29 x 29 mm package trace lengths

Ball Name	Length (microns)	XIM delay (ps)	Ball Name	Length (microns)	XIM delay (ps)
DDR_CH0_CK0_N	8252.205	70.4320	DDR_CH1_CK0_N	8252.205	71.2075
DDR_CH0_CK0_P	8231.301	70.4019	DDR_CH1_CK0_P	8231.301	70.3251
DDR_CH0_CK1_N	7122.412	63.2031	DDR_CH1_CK1_N	7122.422	63.7053
DDR_CH0_CK1_P	7116.659	62.7708	DDR_CH1_CK1_P	7116.659	62.8899
DDR_CH0_DCF00	5894.518	52.5252	DDR_CH1_DCF00	5896.059	53.0091
DDR_CH0_DCF01	5369.421	50.9911	DDR_CH1_DCF01	5365.999	50.7991
DDR_CH0_DCF02	6353.172	56.8037	DDR_CH1_DCF02	6353.172	57.0927
DDR_CH0_DCF03	4959.555	44.8336	DDR_CH1_DCF03	4959.555	45.5756
DDR_CH0_DCF04	4639.406	45.3991	DDR_CH1_DCF04	4639.406	44.4202
DDR_CH0_DCF05	4734.544	44.8435	DDR_CH1_DCF05	4734.544	44.8185
DDR_CH0_DCF06	5464.536	47.6858	DDR_CH1_DCF06	5464.536	49.6408
DDR_CH0_DCF07	7733.346	65.9861	DDR_CH1_DCF07	7733.346	67.4829
DDR_CH0_DCF08	6581.169	57.5524	DDR_CH1_DCF08	6581.178	58.3514
DDR_CH0_DCF09	8442.241	71.1543	DDR_CH1_DCF09	8442.232	69.0238
DDR_CH0_DCF10	7135.477	62.1810	DDR_CH1_DCF10	7135.477	62.1676
DDR_CH0_DCF11	8034.133	68.0766	DDR_CH1_DCF11	8034.143	68.2538
DDR_CH0_DCF12	6724.164	59.1363	DDR_CH1_DCF12	6724.154	59.7347
DDR_CH0_DCF13	6036.270	52.7991	DDR_CH1_DCF13	6036.279	53.2113
DDR_CH0_DCF14	9374.566	76.0970	DDR_CH1_DCF14	9374.576	76.4025
DDR_CH0_DCF15	10184.452	82.7146	DDR_CH1_DCF15	10184.459	83.0032
DDR_CH0_DCF16	8665.398	69.7528	DDR_CH1_DCF16	8665.398	71.0229
DDR_CH0_DCF17	4831.641	45.2551	DDR_CH1_DCF17	4831.641	45.4623
DDR_CH0_DCF18	5750.691	52.8533	DDR_CH1_DCF18	5755.049	53.4975
DDR_CH0_DCF19	5318.163	49.2262	DDR_CH1_DCF19	5322.528	49.4664
DDR_CH0_DCF20	2820.533	31.5224	DDR_CH1_DCF20	2820.533	31.6700
DDR_CH0_DCF21	4433.669	41.8996	DDR_CH1_DCF21	4437.579	43.0937
DDR_CH0_DCF22	7691.037	65.7764	DDR_CH1_DCF22	7691.037	64.9914
DDR_CH0_DCF23	3776.834	37.7154	DDR_CH1_DCF23	3776.834	38.3014
DDR_CH0_DCF24	4903.692	46.4388	DDR_CH1_DCF24	4903.692	46.8339
DDR_CH0_DCF25	7584.973	65.4216	DDR_CH1_DCF25	7584.973	65.2606

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Table 23. i.MX8 QM DDR 29 x 29 mm package trace lengths*...continued*

Ball Name	Length (microns)	XIM delay (ps)	Ball Name	Length (microns)	XIM delay (ps)
DDR_CH0_DCF26	5704.160	53.1375	DDR_CH1_DCF26	5704.160	52.9999
DDR_CH0_DCF27	7410.269	63.7375	DDR_CH1_DCF27	7410.269	63.2216
DDR_CH0_DCF28	6878.795	60.3078	DDR_CH1_DCF28	6878.795	59.5766
DDR_CH0_DCF29	6259.099	56.3228	DDR_CH1_DCF29	6259.099	55.9878
DDR_CH0_DCF30	8054.345	65.6790	DDR_CH1_DCF30	8054.345	65.9667
DDR_CH0_DCF31	10000.825	83.3056	DDR_CH1_DCF31	10000.825	82.7283
DDR_CH0_DCF32	8689.205	72.0970	DDR_CH1_DCF32	8689.205	72.0274
DDR_CH0_DCF33	5597.283	50.6105	DDR_CH1_DCF33	5597.283	50.5537
DDR_CH0_DM0	9660.570	79.2537	DDR_CH1_DM0	9660.580	78.6072
DDR_CH0_DM1	5987.415	54.3347	DDR_CH1_DM1	5897.415	54.7433
DDR_CH0_DM2	5638.407	51.4494	DDR_CH1_DM2	5638.407	51.6074
DDR_CH0_DM3	8342.093	70.9267	DDR_CH1_DM3	8342.093	70.6812
DDR_CH0_DQ00	4248.491	42.2890	DDR_CH1_DQ00	4248.482	42.2313
DDR_CH0_DQ01	5110.174	47.6881	DDR_CH1_DQ01	5110.174	47.6921
DDR_CH0_DQ02	6989.995	62.0198	DDR_CH1_DQ02	6990.004	60.7041
DDR_CH0_DQ03	7468.086	64.4777	DDR_CH1_DQ03	7468.086	65.2432
DDR_CH0_DQ04	8773.313	73.1117	DDR_CH1_DQ04	8777.000	73.2824
DDR_CH0_DQ05	10282.44	82.9998	DDR_CH1_DQ05	10279.216	81.4069
DDR_CH0_DQ06	9811.696	80.6749	DDR_CH1_DQ06	9811.696	81.3402
DDR_CH0_DQ07	3974.988	39.0745	DDR_CH1_DQ07	3976.043	39.3622
DDR_CH0_DQ08	7541.890	64.3642	DDR_CH1_DQ08	7541.890	64.7117
DDR_CH0_DQ09	8384.909	70.1491	DDR_CH1_DQ09	8384.909	70.9403
DDR_CH0_DQ10	8222.123	69.6776	DDR_CH1_DQ10	8222.133	70.8199
DDR_CH0_DQ11	9030.683	76.8537	DDR_CH1_DQ11	9030.683	76.9652
DDR_CH0_DQ12	5189.988	47.4530	DDR_CH1_DQ12	5189.988	48.5738
DDR_CH0_DQ13	7209.390	63.5065	DDR_CH1_DQ13	7209.182	62.3698
DDR_CH0_DQ14	7372.008	64.1910	DDR_CH1_DQ14	7372.018	64.3040
DDR_CH0_DQ15	6487.728	58.7702	DDR_CH1_DQ15	6483.533	58.2495
DDR_CH0_DQ16	7384.314	63.7602	DDR_CH1_DQ16	7384.314	63.6592
DDR_CH0_DQ17	6432.896	57.8759	DDR_CH1_DQ17	6432.896	57.8504
DDR_CH0_DQ18	7460.646	64.7639	DDR_CH1_DQ18	7460.646	65.1017
DDR_CH0_DQ19	7400.361	63.9434	DDR_CH1_DQ19	7400.361	64.1530
DDR_CH0_DQ20	6982.343	61.7828	DDR_CH1_DQ20	6982.343	61.3076
DDR_CH0_DQ21	5041.774	47.9700	DDR_CH1_DQ21	5041.774	48.5268
DDR_CH0_DQ22	6243.134	57.8368	DDR_CH1_DQ22	6243.134	54.7315
DDR_CH0_DQ23	7123.794	61.7699	DDR_CH1_DQ23	7123.794	62.2260

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Table 23. i.MX8 QM DDR 29 x 29 mm package trace lengths*...continued*

Ball Name	Length (microns)	XIM delay (ps)	Ball Name	Length (microns)	XIM delay (ps)
DDR_CH0_DQ24	4257.179	42.5126	DDR_CH1_DQ24	4257.179	42.9151
DDR_CH0_DQ25	3236.439	34.3296	DDR_CH1_DQ25	3236.439	34.5683
DDR_CH0_DQ26	6404.608	57.1079	DDR_CH1_DQ26	6404.608	56.9504
DDR_CH0_DQ27	6032.358	55.3496	DDR_CH1_DQ27	6032.358	54.6117
DDR_CH0_DQ28	8867.673	72.0245	DDR_CH1_DQ28	8867.673	72.4703
DDR_CH0_DQ29	7490.208	65.3391	DDR_CH1_DQ29	7490.208	65.2011
DDR_CH0_DQ30	3294.308	34.4553	DDR_CH1_DQ30	3294.577	34.8851
DDR_CH0_DQ31	7885.148	68.0874	DDR_CH1_DQ31	7885.148	68.1579
DDR_CH0_DQS0_N	10907.430	87.3574	DDR_CH1_DQS0_N	10907.421	87.0990
DDR_CH0_DQS0_P	10922.363	88.4719	DDR_CH1_DQS0_P	10922.363	88.1746
DDR_CH0_DQS1_N	9643.900	78.8950	DDR_CH1_DQS1_N	9643.900	79.2363
DDR_CH0_DQS1_P	9645.091	78.7201	DDR_CH1_DQS1_P	9645.091	79.6704
DDR_CH0_DQS2_N	8747.836	73.9677	DDR_CH1_DQS2_N	8748.035	73.0549
DDR_CH0_DQS2_P	8750.730	73.3214	DDR_CH1_DQS2_P	8750.730	73.2617
DDR_CH0_DQS3_N	9174.029	75.6440	DDR_CH1_DQS3_N	9174.029	75.1700
DDR_CH0_DQS3_P	9174.778	77.2702	DDR_CH1_DQS3_P	9175.492	76.2203

3.4.3 i.MX8 QXP DDR package conductor lengths

When performing the required trace length matching for LPDDR4/DDR3L routing, the bond wires within the i.MX8 QXP package must be accounted for and included in the match calculation. Table 24 lists the lengths from each die I/O to the package ball, as well as the propagation/fly time from the die I/O to the package ball.

Note: *The values for substrate lengths and delay time are determined by the CAD program used to design the package substrate. For simulation tools that use delay times as an input, the delay time numbers can be used, because they are more accurate. The customer must ensure that the simulation tool is properly set up for using delay times. The package trace lengths provided are exact, but no information is provided for the package substrate stack-up, so determining the delay time directly from the trace length can only be done as an approximation. NXP has determined that using trace lengths with Cadence Allegro provides more consistent results.*

Table 24. i.MX8 QXP DDR 21 x 21 mm package trace lengths/delays

Ball Name	Length (microns)	XIM delay (ps)	Ball Name	Length (microns)	XIM delay (ps)
DDR_CK0_N	5767.55	45.4423	DDR_DQS3_N	11842.2	87.5602
DDR_CK0_P	5769.1	45.0604	DDR_DQS3_P	11881.8	88.0695
DDR_CK1_N	5886	46.3205	DDR_DQ00	5854.11	45.3221
DDR_CK1_P	5915.93	46.7442	DDR_DQ01	5394.75	43.6784
DDR_DCF00	6986.18	54.3919	DDR_DQ02	6342.16	50.0838
DDR_DCF01	6571.69	50.4883	DDR_DQ03	5295.38	42.5401
DDR_DCF03	7028.2	54.2384	DDR_DQ04	8801.75	66.9252

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Table 24. i.MX8 QXP DDR 21 x 21 mm package trace lengths/delays*...continued*

Ball Name	Length (microns)	XIM delay (ps)	Ball Name	Length (microns)	XIM delay (ps)
DDR_DCF04	4753	38.5093	DDR_DQ05	9059.98	67.8974
DDR_DCF05	5206.58	40.8504	DDR_DQ06	7946.05	61.2384
DDR_DCF07	6575.27	50.6632	DDR_DQ07	8184.38	62.4339
DDR_DCF08	5858.04	46.7262	DDR_DQ08	9165.63	69.5853
DDR_DCF09	5524.3	44.5018	DDR_DQ09	8400.91	63.702
DDR_DCF10	6853.59	53.6322	DDR_DQ10	8597.51	64.9578
DDR_DCF11	6790.65	52.6494	DDR_DQ11	7845.62	60.7429
DDR_DCF12	4640.87	37.0673	DDR_DQ12	6704.62	51.7953
DDR_DCF14	7425.57	57.2044	DDR_DQ13	7313	56.3702
DDR_DCF15	6488.67	50.7055	DDR_DQ14	7311.64	56.0756
DDR_DCF16	4278.94	35.65	DDR_DQ15	8095.44	62.3991
DDR_DCF17	6835.25	52.3421	DDR_DQ16	9902.43	73.7108
DDR_DCF18	8802.86	66.1865	DDR_DQ17	8170.79	63.8656
DDR_DCF19	7923.69	60.3259	DDR_DQ18	7585.53	58.9951
DDR_DCF20	6384.93	49.2981	DDR_DQ19	8721.6	66.4481
DDR_DCF21	4281.75	35.3493	DDR_DQ20	7733.88	59.4337
DDR_DCF22	7341.69	55.6365	DDR_DQ21	8134.63	61.4536
DDR_DCF23	5443.42	43.8914	DDR_DQ22	6867.58	53.8569
DDR_DCF24	5213.64	41.3148	DDR_DQ23	7483.71	57.6748
DDR_DCF25	6389.06	50.0117	DDR_DQ24	12396.4	91.455
DDR_DCF26	5323.56	43.9052	DDR_DQ25	12086.1	90.1234
DDR_DCF27	6966.31	53.0627	DDR_DQ26	11689.6	86.6571
DDR_DCF28	6484.39	50.4087	DDR_DQ27	12943.3	94.8301
DDR_DCF29	7756.88	58.7207	DDR_DQ28	8532.32	64.2572
DDR_DCF30	4057.33	33.5742	DDR_DQ29	9663.79	71.9756
DDR_DCF31	6973.54	54.6613	DDR_DQ30	10704.9	78.4097
DDR_DCF32	7058.2	54.0296	DDR_DQ31	9234.2	70.1656
DDR_DCF33	3586.36	30.766	DDR_DQ32	11196.3	82.8866
DDR_DM0	6506.84	50.9618	DDR_DQ33	10866.6	80.1328
DDR_DM1	6837.43	53.0854	DDR_DQ34	9882.26	74.3689
DDR_DM2	8702.77	66.0263	DDR_DQ35	11602.4	84.4436
DDR_DM3	11941.5	87.9312	DDR_DQ36	7619.44	58.4747
DDR_DM4	8130.6	61.666	DDR_DQ37	8183.16	61.6764
DDR_DQS0_N	7881.46	60.2778	DDR_DQ38	8298.95	63.0339
DDR_DQS0_P	7874.83	60.2327	DDR_DQ39	8217.36	63.5505
DDR_DQS1_N	8618.61	65.7222	DDR_DQS2_P	8732.72	66.6938

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Table 24. i.MX8 QXP DDR 21 x 21 mm package trace lengths/delays*...continued*

Ball Name	Length (microns)	XIM delay (ps)	Ball Name	Length (microns)	XIM delay (ps)
DDR_DQS1_P	8641.27	64.8686	DDR_DQS4_N	9959.44	73.5807
DDR_DQS2_N	8761.63	65.8288	DDR_DQS4_P	9958.73	74.6451

Table 25. i.MX8 QXP DDR 17 x 17 mm package trace lengths/delays

Ball Name	Length (microns)	XIM delay (ps)	Ball Name	Length (microns)	XIM delay (ps)
DDR_CK0_N	9449.88	70.8242	DDR_DCF28	7684.51	59.1856
DDR_CK0_P	9158.14	67.9972	DDR_DCF29	6663.57	52.0228
DDR_CK1_N	10120.9	75.0713	DDR_DCF30	5197.86	40.5424
DDR_CK1_P	9896.86	74.2075	DDR_DCF31	7121.98	54.6766
DDR_DCF00	8754.86	65.8329	DDR_DCF32	6487.17	51.1687
DDR_DCF01	11309.9	83.5447	DDR_DCF33	6150.32	48.6505
DDR_DCF03	8986.16	67.4538	DDR_DM0	6796.77	52.196
DDR_DCF04	5132.16	40.9709	DDR_DM1	3847.74	30.3047
DDR_DCF05	9058.4	67.7856	DDR_DQ00	8859.27	68.0011
DDR_DCF07	10139.1	75.6965	DDR_DQ01	7524	56.764
DDR_DCF08	8607.45	65.8647	DDR_DQ02	9491.6	71.3627
DDR_DCF09	8024.11	61.4408	DDR_DQ03	7057.53	53.7638
DDR_DCF10	10883.1	80.6124	DDR_DQ04	6528.95	50.6725
DDR_DCF11	7270.83	56.1378	DDR_DQ05	5859.65	46.0148
DDR_DCF12	11795.9	87.1921	DDR_DQ06	6481.95	50.2348
DDR_DCF14	8636.8	65.2871	DDR_DQ07	5616.71	44.0571
DDR_DCF15	10912	81.5138	DDR_DQ08	4149.83	34.3367
DDR_DCF16	5282.96	40.2926	DDR_DQ09	5482.01	44.2618
DDR_DCF17	9305.29	67.6591	DDR_DQ10	4897.01	37.5122
DDR_DCF18	10262.6	77.7681	DDR_DQ11	5932.84	47.1587
DDR_DCF19	6649.2	51.593	DDR_DQ12	6192.49	47.1092
DDR_DCF20	9160.92	69.4842	DDR_DQ13	8031.6	61.4137
DDR_DCF21	12748.4	93.2986	DDR_DQ14	6216.45	47.3891
DDR_DCF22	8400.13	64.0358	DDR_DQ15	6612.79	49.4634
DDR_DCF23	5342.64	41.9257	DDR_DQS0_N	9059.76	68.8765
DDR_DCF24	6846.35	53.3579	DDR_DQS0_P	9237.78	68.2606
DDR_DCF25	10998.4	50.6743	DDR_DQS1_N	6316.13	47.4771
DDR_DCF26	8592.59	65.9814	DDR_DQS1_P	6177.19	45.6418
DDR_DCF27	6287.16	48.9159	-		

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3.4.4 i.MX8 DXL DDR package conductor lengths

When performing the required trace length matching for LPDDR4/DDR3L routing, the bond wires within the i.MX8 DXL package must be accounted for and included in the match calculation. Table 26 lists the lengths from each die I/O to the package ball as well as the propagation / fly time from the die I/O to the package ball.

Note: *The values for substrate lengths and delay time are determined by the CAD program used to design the package substrate. For simulation tools that use delay times as an input, the delay time numbers can be used, because they are more accurate. The customer must ensure that the simulation tool is properly set up for using delay times. The package trace lengths provided are exact, but no information is provided for the package substrate stack-up, so determining the delay time directly from the trace length can only be done as an approximation. NXP has determined that using trace lengths with Cadence Allegro provides more consistent results.*

Table 26. i.MX8 DXL package trace lengths / delays

Ball Name	Length (microns)	XIM delay (ps)	Ball Name	Length (microns)	XIM delay (ps)
DDR_CK0_N	9075.78	67.693	DDR_DCF28	4872.19	39.4997
DDR_CK0_P	9069.63	67.7646	DDR_DCF30	4886.10	38.162
DDR_DCF00	6435.56	49.6818	DDR_DCF32	7358.16	56.764
DDR_DCF01	8558.98	63.1366	DDR_DCF33	6875.30	52.8145
DDR_DCF03	8010.57	59.2997	DDR_DM0	7017.52	52.5363
DDR_DCF04	10959.50	79.1304	DDR_DM1	6558.63	49.7746
DDR_DCF05	6058.38	46.4206	DDR_DQ00	7094.77	54.9497
DDR_DCF07	8616.79	62.4037	DDR_DQ01	7331.18	55.2126
DDR_DCF08	8074.74	60.2161	DDR_DQ02	8226.62	62.0848
DDR_DCF09	11844.10	84.5137	DDR_DQ03	7392.70	56.149
DDR_DCF10	7732.82	58.117	DDR_DQ04	7799.23	57.2762
DDR_DCF11	6508.61	48.4322	DDR_DQ05	7599.30	56.2057
DDR_DCF12	6154.98	45.7943	DDR_DQ06	7301.68	56.1834
DDR_DCF14	6501.11	48.3971	DDR_DQ07	7007.87	54.3704
DDR_DCF15	7223.53	53.4077	DDR_DQ08	6927.80	52.9389
DDR_DCF16	5902.69	44.0336	DDR_DQ09	7191.28	55.5978
DDR_DCF17	9181.60	68.2761	DDR_DQ10	6709.30	52.8039
DDR_DCF18	7565.95	56.8453	DDR_DQ11	6384.39	51.8193
DDR_DCF19	9966.38	72.5725	DDR_DQ12	6262.08	47.794
DDR_DCF20	9618.85	73.5065	DDR_DQ13	6172.39	46.5743
DDR_DCF21	7701.25	56.9786	DDR_DQ14	6027.65	47.7682
DDR_DCF22	10790.80	80.2252	DDR_DQ15	5799.80	43.987
DDR_DCF23	8093.43	60.4599	DDR_DQS0_N	9145.29	68.0333
DDR_DCF24	9171.43	70.2573	DDR_DQS0_P	9158.40	69.4686
DDR_DCF26	8711.10	64.7308	DDR_DQS1_N	6196.44	49.0494
DDR_DCF27	7520.79	56.338	DDR_DQS1_P	6171.09	47.8511

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3.4.5 Length matching guides

The DDR Memory Controller and PHY used in the i.MX8 QM, i.MX8 QXP, and i.MX8 DXL processors are capable of training out trace mismatches between individual DQ and CA traces, but NXP continues to recommend designing PCB with length matching as close as possible, because the training procedures are only able to align timing within a finite number of picoseconds. With good trace matching techniques, it is possible to achieve a more accurate trace match than by relying on the automatic training routines to match signal timing.

Length matching consists of taking all data or command/address traces in a group, making sure that the complete trace length of each trace within that group is matched together and to the strobe/clock that latches those signals into the target device.

An example of a length match calculation of the control signals is shown in Table 27. This analysis was done for the LPDDR4-3200 implementation using the i.MX8 QM, but the mechanism would be the same for the LPDDR4-2400 (with relaxed timing due to the 1.2 GHz clock rate vs. 1.6 GHz clock rate). In this table, the "PCB Length" column was obtained from an Allegro PCB file, and the "Pkg Length" column is the package conductor length, obtained from Section 3.4.2.

The "Via Length" column was obtained from the board stack-up, adding the total copper and dielectric thicknesses from Layer 1 down to layer 10, and adding this number twice as the net goes through two via transitions (L1 to L10, then back up to L1):

Total Length = PCB Length + Pkg Length + 2 x Via Length

The required matching is to the true clock signal within $\pm$ 1 ps, which is approximately 6 mils. All nets are within this range (1004.833 to 1016.833 mils). See Section 3.4.7 and Section 3.4.8 for examples of LPDDR4 routing.

Table 27. LPDDR4 length matching example (control signals)

Net Name	PCB Length	Pkg Length	Via Length	Comment
DDR_CH0_CK0_P	586.13	324.067	50.318	Vias are L1-> L10->L1
	1010.833			Total Net Length
DDR_CH0_CK0_N	581.09	324.890	50.318	Vias are L1-> L10->L1
	1006.616			Total net length (mils)
DDR_CH0_CA0_A	699.60	316.304	N/A	DCF11 in package, L1 trace only
	1015.904			Total net length (mils)
DDR_CH0_CA1_A	675.20	341.157	N/A	DCF16 in package, L1 trace only
	1016.357			Total net length (mils)
DDR_CH0_CA2_A	673.80	232.068	50.318	DCF00 in package, Vias are L1-> L10->L1
	1006.504			Total net length (mils)
DDR_CH0_CA3_A	649.78	259.101	50.318	DCF08 in package, Vias are L1-> L10->L1
	1009.517			Total net length (mils)
DDR_CH0_CA4_A	697.01	211.395	50.318	DCF01 in package, Vias are L1-> L10->L1
	1009.041			Total net length (mils)
DDR_CH0_CA5_A	715.63	195.258	50.318	DCF03 in package, Vias are L1-> L10->L1
	1011.524			Total net length (mils)
DDR_CH0_CS0_A	627.03	280.924	50.318	DCF10 in package, Vias are L1-> L10->L1
	1007.960			Total net length (mils)

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Table 27. LPDDR4 length matching example (control signals)*...continued*

Net Name	PCB Length	Pkg Length	Via Length	Comment
DDR_CH0_CKE0_A	537.29	369.077	50.318	DCF14 in package, Vias are L1-> L10->L1
	1007.003			Total net length (mils)
DDR_CH0_CS1_A	649.06	264.731	50.318	DCF12 in package, Vias are L1-> L10->L1
	1014.427			Total net length (mils)
DDR_CH0_CKE1_A	607.84	400.963	N/A	DCF15 in package, L1 trace only
	1008.803			Total net length (mils)

An example of the length match calculation of the byte lane 1 signals for the i.MX8 QM is shown in Table 28. In this table, the "PCB Length" column was obtained from an Allegro PCB file and the "Pkg Length" column is the package conductor length obtained from the Section 3.4.2.

The "Via Length" column is ignored for this match calculation, because all signals are routed on layer 3, which means that the via lengths are equal and they cancel each other out.

Table 28. LPDDR4 length matching example (byte lane 1 signals)

Net Name	PCB Length	Pkg Length	Via Length	Comment
DDR_CH0_DQS1_P	459.06	379.728	N/A	Vias are L1->L3->L1
	838.788			Total net length (mils)
DDR_CH0_DQS1_N	467.06	379.681	N/A	Vias are L1->L3->L1
	846.741			Total net length (mils)
DDR_CH0_DM1	607.66	235.725	N/A	Vias are L1->L3->L1
	843.385			Total net length (mils)
DDR_CH0_DQ8	538.45	296.925	N/A	Vias are L1->L3->L1
	835.375			Total net length (mils)
DDR_CH0_DQ9	504.71	330.115	N/A	Vias are L1->L3->L1
	834.825			Total net length (mils)
DDR_CH0_DQ10	514.51	323.706	N/A	Vias are L1->L3->L1
	838.216			Total net length (mils)
DDR_CH0_DQ11	480.39	355.539	N/A	Vias are L1->L3->L1
	835.929			Total net length (mils)
DDR_CH0_DQ12	630.51	204.330	N/A	Vias are L1-L3->L1
	834.840			Total net length (mils)
DDR_CH0_DQ13	551.58	283.834	N/A	Vias are L1->L3->L1
	835.414			Total net length (mils)
DDR_CH0_DQ14	544.91	290.237	N/A	Vias are L1->L3->L1
	835.147			Total net length (mils)
DDR_CH0_DQ15	581.26	255.423	N/A	Vias are L1->L3->L1
	836.683			Total net length (mils)

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3.4.6 LPDDR4-2400/3200 general design recommendations

The following list details generic guidelines that should be adhered to when implementing i.MX8 QM, i.MX8 QXP, or i.MX8 DXL designs using LPDDR4.

1. It is expected that the layout engineer and design team already have experience and training with DDR designs at speeds of 1.6 GHz / 3200 MT/s or 1.2 GHz / 2400 MT/s.
2. Use PCB materials with good dielectric constants (< 3.7 @ 5 GHz is desired). Some examples are Megtron6, Megtron4, ThunderClad2, and MCL-HE-679G Type(S).
3. 8QXP, 8DXL: The 3 W rule center-to-center is desired after breakout, except for special declarations.
4. 8QM: The 2 W rule center-to-center is desired after a breakout, except for special declarations. The 3 W spacing rule should be followed for DQS and CLK.
5. The total number of vias should be two or less on each point-to-point single-ended/differential trace.
    a. The 45r20 metric via is simulated on the i.MX8 QM development platform.
    b. The 18r10 imperial via is simulated on the i.MX8 QXP development platform.
    c. The 18r10 imperial via is simulated on the i.MX8 DXL development platform.
6. The DQS and DMI with the same slice should have the same number of vias/layer changes.
7. Place at least one ground-stitching via within 40 mils of the signal via when switching reference planes.
8. All length / delay-matching calculations must take the PCB trace lengths plus the IC package delays into account.
9. The lengths of vias should also be taken into account when performing trace-matching calculations.
10. It is suggested to incorporate the package trace lengths into the CAD tool’s constraint manager.
11. Only point-to-point PCB designs are supported. Designs where the signal traces are branched on the PCB are not allowed.
12. i.MX 8QM designs must utilize the full data bus width of each used DDR subsystem (2x32-bit if both DDR subsystems are used, 1x32-bit if one DDR subsystem is used). Designs with 16-bit data bus width per DDR subsystem are not allowed.
13. CA bit swapping is not supported.
14. Data byte swapping within each 16-bit channel is good for i.MX8 QM and i.MX8 QXP.
15. **Data byte swapping within the 16-bit channel is not supported on i.MX8 DXL.**
16. Bit swapping within each slice/byte lane is good. Follow the custom bit swap done on NXP’s circuit boards to facilitate easier/faster software support and bring-up.
17. All trace impedances are referenced to the associated ground plane. Reference only the ground planes when determining impedance.
18. Referencing the 1.1 V power plane as the sole signal return path is not supported due to the dedicated package design.
19. A full high-speed simulation of the LPDDR4 layout is required.
20. For i.MX8 QM, QXP, or DXL designs, DCF09 and DCF25 on the processor must be left unconnected when using LPDDR4. The ODT_CA balls on the LPDDR4 devices should be connected directly to the VDD2 supply.
21. The 200-ball LPDDR4 package should be placed 100 mils from i.MX8 QM, i.MX8 QXP, or i.MX8 DXL.
22. The DBI (Data Bus Inversion) feature must be enabled by software.
23. **If inline ECC is planned to be enabled (DXL only), the usage of memory devices with non-binary densities per die/channel is not recommended.**

3.4.7 i.MX8 QM LPDDR4-3200 routing recommendations

Note: *It is strongly recommended to adopt the NXP layout if possible. The design files are available at www.nxp.com or upon request.*

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LPDDR4-3200 must be routed with signal fly times matched, as shown in Table 29. Note that if the matched groups are not all routed on the same layers with the same number of via transitions, then the trace length/delay of the via transitions must be included in the overall calculation.

NXP recommends that users simulate their LPDDR4 implementation before fabricating PCBs.

Total Length = PCB Length + Pkg Length + 2 x Via Length

Table 29. i.MX8 QM LPDDR4-3200 routing recommendations

LPDDR4-3200				
LPDDR4 signal (each 16-bit channel)	**Group**	**PCB and Package Prop Delay**		**Considerations**
		Min	**Max**	
CK_t/CK_c	Clock	As short as possible	225 ps (do not exceed 1125 mils)	Match the true/complement signals within 1 ps (the timing includes the package length). Incorporate package lengths/delays into the constraint manager.
CA[5:0]	Address/ Command/ Control	CK_t + package length -1 ps	CK_t + package length + 1 ps	Keep the maximum total PCB + package length skew of CA/CTL bus within ± 1.0 ps of CK_t. Incorporate package lengths/delays into the constraint manager.
CS				
CKE				
DQ[7:0]	Byte 0	As short as possible	190 ps (260 ps with package delta) do not exceed 1150 mils)	Match the differential signals of DQS within 1.0 ps. Keep the maximum total PCB + package delta skew of each DQS/DQ/DMI slice within ± 1.0 ps. Incorporate package lengths/delays into the constraint manager.
DM0				
DQS0_t/DQS0_c				
DQ[15:8]	Byte1	As short as possible	190 ps (260 ps with package delta) do not exceed 1150 mils)	
DM1				
DQS1_t/DQS1_c				

The following figures show the placement and routing of the LPDDR4 signals on the i.MX8 QM development (MEK) platform. Note from the schematic that the individual bits and byte lanes are swapped between the processor and the LPDDR4 memories. It should also be noted that the swapping is different between the west side and east side memories (left and right sides of the processor, respectively). This was done to ease routing and this connectivity scheme should be duplicated on a customer design using LPDDR4.

The back side of the PCB (layer 12) is used for signal routing, but it had no LPDDR4 signals on it, and is thus not shown.

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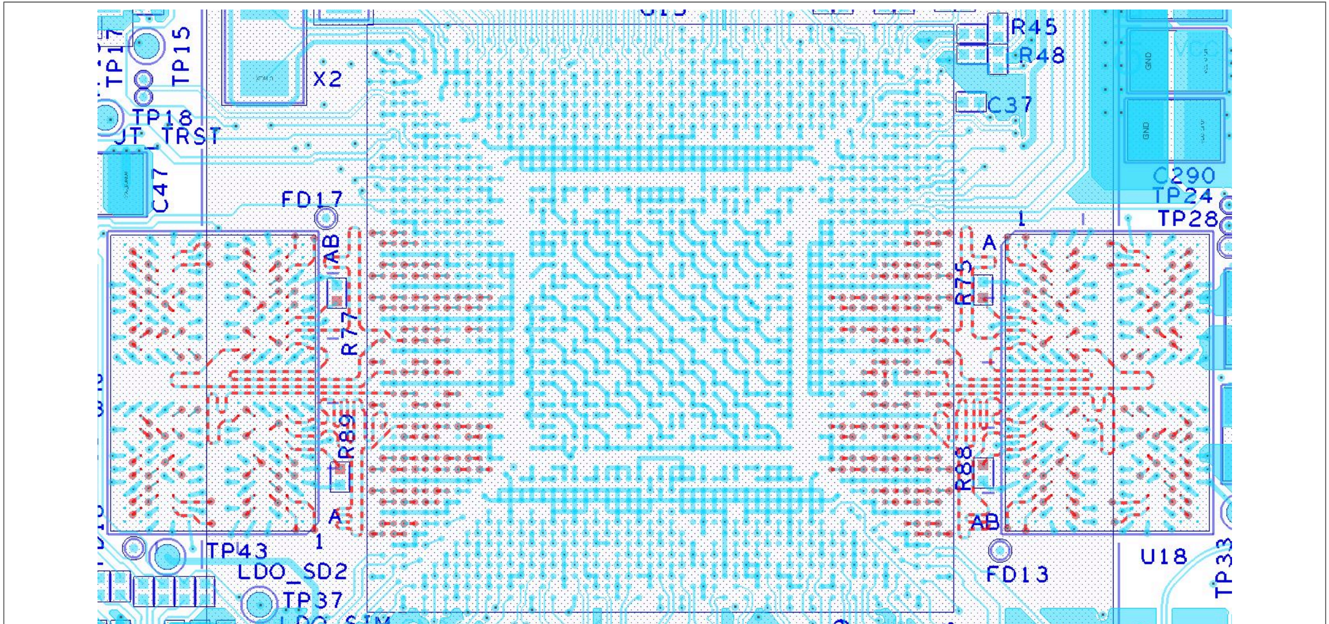

Figure 3. i.MX8 QM LPDDR4 MEK platform routing (top layer)

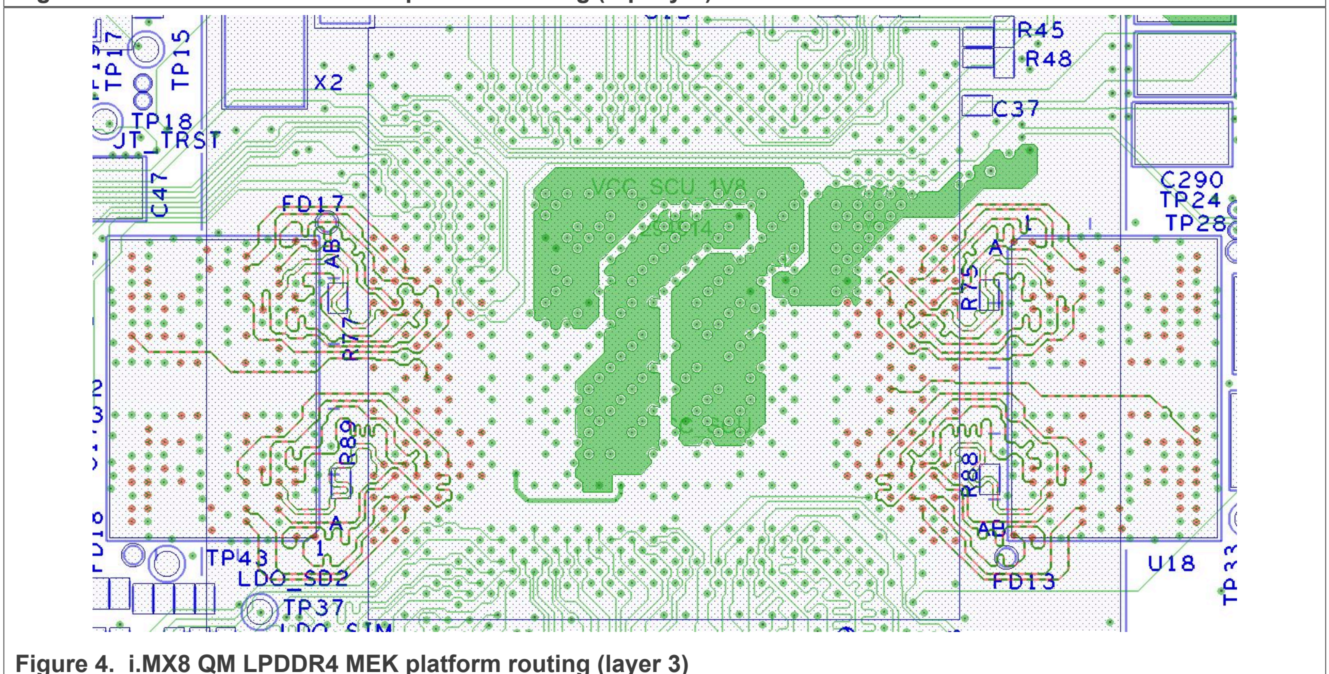

Figure 4. i.MX8 QM LPDDR4 MEK platform routing (layer 3)

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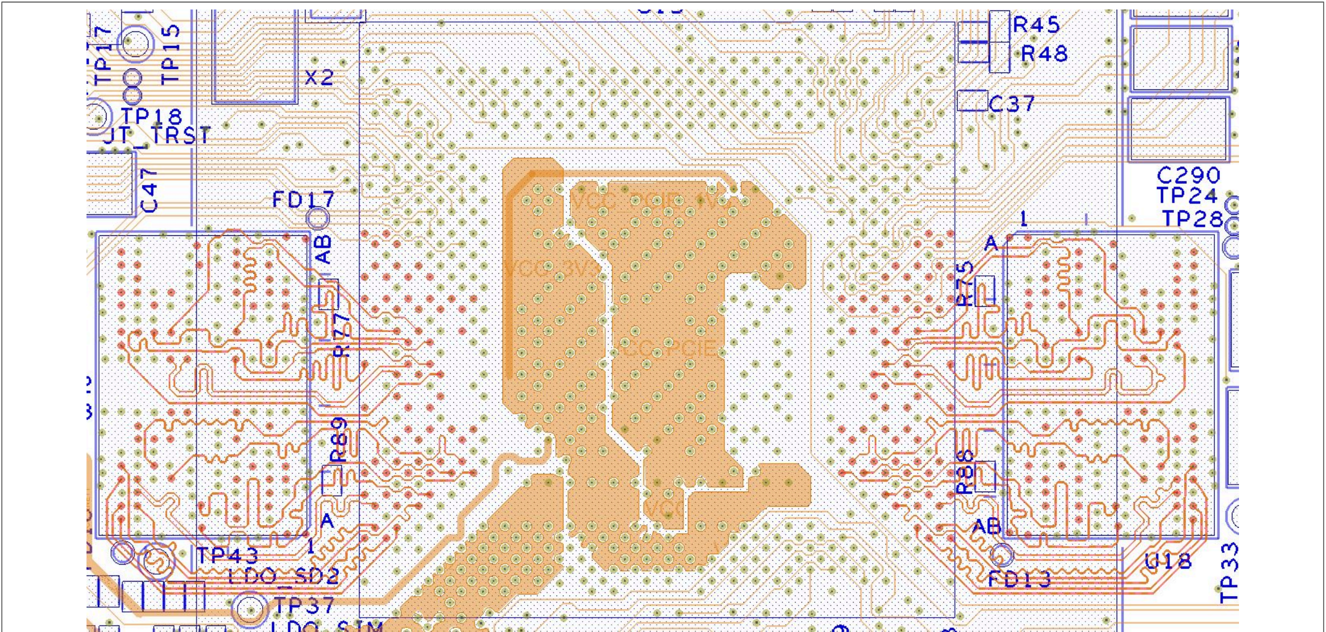

Figure 5. i.MX8 QM LPDDR4 MEK platform routing (layer 5)

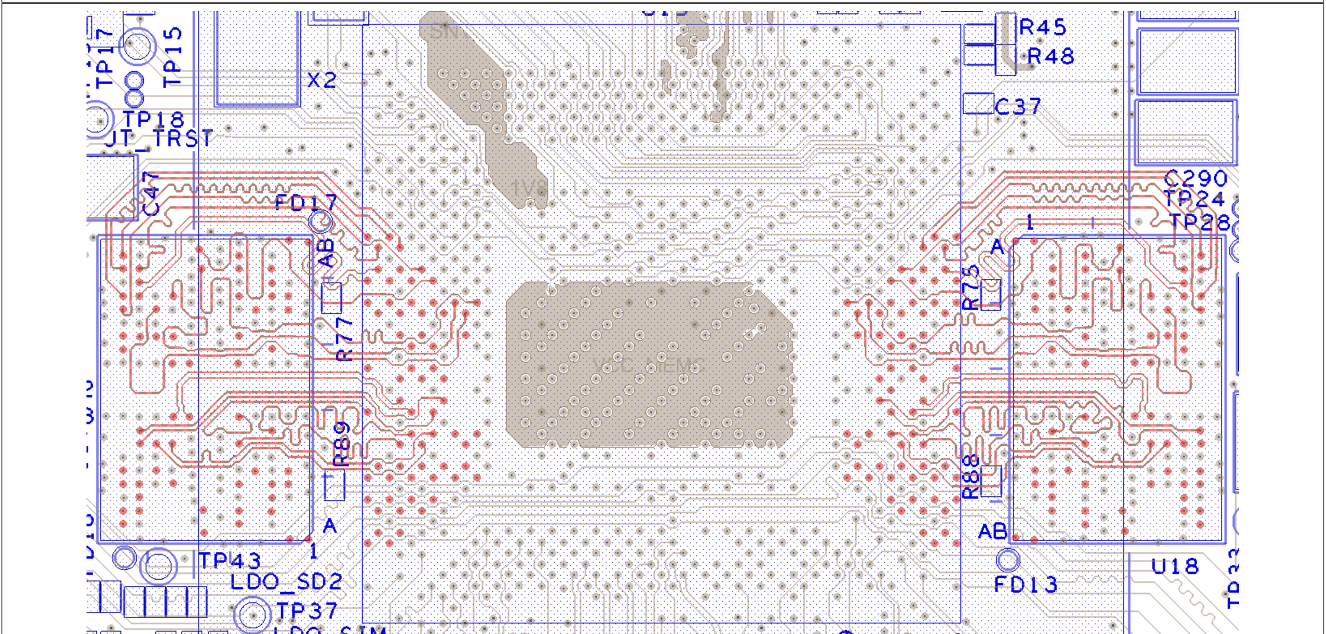

Figure 6. i.MX8 QM LPDDR4 MEK platform routing (layer 10)

3.4.8 i.MX8 QXP LPDDR4-2400 routing recommendations

Note: *It is strongly recommended to adopt NXP layout if possible. The design files are available at nxp.com or upon request.*

LPDDR4-2400 must be routed with signal fly times matched, as shown in Table 30. Note that if the matched groups are not all routed on the same layers with the same number of via transitions, the trace length/delay of the via transitions must be included in the overall calculation.

NXP recommends that users simulate their LPDDR4 implementation before fabricating PCBs.

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Table 30. i.MX8 QXP LPDDR4-2400 routing recommendations

LPDDR4-2400				
LPDDR4 signal (each 16-bit channel)	Group	PCB and Package Prop Delay		Considerations
		Min	Max	
CK_t/CK_c	Clock	As short as possible	225 ps	Match the true/complement signals within 1.5 ps (PCB + package). Incorporate package lengths/delays into the constraint manager.
CA[5:0]	Address/ Command/ Control	CK_t + package length -1.5 ps	CK_t + package length + 1.5 ps	Keep the maximum delay skew of the CA/CTL bus within ± 1.5 ps of CK_t. Incorporate package lengths/delays into the constraint manager.
CS				
CKE				
DQ[7:0]	Byte 0	As short as possible	300 ps	Keep the maximum total PCB + package length skew of each DQS/ DQ/DMI slice within ± 1.5 ps. Incorporate package lengths/delays into the constraint manager.
DM0				
DQS0_t/DQS0_c				
DQ[15:8]	Byte1	As short as possible	300 ps	
DM1				
DQS1_t/DQS1_c				

The following figures show the placement and routing of the LPDDR4 signals on the i.MX8 QXP MEK development platform. Note from the schematic that the individual bits and byte lanes are swapped between the processor and the LPDDR4 memories. This was done to ease routing and this connectivity scheme should be duplicated on customer designs using LPDDR4.

The back side of the PCB (layer 8) is used for signal routing, but it had no LPDDR4 signals on it, and is thus not shown.

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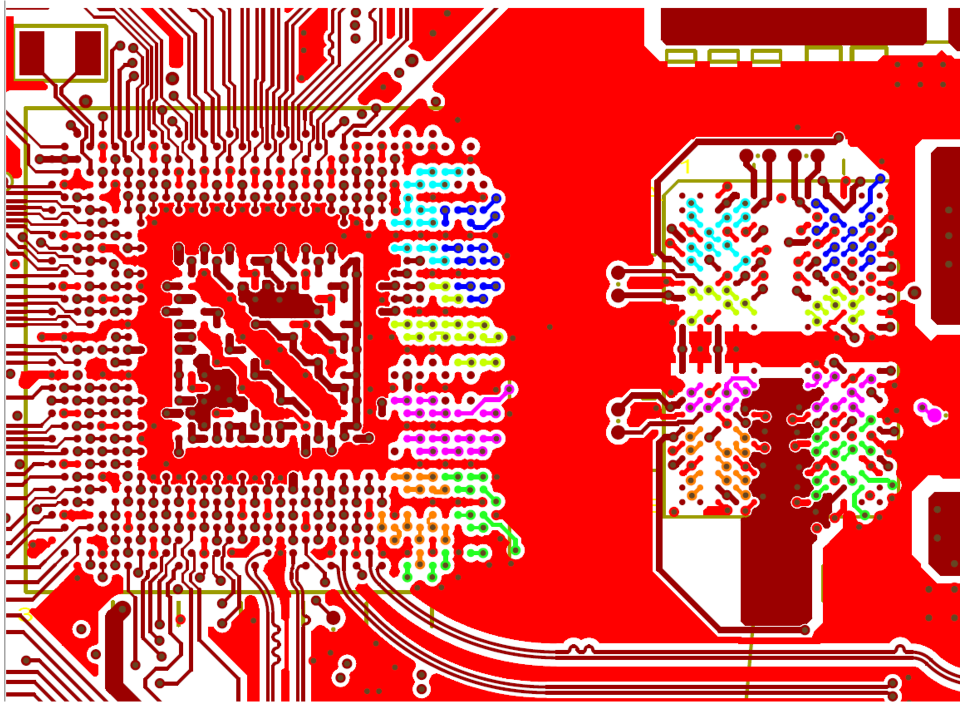

Figure 7. i.MX8 QXP LPDDR4 MEK platform routing (layer 1)

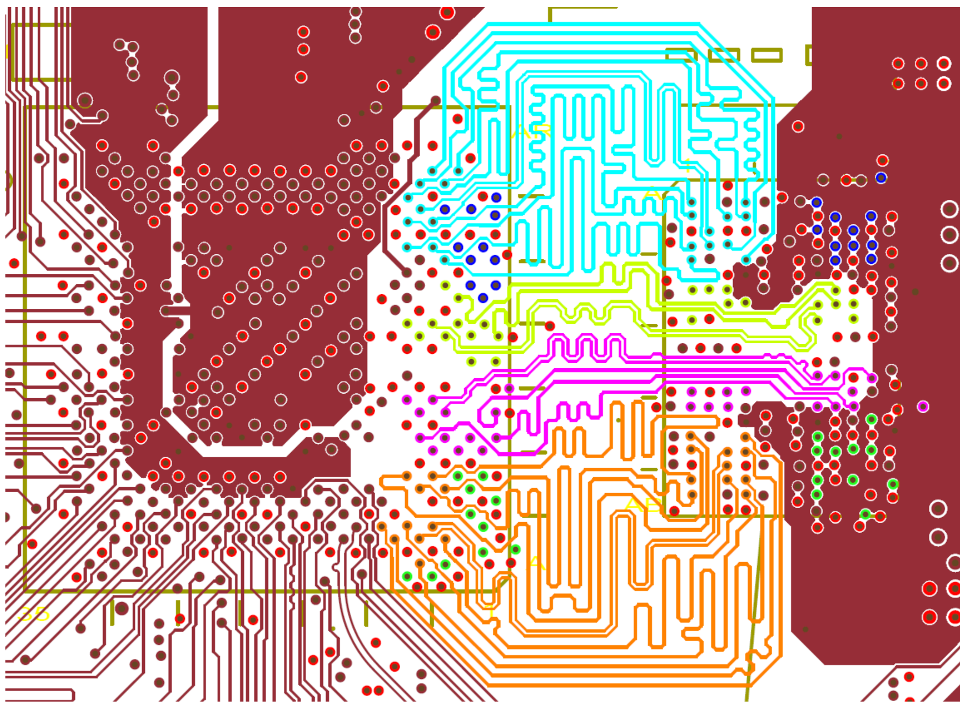

Figure 8. i.MX8 QXP LPDDR4 MEK platform routing (layer 3)

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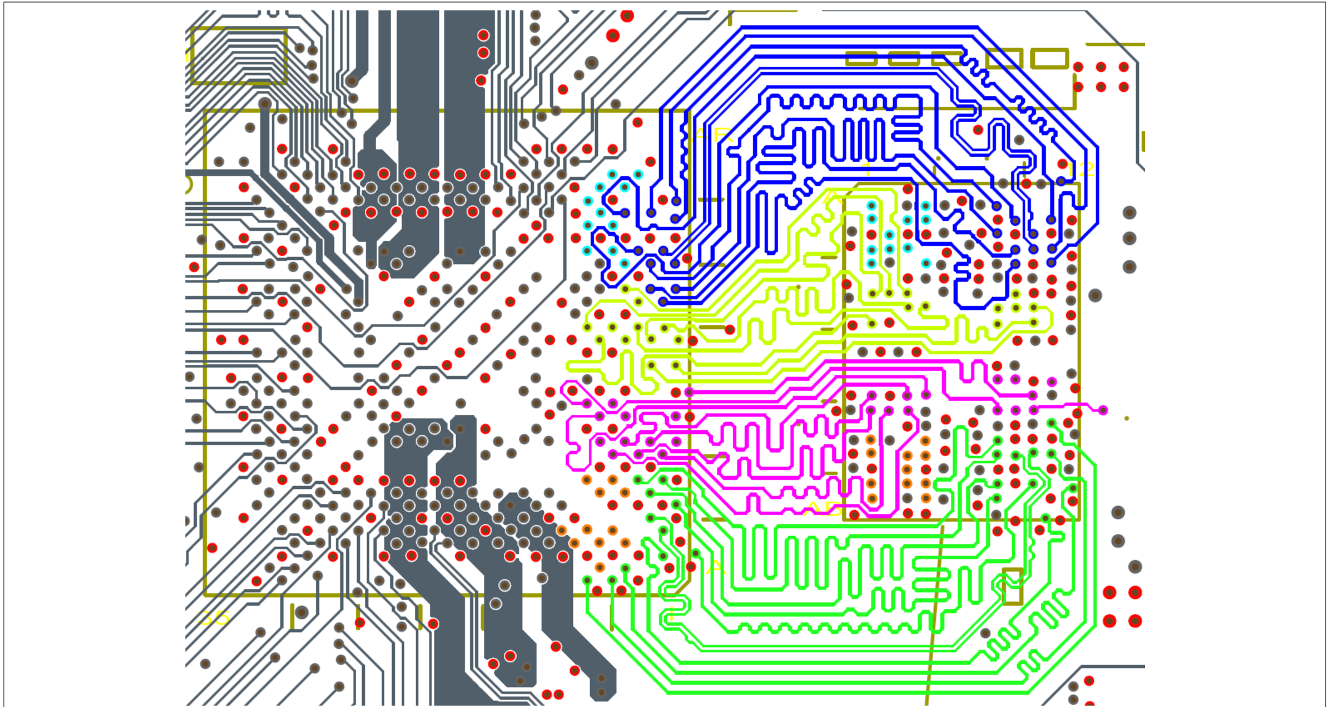

Figure 9. i.MX8 QXP LPDDR4 MEK platform routing (layer 6)

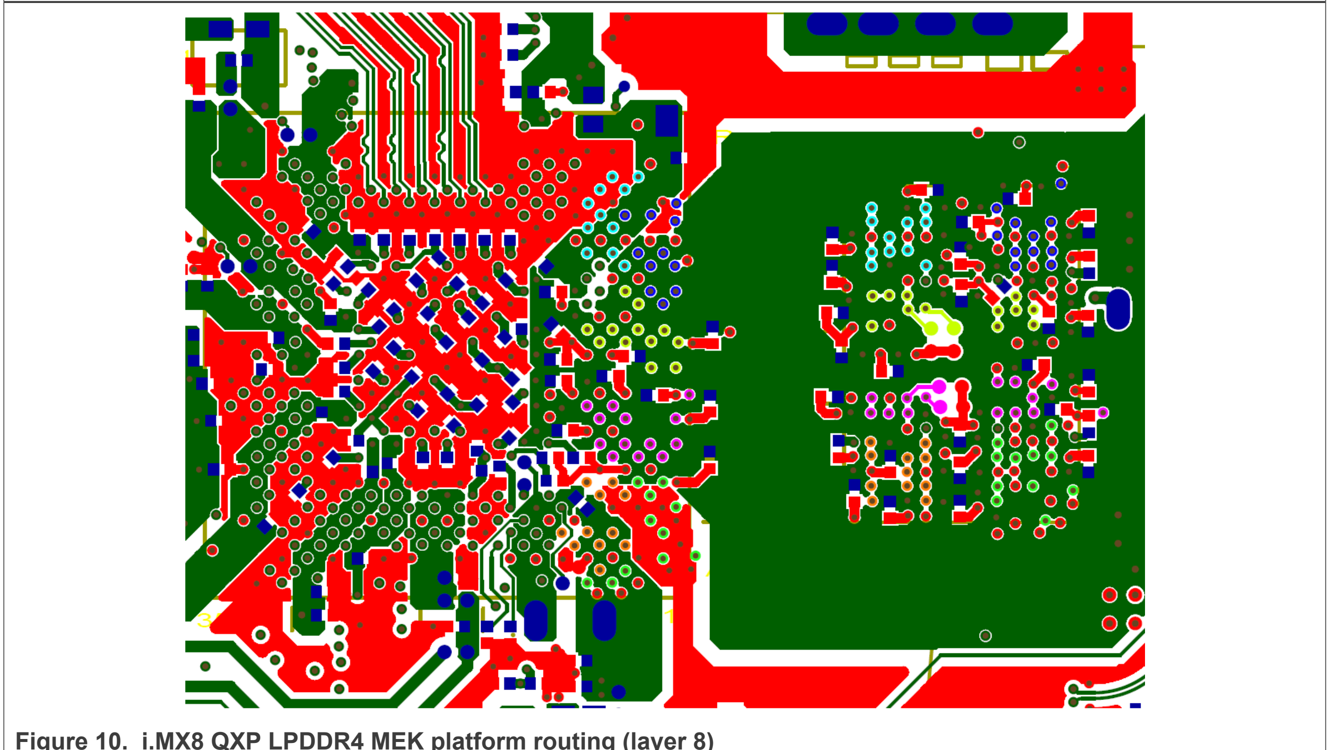

Figure 10. i.MX8 QXP LPDDR4 MEK platform routing (layer 8)

3.4.9 i.MX8 DXL LPDDR4-2400 routing recommendations

Note: *It is strongly recommended to adopt the NXP layout if possible. The design files are available at www.nxp.com or upon request.*

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LPDDR4-2400 must be routed with signal fly times matched, as shown in Table 31. If the matched groups are not all routed on the same layers with the same number of via transitions, the trace length/delay of the via transitions must be included in the overall calculation.

NXP recommends to simulate the LPDDR4 implementation before fabricating PCBs.

Note: Byte swapping within the 16-bit channel is not supported on i.MX8 DXL.

Table 31. i.MX8 DXL LPDDR4-2400 routing recommendations

LPDDR4-2400				
LPDDR4 signal	**Group**	**PCB and Package Prop Delay**		**Considerations**
		Min	**Max**	
CK_t/CK_c	Clock	As short as possible	225 ps	Match the true/ complement signals within 1.5 ps. Incorporate package lengths/delays into the constraint manager.
CA[5:0]	Address/ Command/ Control	CK_t – 50 ps	CK_t + 50 ps	Internal de-skew feature must be utilized. Incorporate package lengths/delays into the constraint manager.
CS				
CKE				
DQ[7:0]	Byte 0 - Data	DQS0_t – 50 ps	DQS0_t + 50 ps	Match the true/ complement signals of each DQS within 1.5 ps. Internal de-skew feature must be utilized. DMI0, DMI1 may not be the longest nor shortest of the 9 single-ended traces in each slice. The internal de-skew feature measures and de-skews of the 8 data bits of each slice individually. The DMIx de-skew is not measured, but calculated as an average of the 8 data skews. Therefore, please route the DMIx to be one of the median-length traces of the slice. Incorporate package lengths/delays into the constraint manager.
DMI0				
DQS0_t/DQS0_c	Byte 0 - DQS	CK_t – 75 ps	CK_t + 75 ps	
DQ[15:8]	Byte1 - Data	DQS1_t – 50 ps	DQS1_t + 50 ps	
DMI1				
DQS1_t/DQS1_c	Byte 1 – DQS	CK_t – 75 ps	CK_t + 75 ps	

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The following figures show the placement and routing of the LPDDR4 signals on the i.MX8 DXL EVK development platform.

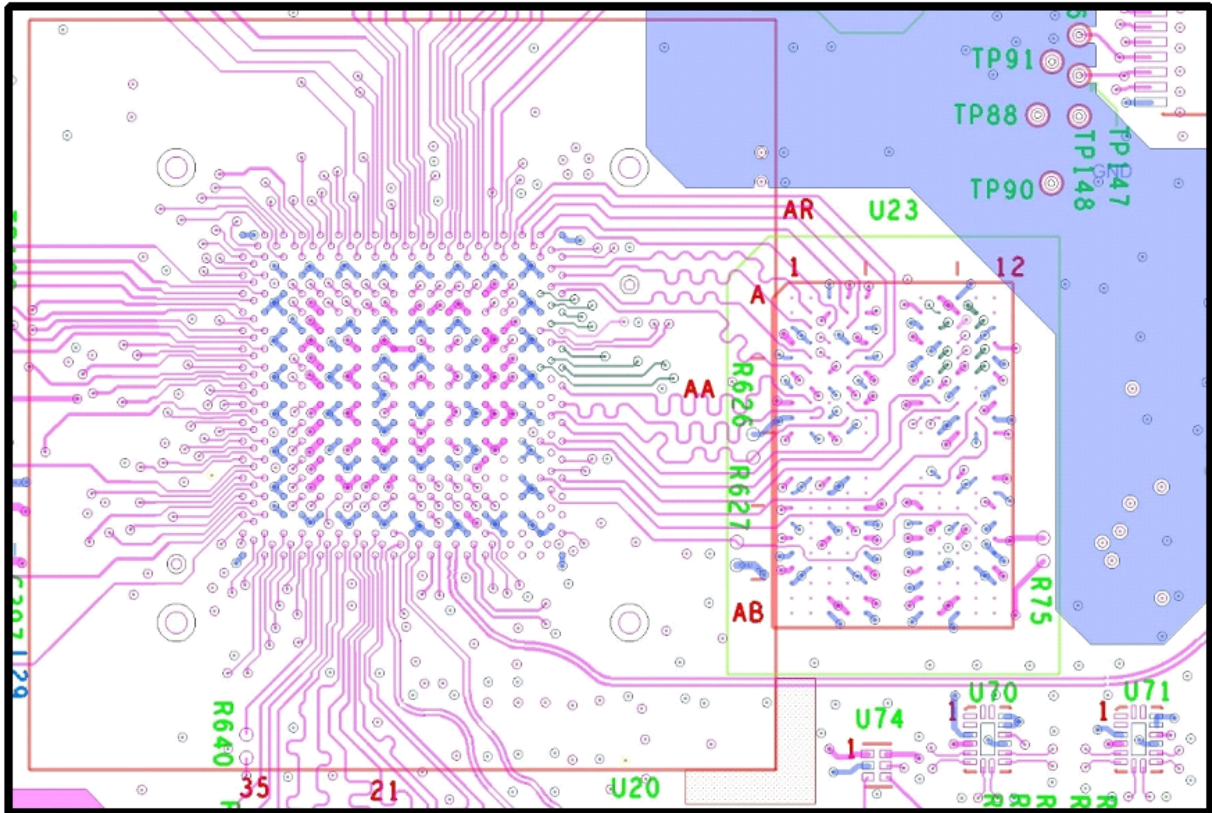

Figure 11. i.MX8 DXL LPDDR4 EVK platform routing (layer 1)

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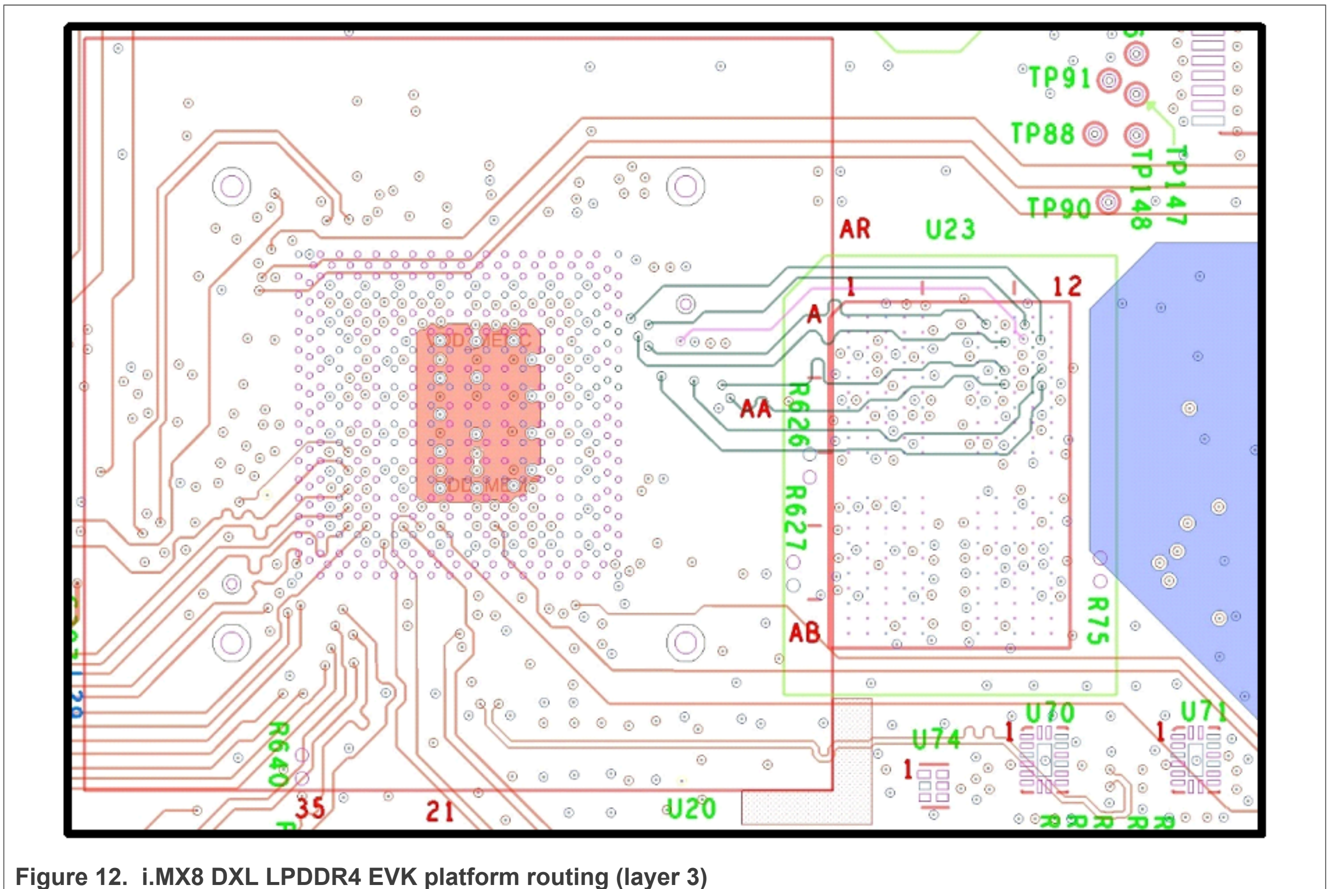

Figure 12. i.MX8 DXL LPDDR4 EVK platform routing (layer 3)

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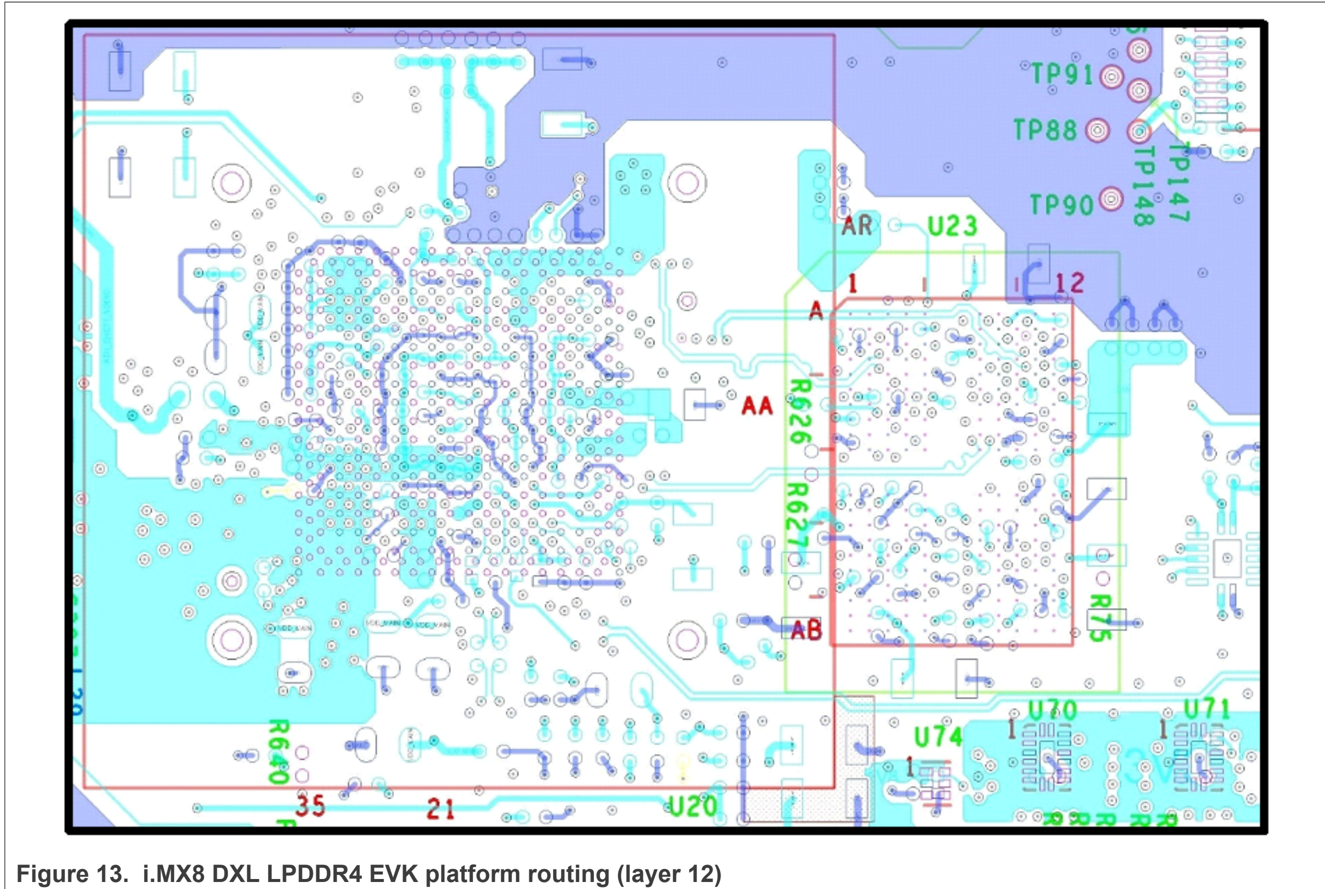

Figure 13. i.MX8 DXL LPDDR4 EVK platform routing (layer 12)

3.4.10 i.MX8 QXP / DXL general DDR3L-1866 design recommendations

The following list details generic guidelines that should be adhered to when implementing i.MX8 QXP or i.MX8 DXL designs using DDR3L.

1. It is expected that the layout engineer and design team already have experience and training with DDR designs at speeds of 933 MHz/1866 MT/s.
2. Use PCB materials with good dielectric constants (< 3.7 @ 5 GHz is desired). Some examples are Megtron6, Megtron4, ThunderClad2, and MCL-HE-679G Type(S).
3. The 3W rule center to center is desired after the breakout, except for special declarations. The 2W rule is acceptable for DDR3L ADD/CTRL/CMD signals for the strip line. 1W is defined as the dielectric distance between a trace and the referenced GND plane.
4. The total number of vias should be two (or less) on each point-to-point single-ended/differential trace. An 18r10 imperial via was simulated on the i.MX8 QXP and i.MX8 DXL development platform.
5. The DQS and DM with the same slice should have the same number of vias/layer changes.
6. Place at least one ground stitching via within 40 mils of the signal via when switching reference planes.
7. All length/delay matching calculations must take into account the PCB trace lengths plus the IC package delays.
8. Lengths of vias should also be taken into account when performing trace matching calculations.
9. It is suggested to incorporate the package trace lengths into the CAD tool's constraint manager.
10. Swapping of the Address/Command/Control bits is not supported.
11. Data bit swapping within each slice/byte lane is OK. Follow the custom bit swap done on NXP's circuit boards to facilitate easier/faster software support and bring-up.

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12. All trace impedances are referenced to the associated ground plane. Only reference the ground planes when determining impedance.
13. Referencing the 1.35 V power plane as the sole signal return path is not supported due to the dedicated package design.
14. A full high-speed simulation of the DDR3L layout is required.
15. Despite the SoC design similarities of i.MX8 QXP and i.MX8 DXL, the PCB routing recommendations for one cannot be applied to the other due to different PCB design approaches assumed for each SoC.

3.4.11 i.MX8 QXP DDR3L-1866 routing recommendations

Note: *It is strongly recommended to adopt NXP layout if possible. The design files are available upon request.*

The DDR3L-1866 must be routed with signal fly times matched, as shown in Table 32. Note that if the matched groups are not all routed on the same layers with the same number of via transitions, then the trace length/delay of the via transitions must be included in the overall calculation.

NXP recommends that users simulate their DDR3L implementation before fabricating PCBs.

Table 32. i.MX8 QXP DDR3L-1866 routing recommendations

DDR3L-1866 Fly-by				
DDR3L	**Group**	**PCB and Package Prop Delay**		**Considerations**
		Min	**Max**	
CK_t/CK_c	Clock	As short as possible	1100 ps	Match the CK_t/CK_c within 2 ps for each DDR3L sub-end. Incorporate package lengths/delays into the constraint manager.
ADDR[15:0]	Address Command Control	CK_t – 2 ps	CK_t + 2 ps	Keep the maximum delay skew of the ADD/CTL/ CMD bus within ±2 ps of CK_t for each DDR3L sub-end. Incorporate package lengths/delays into the constraint manager.
BA[2:0],CAS,RAS,WE				
CKE,CS,RESET,ODT				
DQ[7:0]	Byte 0	As short as possible	300 ps	Keep the maximum delay skew of DQS/DQ/DMI within ±2 ps. Incorporate package lengths/delays into the constraint manager.
DMI0				
DQS0_t/DQS0_c				
DQ[15:8]	Byte 1	As short as possible	300 ps	
DMI1				
DQS1_t/DQS1_c				
DQ[23:16]	Byte 2	As short as possible	300 ps	
DMI2				
DQS2_t/DQS2_c				
DQ[31:24]	Byte 3	As short as possible	300 ps	
DMI3				
DQS3_t/DQS3_c				
DQ[39:32]	Byte 4 (ECC)	Short as possible	300 ps	

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Table 32. i.MX8 QXP DDR3L-1866 routing recommendations_...continued_

DDR3L-1866 Fly-by				
DDR3L	Group	PCB and Package Prop Delay		Considerations
		Min	Max	
DMI4				
DQS4_t/DQS4_c				

3.4.12 NXP i.MX8 QXP DDR3L-1866 validation board

The i.MX8 QXP DDR3L validation board used three 16-bit DDR3L devices in a fly-by topology: Two for the 32-bits of data and one to support the ECC function. The i.MX8QXP board design differs from the previous fly-by topology boards in that two more series resistors are added to each of the command/address traces. The first one is a 50 Ω resistor inserted in series with the nearest DDR3L device and the second one is a 33 Ω resistor inserted in series with the middle DDR3L device. The details are as follows:

- 40 Ω single-ended trace impedance[1] is recommended for the trace up to the point where the trace branches to the nearest DDR3L device. In addition, the trace branch connected to the termination resistor should also use 40 Ω single-ended line impedance (the exception is that if the trace length is less than 30 mils, a 52 Ω impedance may be used). The remaining trace segments should use a 52 Ω single-ended trace impedance[2].
- Place the series resistors on the top layer to reduce the number of vias used. The series resistors on the differential pair CLK can be placed on the bottom layer. The via number can be increased. As a rule of thumb, the number of vias used should be equal to (or less than) the number of IC devices. Example: If there are four devices including the CPU, the max via number should be 4.
- The termination resistor should be 40 Ω and it should be connected to the VTT supply. Capacitor placement on the VTT is very important and NXP recommends at least one decoupling capacitor for every three traces connected to the VTT.
- Consider the trace that connects the processor ball to the termination resistor at the end of the trace as the main portion of the trace. The trace portions that branch off this main trace (typically through a via) going to each of the three DDRL devices are considered stubs. The three stub lengths should be matched in length, and their length should be between 170 mil and 360 mil, based on NXP simulations.
- The NXP validation board layout is available for further reference.
- If ECC is not used and there are only two 16-bit DDR devices in the design, the validation board layout strategy for the command/address traces can still be used. Simply remove the first (closest to the processor) device and trace stub.
- Regardless of whether the NXP layout is used as a base or a new layout is created from scratch, running signal analysis using simulation tools (Sigrity, Hyperlynx) is highly recommended.

NOTE 1,2: if 40 Ω and 52 Ω impedance controls are hard to achieve, make them as near as possible to the target value.

The following figures show the placement and routing of the DDR3L signals on the i.MX8 QXP DDR3L validation board.

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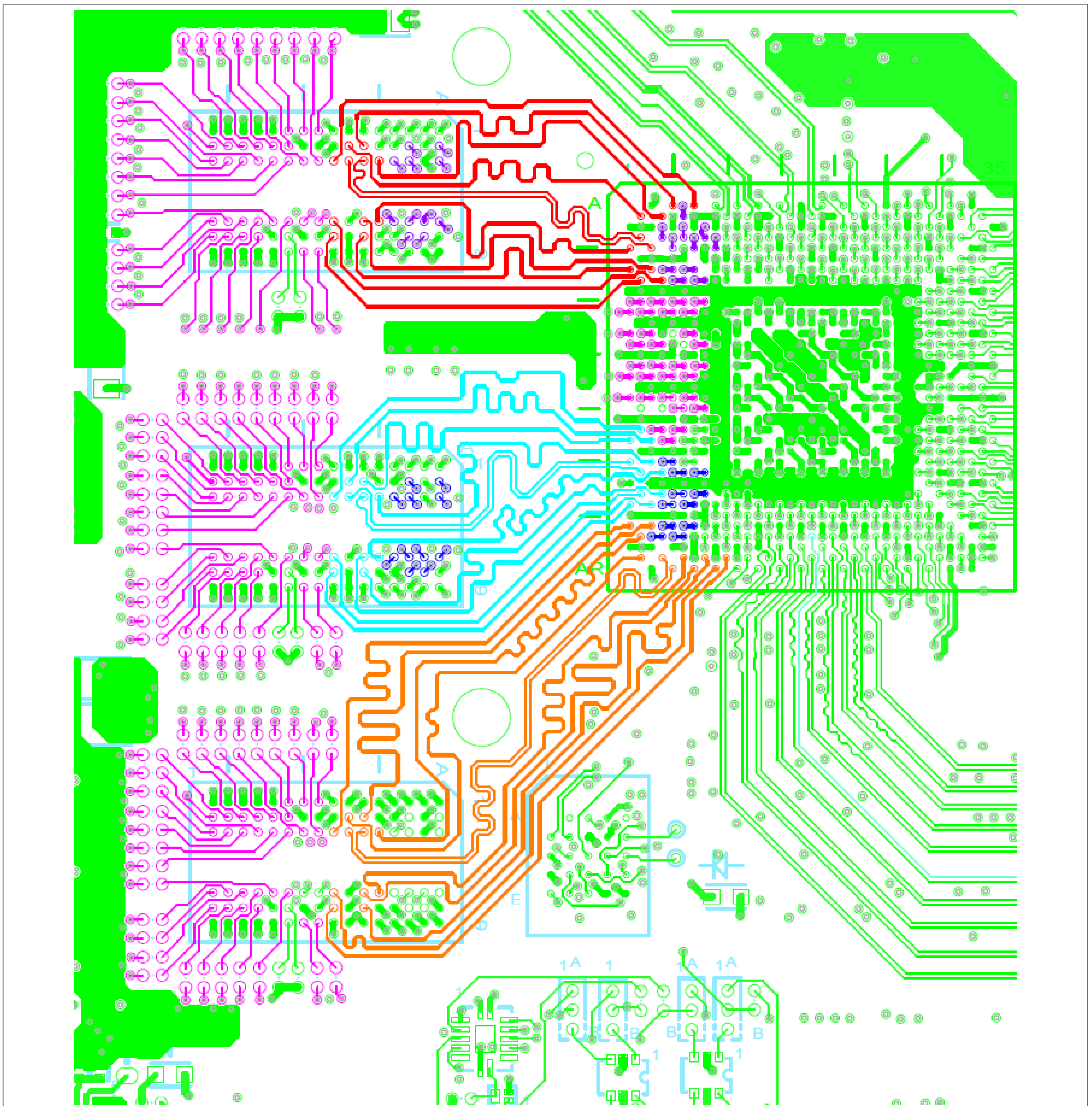

Figure 14. i.MX8 QXP development platform DDR3L routing (layer 1)

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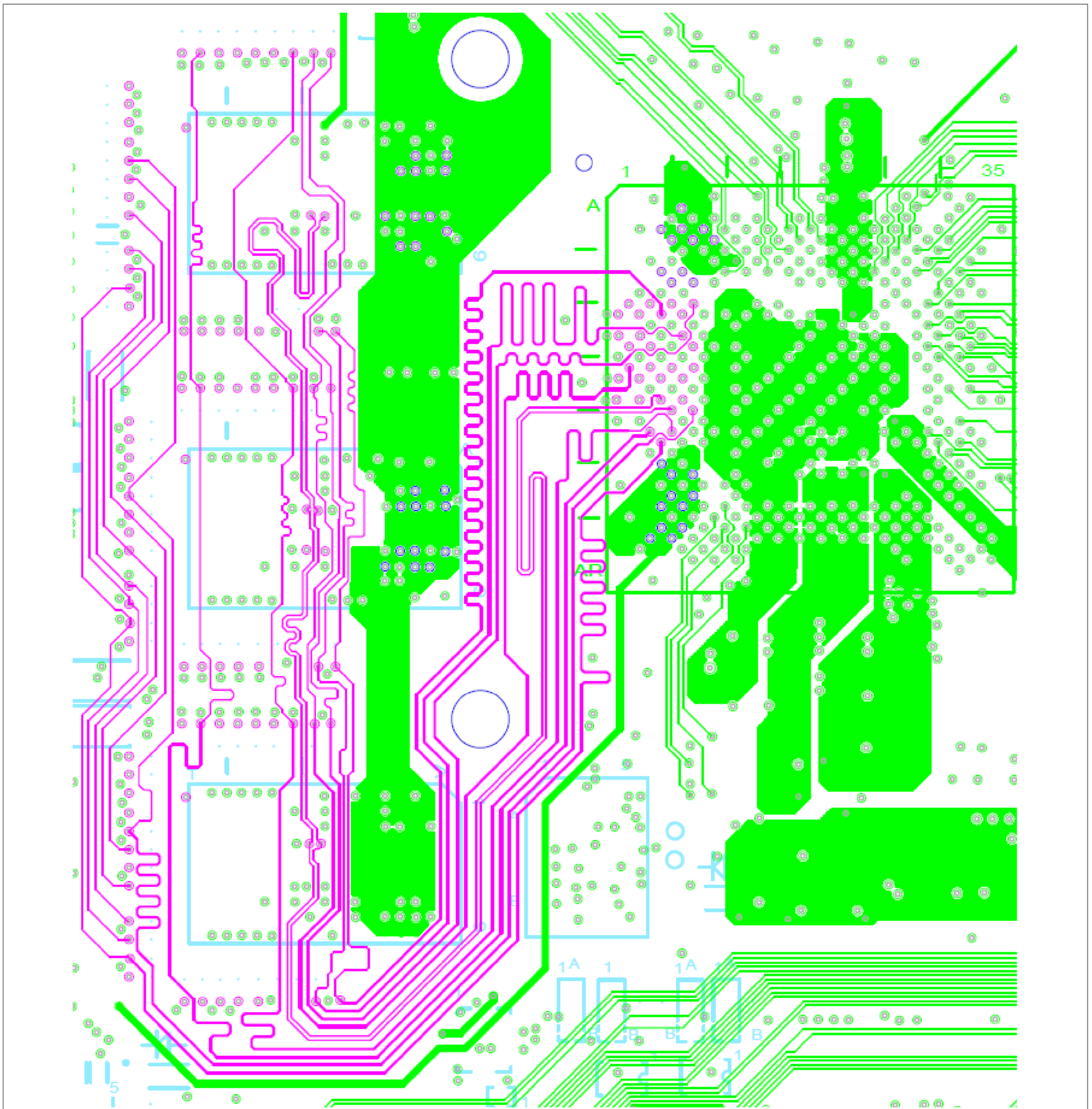

Figure 15. i.MX8 QXP development platform DDR3L routing (layer 3)

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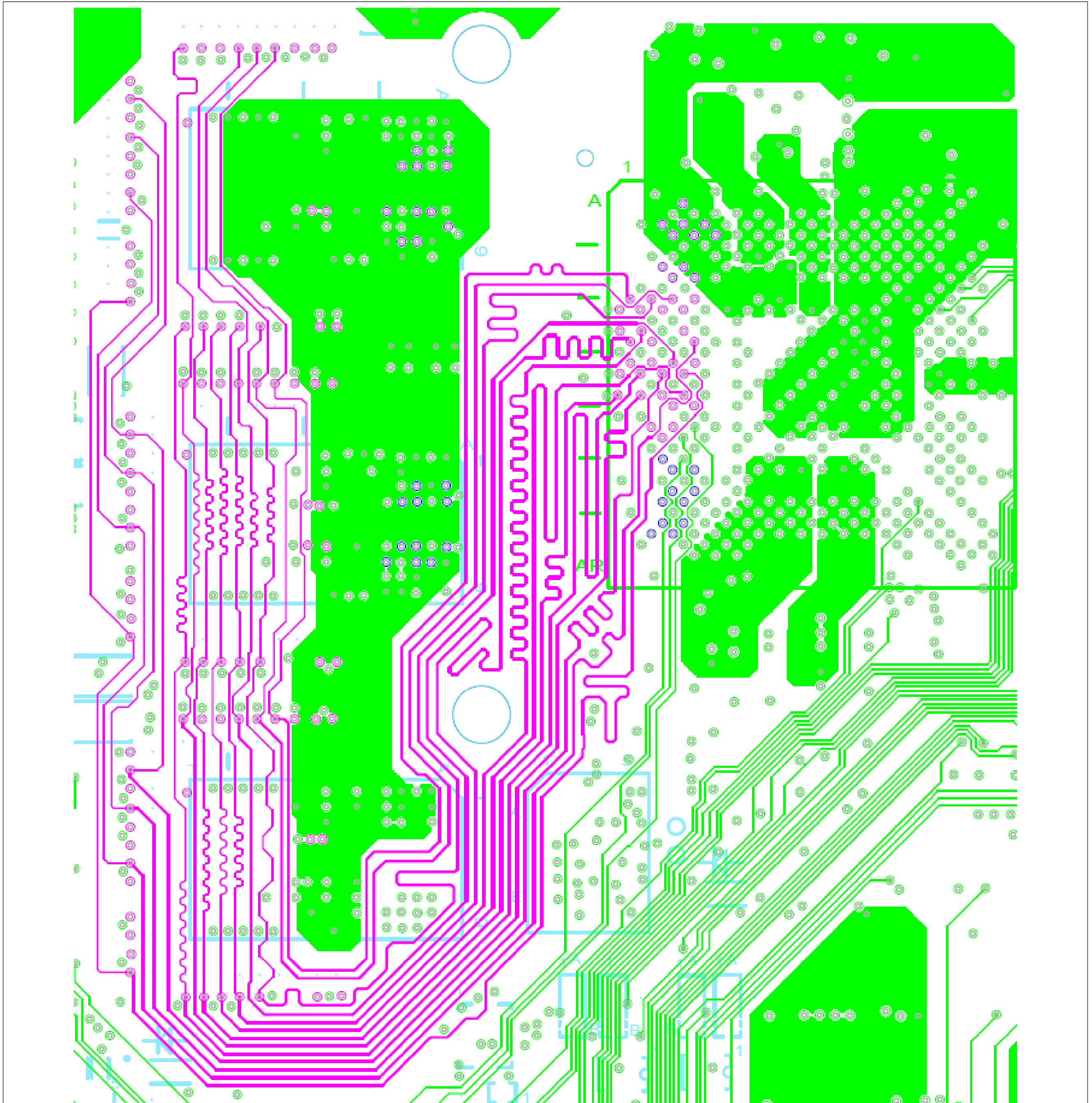

Figure 16. i.MX8 QXP development platform DDR3L routing (layer 8)

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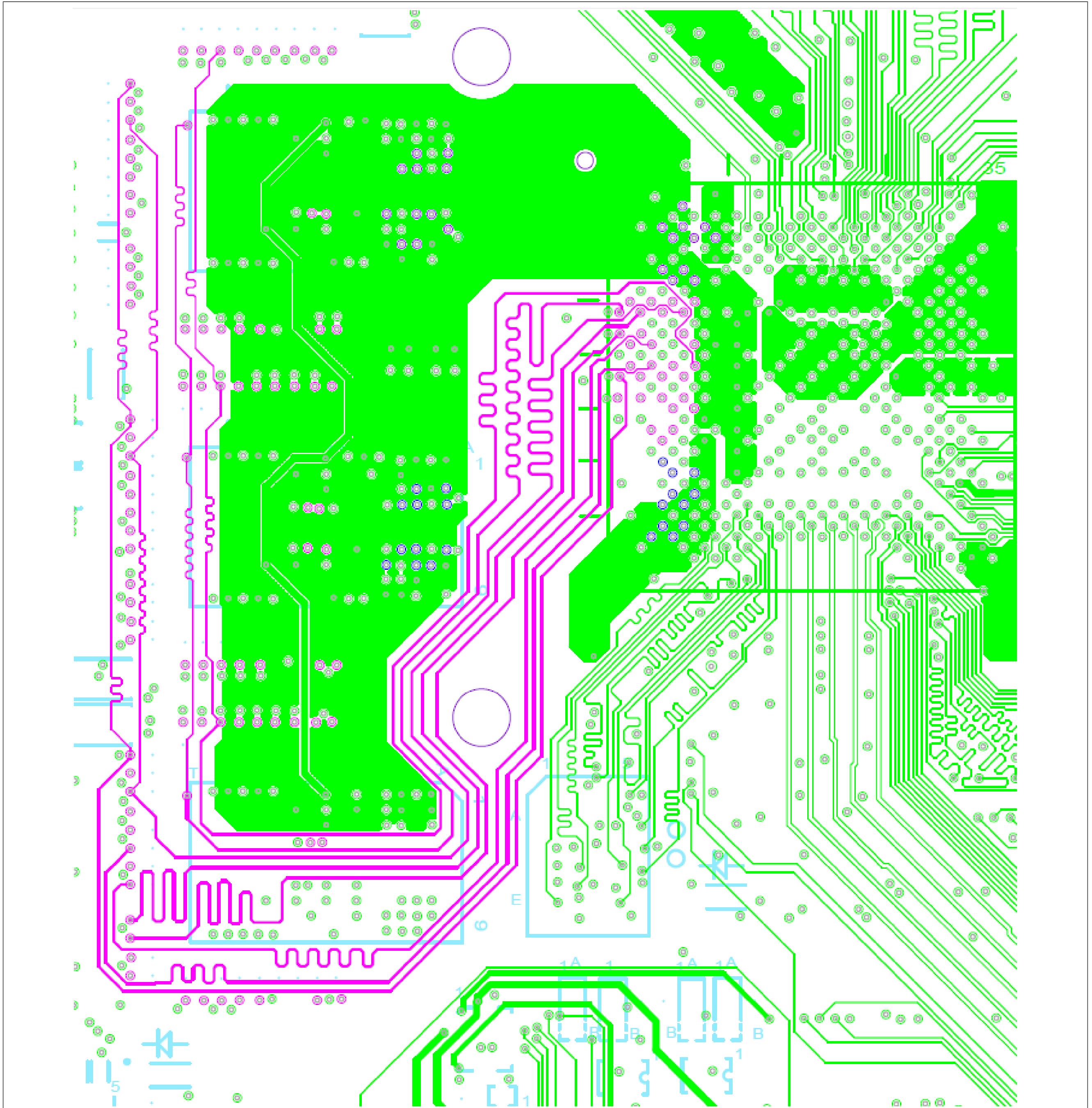

Figure 17. i.MX8 QXP development platform DDR3L routing (layer 5)

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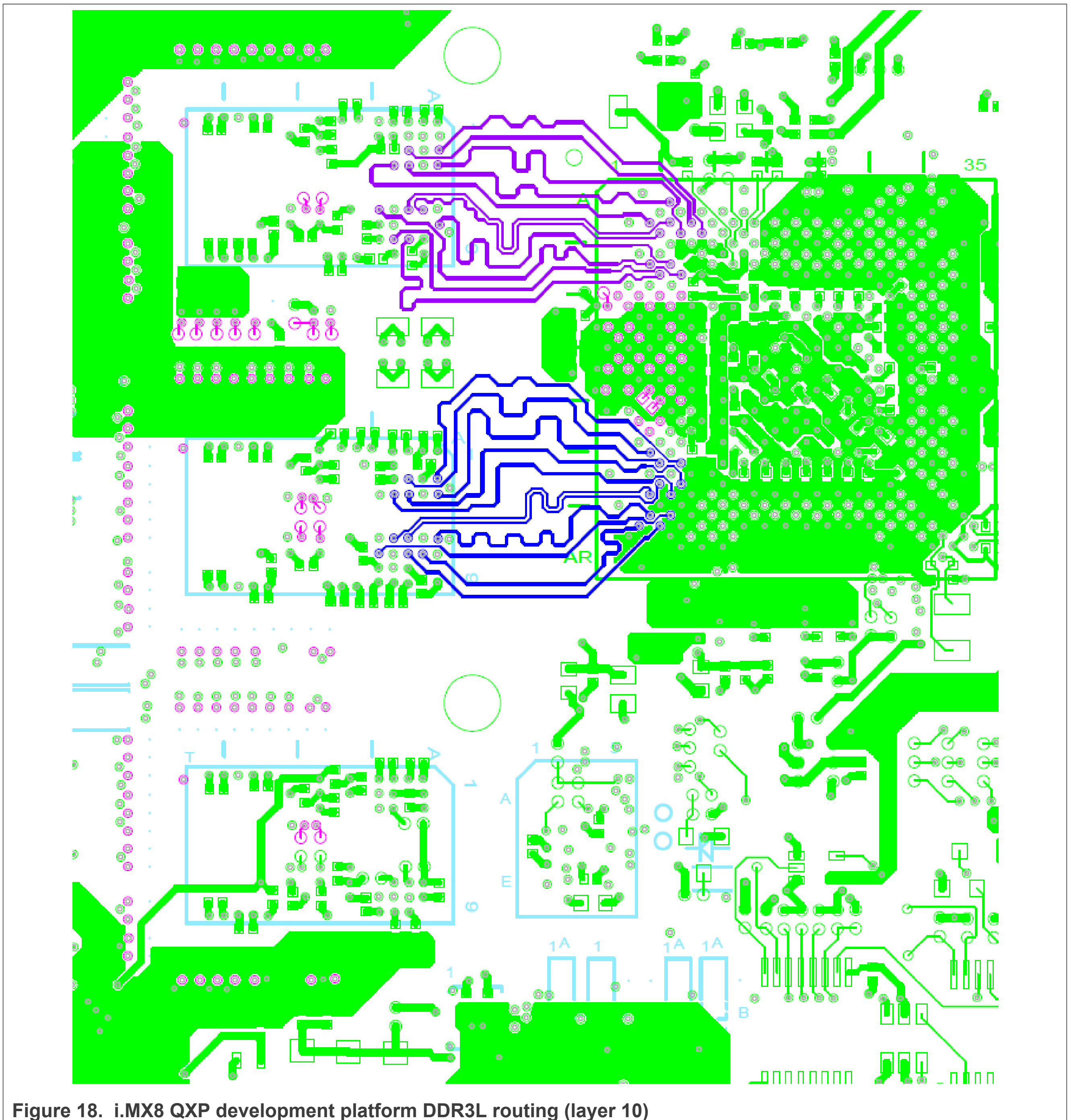

Figure 18. i.MX8 QXP development platform DDR3L routing (layer 10)

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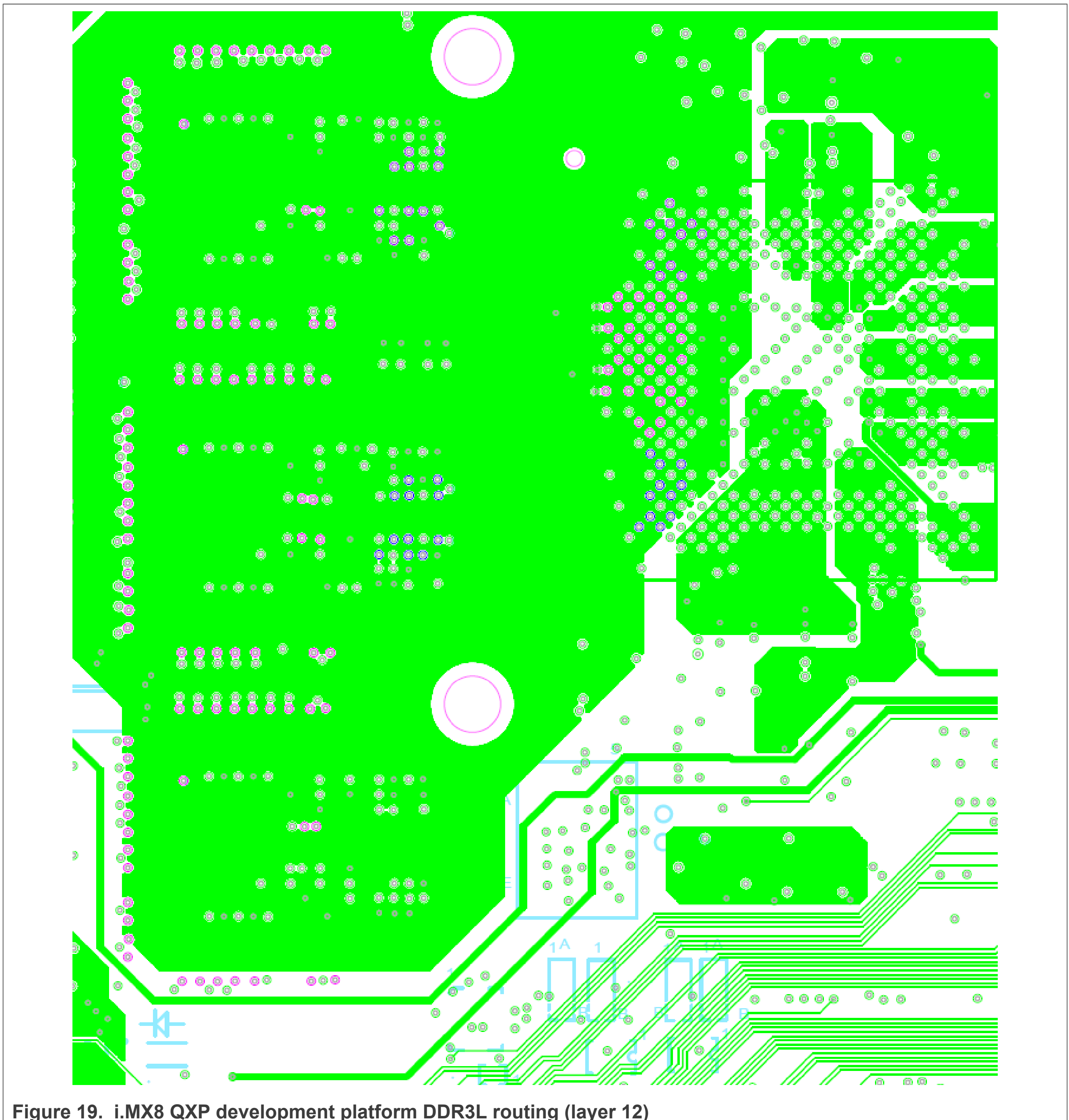

Figure 19. i.MX8 QXP development platform DDR3L routing (layer 12)

3.4.13 i.MX8 DXL DDR3L-1866 routing recommendations

Note: *It is strongly recommended to adopt NXP layout (if possible). The design files are available upon request.*

DDR3L-1866 must be routed with signal fly times matched, as shown in Table 33. If the matched groups are not all routed on the same layers with the same number of via transitions, the trace length/delay of the via transitions must be included in the overall calculation.

NXP recommends to simulate the DDR3L implementation before fabricating PCBs.

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Note: i.MX8 DXL supports only single-rank designs with DDR3L.

Table 33. i.MX8 DXL DDR3L-1866 routing recommendations

DDR3L-1866				
DDR3L	**Group**	**PCB and Package Prop Delay**		**Considerations**
		Min	**Max**	
CK_t/CK_c	Clock	As short as possible	225 ps	Match the true/ complement signals within 2 ps Incorporate package delay into the constraint manager.
ADDR[15:0]	Address Command Control	CK_t – 2 ps	CK_t + 2 ps	Incorporate package delay into constraint manager.
BA[2:0],CAS,RAS,WE				
CKE,CS,RESET,ODT				
DQ[7:0]	Byte 0	DQS0_t – 2 ps	DQS0_t + 2 ps	Match the true/ complement signals within 2 ps Incorporate package delay into the constraint manager.
DMI0				
DQS0_t/DQS0_c		As short as possible	CK_t	
DQ[15:8]	Byte 1	DQS1_t – 2	DQS1_t + 2 ps	
DMI1				
DQS1_t/DQS1_c		As short as possible	CK_t	

3.4.14 i.MX 8DXL DDR3L-1866 validation board

The i.MX8 DXL DDR3L validation board is based on point-to-point design with one 16-bit DDR3L memory device. The termination of the address/command/control bus to VTT is not used.

The following figures show the placement and routing of the DDR3L signals on the i.MX8 DXL DDR3L validation board.

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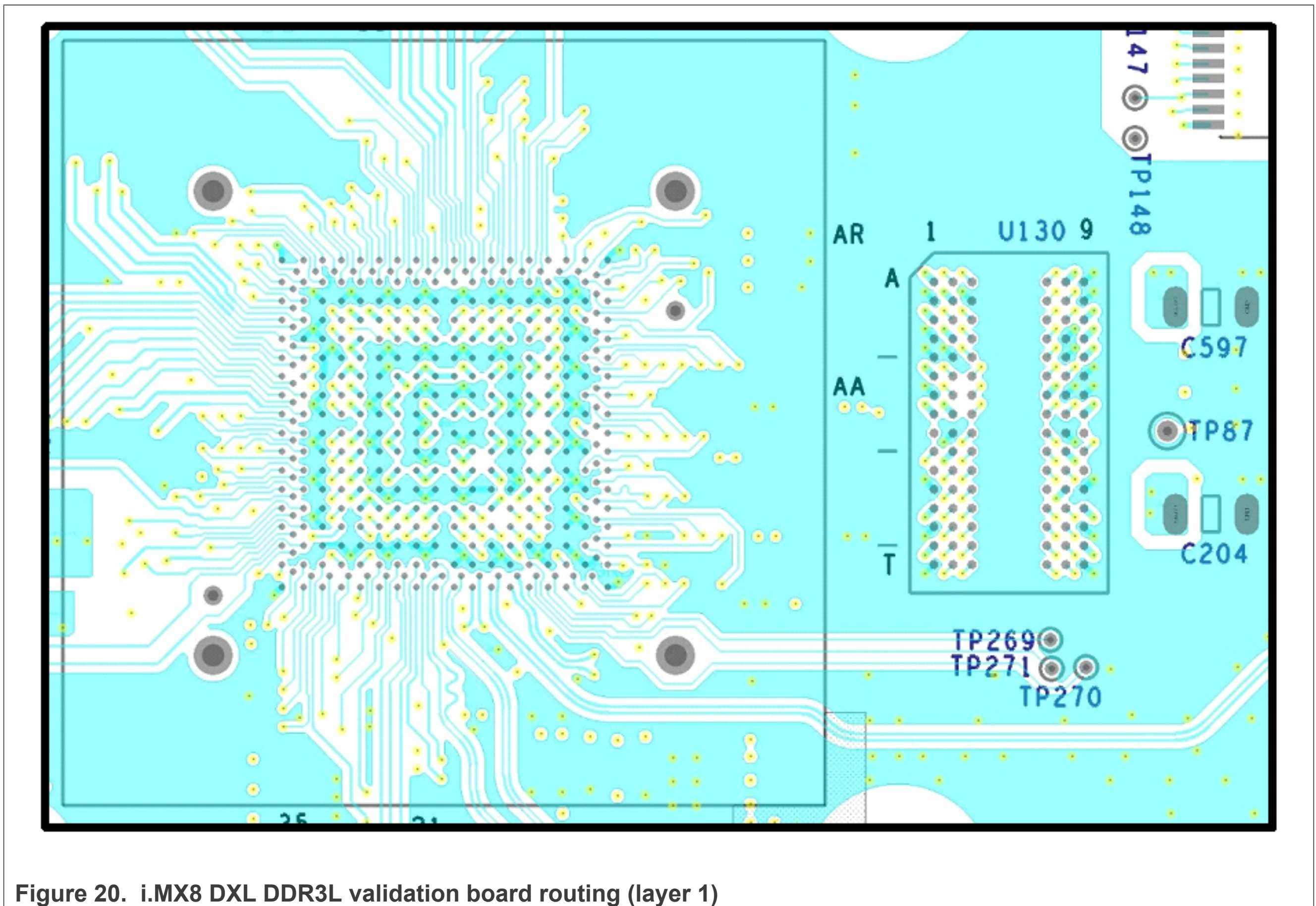

Figure 20. i.MX8 DXL DDR3L validation board routing (layer 1)

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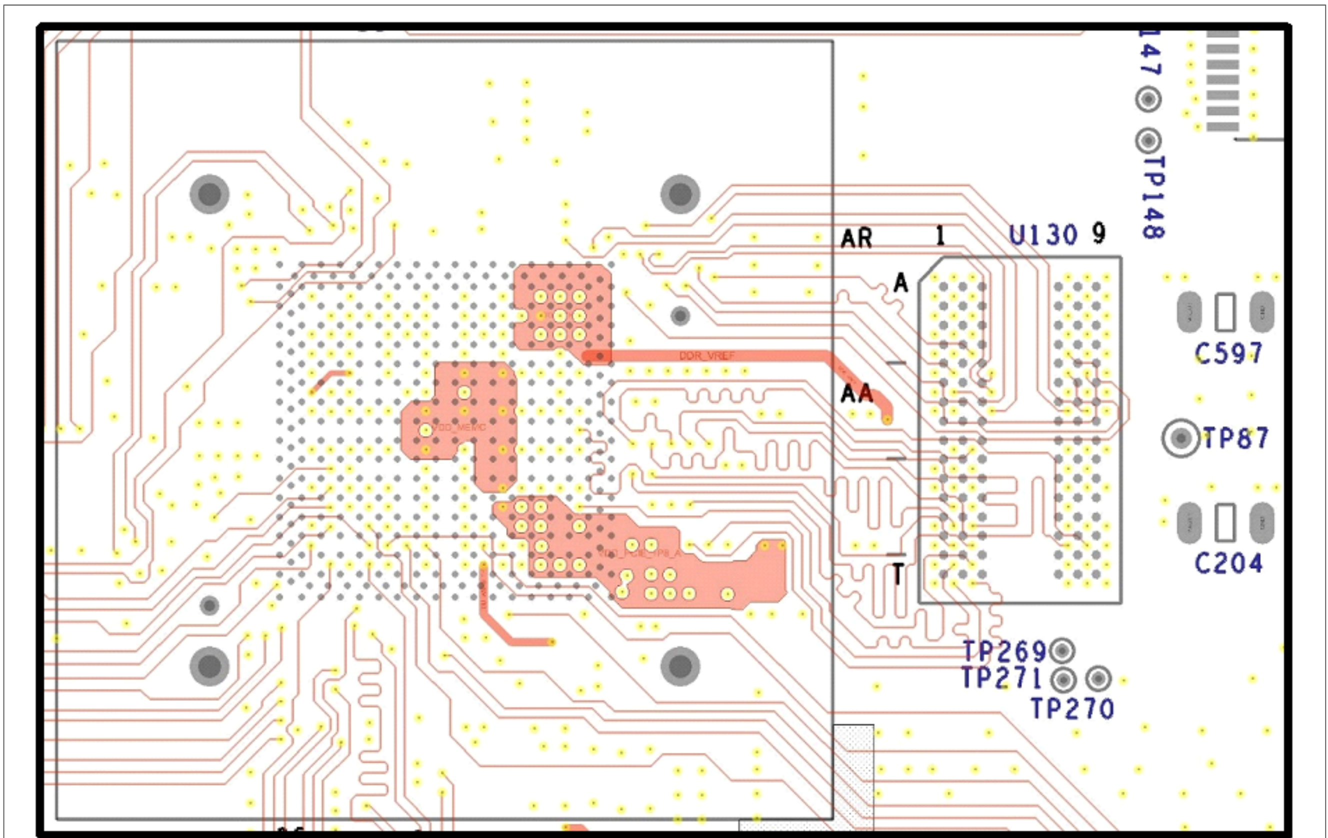

Figure 21. i.MX8 DXL DDR3L validation board routing (layer 3)

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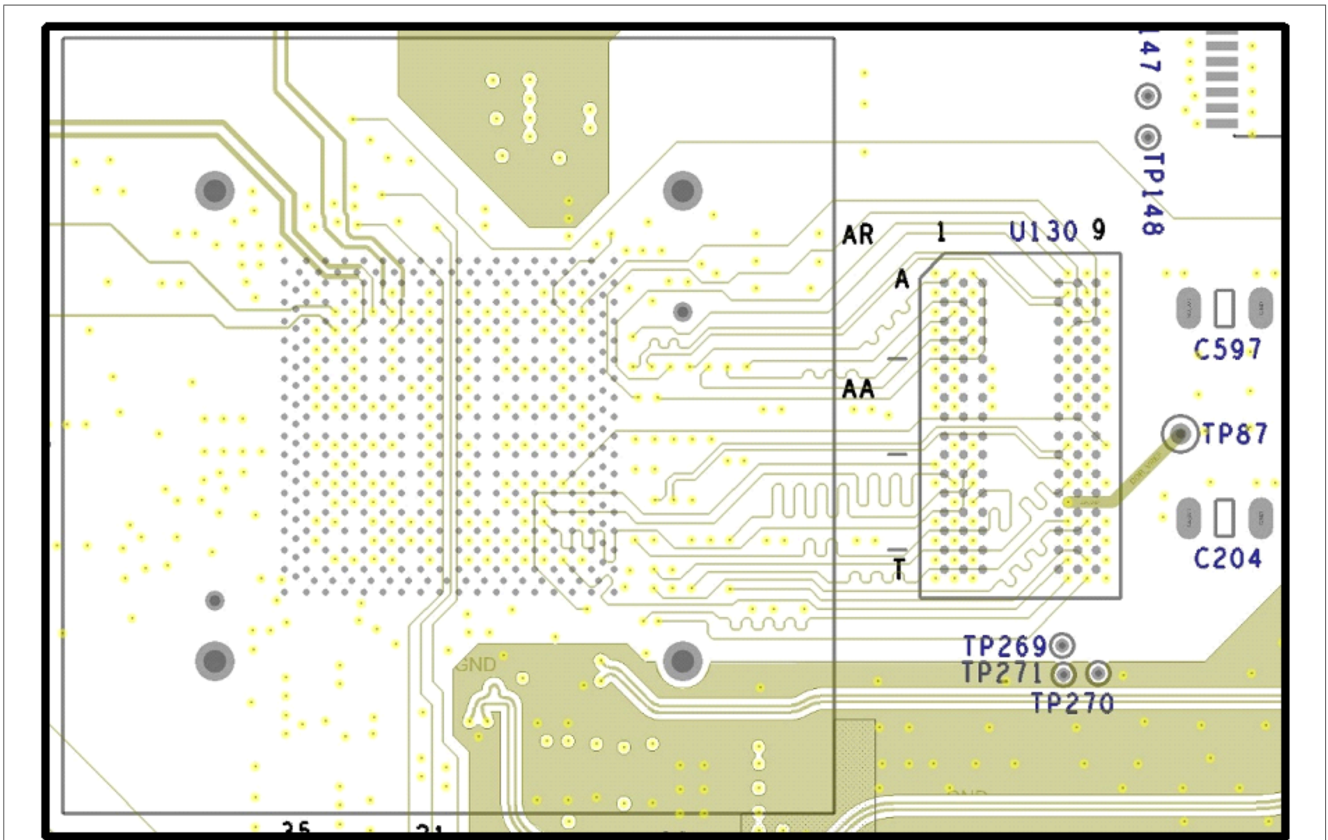

Figure 22. i.MX8 DXL DDR3L validation board routing (layer 9)

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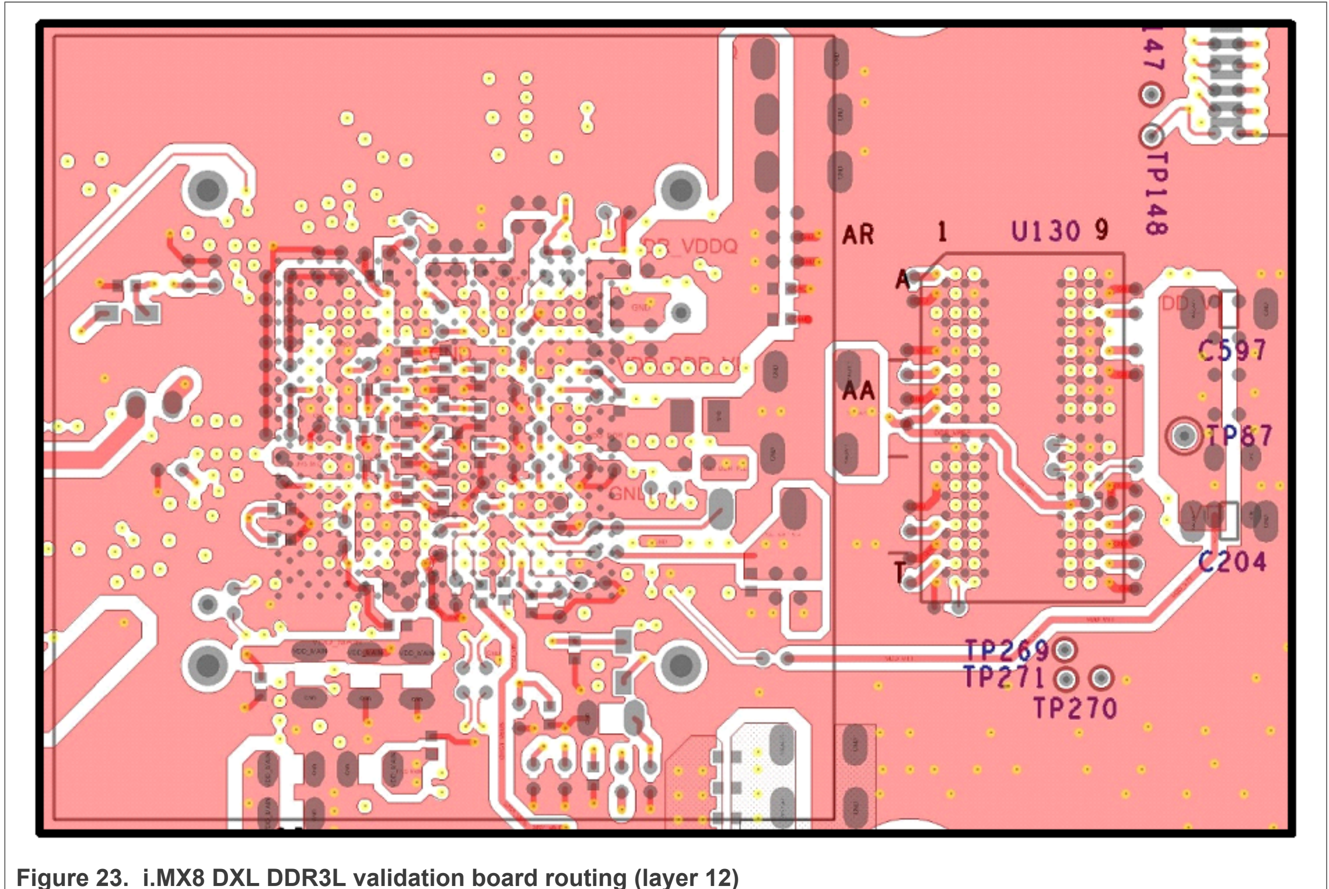

Figure 23. i.MX8 DXL DDR3L validation board routing (layer 12)

3.4.15 DRAM SI simulation guide

The simulation architecture includes the DDR controller (i.MX8 processor), the PCB, and the DDR device. The IBIS model for the i.MX8 QM, i.MX8 QXP, or i.MX8 DXL processors is available from NXP. The DRAM device IBIS model must be obtained from the memory vendor.

The overview of how to check the SI performance of the DRAM layout is as follows:

Firstly, perform the S-parameter extraction:

- Requires a 2.5D full-wave extraction tool, such as Power-SI from Cadence.
- The bandwidth is recommended to be configured to 12 GHz.
- Reference impedance: 50 Ω for signals and 0.1 Ω for power rails.
- Coupled mode: the rise time is set to 20 ps, and the coupling coefficient is set to 1 %.

Secondly, perform the time domain simulation:

- Stimulus pattern: a 500-bit random code and a different pattern for each signal within the same byte.
- Ideal power.
- The drive strength and ODT values should match the default settings in the Register Programming Aid (RPA) for the given combination of the SoC and memory type.
- Probe at the die.
- Simulation at slow or fast corner (worst case).
- The eye waveform is triggered by aligning it with the timing reference (DQS/CLK).
- See the appropriate JEDEC standards for the Rx Mask definition: JESD209-4A for LPDDR4 and JESD79-3F for DDR3L.

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Table 34. Simulation eye width recommendations

i.MX8QM LPDDR4 Simulations – 1.6 GHz		
	JEDEC Specifications	Simulation Recommendation
CA Eye Width	Min: 375 psec	> 540 psec
DQ Write Eye Width	-	> 253 psec
i.MX8 QXP and i.MX8 DXL LPDDR4 Simulations – 1.2 GHz		
	JEDEC Specifications	**Simulation Recommendation**
CA Eye Width	Min: 500 psec	> 720 psec
DQ Write Eye Width	-	> 338 psec
i.MX8 QXP and i.MX8 DXL DDR3L Simulations – 933 MHz		
	JEDEC Specifications	**Simulation Recommendation**
CA Eye Width	-	> 980 psec
DQ Write Eye Width	-	> 468 psec

Note: *The simulation target recommendations by NXP are tighter than the JEDEC specifications to ensure any errors in simulation techniques (for example, ideal power sources) do not result in the manufactured PCB missing the required JEDEC specifications.*

Note: *NXP provides Hyperlynx timing models for the i.MX8 QM / QXP / DXL devices that can be used in this software to perform batch simulations, which can help to further asses both read and write margins.*

3.4.16 JEDEC specification compliance

The i.MX 8 family of processors are designed and tested to work with the JEDEC JESD209-4A–compliant LPDDR4 and JEDEC JESD79-3F-compliant DDR3L memories. Timing diagrams and tolerances required to work with these memories are specified in the respective documents and are not reprinted here.

Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. In this document, NXP cannot cover all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part variation. The PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, VIA placement, GND and supply planes layout, and DDR controller/PHY register settings all are factors affecting the performance of the memory system. Nevertheless, this hardware user’s guide contains a large amount of valuable design information that NXP believes aid the design engineers in developing a DRAM memory system compliant with the JEDEC standards. NXP has validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors, and DDR trace routing between the processor and the selected DDR memory.

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as a closure to a customer-reported DDR issue. Customers bear the responsibility of properly designing the printed circuit board, correctly simulating and modeling the designed DDR system, and validating the system under all expected operating conditions (temperatures, voltages) before releasing their product to the market.

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3.5 High-speed routing recommendations

For more information about general high-speed routing considerations, see *High-Frequency Design Considerations* (document AN12298).

The following list provides generic recommendations for routing traces for high-speed signals. Note that the propagation delay and the impedance control should match to ensure the correct communication with the devices.

- High-speed signals (DDR, PCIe, RGMII, MIPI) must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in reference planes. Review via placements to ensure that they do not inadvertently create splits/voids (space vias out to eliminate this possibility).
- Ensure that ground stitching vias are present within 50 mils from signal layer transition vias on high-speed signals when transitioning between different reference ground planes.
- A solid GND plane must be directly under crystals and the associated components and traces.
- Clocks or strobes that are on the same layer need at least 2.5x spacing from adjacent traces (2.5x height from the reference plane) to reduce crosstalk.
- All synchronous interfaces should have appropriate bus length matching and relative clock length control.

For SD module interfaces:

- Match the data and CMD trace lengths (allowable delta depends on the access rate used).
- CLK should be longer than the longest signal in the Data/CMD group (+5 mils).

For the FlexSPI interface:

- Routing of the FlexSPI signals must follow the above rules, because the operating frequency of the interface can reach up to 200 MHz with fast edges.

3.6 Disclaimers

Nothing in this document relieves the design engineer/customer from ultimate responsibility in producing a proper functioning DRAM subsystem that meets JEDEC specifications.

It is expected that the design engineer already has a strong understanding of PCB design using high-speed components. This is not an all-encompassing training document that can be used by beginning designers to produce reliable PCB designs using modern processors.

Design engineers should use all available design guidelines provided by the manufacturers of other high-speed components used in the system. Should a conflict arise between this document and the guidelines from other manufactures, contact NXP for resolution (community.nxp.com).

NXP strongly recommends that one of the example layouts provided for the i.MX8 designs be copied exactly for the placement of the processor, DRAM device, decoupling capacitors underneath the processor, and the interconnecting traces/vias between these parts. This includes the board stack-up design and PCB dielectric materials chosen. These designs have been tested and validated at NXP and they are proven reliable. While NXP does not expect every customer to copy our designs, customers must expect that the amount of support that can be provided for assisting a new design cannot be as great as the support provided for designs already known to NXP.

NXP provides the processor IBIS models and timing models necessary for performing complete DRAM simulations of a design. NXP strongly recommends that the end users perform simulations of any new designs before the release of a PCB layout design for manufacturing.

Processor reference manuals and user's guides are continuously reviewed and revised to contain the most up-to-date information regarding the processor. In addition, errata and engineering bulletins may be issued to document unintended processor behavior. The design engineers should consult the official NXP website for the

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latest versions of these documents as a part of the final checks of a PCB design before releasing the board to manufacturing.

When a fully assembled board is returned to the design engineer, it is the engineer's responsibility to perform a complete check of the board design to ensure that all subsystems are functioning correctly. See Section 4 for recommended board bring-up guidelines.

3.7 Trace impedance recommendations

Use Table 35 as a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 35. Trace impedance recommendations

Signal Group	Impedance	PCB Manufacturer Tolerance (+/-)
LPDDR4 signals (other than differentials)	42 Ω Single-ended (QXP)	10 %
	42-44 Ω Single-ended (QM)	
	50 Ω Single-ended (DXL)	
All user-critical signals, unless specified	50 Ω Single-ended	10 %
DDR (QM), PCIe transmit/receive data pairs	85 Ω differential	10 %
DDR (QXP), USB differential signals	90 Ω differential	10 %
Differential signals, including Ethernet, PCIe clocks, LVDS, MIPI (CSI and DSI), SATA and DDR (DXL)	100 Ω differential	10 %

Figure 24 shows the dimensions of a strip line and microstrip pair. Figure 25 shows the differential pair routing. Note the following:

- The space between two adjacent differential pairs should be greater than or equal to twice the space between the two individual conductors.
- The skew between LVDS pairs should be within the minimum recommendation (± 100 mil).

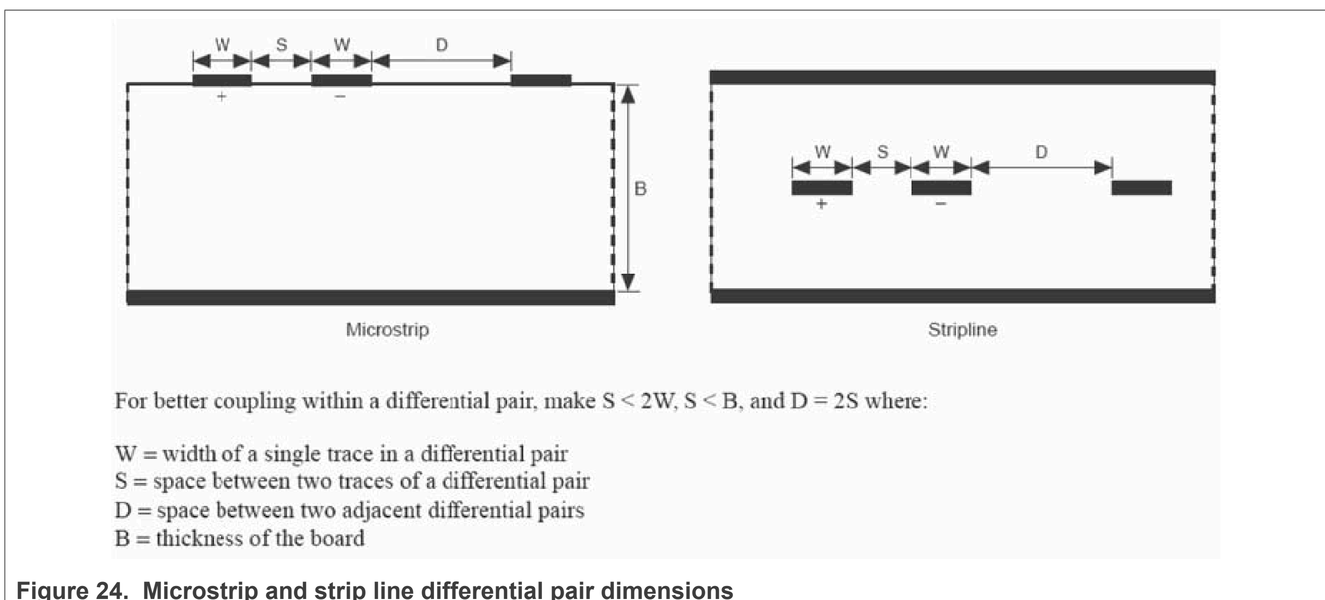

Figure 24. Microstrip and strip line differential pair dimensions

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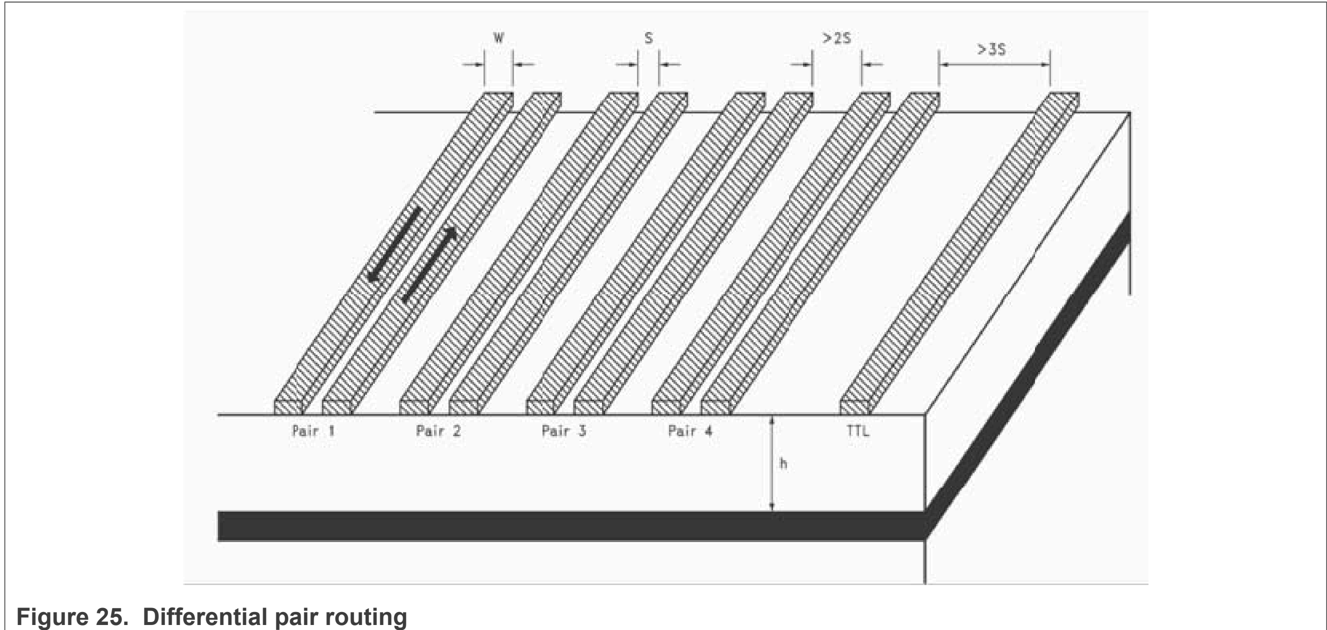

Figure 25. Differential pair routing

3.8 Reset architecture/routing

A debounced reset button may be logically connected to the PMIC WDI pin for development purposes. By default, the PMIC WDI will assert POR_B to the CPU and reset all voltages to their initial default power-on state. See Figure 26 and Figure 27 for diagrams of the recommended reset functionalities.

The depressing push-button switch SW1 (8QXP) or SW2 (8DXL) causes the supervisor IC at U5 (QXP) U105 (*DXL) to assert its RSTn output and drive POR_B_1V8 and POR_RST_3V3_B (SYS_RST_3V3_B and SYS_RST_1V8_B on 8DXL) low. This will also generate a watchdog event to the PMIC. The RSTn will be released by the supervisor IC approximately 210 ms after the push-button is released. However, the PMIC will then assert its POR_B output, which will keep the POR_B_1V8, POR_RST_3V3_B / SYS_RST_3V3_B, and SYS_RST_1V8_B asserted until the PMIC supplies have reached their operating voltages, at which time POR_B will be negated and the CPU may begin booting from reset.

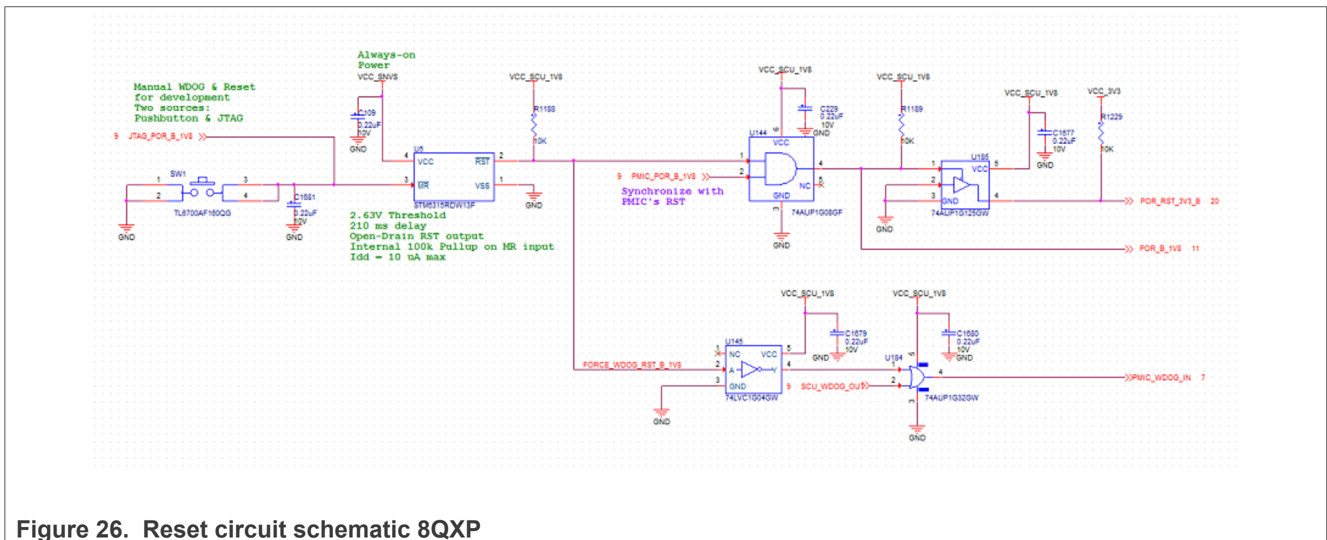

Figure 26. Reset circuit schematic 8QXP

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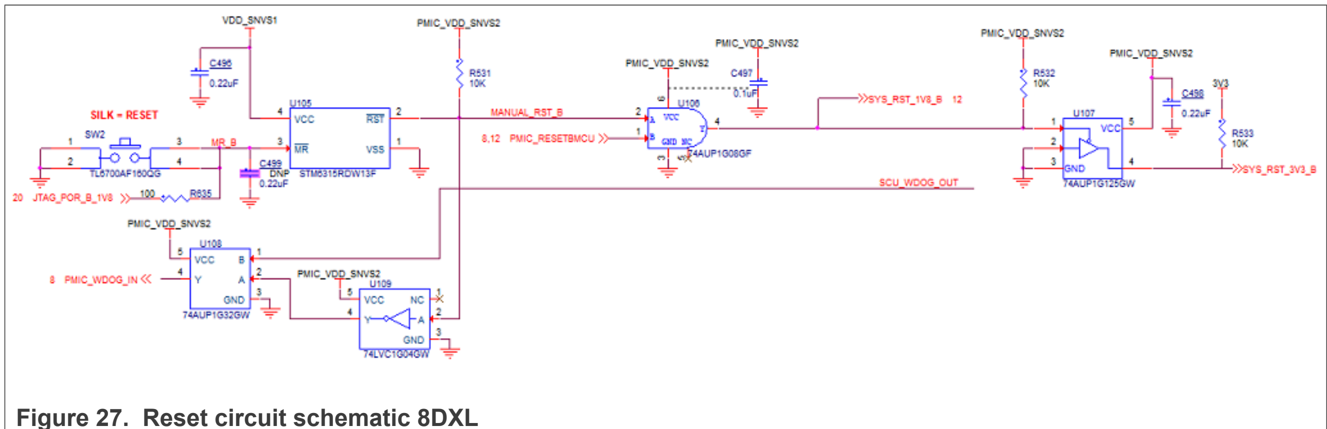

Figure 27. Reset circuit schematic 8DXL

3.9 Clock crystal considerations

3.9.1 Oscillator tolerance (24 MHz)

Table 36 provides 24 MHz oscillator tolerance guidelines (see Table 17, recommendations #3 and #4). Because these are the guidelines, the designer must verify all tolerances per the official specifications.

Table 36. 24 MHz crystal tolerance guidelines

Interface	Tolerance (± ppm)
Ethernet	50
HDMI	100
PCIE	150
SATA	350
USB2.0	150
USB3.0	150

3.9.2 Clock options (32.768 kHz)

The i.MX8 QM, i.MX8 QXP, and i.MX8 DXL reference designs utilize a crystal connected across the RTC_XTALI and RTC_XTALO balls for their 32.768 kHz clock input (see Table 17). However, the i.MX8 processor can also accept a 1.8 V logic level clock on the RTC_XTALI input. If feeding a 1.8 V logic level clock into the processor, the RTC_XTALO pin should be left unconnected.

Never drive a level higher than 1.8 V onto the oscillator input. If a 3.3 V logic level 32.768 clock signal is available, it may still be used to drive the input of the i.MX8 QM, QXP, or DXL. To do this, a 74AUP1G04 inverter can be used. This inverter has a fail-safe input that can accept input voltages higher than the supply voltage and provides faster and cleaner edges to the processor than a diode circuit.

To do this, the inverter circuit should be implemented as follows:

- Connect the 3.3 V clock source to the input of the inverter.
- Connect the output of the inverter to the 8QM / 8QXP / 8DXL RTC_XTALI ball.
- Connect the power pin of the inverter to the 1.8 V always on system rail and the inverter ground pin to the system ground.

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3.9.3 Internal load capacitor trimming (24 MHz and 32.768 kHz)

See the appropriate i.MX8 data sheet for guidelines on selecting the 24 MHz and 32.768 kHz crystals.

Choosing the appropriate crystal element for an oscillator is important. NXP recommends starting the selection process by looking at the parts chosen for NXP's MEK reference designs. Whilst many different crystals can work to create a successful oscillator, NXP has the most experience with the crystal model on the MEK.

Start-up time for the 24 MHz oscillator is monitored by the ROM code. It must be stable within 5 milliseconds of POR_B de-asserting, or the boot process will fail. If a crystal start-up violates this limit, a reset will occur. Longer start-up times are associated with crystals with higher series resistance. It is importance to select a crystal with an ESR of less than 60 Ω. Higher load capacitances will also result in longer start-up times. It is important to consider parasitic capacitances present in the PCB and device pin when selecting the desired internal load capacitor. However, a correct operating frequency is also dependent on load capacitance. Choosing too small a value for start-up reasons may result in an incorrect operating frequency.

Selecting the correct crystal load capacitance (C_L) is an important part of any oscillator design, because it impacts the clock performance, stability, and start-up time. Typically, higher C_L values should be used for higher clock performance. However, as many factors (including board layout) can impact performance, NXP recommends characterization testing to be carried out with the selected crystal vendor.

i.MX8 QM, i.MX8 QXP, and i.MX8 DXL provide programmable internal load capacitors for both the 24 MHz and 32.768 kHz oscillator designs. Although external load capacitors can be used, NXP has designed this module to use internal capacitors, because they are less impacted by external factors, whilst providing an overall cost saving.

Default internal C_L values are provided for both the 24 MHz (20 pF) and 32.768 kHz (16 pF) oscillators to enable the initial boot and testing. If it is determined that the default values are not appropriate after the crystal characterization is completed, fuse settings (Fuse Row Index 768) can be used to trim the internal C_L value.

The default values were selected specifically for the MEK reference designs and should prove good enough for other designs in general.

Note: *The impact of stray capacitance C_{stray} [1), typically 16 pF [2), should be included when programming trimmed values, for example $C_L = (C_{L1} \times C_{L2})/ (C_{L1} + C_{L2}) + C_{stray}/2$. Then the needed trim value can be estimated [3) as $C_{trim} = 2 \times C_L - C_{stray}$. For the 24 MHz crystal, usage of the internal capacitors is strongly recommended to reduce the cost and simplify the PCB layout. A 24 MHz crystal with C_L equal to or larger than 12 pF is recommended.*

The following is an example of calculation for a crystal with C_L = 12 pF:

$C_{trim} = 2 \times C_L – C_{stray} = 2 \times 12 – 16 = 8$ pF

[1) C_{stray} is understood as the cumulative effect of the typical PCB parasitic capacitance and the on-chip and package capacitances.

[2) The value is per-pin and applicable only for the pins of the 24 MHz crystal.

[3) Characterization must be performed to confirm the correct trim setting.

Table 37. Fuse row index 768

Bits	Description
31	BRD_OSC_24M_TRIM_VALID 0 – use 20 pF default value 1 – use **TRIM_VALUE_24M**
30	Reserved (**MUST BE 0**)
29	BRD_OSC_32K_TRIM_VALID 0 – use 16 pF default value

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Table 37. Fuse row index 768*...continued*

Bits	Description
	1 – use **TRIM_VALUE_32K**
28..20	Reserved
19..16	BRD_OSC_CAP_**TRM_VALUE_32K** See Section 3.9.3
15..4	Reserved
3..0	BRD_OSC_CAP_**TRIM_VALUE_24M** See Section 3.9.3

Note 1: The fuse row index 768 is a one-time only programmable 32-bit word. Programming bit 30 to 1 may result in parts that are unable to boot and they will have to be replaced.

Note 2: The trim values are listed per capacitor. For example, if the default value is set for BRD_OSC_CAP_TRM_VALUE_32K (0000), CL1 = 16 pF, CL2 = 16 pF.

Table 38. BRD_OSC_CAP_TRM_VALUE_32K

BRD_OSC_CAP_TRM_VALUE_32K[19..16]	CL1 and CL2 capacitance
1000	0 pF
1001	2 pF
1010	4 pF
1011	6 pF
1100	8 pF
1101	10 pF
1110	12 pF
1111	14 pF
0000 (default)	16 pF
0001	18 pF
0010	20 pF
0011	22 pF
0100	24 pF
0101	26 pF
0110	28 pF
0111	30 pF

Table 39. BRD_OSC_CAP_TRM_VALUE_24M

BRD_OSC_CAP_TRM_VALUE_24M[3..0]	CL1 and CL2 capacitance
0000	0 pF
0001	2 pF
0010	4 pF
0011	6 pF
0100	8 pF
0101	10 pF
0110	12 pF
0111	14 pF
1000	16 pF
1001	18 pF
1010 (default)	20 pF

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Table 39. BRD_OSC_CAP_TRM_VALUE_24M

BRD_OSC_CAP_TRM_VALUE_24M[3..0]	CL1 and CL2 capacitance
1011	22 pF
1100	24 pF
1101	26 pF
1110	28 pF
1111	30 pF

Note: *The 32K trim value is a signed offset from the default value of 16 pF, whereas the 24M trim value is an unsigned offset starting from 0.*

The fuses can be programmed in a number of ways, for example with the SCU debug monitor commands

```
fuse.w fuse_row_index value and fuse.r fuse_row_index
or with the uboot commands fuse prog 0 fuse_row_index value
and fuse read 0 fuse_row_index.
```

3.9.4 XTALI specifications (8DXL)

The 24 MHz oscillator can be driven with an external signal at the XTALI pin. The requirements for the external signal are shown in Table 40. The input voltage should never exceed the oscillator supply voltage.

Table 40. XTALI specifications (8DXL)

		Note
Vcm	900 mV or VDDXTAL/2	common voltage/ DC offset on XTALI
Vpp	> 600 mV	xtal-extal/input signal level (pp)
Duty cycle	45-55 %	

3.10 Power connectivity/routing

Delivering clean and reliable power to the i.MX8 QM, i.MX8 QXP, and i.MX8 DXL internal power rails is critical to a successful board design. The PCB PDN should be designed to accommodate the maximum output current from each SMPS into the i.MX8 supply balls. See Table 41 for the design goals for each of the high-current i.MX8 QM, i.MX8 QXP, and i.MX8 DXL power rails.

Table 41. i.MX8 maximum current design levels

Supply Input	i.MX8 QM Max Current	i.MX8 QXP Max Current	i.MX8 DXL Max Current
VDD_MAIN	5A	5A	2.5A
VDD_GPU0(1)	5A	2.5A	----
VDD_GPU1	5A	-----	----
VDD_A72	5A	-----	----
VDD_A53	2.5A	-----	----
VDD_A35	-----	2.5A	----
VDD_DDR_CH0	2.5A	-----	----
VDD_DDR_CH1	2.5A	-----	----
VDD_DDR_VDDQ	-----	1.2A(2)	0.7A(2)

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Table 41. i.MX8 maximum current design levels...*continued*

Supply Input	i.MX8 QM Max Current	i.MX8 QXP Max Current	i.MX8 DXL Max Current
VDD_MEMC	2.5A	-----	2.5A

1. *There is only a single GPU power rail on the i.MX8 QXP*
2. *This does not include the current used by the external memory*

3.10.1 i.MX8 QM / QXP / DXL power distribution block diagram

There are companion PMICs that provide a low-cost and efficient solution for powering the i.MX8 QM, i.MX8 QXP, and i.MX8 DXL processors.

Figure 28 shows a block diagram of the power tree of the NXP i.MX8 QM development platform. It uses two PF8100 PMICs to supply the power rails of the QM processor.

Figure 29 shows a block diagram of the power tree of the NXP i.MX8 QXP development platform. It uses a single PF8100 PMIC to supply the power rails of the QXP processor.

Note: *There are two companion power ICs that may be used (PF8100 and PF8200). These parts are substantially the same (the PF8200 contains monitoring circuitry to support ASIL B safety level). Even though the NXP development platforms utilize the PF8100, the PF8200 can be used in its place.*

Figure 30 shows a block diagram of the NXP i.MX8 DXL development platform power tree. It uses a single PF7100 PMIC to supply the power rails of the DXL processor. For i.MX8 DXL, it is recommended to add 100-uF capacitors to the PMIC outputs that supply the VDD_DDRIO and VDD_1V8 power rails, because it improves the stability of the DDR interface. See the reference design for a specific implementation.

Note: *If the FS5600 device is used (i.MX8 DXL), it is recommended to add a 1-uF decoupling capacitor to its VDDIO pin and place it close to this pin. This helps to avoid possible ESD damage. See the reference design for a specific implementation.*

Note: *If you implement the power measurement infrastructure using shunt resistors, pay attention to the resistance values, because the resistors may have significant impact on the stability of the power rails and increase the voltage ripple beyond acceptable values if a high value is chosen. If you encounter this issue, replace the shunt resistors by 0R resistors to verify it.*

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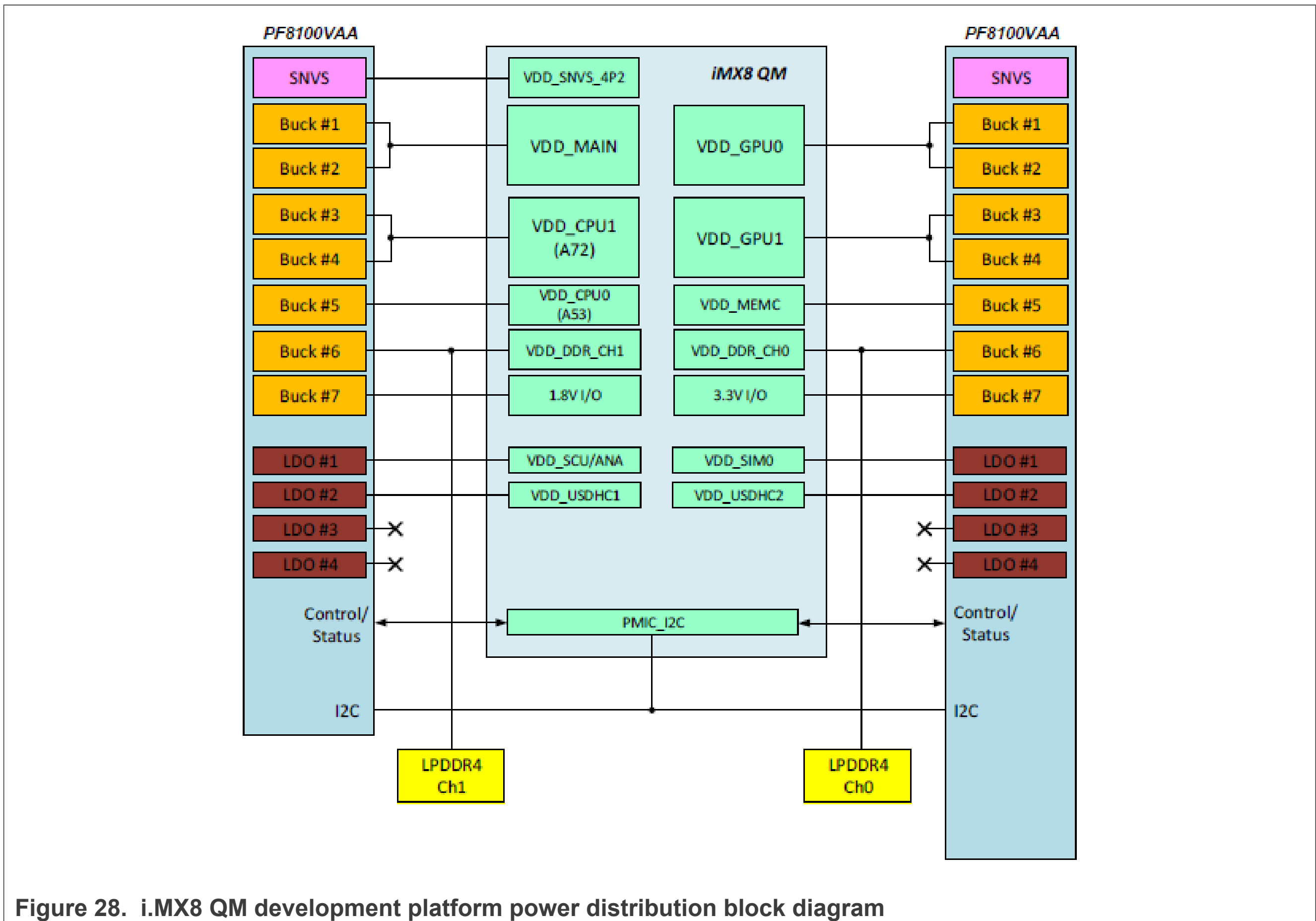

Figure 28. i.MX8 QM development platform power distribution block diagram

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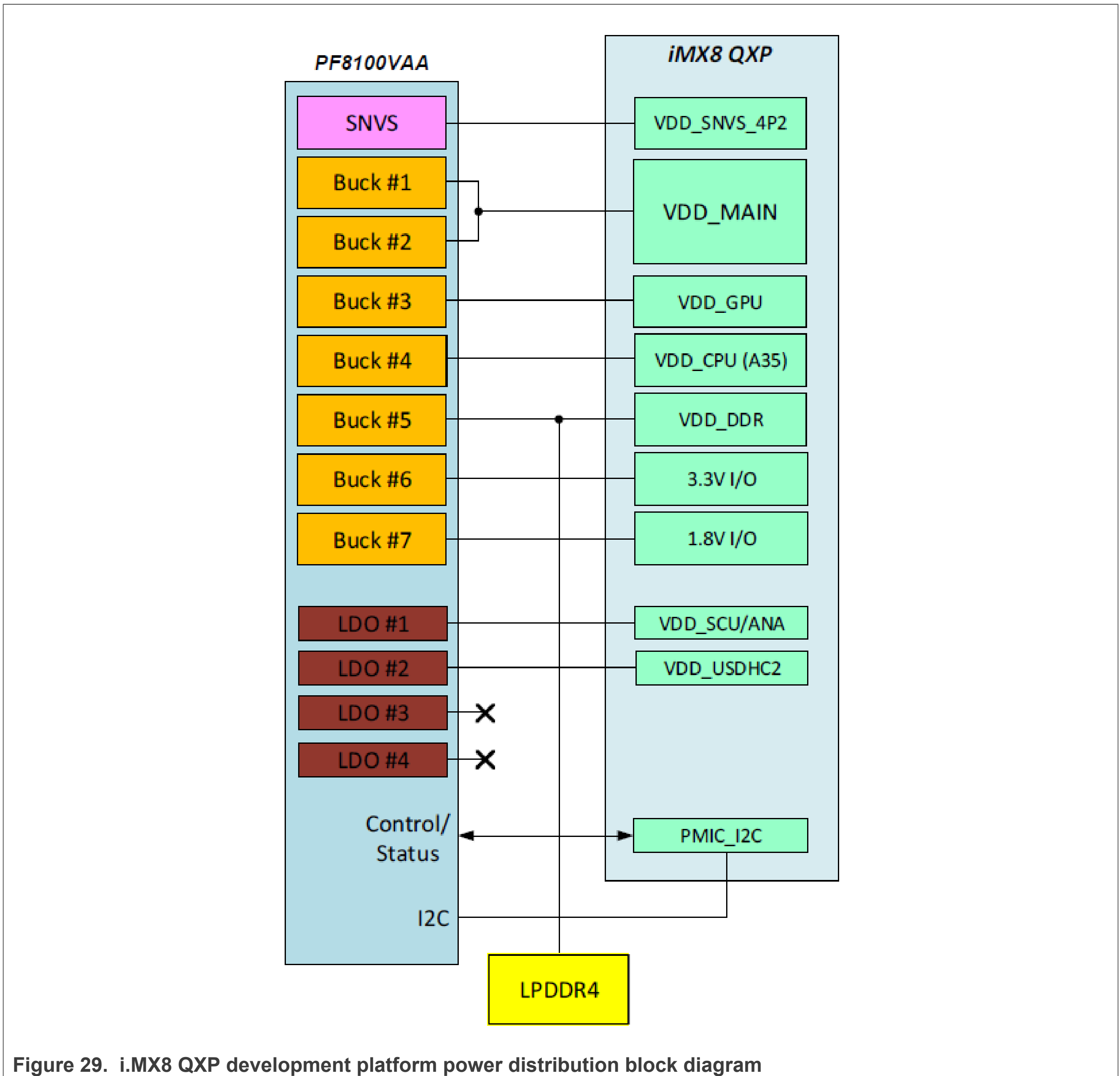

Figure 29. i.MX8 QXP development platform power distribution block diagram

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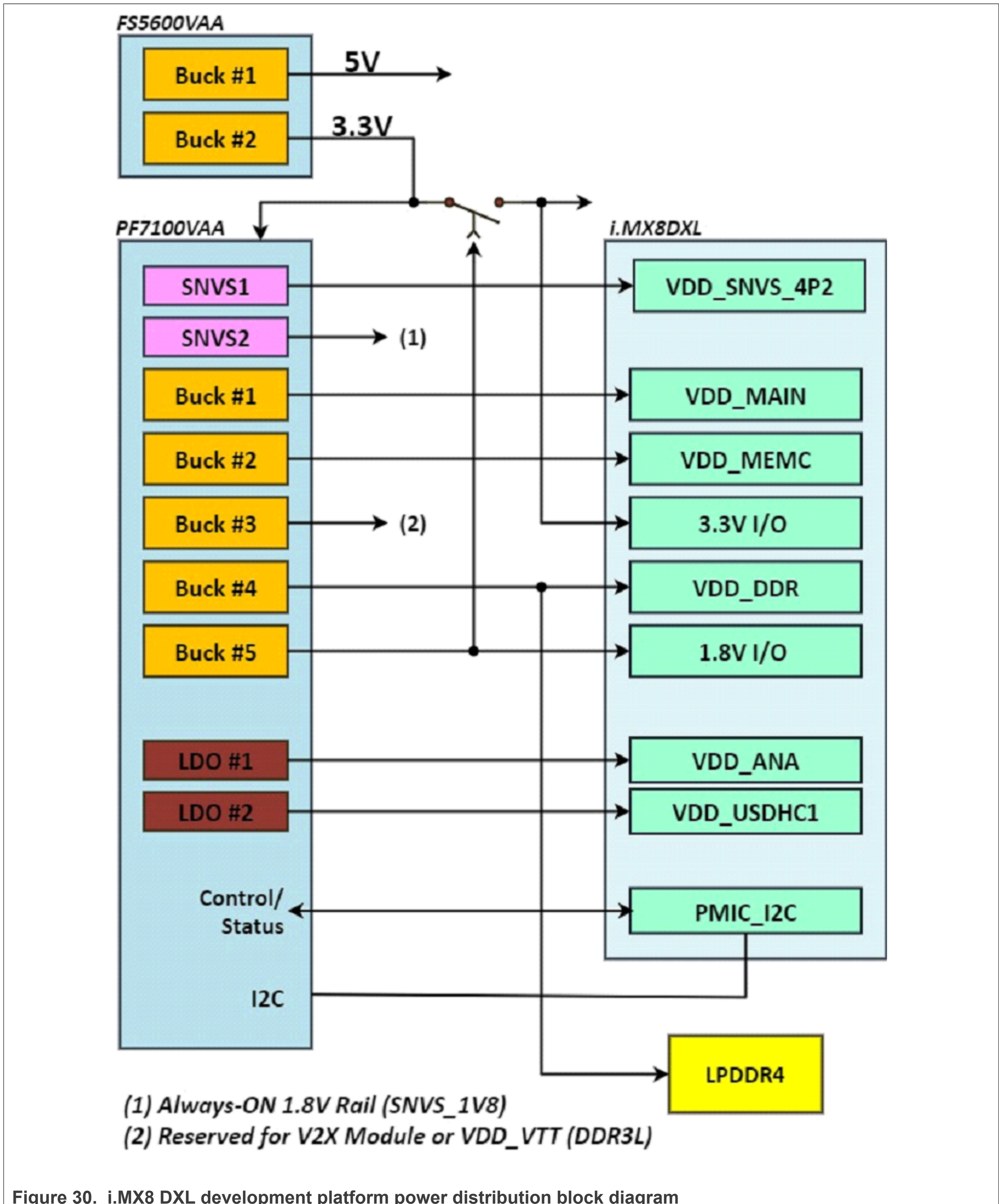

Figure 30. i.MX8 DXL development platform power distribution block diagram

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3.10.2 Power routing/distribution requirements

Designing a good Power Delivery Network (PDN) requires multiple steps to be completed. These steps include:

1. Choose a good PCB stack-up (adequate Cu thicknesses, and layer assignments/utilization).
2. Optimize the placement and routing of the PDN. This includes good placement of the decoupling capacitors and connecting them to the power ground planes with as short and wide trace/plane as possible (because the increased inductance of a longer etch will degrade the effectivity of the capacitor). Using the number/ placement of capacitors on the NXP development platforms is recommended. This is required also for the PCB connectivity associated with the internal LDOs (VDD_xxx_CAP).
3. Optimize the static IR drop. This involves using very wide traces/plane fills to route high-current power nets and ensure an adequate number of vias on the power net layer transitions. The neck down of fill areas and the current density should be minimized. The maximum static IR drop on a board should be 1 % of the voltage rail (on a 1.1 V rail, the maximum voltage drop should be 0.011 V).
4. AC resonance check – the target impedance at different frequencies should be near or below the specified values.
5. See Table 42 and Table 43 for the impedance targets vs. the frequency for the specified power rails for the i.MX8 QM, i.MX8 QXP, and i.MX8 DXL PCB designs, respectively.

Snapshots of the PDN breakout/routing for the i.MX8 QM development platform are included for illustrative purposes. Figure 31 shows the breakout of the high-current rails supplied by PMIC #1, while Figure 32 shows the breakout of the high-current rails supplied by PMIC #2.

Figure 33, Figure 34, Figure 35, and Figure 36 show how each of these rails is connected to the i.MX8 QM. Note that many rails are connected on multiple layers (VCC_CPU0/VCC_CPU1 on power layers 1 and 2, VCC_GPU0/VCC_GPU1 on layers 1 and 4, and VDD_MEMC on power layers 2 and 4).

Table 42. i.MX8 QM PDN impedance targets

Supply Input	< 20 MHz (max mΩ)	20 - ~ 100 MHz (max mΩ)
VDD_MAIN	20 mΩ	100 mΩ
VDD_GPU0	32 mΩ	160 mΩ
VDD_GPU1	32 mΩ	160 mΩ
VDD_A72	30 mΩ	150 mΩ
VDD_A53	50 mΩ	250 mΩ
VDD_DDR_CH0	30 mΩ	150 mΩ
VDD_DDR_CH1	30 mΩ	150 mΩ
VDD_MEMC	30 mΩ	150 mΩ

Table 43. i.MX8 QXP PDN impedance targets

Supply Input	< 20 MHz (max mΩ)	20 - ~ 100 MHz (max mΩ)
VDD_MAIN	11 mΩ	50 mΩ
VDD_DDRIO	20 mΩ	84 mΩ
VDD_GPU_1P1	21 mΩ	107 mΩ
VDD_CPU_1P1	24 mΩ	133 mΩ

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Table 44. i.MX8 DXL PDN impedance targets

Supply Input	< 20 MHz (max mΩ)	20 - ~ 100 MHz (max mΩ)
VDD_MAIN	20 mΩ	90 mΩ
VDD_MEMC	25 mΩ	115 mΩ
VDD_DDR_VDDQ	25 mΩ	115 mΩ

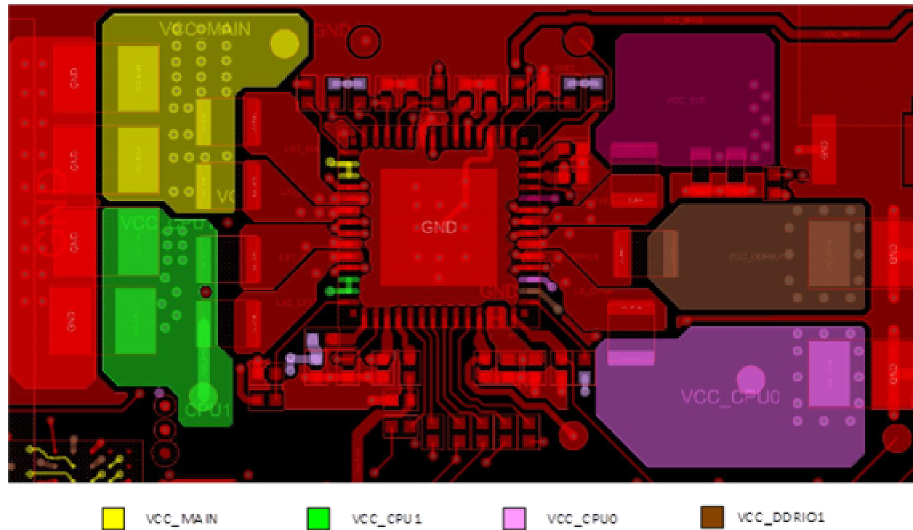

Figure 31. PMIC #1 (U10) top side power breakout

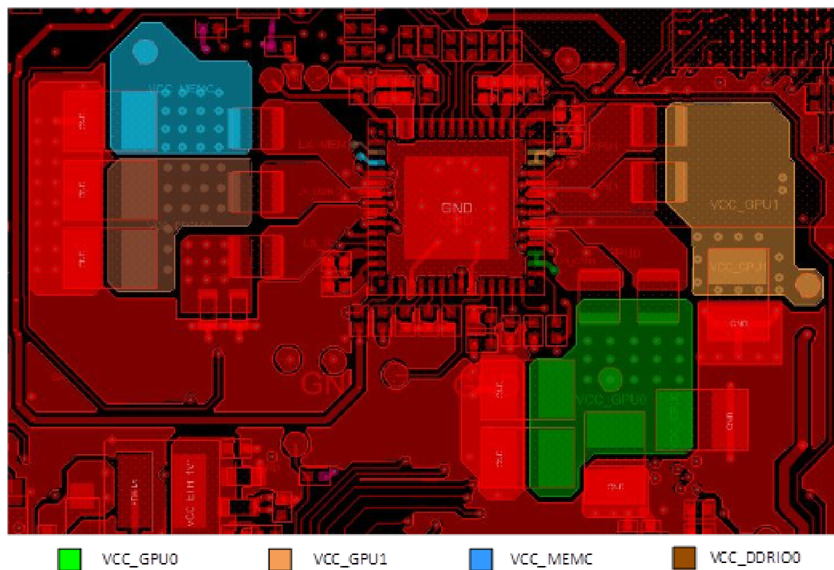

Figure 32. PMIC #2 (U23) top side power breakout

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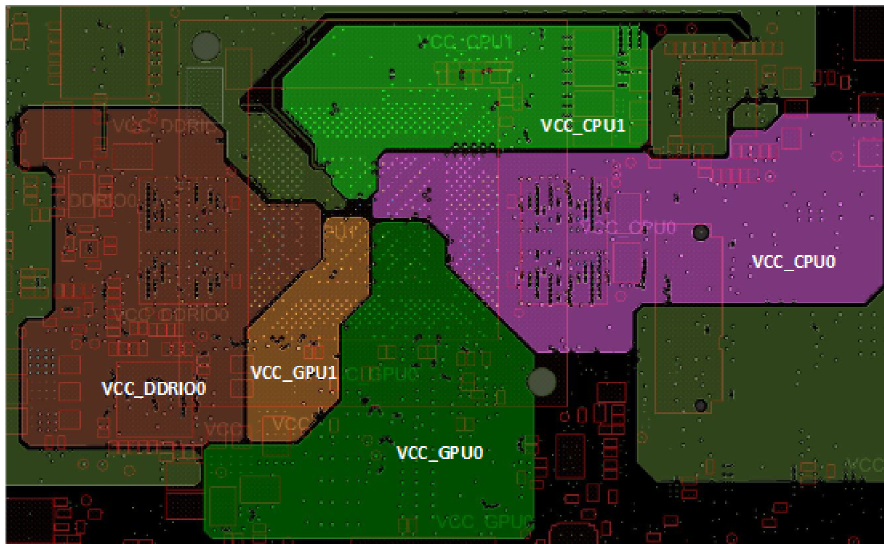

Figure 33. Power layer #1 routing

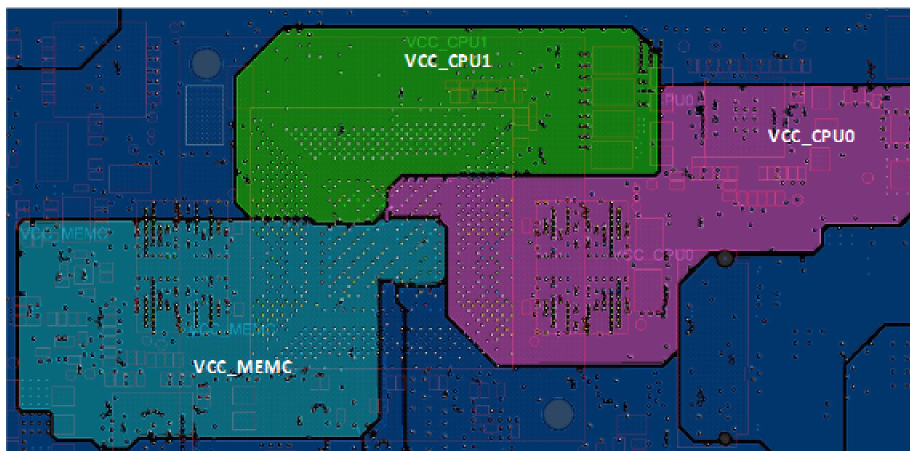

Figure 34. Power layer #2 routing

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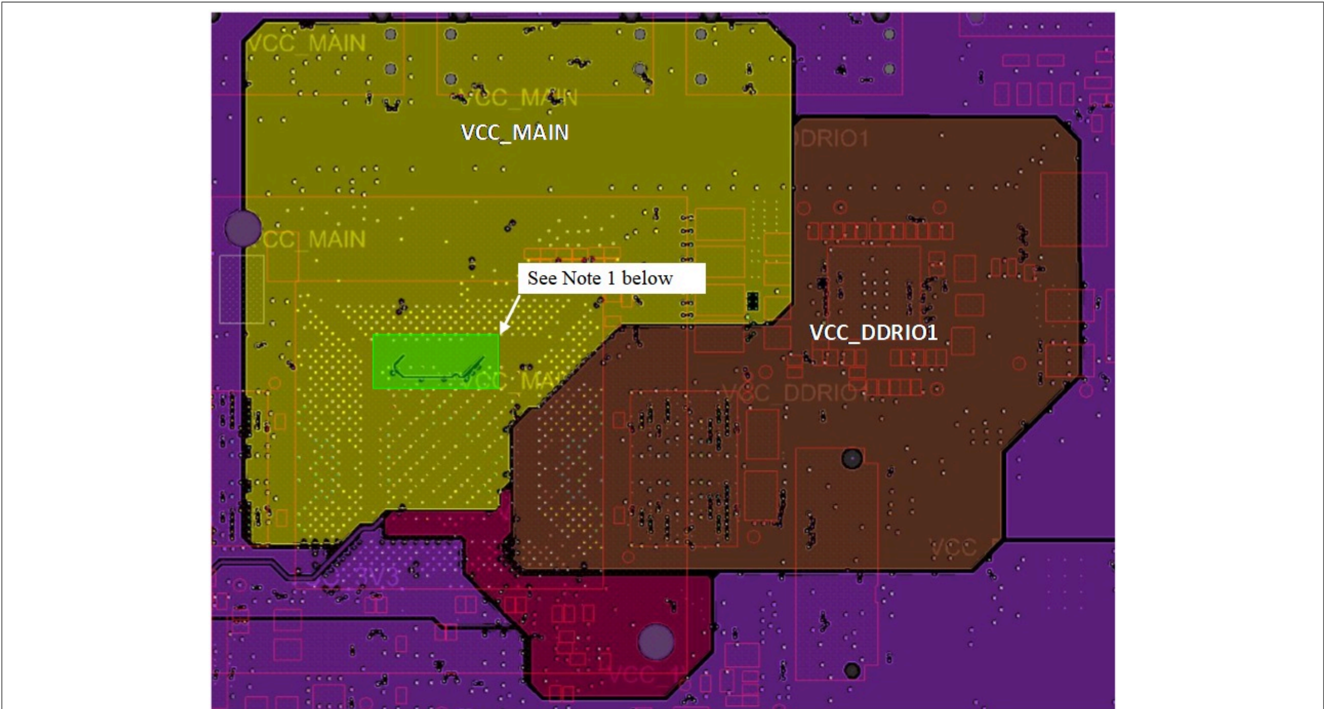

Figure 35. Power layer #3 routing

Note 1: The area shown in Figure 37.

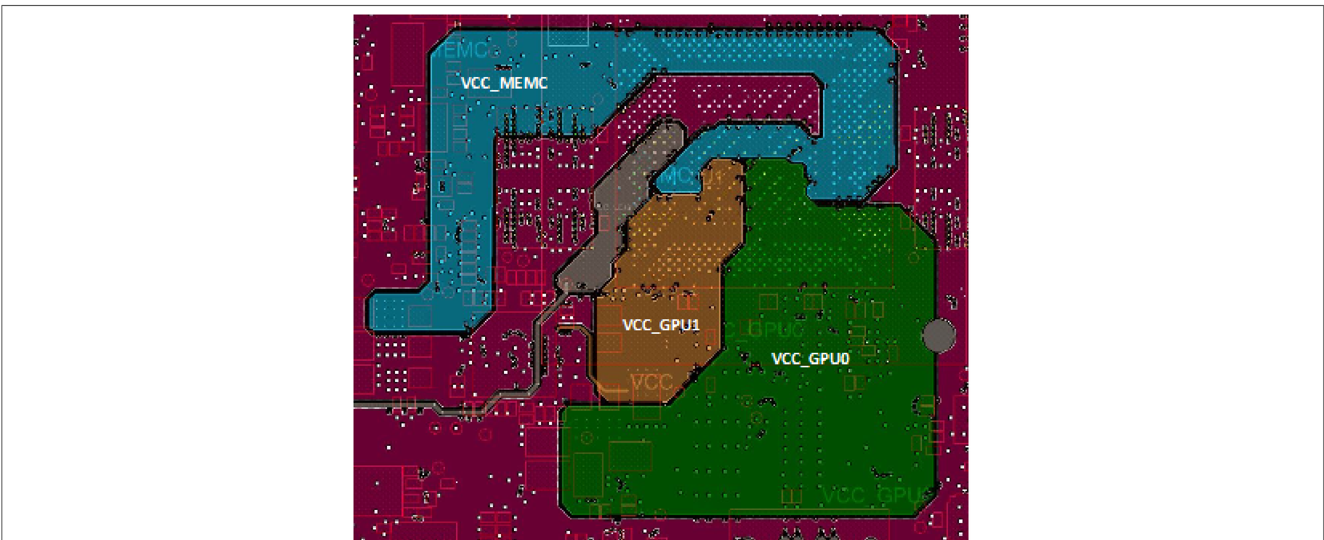

Figure 36. Power layer #4 routing

3.11 VDD_MAIN routing guidance (i.MX8 QM)

There are eight i.MX8 QM balls connected to the VDD_MAIN power supply that are not actually VDD_MAIN pins. These balls are:

1. VDD_LVDS0_1P0 – ball AV36
2. VDD_LVDS1_1P0 – ball AW35
3. VDD_MIPI_CSI0_1P0 – ball AV26

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4. VDD_MIPI_CSI1_1P0 – ball AW25
5. VDD_MIPI_DSI0_1P0 – ball AU29
6. VDD_MIPI_DSI1_1P0 – ball AV28
7. VDD_MIPI_DSI0_PLL_1P0 – ball AW29
8. VDD_MIPI_DSI1_PLL_1P0 – ball AW27

The VDD_MAIN connectivity on the 12-layer development platform PCB is shown in Figure 37. In this figure, the purple is the copper fill on the power plane layer PWR3 (layer 8) and the red is the etch on the top layer that provides connectivity from the processor balls to the vias. The four vias providing the connectivity for the eight pins referenced above and the pins themselves are highlighted in yellow.

Directly below these vias is a roughly U-shaped slot in the VDD_MAIN plane fill. The vias highlighted in green are the vias that provide the connectivity to layer 8 for the VDD_MAIN balls AU35, AT30, and AT26 from left to right (VDD_MAIN_39:37, respectively). Note that there is no physical connection across the slot between the VDD_MAIN pins and the VDD_LVDS/ VDD_MIPI pins, even though they are connected together on the schematic.

This slot forces the current flow for the remaining VDD_MAIN pins (and their return current) to go either to the right or left of this slot and not through these pins/vias. This minimizes the noise on the LVDS/MIPI power inputs. It is recommended that i.MX8 users implement this type of connectivity feature on their i.MX8 QM PCB designs.

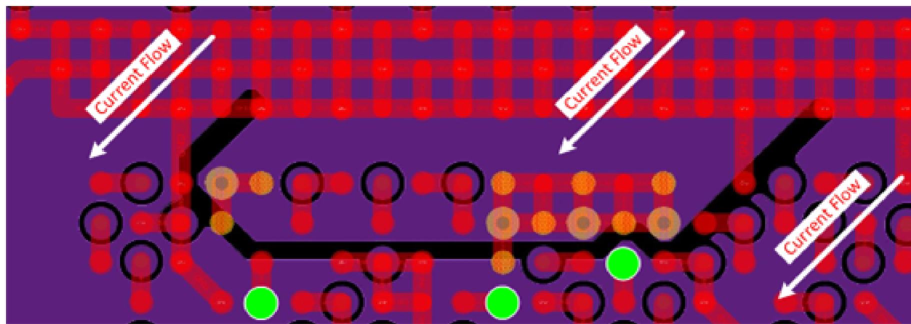

Figure 37. VDD_MAIN connectivity (PWR3/layer 8)

3.12 USB connectivity

The i.MX8 QM and i.MX8 QXP both provide a USB2 port and a USB3 port, whereas the i.MX8 DXL provides only 2 USB2 ports. The USB3 port on i.MX8 QM/QXP consist of the SS signal pairs (from the USB3 controller/ PHY) and the Dm/Dp signals from the OTG2 controller, as shown in Figure 38.

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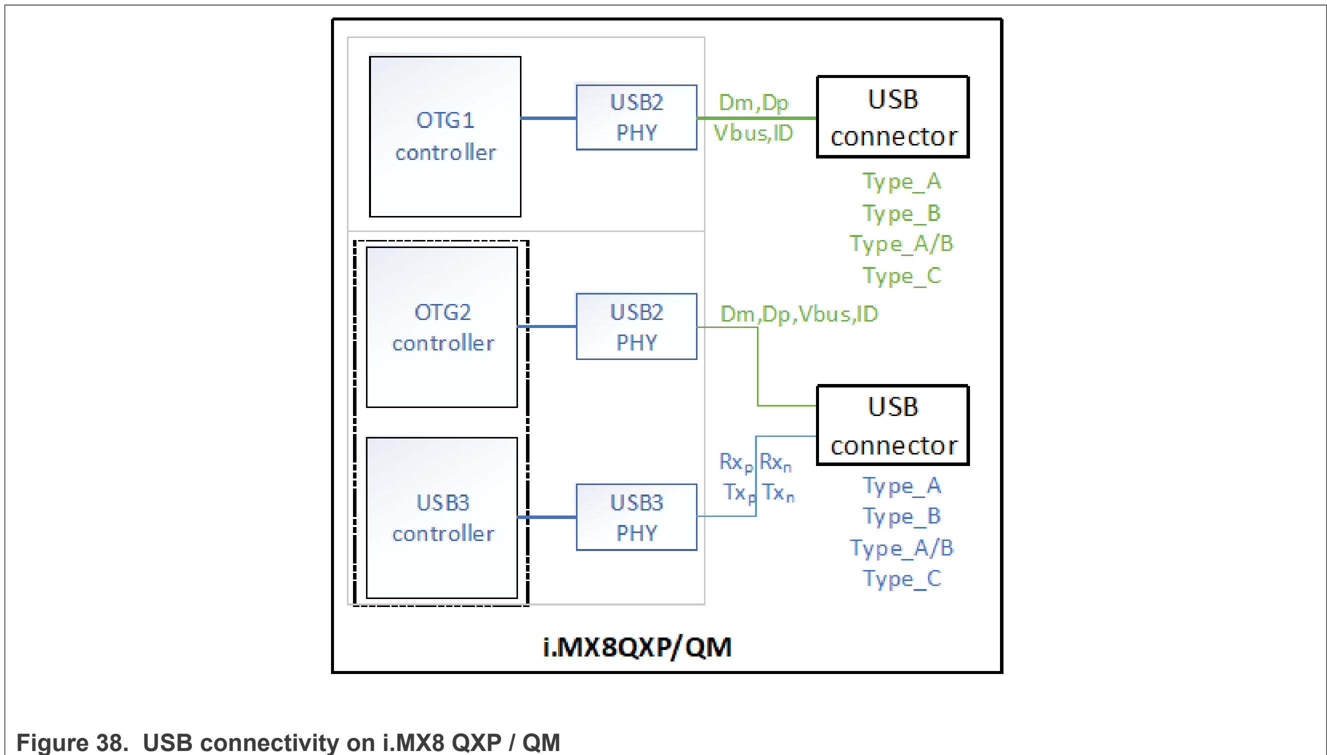

Figure 38. USB connectivity on i.MX8 QXP / QM

If USB3 is to be supported, then both OTG2 and USB3 controllers will be used for that port. The OTG2 controller supports the HS/FS/LS communication for backward compatibility and the USB3 controllers handle the SuperSpeed devices. When a new device is connected, the USB3 controller will try to connect to it first. If that fails, it will hand off the connection to the USB2 (OTG2) controller. USB3 and OTG2 cannot be used concurrently for different purposes.

OTG2 can be used without USB3 when only USB2 connections are to be made. The USB3 controller remains unused in that case.

The i.MX8 DXL device does not have a USB3 controller. It has two identical OTG controllers. They use the same controller and PHY IP as OTG1 on the QXP / QM devices.

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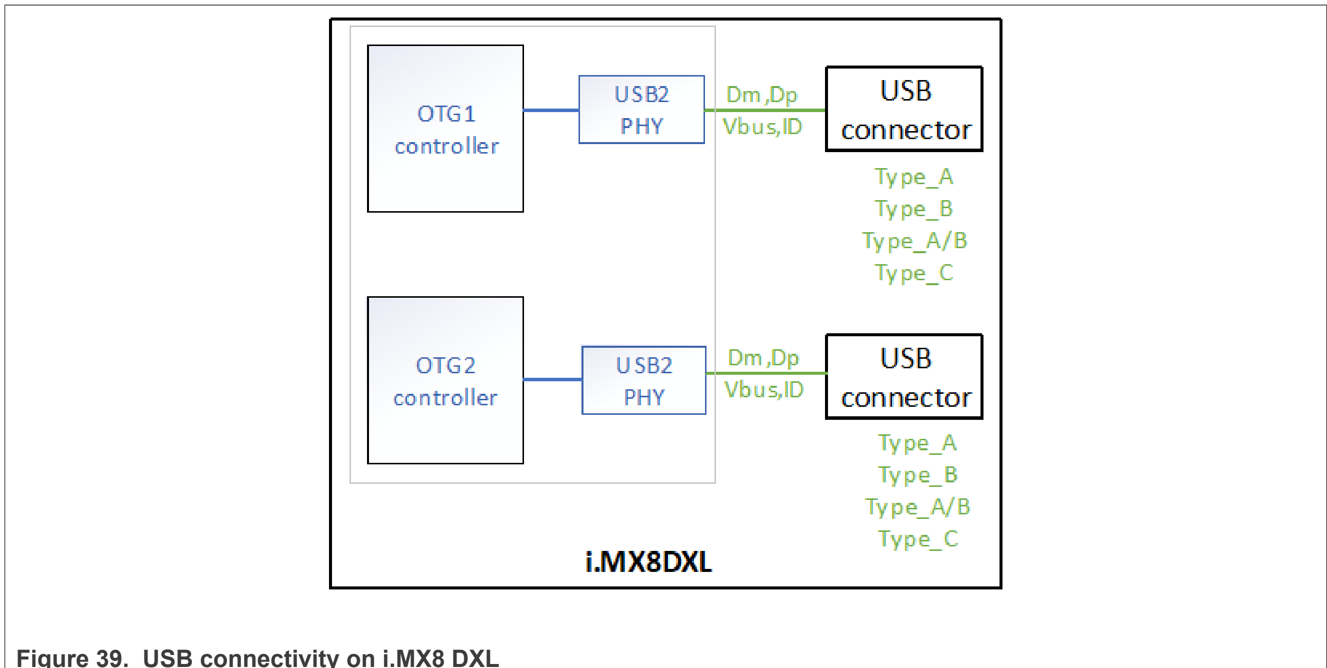

Figure 39. USB connectivity on i.MX8 DXL

The connector type used depends on the functionality (host, peripheral, OTG) that is needed. If a Type-C connector is required, external components are needed to handle the configuration channels.

See the NXP development platform schematic for an example USB Type-C implementation. See this useful link for additional USB Type-C information.

3.12.1 USB routing recommendations

Use the following recommendations when routing USB signals:

- Route the DP/DM and SS_TX/SS_RX differential pairs first.
- Route the DP/DM and SS_TX/SS_RX signals on the top or bottom layer of the board if possible.
  - Keep the DP/DM and SS_TX/SS_RX traces as short as possible.
  - Route the DP/DM and SS_TX/SS_RX signals with a minimum number of corners. Use 45° turns instead of 90° turns.
  - Minimize the layer changes (vias) on the DP/DM and SS_TX/SS_RX signals. Do not create stubs or branches.
- The trace width and spacing of the DP/DM and SS_TX/SS_RX signals should meet the differential impedance requirement of 90 Ω.
- Route the traces over continuous planes (power or ground).
  - They should not pass over any power/GND voids or anti-etch.
- When placing connectors, make sure the ground plane clear-outs around each through-hole pin have ground continuity between all pins.
- Maintain the parallelism (skew matched) between DP/DM and SS_TX/SS_RX and match the overall differential length difference to less than 5 mils.
- Maintain symmetric routing for each differential pair.
- Do not route the DP/DM and SS_TX/SS_RX traces under oscillators or in parallel to the clock traces and/or data buses.
- Minimize the lengths of high-speed signals that run in parallel to the DP/DM and SS_TX/SS_RX pairs.
- Provide ground return vias within 50-mil distance from signal layer-transition vias when transitioning between different reference ground planes.

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3.12.2 USB VBUS and ID pin voltages

The i.MX8xXP/xM family processors use two different sets of IP for USB solutions. One IP is used for the USB_OTG1 implementation and a second IP is used for the USB_OTG2/USB3 implementation. These different solutions have different voltages allowed on the VBUS and USB-ID pins. It is important to ensure that the PCB applies the correct voltage supply levels to the VBUS pins and the correct TTL logic levels to the USB-ID pins. See Table 45 for the correct voltage levels (as specified by the data sheets).

Table 45. USB pin voltage limits for i.MX8xXP/i.MX8xM

	ID Input On-Chip Pull-Up Voltage*	VBUS
USB_OTG1	1.8 V	5.0 V
USB_OTG2	3.3 V	3.3 V

* In a typical application, the ID pin does not require an external pull-up due to the on-chip pull-up. No connection results in the device mode and grounding results in the host mode.

Table 46. USB pin voltage limits for i.MX8 xXL

	ID Input On-Chip Pull-Up Voltage*	VBUS
USB_OTG1	1.8 V	5.0 V
USB_OTG2	1.8 V	5.0 V

* In a typical application, the ID pin does not require an external pull-up due to the on-chip pull-up. No connection results in the device mode and grounding results in the host mode.

3.12.3 USB Type-C considerations

If PTN5110NTHQ is used as the PD PHY IC, the CC pins must be isolated from the Type-C connector when the device is not powered to pass the Type-C compliance test TD 4.1.2. This can be realized by inserting one N-channel MOSFET between each CC pin and the Type-C connector.

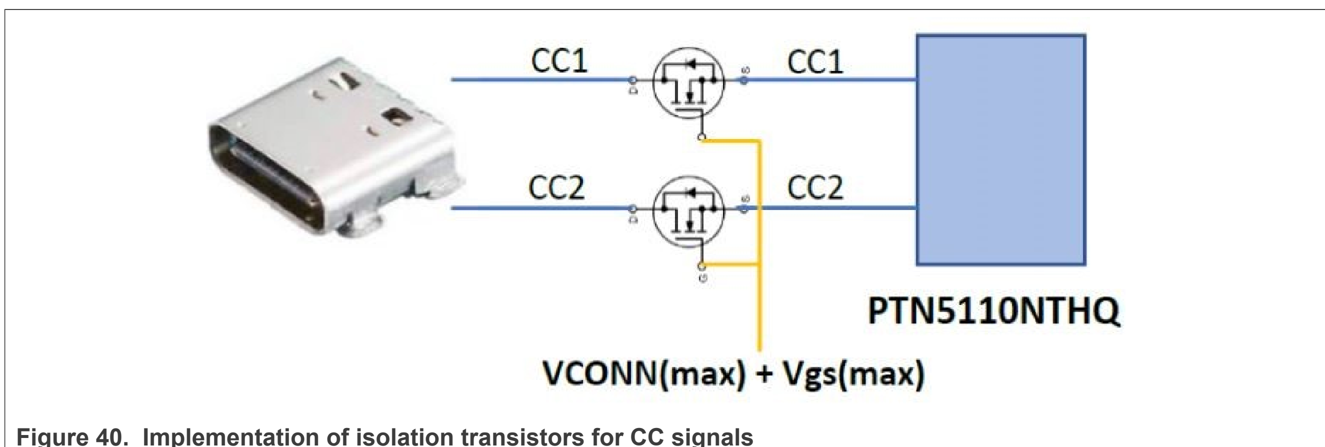

Figure 40. Implementation of isolation transistors for CC signals

The transistors will be off when the board is not powered (isolating the CC pins from the connector) and on when the board is powered (connecting the pins to the connector). For more details, see https://www.nxp.com/docs/en/errata/ES_PTN5110NTHQ.pdf.

3.13 HDMI/DisplayPort connectivity (i.MX8 QM)

The i.MX8 QM provides an HDMI transmitter capable of supporting an HDMI2.0-compatible output, a DisplayPort-1.3 compatible output, or an embedded DisplayPort 1.4-compatible output.

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The connectivity to the i.MX8 QM is different, depending on whether the HDMI or the DP is implemented. Figure 41 shows the DisplayPort connectivity of the i.MX8 QM, while Figure 42 shows the HDMI connectivity. For the HDMI output, note that there are 604 Ω resistors on the positive and negative sides of each high-speed output pair that are grounded through a FET. The gate to this FET should be tied to the 1.8 V power for the HDMI transmit circuitry (VDD_HDMI_TX0_1P8, ball AW17). This will disconnect the resistors automatically when the HDMI transmit circuitry is powered down. The resistors are required if the signals are connected to a connector. If the signals are connected to another IC instead (serializer), usage of the resistors may not be needed or allowed. Please consult the data sheet of the IC or its vendor for further reference.

Note that Figure 41 and Figure 42 do not show the optional circuitry (common mode chokes).

The HDMI input/output interfaces are not available on the i.MX8 QXP and i.MX8 DXL devices.

Note: The DisplayPort silicon IP natively supports the DisplayPort Dual Mode (DP++). There are no current plans to support this functionality in the BSP or to validate this feature in the silicon.

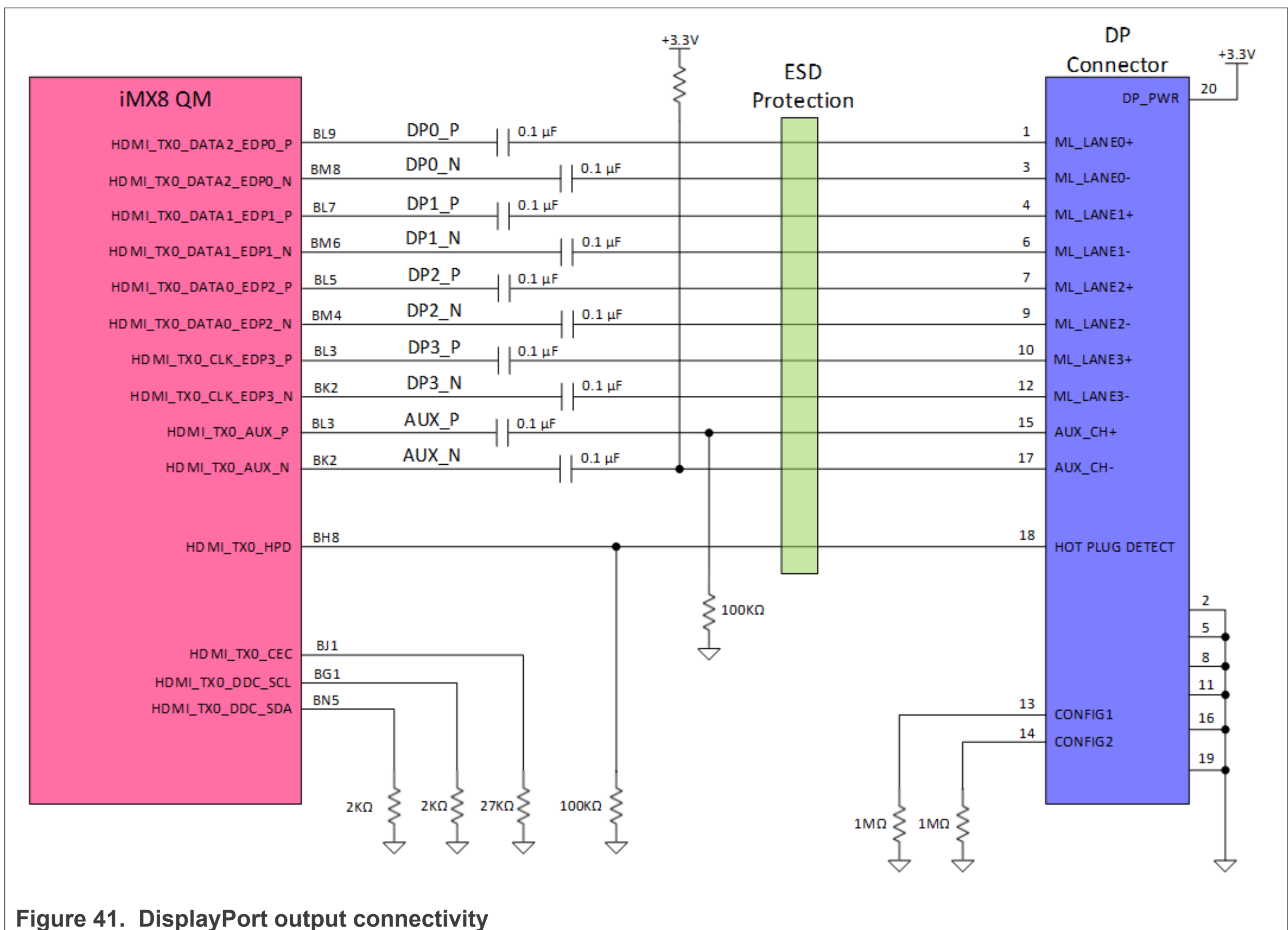

Figure 41. DisplayPort output connectivity

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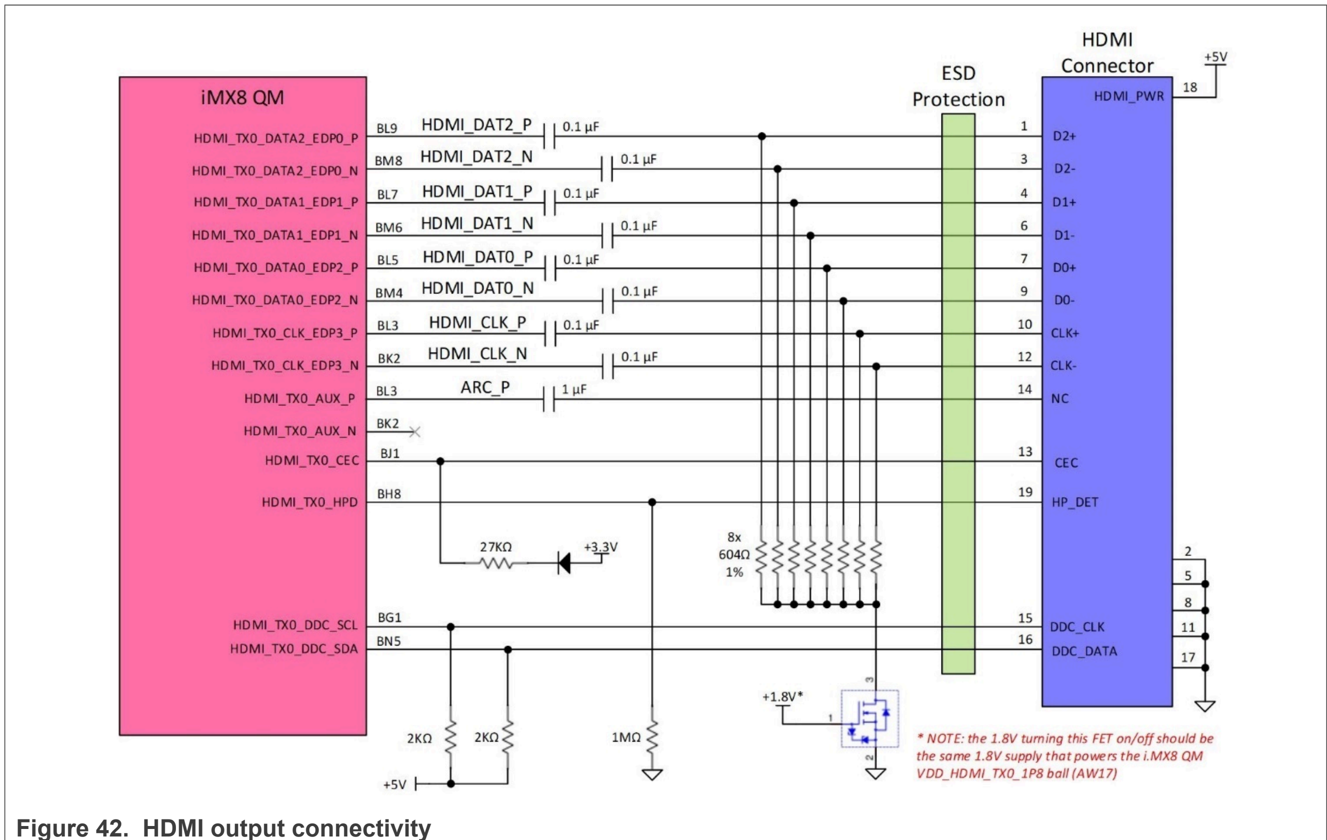

Figure 42. HDMI output connectivity

3.14 Unused input/output terminations

3.14.1 i.MX8 QM unused input/output guidance

If a function on the i.MX8 QM is not used, the I/Os and power rails of that function can be terminated to reduce overall board power. See Table 47 for recommended connectivity for unused power supply rails and see Table 48 for recommended connectivity for unused signal contacts/interfaces.

Table 47. i.MX8 QM unused power rail strapping recommendations

Function	Ball Name	Recommendation if unused
ADC	VDD_ADC_1P8	Must be powered; directly connected to VDD_ADC_DIG_1P8
Analog Test	VDD_SCU_ANA_1P8	Must be powered
Charge Pump	VDD_CP_1P8, VDD_M1P8_CAP	Must be powered with capacitor installed
HDMI-RX	VDD_HDMI_RX0_1P8, VDD_HDMI_RX0_LDO0_1P0_CAP, VDD_HDMI_RX0_LDO1_1P0_CAP, VDD_HDMI_RX0_VH_RX_3P3	Ground
HDMI-TX	VDD_HDMI_TX0_1P0, VDD_HDMI_TX0_ 1P8, VDD_HDMI_TX0_LDO_1P0_CAP	Ground

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Table 47. i.MX8 QM unused power rail strapping recommendations*...continued*

Function	Ball Name	Recommendation if unused
LVDS	VDD_LVDS0_1P0, VDD_LVDS0_1P8, VDD_LVDS1_1P0, VDD_LVDS1_1P8	10 kΩ to ground[1]
CPU0	VDD_A53 (7 balls in total)	10 kΩ to ground[1]
GPU	VDD_GPU0 (10 balls in total) VDD_GPU1 (10 balls total)	10 kΩ to ground[1]
DDR_CH1	VDD_DDR_CH1_VDDQ (10 balls in total), VDD_DDR_CH1_VDDQ_CKE (3 balls in total)	10 kΩ to ground[1]
MIPI-DSI	VDD_MIPI_DSI0_1P8, VDD_MIPI_DSI1_1P8	10 kΩ to ground[1]
	VDD_MIPI_DSI0_1P0, VDD_MIPI_DSI0_PLL_1P0, VDD_MIPI_DSI1_1P0, VDD_MIPI_DSI1_PLL_1P0	10 kΩ to ground[1, 5]
MIPI-CSI	VDD_MIPI_CSI0_1P0, VDD_MIPI_CSI0_1P8, VDD_MIPI_CSI1_1P0, VDD_MIPI_CSI1_1P8	10 kΩ to ground[1]
MLB	VDD_MLB_1P8	10 kΩ to ground[1]
Common PCIe balls	VDD_PCIE_LDO_1P8, VDD_PCIE_LDO_1P0_CAP, VDD_PCIE0_1P0, VDD_PCIE1_1P0, VDD_PCIE_IOB_1P8, VDD_PCIE0_PLL_1P8, PCIE0_PHY_PLL_REF_RETURN	Leave unconnected[2]
PCIe1	VDD_PCIE1_PLL_1P8, PCIE1_PHY_PLL_REF_RETURN	Leave unconnected
PCIe/SATA	VDD_PCIE_SATA0_PLL1P8, VDD_PCIE_SATA0_ 1P0, PCIE_SATA0_PHY_PLL_REF_ RETURN	Leave unconnected
USB HSIC	VDD_USB_HSIC0_1P2, VDD_USB_HSIC0_1P8	Leave unconnected
USB PHYs	VDD_ANA0_1P8	10 kΩ to ground[1,3,4]
USB OTG1	VDD_USB_OTG1_1P0, VDD_USB_OTG1_3P3	10 kΩ to ground[1,4]
USB OTG1	USB_OTG1_VBUS	Leave unconnected[4]
USB OTG2	VDD_USB_OTG2_1P0, VDD_USB_OTG2_3P3, USB_OTG2_VBUS	10 kΩ to ground[1,4]
Digital I/ O supplies	VDD_MIPI_CSI_DIG_1P8, VDD_MIPI_DSI_DIG_1P8_3P3, VDD_LVDS_ DIG_1P8_3P3, VDD_ESAI0_MCLK_1P8_3P3, VDD_ESAI1_SPDIF_ SPI_1P8_3P3, VDD_ENET_MDIO_1P8_2P5_3P3, VDD_ENET0_1P8_2 P5_3P3, VDD_ENET1_1P8_2P5_3P3, VDD_USDHC1_1P8_3P3, VDD_ USDHC2_1P8_3P3, VDD_USDHC_VSELECT_1P8_3P3, VDD_QSPI0_ 1P8_3P3, VDD_QSPI1A_1P8_3P3, VDD_SPI_SAI_1P8_3P3, VDD_ EMMC0_1P8_3P3, VDD_FLEXCAN_1P8_3P3, VDD_MLB_DIG_1P8_ 3P3, VDD_ADC_DIG_1P8, VDD_M4_GPT_UART_1P8_3P3, VDD_ PCIE_DIG_1P8, VDD_SIM0_1P8_3P3, VDD_HDMI_TX0_DIG_3P3	These digital I/O supplies can be left unconnected when the associated I/ O balls are not in use ***CAUTION:*** *CAUTION: Driving/connecting associated I/O balls is prohibited when the supply is not powered.*

[1] *– All balls can be connected and pulled down to ground as one group through one 10 kΩ resistor, or as multiple groups (according to ball map location) through multiple 10 kΩ resistors. If the associated supply is not powered, the signal balls can be left unconnected.*

[2] *– These balls supply all three PCIe interfaces (PCIe0, PCIe1, and PCIe/SATA) and they must be properly connected/ powered if any one of the three PCIe ports is used.*

[3] *– The “USB Phys” designation includes all USB interfaces (USB_OTG1, USB_OTG2, and USB3). This power pin must be properly connected/powered if any one of the three USB interfaces is used. VDD_USB_SS3_LDO_1P0_CAP must always be powered, whether using an USB interface or not.*

[4] *– If the serial download mode is required, all USB OTG rails (1 and 2) MUST be powered, as per the data sheet operating ranges table. In the serial download mode, both OTG ports are polled until activity is detected on one of the*

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Table 47. i.MX8 QM unused power rail strapping recommendations*...continued*

Function	Ball Name	Recommendation if unused
ports. This process will fail if either OTG port is not powered correctly. Only if the serial download mode is never required, either of the OTG supply rails can be considered unused.		
[5] *– If the MIPI DSI module is not used and the associated IO pins are used as GPIOs, the power rails must remain powered.*		

Table 48. i.MX8 QM unused signal strapping recommendations

Function	Ball Name	Recommendation if unused
ADC	ADC_IN[0:7]	Leave unconnected
	ADC_VREFH	Connect to VDD_ ADC_DIG_1P8
	ADC_VREFL	Ground
HDMI RX	HDMI_RX0_ARC_P/N, HDMI_RX0_CEC, HDMI_RX0_HPD, HDMI_RX0_MON_5V	Leave unconnected
	HDMI_RX0_CLK_P/N, HDMI_RX0_DATAx_P/N, HDMI_RX0_REXT	Ground
HDMI_TX	HDMI_TX0_AUX_P/N, HDMI_TX0_CEC, HDMI_TX0_CLK_ EDP3_P/N, HDMI_TX0_DATAx_EDPx_P/N, HDMI_TX0_HPD	Leave unconnected
	HDMI_TX0_REXT	Ground
LVDS	LVDSx_CHx_CLK_P/N, LVDS_CHx_TXx_P/N	10 kΩ to ground[1]
MIPI-CSI	MIPI_CSIx_CLK_P/N, MIPI_CSIx_DATAx_P/N	10 kΩ to ground[1]
MIPI_DSI	MIPI_DSIx_CLK_P/N, MIPI_DSIx_DATAx_P/N	10 kΩ to ground[1]
MLB	MLB_CLK_P/N, MLB_DATA_P/N, MLB_SIG_P/N	10 kΩ to ground[1]
Common PCIe interface balls	PCIE_REF_QR, PCIE_REXT,PCIE_PHY_PLL_ REF_RETURN, PCIE_SATA_REFCLK100M_P/N	Leave unconnected[2]
DDR	DDR_CHx_DCFxx, DDR_CHx_CKx_P/N, DDR_ CHx_DQxx, DDR_CHx_DMx, DDR_CHx_DQSx_P/N	Leave unconnected
PCIe0	PCIE_TX0_P/N, PCIE_RX0_P/N	Leave unconnected
PCIe1	PCIE1_TX0_P/N, PCIE1_RX0_P/N	Leave unconnected
PCIe/SATA	PCIE_SATA_TX0_P/N, PCIE_SATA_RX0_P/N	Leave unconnected
SNVS/SCU	PMIC_EARLY_WARNING	Leave unconnected
	SNVS_TAMPER_IN[1:0], SNVS_TAMPER_OUT[1:0]	10 kΩ to ground[1]
USB HSIC	USB_HSIC0_DATA, USB_HSIC_STROBE	Leave unconnected
USB_OTG1	USB_OTG1_DP/DN, USB_OTG1_ID	Leave unconnected[3]
USB_OTG2	USB_OTG2_DP/DN, USB_OTG2_ID, USB_OTG2_REXT	10 kΩ to ground[1,3]
USB3	USB3_SS_REXT, USB_SS3_TX_P/N, USB_SS3_RX_P/N	10 kΩ to ground[1]
	USB3_SS_TCx	Leave unconnected
[1] *– All balls can be connected and pulled down to ground as one group through one 10 kΩ resistor or as multiple groups (according to the ball map location) through multiple 10 kΩ resistors. This solution is applicable only if all power domains*		

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Table 48. i.MX8 QM unused signal strapping recommendations*...continued*

Function	Ball Name	Recommendation if unused
associated with each I/O group are off or tied to ground. If some of the domains remain powered, unused I/Os falling into those domains must either be left floating or tied to the ground separately, each signal through its own 10-kΩ resistor.		
[2] *– These balls must be properly designed/connected if any one of the three PCIe ports (PCIe0, PCIe1, and PCIe/SATA) is used.*		
[3] *– When the Serial Download Mode (SDP) is required, at least one OTG port must be connected. On entering the SDP mode, the ROM code will poll both OTG ports until a connection is detected. The first port a connection is detected on is expected to be the SDP port, at which point the other port will be ignored.*		

3.14.2 i.MX8 QXP unused input/output guidance

If a function on the i.MX8 QXP is not used, the I/Os and power rails of that function can be terminated to reduce overall board power. See Table 49 for the recommended connectivity for unused power supply rails and see Table 50 for the recommended connectivity for unused signal contacts/interfaces.

Table 49. i.MX8 QXP unused power rail strapping recommendations

Function	Ball Name	Recommendation if unused
ADC	VDD_ADC_1P8	Must be powered; directly connect to VDD_ADC_DIG_1P8
GPU	VDD_GPU (8 balls in total)	10 kΩ to ground
Tamper/CSI	VDD_CSI_1P8_3P3, VDD_TMPR_CSI_1P8_3P3	Leave unconnected
MIPI-CSI & MIPI-DSI	VDD_MIPI_1P8	10 kΩ to ground[1]
	VDD_MIPI_1P0	10 kΩ to ground[1, 4]
PCIe	VDD_PCIE_1P8, VDD_PCIE_LDO_1P0_CAP	Leave unconnected
USB PHYs	VDD_USB_OTG_1P0, VDD_USB_3P3	10 kΩ to ground[1,2,3]
	VDD_USB_1P8	Must be powered
USB OTG1	USB_OTG1_VBUS	Leave unconnected[3]
USB OTG2	USB_OTG2_VBUS	10 kΩ to ground[1,3]
Digital I/O supplies	VDD_ADC_DIG_1P8, VDD_CAN_UART_1P8_3P3, VDD_CSI_1P8_3P3, VDD_EMMC0_1P8_3P3, VDD_EMMC0_VSELECT_1P8_3P3, VDD_MIPI_CSI_DIG_1P8_3P3, VDD_MIPI_DSI_DIG_1P8_3P3, VDD_PCIE_DIG_1P8_3P3, VDD_QSPI0A_1P8_3P3, VDD_QSPI0B_1P8_3P3, VDD_SPI_MCLK_UART_1P8_3P3, VDD_SPI_SAI_1P8_3P3, VDD_USDHC1_1P8_3P3, VDD_USDHC1_VSELECT_1P8_3P3, VDD_ENET0_1P8_2P5_3P3, VDD_ENET0_VSELECT_1P8_2P5_3P3, VDD_ENET_MDIO_1P8_3P3, VDD_ESAI_SPDIF_1P8_2P5_3P3	These digital I/O supplies can be left unconnected when the associated I/O balls are not in use ***CAUTION:*** *Driving/connecting associated I/O balls is prohibited when the supply is not powered*
[1] *– All balls can be connected and pulled down to ground as one group through one 10 kΩ resistor or as multiple groups (according to the ball map location) through multiple 10 kΩ resistors.*		
[2] *– The "USB Phys" designation includes all USB interfaces (USB_OTG1, USB_OTG2, and USB3). These power pins must be properly connected/powered if any one of the three USB interfaces is used. VDD_USB_SS3_LDO_1P0_CAP must always be powered, whether using an USB interface or not.*		
[3] *– If the serial download mode is required, all USB OTG rails (1 and 2) MUST be powered, as per the data sheet operating ranges table. In the serial download mode, both OTG ports are polled until activity is detected on one of the ports. This process will fail if either OTG port is not powered correctly. Only if the serial download mode is never*		

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Table 49. i.MX8 QXP unused power rail strapping recommendations*...continued*

Function	Ball Name	Recommendation if unused
required, either of the OTG supply rails can be considered unused.		
[4] *– If the MIPI DSI module is not used and the associated IO pins are used as GPIOs, the power rail must remain powered.*		

Table 50. i.MX8 QXP unused signal strapping recommendations

Function	Ball Name	Recommendation if unused
ADC	ADC_IN[0:5]	Leave unconnected
	ADC_VREFH	Connect to VDD_ ADC_DIG_1P8
	ADC_VREFL	Ground
DDR	DDR_DCFxx, DDR_CKx_P/N, DDR_ DQxx, DDR_DMx, DDR_DQSx_P/N	Leave unconnected[3]
Tamper/CSI	CSI_D[0:7], CSI_EN, CSI_HSYNC, CSI_ MCLK, CSI_PCLK, CSI_RESET, CSI_VSYNC	Leave unconnected
MIPI-CSI	MIPI_CSI0_CLK_P/N, MIPI_CSI0_DATAx_P/N	10 kΩ to ground[1]
MIPI_DSI	MIPI_DSIx_CLK_P/N, MIPI_DSIx_DATAx_P/N	10 kΩ to ground[1]
PCIe	PCIE_REF_QR, PCIE_REXT, PCIE_PHY_PLL_REF_RETURN, PCIE_ REFCLK100M_P/N, PCIE0_TX0_P/N, PCIE0_RX0_P/N	Leave unconnected
USB2_OTG1	USB_OTG1_DP/DN, USB_OTG1_ID	Leave unconnected[2]
USB2_OTG2	USB_OTG2_DP/DN, USB_OTG2_ID, USB_OTG2_REXT	10 kΩ to ground[1,2]
USB3	USB3_SS_REXT, USB_SS3_TX_P/N, USB_SS3_RX_P/N	10 kΩ to ground[1]
	USB3_SS_TCx	Leave unconnected
[1] *– All balls can be connected and pulled down to ground as one group through one 10 kΩ resistor or as multiple groups (according to the ball map location) through multiple 10 kΩ resistors. This solution is applicable only if all power domains associated with each I/O group are off or tied to ground. If some of the domains remain powered, unused I/Os falling into those domains must either be left floating or tied to ground separately, each signal through its own 10-kΩ resistor.*		
[2] *– When the Serial Download Mode (SDP) is required, at least one OTG port must be connected. On entering the SDP mode, the ROM code will poll both OTG ports until a connection is detected. The first port a connection is detected on is expected to be the SDP port, at which point the other port will be ignored.*		
[3] *- The DDR pins that are not used by the technology chosen for the design (LPDDR4/DDR3L) should be left unconnected.*		

3.14.3 i.MX8 DXL unused input/output guidance

If a function on the i.MX8 DXL is not used, the I/Os and power rails of that function can be terminated to reduce overall board power. See Table 51 for the recommended connectivity for unused power supply rails, and see Table 52 for the recommended connectivity for unused signal contacts/interfaces.

Table 51. i.MX8 DXL unused power rail strapping recommendations

Function	Ball Name	Recommendation if unused
ADC	VDD_ADC_1P8	Must be powered; directly connected to VDD_ADC_DIG_1P8
Tamper	VDD_TMPR_CSI_1P8_3P3	See Table 10

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Table 51. i.MX8 DXL unused power rail strapping recommendations*...continued*

Function	Ball Name	Recommendation if unused
	VDD_CSI_1P8_3P3	Leave unconnected
PCIe	VDD_PCIE_1P8, VDD_PCIE_LDO_1P0_CAP	Leave unconnected
USB PHYs	VDD_USB_3P3	10 kΩ to ground[1,2,3]
	VDD_USB_1P8	Must be powered
USB OTG1	USB_OTG1_VBUS	Leave unconnected
USB OTG2	USB_OTG2_VBUS	Leave unconnected
Digital I/O supplies	VDD_ADC_DIG_1P8, VDD_CAN_UART_1P8_3P3, VDD_CSI_1P8_3P3, VDD_EMMC0_1P8_3P3, VDD_PCIE_DIG_1P8_3P3, VDD_QSPI0A_1P8_3P3, VDD_QSPI0B_1P8_3P3, VDD_SPI_MCLK_UART_1P8_3P3, VDD_SPI_SAI_1P8_3P3, VDD_USDHC1_VSELECT_1P8_3P3, VDD_ENET0_VSELECT_1P8_2P5_3P3, VDD_ENET_MDIO_1P8_3P3, VDD_ESAI_SPDIF_1P8_3P3	These digital I/O supplies can be left unconnected when the associated I/O balls are not in use. ***CAUTION:*** *Driving/connecting associated I/O balls is prohibited when the supply is not powered.*

1 – *All balls can be connected and pulled down to ground as one group through one 10 kΩ resistor, or as multiple groups (according to the ball map location) through multiple 10 kΩ resistors.*

2 – *The "USB Phys" designation includes all USB interfaces (USB_OTG1 and USB_OTG2). These power pins must be properly connected/powered if any of the three USB interfaces is used. VDD_USB_SS3_LDO_1P0_CAP must be always powered, whether using any USB interfaces or not.*

3 – *If a serial download mode is required, all USB OTG rails (1 and 2) must be powered, as per the data sheet operating ranges table. In the serial download mode, both OTG ports are polled until activity is detected on one of the ports. This process will fail if either OTG port is not powered correctly. Only if the serial download mode is never required, either of the OTG supply rails can be considered unused.*

Table 52. i.MX8 DXL unused signal strapping recommendations

Function	Ball Name	Recommendation if unused
ADC	ADC_IN[0:5]	Leave unconnected
	ADC_VREFH	Connect to VDD_ADC_DIG_1P8
	ADC_VREFL	Ground
DDR	DDR_DCFxx, DDR_DQxx, DDR_DMx, DDR_DQSx_P/N	Leave unconnected[3]
Tamper	SNVS_TAMPER_OUT[0:4], SNVS_TAMPER_IN[0:4]	Leave unconnected
PCIe	PCIE_REF_QR, PCIE_REXT, PCIE_PHY_PLL_REF_RETURN, PCIE_REFCLK100M_P/N, PCIE0_TX0_P/N, PCIE0_RX0_P/N	Leave unconnected
USB2_OTG1	USB_OTG1_DP/DN, USB_OTG1_ID	Leave unconnected[2]
USB2_OTG2	USB_OTG2_DP/DN, USB_OTG2_ID	10 kΩ to ground[1, 2]

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Table 52. i.MX8 DXL unused signal strapping recommendations*...continued*

Function	Ball Name	Recommendation if unused
1 – *All balls can be connected and pulled down to ground as one group through one 10 kΩ resistor, or as multiple groups (according to ball map location) through multiple 10 kΩ resistors. This solution is applicable only if all power domains associated with each I/O group are off or tied to ground. If some of the domains remain powered, unused I/O falling into those domains must either be left floating or tied to ground separately, each signal through its own 10 kΩ resistor.*		
2 – *When the Serial Download Mode (SDP) is required, at least one OTG port must be connected. On entering the SDP mode, the ROM code will poll both OTG ports until a connection is detected. The first port a connection is detected on is expected to be the SDP port, at which point the other port will be ignored.*		
3- *The DDR pins that are not used by the technology chosen for the design (LPDDR4/DDR3L) should be left unconnected.*		

3.15 GPIO pin strategies

3.15.1 Allocating GPIOs

Many different software systems can be run on the same device. This includes multiple CPUs (Cortex-A, Cortex-M, DSP, and so on) and security states (ATF, OP-TEE, OS, and so on). These different software systems must be usually isolated from each other using available hardware like MMU, SMMU, XRDC2, XRDC, RDC, and so on. All of this isolation hardware protects on IP boundaries or MMU pages (which is why the IP is mapped to separate pages). As a result, the allocation of the GPIO and other interfaces is critical. Not allocating it correctly can result in a lack of isolation leading to safety/reliability issues that can only be overcome with complex software such as virtual drivers.

The GPIO signals are grouped, 8 to 32 per the GPIO module. The SoC's hardware responsible for providing isolation has access controls on a per-module basis, not on a per-signal basis. As a result, the GPIO modules must first be allocated to software systems. The GPIO signal usage must then be mapped to these modules, based on which software system has the access. If an input signal must be read by multiple software systems, then this signal must be connected to multiple GPIO inputs, each mapped to different GPIO modules allocated to the said software systems.

Example mapping:

- SCU.GPIO0 for SCU
- LSIO.GPIO0 for M4_0
- LSIO.GPIO1 for M4_1
- LSIO.GPIO2 for secure AP
- LSIO.GPIO3-6 for non-secure AP

Similarly, I^2C, SPI, and other interfaces that can be used to communicate to multiple devices must first be allocated to a software system. Devices are then attached to interfaces owned by the software system that will use the device. This includes IOEXP modules. These should be allocated to a software system and then connected to an interface allocated to the same software system. The resets for the IOEXP must be connected to the GPIO or other IOEXP also owned by the same software system.

The board devices can only share a reset signal if the devices and the GPIO/IOEXP that drives the reset are owned by the same software system.

Note: *The GPIO signals that are best associated with the SCU are especially critical. These GPIOs must be connected to the SCU.GPIOn as accessing any of the LSIO. GPIOn requires much of the SoC fabric to be powered up, which only happens late in the boot process.*

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If the VDD_MAIN and VDD_ANA1_1P8 (8QXP and 8DXL)/VDD_SCU_1P8 (8QM) power rails are powered up simultaneously, the following GPIOs may experience a glitch (< 800 mV, < 20 µs), which should be considered dependent on the function selected by the IOMUX:

SCU_BOOT_MODE0

SCU_BOOT_MODE1

SCU_BOOT_MODE2

SCU_BOOT_MODE3 (8QM only)

SCU_BOOT_MODE4 (8QM only)

SCU_BOOT_MODE5 (8QM only)

SCU_GPIO0_00

SCU_GPIO0_01

SCU_GPIO0_02 (8QM only)

SCU_GPIO0_03 (8QM only)

SCU_GPIO0_04 (8QM only)

SCU_GPIO0_05 (8QM only)

SCU_GPIO0_06 (8QM only)

SCU_GPIO0_07 (8QM only)

SCU_PMIC_STANDBY

PMIC_INT_B

PMIC_EARLY_WARNING (8QM only)

PMIC_I2C_SCL

PMIC_I2C_SDA

JTAG_TRST_B

SCU_WDOG_OUT

JTAG_TDO

JTAG_TMS

JTAG_TDI

JTAG_TCK

PMIC operations are not affected by the glitch, because they are ignored during the power-up sequence and the peak voltage is lower than the PMIC VIH requirement.

3.15.2 Planning for GPIO voltage supplies

The i.MX8 family of processors are designed to group GPIO pins with primary functions associated with a particular function into an I/O power group necessary for that functionality. Examples include QSPI, UART, ESAI, EMMC, and USDHC. Changing the logic voltage level of a particular function to meet interfaced components only requires changing the voltage supplied to an I/O supply pin. The i.MX8 data sheets provide a detailed listing on the power group associated with the GPIO pins in the functional contact assignments table.

If a particular functionality is not required in the custom design, the GPIO pins within that I/O power group become available for other uses. Each pin is assigned an alternate functionality that can be found in the

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IOMUXD chapter of the reference manual and it is cross-referenced in the reference manual chapter that describes the alternate functionality. Software drivers provided by NXP can easily be reconfigured to use alternate pins for all functions listed as alternate uses for a pin. It is recommended to use a pin with alternate functionality in preference to assigning a pin a general GPIO functionality. This requires the end user to modify the software drivers to define explicitly how the pin should be used (bit-bang).

The voltage rail assigned to a particular I/O power group defines the logic level for all pins within that group. The designer should try to group pins that require the same voltage logic level together on the same I/O power group. If a particular I/O power group has no active pins assigned to it, then the design engineer can simply not connect the I/O power group pin for power saving.

For the maximum power saving, the design engineer can group the pins together in the same I/O power groups sorted by whether the pins will be used only during periods of maximum functionality, low activity, or when in deep sleep (wake-up functions). In this way, the design engineer can turn off the supply to the power rails at the board level when they are not needed.

3.15.3 Facilitating debug

The SCU is the system control unit. The boards designed for development should make the SCU UART TX output available to users. The access to this UART port should only be eliminated on boards designed for final customer production, where all software development (porting, testing, and so on) of the SCFW (System-Controller Firmware) was previously completed.

In addition, when using NXP's DDR Stress test tool, it is recommended to make the SCU UART and the Application Processor (AP, also known as the Cortex-A core) UART available. Furthermore, it is highly recommended to reuse the same AP UART port that is used on NXP's development boards. In these cases, UART0 is used (UART0_TX and UART0_RX). Choosing another UART port may make the DDR Stress test tool unusable, because it relies on the proper UART0 port for communication with the user.

4 Thermal considerations

4.1 Introduction

This chapter introduces basic thermal considerations that must be considered when designing an i.MX 8/8X series processor-based system. PCB's should be designed with the thermal requirements factored in early, because only remedial actions are possible after that. Factoring thermal management at the end of the design cycle will increase the cost of the overall design and delay productization. This section provides a few key design considerations to improve the thermal management of the final i.MX 8-based system/product.

The Thermal Design Power (TDP) represents the maximum sustained power dissipated by the processor across a set of realistic applications. The activity profile of the application can have a significant impact on the thermal management techniques used and on the TDP.

If the customer application requires high performance for extended periods of time and/or if the product is required to work in high ambient temperatures, the usage of passive thermal management techniques, such as a heatsink, becomes necessary. For very high ambient operating environments, active thermal management techniques, such a cooling fan or forced convection, may also be required in addition to the heatsink.

For less demanding applications, it may be feasible to consider the PCB as one of the primary heat dissipation media if good design practices are followed. In such cases, NXP recommends cooling fins as a minimum to be mounted to the lid of the processor using thermal paste or appropriate Thermal Interface Materials (TIM).

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4.2 PCB dimensions

The dimensions of the PCB directly affect its capability to dissipate the heat. Typically, more than 80 % of the heat generated by a high-power component is dissipated through the system board when no thermal solution is implemented. The bigger the board, the larger the surface area through which heat can spread away from the source component and it can be also transferred more efficiently into free space.

An NXP conducted PCB sensitivity simulation shown a 50 % reduction in PCB x-y dimensions results in an increase of between 44-65 % in package thermal resistance due to the loss in conductive volume to dissipate heat. System designers must be careful when designing smaller form factor boards that have multiple high-power components.

4.3 Copper volume

Increasing the heat dissipation (reducing thermal resistance) can also be achieved by increasing the metallization in the system board. PCBs are made up of copper and dielectric material with the copper being orders of magnitude more thermally conductive. Copper volume influences the heat capacity of the board. With higher copper volume, the board can accept more heat, so an i.MX 8 processor-based system can operate in a high-performance state (or near the maximum TDP) for longer time periods. The copper volume can be increased by increasing the dimensions of the board, by addition of ground layers, or by increasing the thicknesses of the layers on which power and ground planes are located. The PCB stack-ups of the 8QXP and 8QM MEK boards shown in Figure 43 can serve as examples.

PCB Stack-up			
Layer	Type	Material	thickness (mil)
L1	signal	copper	1.378 mils
	dielectric		3.150 mils
L2	GND	copper	1.378 mils
	dielectric		3.940 mils
L3	signal	copper	1.378 mils
	dielectric		4.880 mils
L4	power	copper	1.378 mils
	dielectric		3.940 mils
L5	signal	copper	1.378 mils
	dielectric		4.880 mils
L6	GND	copper	1.378 mils
	dielectric		3.940 mils
L7	power	copper	1.378 mils
	dielectric		4.880 mils
L8	power	copper	1.378 mils
	dielectric		3.940 mils
L9	power	copper	1.378 mils
	dielectric		4.880 mils
L10	signal	copper	1.378 mils
	dielectric		3.940 mils
L11	GND	copper	1.378 mils
	dielectric		3.150 mils
L12	signal	copper	1.378 mils

Figure 43. PCB stack-up of the i.MX8QM MEK board

If a board stack-up with a lower layer count is desired, use higher-density copper layers for the power and ground planes to assist with the board's thermal dissipation.

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PCB Stack-up			
Layer	Type	Material	thickness (mil)
L1	signal	copper	1.500 mils
	dielectric		3.500 mils
L2	GND	copper	1.300 mils
	dielectric		3.000 mils
L3	signal	copper	1.300 mils
	dielectric		8.000 mils
L4	power	copper	2.600 mils
	dielectric		18.000 mils
L5	power	copper	2.600 mils
	dielectric		8.000 mils
L6	signal	copper	1.300 mils
	dielectric		3.000 mils
L7	GND	copper	1.300 mils
	dielectric		3.500 mils
L8	signal	copper	1.500 mils

Figure 44. Stack-up of the i.MX8QXP MEK board

4.4 PCB material selection

The PCB material selection is extremely important for systems with high-speed routing. The thermal properties should also be considered when choosing PCB materials for multi-layer designs, in which the system is expected to endure excessive short-term thermal steps. Specific attention should be paid to the fact that thermal properties of dielectrics are often different in horizontal and vertical directions.

Material characteristics, such as the Coefficient of Thermal Expansion (CTE), should be considered. The CTE describes how a material changes dimensions with temperature. Ideally, a PCB material's CTE should be closely matched to copper, which is about 17 ppm °C. CTE is a concern, because when the PCB expands during heating, it can elongate plated via holes and cause fracturing. If the CTE is closely matched to copper, expansion of the PCB material and copper will be more uniform and the plated via holes will be more robust during thermal cycling.

4.5 Thermal resistance

Reducing the thermal resistance close to the die and package is mandatory for good thermal performance. The actual semiconductor die dimensions are relatively small when compared to the size of a typical PCB, which results in a very high heat flux in the die, package, and its immediate vicinity. Therefore, thermal resistance encountered early in the thermal path causes a large temperature gradient. The most effective place to focus resources to reduce thermal resistance is where the thermal gradient is the highest. To efficiently dissipate the heat through the board, thermal resistance between the SoC and the board must be minimized. This can be achieved by utilizing all the ground pads of the component and using underfill with good thermal conductivity properties.

4.5.1 Heat spreaders

Thermal resistance can be reduced when a heat spreader is mounted on the top of a SoC package using a Thermal Interface Material (TIM) with good thermal conductivity properties (thermal paste). If the heat spreader

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is also thermally connected with the PCB, an alternative route for the heat is created, reducing the global thermal resistance. Spreading the heat at the beginning of the thermal path not only reduces the thermal resistance near the source component, but it also provides a broader area to further dissipate the heat.

The type of heat spreader to be used is dependent on the customer application available enclosure space and budget considerations. Graphite heat spreaders are quite common, because they match the thermal performance of copper in two directions (x, y) at a lower weight and cost. The high in-plane (basal) thermal conductivity results in spreading and evening out of the hot spots. Due to its low cost, the area that the graphite heat spreader covers could be potentially larger, covering all heat-generating components on the system board.

4.5.2 Thermal vias

Using a continuous low-thermal-impedance path from the processor to ambient conditions is important and a low thermal resistance must be maintained throughout the PCB. Any small break in the low-impedance path is highly detrimental. System designers should provide redundant thermal paths where possible. This can be achieved by adding an appropriate amount of thermal vias to connect all the ground planes together and allow the heat to spread uniformly through other layers of the PCB. System designers should allocate enough plated through vias around the ground and power balls of the i.MX processor and other heat-generating components.

4.6 Power net design

Modern power electronics devices can have very low on-resistances. It is quite possible that the PCB traces and connector pins that feed current to these devices contribute more ohmic losses to the system than the power transistors do. Such heating may be avoidable if the traces are up-sized. Reducing trace ohmic losses may be the least expensive way to reduce the design's total power dissipation. Trace width calculators, which also predict the trace temperature rise, are readily available on the internet. Using over-sized power transistors is a way to cut the total power and subsequent heat dissipation.

4.7 Component placement

The i.MX 8 processor should always be placed away from edges in the center of the PCB, so that the heat can effectively spread in all directions. Placing the device on the edge or even on the corner of the PCB significantly reduces heat transfer from the device and dissipation capabilities of the PCB, because the heat cannot efficiently spread in the directions where the edges are present. This eventually results in local hot spots and rapid heating of the source component.

In addition, the processor should be mounted on the top side of the PCB, away from the chassis walls. System designers should place heat-generating components as far apart as possible to reduce thermal-coupling effects. The thermal gradient is high near a power dissipating device, so even small amounts of separation help to reduce thermal coupling.

A NXP-conducted PCB sensitivity simulation shown that a non-centered bare i.MX 8 FCBGA package on the PCB will cause approximately 8-10 % increase in the junction temperature due to uneven heat propagation. This study highlights the need for centered component placement.

4.8 PCB surroundings

The surroundings of the PCB also influence the efficiency of heat transfer from the board into free space (air). There should be enough clearance from the top and bottom sides of the PCB. If narrow gaps are created, the air flow is significantly limited, resulting in the accumulation of hot air in the gap. The board cannot therefore effectively transfer heat in such areas. The casing should be also designed in a way that natural air convection could be utilized to improve heat transfer.

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If a narrow gap at the bottom side cannot be avoided (quite common for System on Modules -SOMs), the gap under the i.MX processor should be filled by thermally conductive gap filler. To further improve heat transfer, the exposed copper pads should be added to the base board at the mounting spot of the filler.

4.8.1 Air flow considerations

Heat convection is more efficient for a vertically mounted board. Remember that the components above the heat-producing devices run hotter than those below them. If the board is horizontally mounted, place the heat-generating components on top of the PCB (if possible). A thermal plume (chimney effect) forms more readily on the top side of the board and it helps to disperse heat.

- Consider the system level air flow and air mover placement in the enclosure.
- Avoid sub-optimal component placement that might hinder the airflow or natural convection.
- Avoid placing tall or bulky devices in the air flow path.
- Avoid routing circuitry in an area of mounting holes.
- Plan to make space for the thermal management solution early in the system design phase and consider the complete board and packaging form factor (enclosure).

4.9 Heat sink considerations

The most frequently employed passive cooling device is the heat sink. It is a mass of thermally conductive metal which is physically mounted to a heat-generating component. Adding a heat sink to the processor is an excellent method to dissipate heat. Commonly used heat sink materials are copper and aluminum:

- Copper has better thermal conductivity, but it is more expensive and difficult to process. It is heavier (lots of copper radiators exceed the CPU weight limit), it has small heat capacity, and it oxidizes easily.
- Pure aluminum is very soft, so it cannot be used directly. For most applications, an aluminum heat sink is sufficient.

A few design considerations when planning to add a heat sink into your design are as follows:

- Ensure adequate spacing around the device to accommodate the heat sink.
- Avoid routing circuitry in the area of mounting holes.
  - Space is needed for anchoring the heat sink, such as spring-loaded screws, a clip, or push pins.
- Consider also the bottom side of the PCB, where the space for reinforcing support or securing mechanisms may be required.
  - A backing plate may be necessary on the back side of the printed circuit board (opposite to the flip-chip device) to prevent board warpage.
- Consider the temperature limits beneath the heat sink and ensure that the temperature-sensitive components are not placed there to prevent overheating and damage.
- Ensure that the orientation and spacing of the fins causes the heat to move as quickly as possible from the heat source (see Air Flow Considerations).
  - Improper orientation can inhibit the thermal performance of the heat sink.
- Ensure that the maximum pressing force is not exceeded:
  - Pressing force on the 17x17 package (8QXP) should not exceed 10 lb.
  - Pressing force on the 21x21 package (8QXP) should not exceed 10 lb.
  - Pressing force on the 29x29 package (8QM) should not exceed 21 lb.
  - Pressing force on the 15x15 package (8DXL) should not exceed 3.6 lb.

See *Assembly Handling and Thermal Solutions for Lidless Flip Chip Ball Grid Array Packages* (document AN4871) for more heat sink handling details.

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4.10 Thermal simulations

As illustrated in this section, thermal management is a very complex discipline with numerous variables that must be considered. To determine whether the system is capable of stable operation (no thermal runaways) in the given use case or to identify potentially overlooked issues, thermal simulations must be performed.

NXP can provide FloTHERM simulation models for the i.MX 8 series processor family and strongly encourages customers to perform thermal simulations using these models in their form factor designs and specific use cases to get a holistic system thermal design and identify possible thermal bottlenecks. Thermal simulations become increasingly important in small form factor designs and in operation in high ambient temperatures.

4.11 Software optimization

Software-based power and thermal management techniques can be very effective in reducing the need for more elaborate active or passive thermal management solutions and add little or no additional cost to the system design. Attention should be paid to the required system performance and power requirements, because lowering the i.MX 8 processor power consumption also lowers the heat generated by the processor.

The i.MX 8 series incorporates several low-power design techniques to meet requirements of low-power design, while sustaining high performance. The activity profile of the customer application can have a significant impact on the thermal management techniques used and on the TDP. Carefully defining the system's worst case operating conditions can be an effective way to reduce power and thermal dissipation.

- System designers should utilize and enable all software power-management techniques available for the i.MX 8 series.
- The SoC voltages and core frequencies of modules should be kept at the minimum specified levels and scaled dynamically with respect to the current performance demands of the application, where possible.
- The processor should enter low-power modes under certain use cases whenever possible.
- All unused power rails should be turned off from the PMIC and unused domains should be power-gated, if possible.
- All unused module clocks should be turned off (dynamically handled by the NXP Linux BSP).
- Customers are encouraged to use the latest Linux BSP GA release available on nxp.com that leverages the i.MX 8 processor power-management features and incorporates various Linux OS software power-management techniques.

4.12 Thermal checklist

NXP recommends using the checklist shown in Table 53 as a high-level guide for designing an optimal thermal management solution for your end product.

Table 53. i.MX8 QXP/QM/DXL thermal checklist

Item	Activity	Check
1	Determine the TDP (Thermal Design Power).	
2	Determine the activity profile (use-case dependent).	
3	Determine the product form factor constraints (orientation, x, y, and z limits, and so on).	
4	Determine the environmental operating conditions (ambient temperature, airflow regime - forced or natural convection).	
5	Determine the Tj for the i.MX 8 device to use (automotive, industrial, consumer, package-lidded, and so on).	
6	Factor in the board-design considerations early (PCB layers, metallization, layout, component placement).	

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Table 53. i.MX8 QXP/QM/DXL thermal checklist*...continued*

Item	Activity	Check
7	Run thermal simulations to determine the best thermal management approach using the form factor design and use cases.	
8	Investigate adding heat-spreading techniques and heat sinks to alleviate thermal bottlenecks.	
9	Enable all software power-management techniques which can minimize power consumption (less power, less heat).	
10	Consider a lower power memory and other system components or retarget the use case.	

5 Avoiding board bring-up problems

5.1 Introduction

This chapter provides recommendations for avoiding typical mistakes when bringing up a board for the first time. These recommendations consist of basic techniques that have proven useful in the past for detecting board issues and preventing/locating the three most typical issues encountered: power, clocks, and reset.

5.2 Avoiding power pitfalls - current

Excessive current can cause damage to the board. Avoid this problem by using a current-limiting laboratory supply set to the expected typical main current draw (at most). Monitor the main supply current with an ammeter when powering up the board for the first time. You can use the supply's internal ammeter (if it has one). By monitoring the main supply current and controlling the current limit, any excessive current can usually be detected before permanent damage occurs.

In lieu of this approach, you can simply ohm out all the board power rails to ground before the board testing and verify that there are no short circuits. If there are none, you should be able to apply power to the board with a high degree of confidence that there are no shorts that would cause excessive current leading to board and/or component damage.

5.3 Avoiding power pitfalls - voltage

Incorrect voltage rails are a common power pitfall. To avoid this mistake, create a basic table called a voltage report before board bring-up/testing. This table helps to validate that all the supplies are reaching the expected levels.

To create a voltage report, list the following:

- Board voltage sources
- Default power-up values for the board voltage sources
- Best location on the board to measure the voltage level of each supply

Carefully determine the best measurement location for each power supply to avoid a large voltage drop (IR drop) on the board, which causes inaccurate voltage values to be measured. The following guidelines produce the best voltage measurements:

- Measure closest to the load (in this case the i.MX8 processor).
- Make two measurements: the first after the initial board power-up and the second while running a heavy use-case that stresses the i.MX8 processor.

Ensure that the supplies that power the i.MX8 meet the DC electrical specifications, as listed in the chip-specific data sheet.

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See Table 54 for a sample voltage report.

Note: *This report table is for the i.MX8 QM Development Platform. Sample voltage reports for customer PCBs will be different from this, depending on the processor and Power Management IC (PMIC) used and the assignment of the PMIC power resources.*

Table 54. Sample voltage report

Source	Net Name	Expected (V)	Measured (V)	Measure point	Comment
Ext 5V SMPS	VCC_EXT_5V0	5.0 V		TP27	Main 5 V supply for the board
Ext 3.3V SMPS	VCC_EXT_3V3	3.3 V		TP52	Main 3.3 V supply for the board
PMIC1 SW1&2	VCC_MAIN	1.0 V		TP8	
PMIC1_SW3&4	VCC_CPU1	1.0 V		TP22	
PMIC1_SW5	VCC_CPU0	1.0 V		TP21	
PMIC1_SW6	VCC_DDRIO1	1.1 V		TP33	
PMIC1_SW7	VCC_1V8	1.8 V		TP16	
PMIC2_SW1&2	VCC_GPU0	1.0 V		TP53	
PMIC2_SW3&4	VCC_GPU1	1.0 V		TP42	
PMIC2_SW5	VCC_MEMC	1.1 V		TP36	
PMIC2_SW6	VCC_DDRIO0	1.1 V		TP23	
PMIC2_SW7	VCC_3V3	3.3 V		TP3	
PMIC1_LDO1	VCC_SCU_1V8	1.8 V		TP11	
PMIC1_LDO2	VCC_LDO_SD1	1.8 V/3.3 V		TP78	Can be either one under software control (via USDHC1_ VSELECT)
PMIC2_LDO1	VCC_LDO_SIM	1.8 V/3.3 V		TP37	Can be either one under software control
PMIC2_LDO2	VCC_LDO_SD2	1.8 V/3.3 V		TP43	Can be either one under software control (via USDHC2_ VSELECT)
PMIC1_SNVS	VCC_SNVS	3.0 V		C277-1	
i.MX8 LDO	VDD_SNVS_ LDO_1P8_CAP	1.8 V		C311-1	Internal LDO sourced by i.MX8
i.MX8 LDO	VDD_PCIE_ LDO_1P0_CAP	1.0 V		C417-1	Internal LDO sourced by i.MX8
i.MX8 LDO	VDD_USB_SS3_ LDO_1P0_CAP	1.0 V		C411-1	Internal LDO sourced by i.MX8
i.MX8 LDO	VDD_HDMI_TX0_LDO_1P0_CAP	1.0 V		C306-1	Internal LDO sourced by i.MX8
i.MX8 LDO	VDD_HDMI_RX0_ LDO0_1P0_CAP	1.0 V		C308-1	Internal LDO sourced by i.MX8

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Table 54. Sample voltage report*...continued*

Source	Net Name	Expected (V)	Measured (V)	Measure point	Comment
i.MX8 LDO	VDD_HDMI_RX0_ LDO1_1P0_CAP	1.0 V		C310-1	Internal LDO sourced by i.MX8
Enet PHY	VCC_ENET0_1V8	1.8 V		C412-1	Software sets up Phy for 1.8 V output

5.4 Checking for clock pitfalls

Problems with the external clocks are another common source of board bring-up issues. Ensure that all of the clock sources run as expected.

The XTALI/XTALO and the RTC_XTALI/RTC_XTALO clocks are the main clock sources for the 24 MHz and 32.768 kHz reference clocks respectively.

When checking crystal frequencies, use an active probe to avoid excessive loading. A passive probe typically inhibits the 32.768 kHz and 24 MHz oscillators from starting up. Use the following guidelines:

- The RTC_XTALI clock is running at 32.768 kHz.
- XTALI/XTALO is running at 24 MHz (used for the PLL reference).

5.5 Avoiding reset pitfalls

Follow the following guidelines to ensure that you are booting using the correct boot mode.

- Follow the recommended power-up sequence specified in the i.MX8 data sheet.
- Ensure that the POR_B signal remains asserted (low) until all voltage rails associated with the bootup are on.

The SCU_BOOT_MODE balls and internal fuses control the boot. For a more detailed description of the different boot modes, see the system boot chapter of the chip reference manual.

5.6 Sample board bring-up checklist

Note that the checklist incorporates the recommendations described in the previous sections. Blank cells should be filled in during bring-up, as appropriate.

Table 55. Board bring-up checklist

Checklist Item	Details	Owner	Findings and Status
Note: The following items must be completed serially.			
1. Perform a visual inspection.	Check the major components to make sure nothing is misplaced or rotated before applying power.		
2. Verify all i.MX8 voltage rails.	Confirm that the voltages match the data sheet requirements. Be sure to check the voltages as close to the i.MX8 as possible (on a bypass capacitor). This reveals any IR drops on the board that could cause issues later. Ideally, all of the i.MX8 voltage rails should be checked, but see the guidance below for important rails to check for the i.MX8 QM, i.MX8 QXP, and i.MX8 DXL.		
	i.MX8 QM - VDD_SNVS, VDD_MAIN, VDD_A53, VDD_A72, VDD_ DDR_CH0, VDD_DDR_CH1, VDD_ANA_1P8 (SCU_1V8) and VDD_MAIN are particularly important voltages and they must fall within the parameters provided in the i.MX8 data sheet.		

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Table 55. Board bring-up checklist*...continued*

Checklist Item	Details	Owner	Findings and Status
	i.MX8 QXP - VDD_SNVS, VDD_MAIN, VDD_A35, VDD_DDR, VDD_ANA_1P8 (SCU_1V8) and VDD_MAIN are particularly important voltages and they must fall within the parameters provided in the i.MX8 data sheet.		
	Verify that all voltage supplies meet required ripple tolerances under full load conditions.		
	i.MX8 DXL -VDD_SNVS, VDD_MAIN, VDD_DDR, and VDD_ANA_1P8 (SCU_1V8) must be up and within the margins defined in the data sheet.		
3. Verify the power-up sequence.	Verify that power-on reset (POR_B) is de-asserted (high) after all power rails have come up and are stable. See the i.MX8 data sheet for details about power-up sequencing.		
4. Measure/probe input clocks (32.768 kHz, 24 MHz, and others).	Without proper clocks, the i.MX8 will not function correctly.		
5. Check the JTAG connectivity.	This is one of the most fundamental and basic access points to the i.MX8 to allow the debug and execution of low level code and probe/ access the processor memory.		
Note: The following items may be worked on in parallel with other bring-up tasks.			
Access the internal RAM.	Verify the basic operation of the i.MX8 in the system. The on-chip internal RAM starts at address 0x0090 0000 and its size is 256 KB. Perform a basic test by performing a write-read-verify to the internal RAM. No software initialization is required to access the internal RAM.		
Verify CLKO outputs (measure and verify default clock frequencies for desired clock output options) if the board design supports the probing of clock output balls.	This ensures that the corresponding clock and the PLLs are working. Note that this step requires chip initialization (for example, via the JTAG debugger) to properly set up the IOMUX to output clocks to I/O balls and to set up the clock control module to output the desired clock. See the chip reference manual for more details.		
Measure boot mode frequencies. Set the boot mode switch for each boot mode and measure the following (depending on system availability): • NAND (probe CE to verify the boot and measure the RE frequency). • SPI-NOR (probe the slave select and measure the clock frequency). • MMC/SD (measure the clock frequency).	This verifies the specified signals’ connectivity between the i.MX 8 QM/QXP/8DXL and the boot device and that the boot mode signals are properly set. See the System Boot chapter in the chip reference manual for details about configuring the various boot modes.		
Run the basic DDR initialization and test the memory.	Using the DDR testing tools supplied by NXP (or developed by the user, if desired), run and verify the DDR initialization script. Verify that the entire memory is available for use.		

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Table 55. Board bring-up checklist*...continued*

Checklist Item	Details	Owner	Findings and Status
Test the temperature and voltage.	Verify that the PCB design operates correctly at extreme corners of the specified operating conditions.		

6 Using BSDL for board-level testing

The Boundary Scan Description Language (BSDL) is used for board-level testing after the components are assembled. The interface for this test uses the JTAG pins. The definition is in IEEE Std 1149.1.

6.1 How BSDL works

A BSDL file defines the internal scan chain, which is the serial linkage of the IO cells, within a particular device. The scan chain looks like a large shift register, which provides a means to read the logic level applied to a pin or to output a logic state on that pin. Using JTAG commands, the test tool uses the BSDL file to control the scan chain so that the device-board connectivity can be tested.

For example, when using an external ROM test interface, the test tool performs the following:

1. It outputs a specific set of addresses and controls to the pins connected to the ROM.
2. It performs a read command and scans out the values of the ROM data pins.
3. It compares the values read with the known golden values.

Based on this procedure, the tool determines whether the interface between the two parts is connected properly and does not contain shorts or opens.

6.2 Boundary scan operation

NXP provides BSDL files for the i.MX8 QM, QXP, and DXL processors to enable the boundary scan mode. To enter this mode, it is required to set the needed COMPLIANCE_PATTERN. This pattern involves the TEST_MODE_SELECT and POR_B pins. TEST_MODE_SELECT must be set to 0 and POR_B must be set to 1.

6.3 I/O pin power considerations

The boundary scan mode can set or read values from each of the available pins if the respective IO power supplies are active.

Note: *The boundary scan mode was only tested at 1.8 V.*

7 Revision history

Table 56. Revision history

Revision	Date	Substantive changes
0.0	6/9/2017	Draft version for initial review.
0.1	7/17/2017	Updated per comments from initial review. Began adding QXP information (WIP).
0.2	7/25/2017	Complete addition of QXP info. Distribute for review.
0.3	8/2/2017	Added comments from large group review.
0.4	8/7/2017	Added individual comments.

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Table 56. Revision history...*continued*

Revision	Date	Substantive changes
0.5	12/06/2018	Changes to Table 11 and Table 12, change to Section 3.10.2 single-ended trace impedance recommendation, added i.MX8 QM PDN impedance target values to Table 42, minor changes to paragraph Section 3.10.2. Updated Table 41, Table 42, Table 43, and Table 45. Table 17 – added reference to 24 MHz crystal tolerance table and added load capacitance. Table 16 – added HDMI CEC recommendation. Table 6 – Added debug info. Table 15 – Add VBUS info. Table 41 and Table 43 – Added VBUS and updated ADC power info. Added Eye Diagram widths for DDR Simulations. – Added 24 MHz tolerance requirements – Added layout recommendations for 8QXP DDR3L. Added PDN numbers for MX8QM, updated values for MX8QXP.- Added design DRAM jitter target requirements removed from data sheet. -Added design disclaimers. – Added section for general GPIO recommendations. – Added board stack up diagrams. -Added comment to simulation section for 2T timing. – Updated recommendation for PCIE Ref CLK generator. - Added comment for 24 MHz GND loop.
0.6	01/15/2019	Added fixes for USB implementation on B0 silicon.
1.0	01/2020	Updated Table 24 for QXP B0 DDR 21x21 mm package length.
2.3p	02/2021	- USB connectivity chapter rewritten. - Updated 24 MHz crystal trimming considerations in Clock crystal considerations chapter. - VDD_ANA_1P8 (SCU_1V8) added into Table 55. - Updated VDD_DDR_VDDQ max current guideline for 8QXP. - Updated drive strength and ODT recommendations in the DRAM SI Simulation Guide. - Added considerations for PCIE_SATA0_PHY_PLL_REF_RETURN, PCIE0_PHY_PLL_REF_RETURN, PCIE1_PHY_PLL_REF_RETURN (Table 14) - Deleted 0.1uF capacitor requirement for VDD_GPU in Table 12. - Updated the considerations for HDMI data and clock pull-down resistors in Section 3.13 - Added considerations for ADC_VREFH and ADC_VREFL to Table 48. - FlexSPI signals explicitly included to the group of signals that must follow high-speed signal routing. (Section 3.5) - Added considerations for implementation of the USB Type-C connector – isolation of the CC pins (Section 3.12.3). - Minor update in column names in Table 45. - HDMI_ARC (ARC_P) capacitor changed from 0.1 uF to 1 uF (Figure 42). - Added recommendations for unused DDR pins for i.MX8 QXP (Table 50) - EMC/EMI considerations added to the PCIe design checklist table (Table 14). - Added notes informing that MLB is not supported on i.MX8 QM to Table 11.
2.4p	06/2021	- Added a guideline on how to treat PMIC_ON_REQ when unused to Table 7. - Updated the note for VDD_PCIE_1P8 in Table 12 to mention a 120 Ω ferrite bead instead of a 47 nH inductor. - Updated the information about the material used in the i.MX8QXP MEK stack-up in Section 3.3.2. - Added a guideline that only point-to-point designs are supported to Section 3.4.6. - Added a data sheet reference note to Table 17 for the general crystal requirements of the 32-kHz crystal. - Added a reference to the internal load capacitors to Table 17. - Updated VSS_SCU_XTAL considerations in Table 17.

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Table 56. Revision history...*continued*

Revision	Date	Substantive changes
		- Added a note to Section 3.9.3 to provide better explanation on mapping of the trim settings to capacitor values. - Updated recommendations for the MIPI DSI power rails in Table 47 and Table 49. - Added a guideline that VDD_USB_1P8 must be powered to Table 49. - Added Section 6.
2.5p	26 January 2022	- Added a note to Section 3.4.6 and Section 3.4.10 that swapping the CA (LPDDR4) and Address/Command/Control (DDR3L) bits is not supported. - Corrected the delay of DDR_DCF_25 for the i.MX 8QXP 17x17 mm package (Table 25). - Added Table 20 to Section 2.1. - Added considerations about PCIe DFE settings and reference to Section 3.7 to Table 14. - Added a note about Hyperlynx timing models that are available for i.MX 8QM/8 QXP to Section 3.4.15. - Updated notes in Table 48 and Table 50. - Maximum heat sink pressing forces defined for the packages in Section 4.9. - Added a note to Section 3.15.1.
2.6	20 March 2023	Added information and guidelines for i.MX8 DXL.

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Contents

1 Overview ... 2
1.1 Devices supported ... 2
1.2 Essential reference ... 2
1.3 Suggested reading ... 2
1.3.1 General information ... 2
1.4 Related documentation ... 3
1.5 Conventions ... 3
1.6 Acronyms and abbreviations ... 4
2 i.MX8 QM, QXP, and DXL design checklist ... 5
2.1 Design checklist tables ... 5
2.2 JTAG signal termination ... 18
3 i.MX8 layout/routing recommendations ... 18
3.1 Introduction ... 18
3.2 Basic design recommendations ... 19
3.2.1 Placing decoupling capacitors ... 19
3.3 Stack-up recommendations ... 19
3.3.1 Stack-up recommendation (i.MX8 QM) ... 19
3.3.2 Stack-up recommendation (i.MX8 QXP) ... 20
3.3.3 Stack-up recommendation (i.MX8 DXL) ... 21
3.4 DDR layout routing recommendations ... 22
3.4.1 DDR pin naming ... 22
3.4.2 i.MX8 QM DDR package conductor lengths ... 23
3.4.3 i.MX8 QXP DDR package conductor lengths ... 26
3.4.4 i.MX8 DXL DDR package conductor lengths ... 29
3.4.5 Length matching guides ... 30
3.4.6 LPDDR4-2400/3200 general design recommendations ... 32
3.4.7 i.MX8 QM LPDDR4-3200 routing recommendations ... 32
3.4.8 i.MX8 QXP LPDDR4-2400 routing recommendations ... 35
3.4.9 i.MX8 DXL LPDDR4-2400 routing recommendations ... 38
3.4.10 i.MX8 QXP / DXL general DDR3L-1866 design recommendations ... 42
3.4.11 i.MX8 QXP DDR3L-1866 routing recommendations ... 43
3.4.12 NXP i.MX8 QXP DDR3L-1866 validation board ... 44
3.4.13 i.MX8 DXL DDR3L-1866 routing recommendations ... 50
3.4.14 i.MX 8DXL DDR3L-1866 validation board ... 51
3.4.15 DRAM SI simulation guide ... 55
3.4.16 JEDEC specification compliance ... 56
3.5 High-speed routing recommendations ... 57
3.6 Disclaimers ... 57
3.7 Trace impedance recommendations ... 58
3.8 Reset architecture/routing ... 59
3.9 Clock crystal considerations ... 60
3.9.1 Oscillator tolerance (24 MHz) ... 60
3.9.2 Clock options (32.768 kHz) ... 60
3.9.3 Internal load capacitor trimming (24 MHz and 32.768 kHz) ... 61
3.9.4 XTALI specifications (8DXL) ... 63
3.10 Power connectivity/routing ... 63
3.10.1 i.MX8 QM / QXP / DXL power distribution block diagram ... 64
3.10.2 Power routing/distribution requirements ... 68
3.11 VDD_MAIN routing guidance (i.MX8 QM) ... 71
3.12 USB connectivity ... 72
3.12.1 USB routing recommendations ... 74
3.12.2 USB VBUS and ID pin voltages ... 75
3.12.3 USB Type-C considerations ... 75
3.13 HDMI/DisplayPort connectivity (i.MX8 QM) ... 75
3.14 Unused input/output terminations ... 77
3.14.1 i.MX8 QM unused input/output guidance ... 77
3.14.2 i.MX8 QXP unused input/output guidance ... 80
3.14.3 i.MX8 DXL unused input/output guidance ... 81
3.15 GPIO pin strategies ... 83
3.15.1 Allocating GPIOs ... 83
3.15.2 Planning for GPIO voltage supplies ... 84
3.15.3 Facilitating debug ... 85
4 Thermal considerations ... 85
4.1 Introduction ... 85
4.2 PCB dimensions ... 86
4.3 Copper volume ... 86
4.4 PCB material selection ... 87
4.5 Thermal resistance ... 87
4.5.1 Heat spreaders ... 87
4.5.2 Thermal vias ... 88
4.6 Power net design ... 88
4.7 Component placement ... 88
4.8 PCB surroundings ... 88
4.8.1 Air flow considerations ... 89
4.9 Heat sink considerations ... 89
4.10 Thermal simulations ... 90
4.11 Software optimization ... 90
4.12 Thermal checklist ... 90
5 Avoiding board bring-up problems ... 91
5.1 Introduction ... 91
5.2 Avoiding power pitfalls - current ... 91
5.3 Avoiding power pitfalls - voltage ... 91
5.4 Checking for clock pitfalls ... 93
5.5 Avoiding reset pitfalls ... 93
5.6 Sample board bring-up checklist ... 93
6 Using BSDL for board-level testing ... 95
6.1 How BSDL works ... 95
6.2 Boundary scan operation ... 95
6.3 I/O pin power considerations ... 95
7 Revision history ... 95
8 Legal information ... 98

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