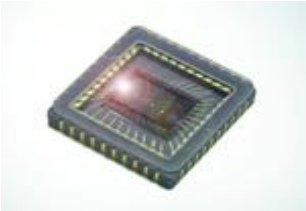
Package layout information Sheet

Crystal Image through
Imaging Innovation
PIXELPLUS



Issue number: PK-701-

PK5210N 64CLCC Package Information

Rev 0.2

Last update : Apr. 12th, 2021

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Revision History

Version	Date [D/M/Y]	Notes	Writer
0.0	06/01/2021	*New release*	HJ Kim
0.1	21/01/2021	*Changed DVDD, DVDDM Pad description (Page 4~5)*	Shine Park
0.2	12/04/2021	*Changed Pin information and description about MIPI (Page 3~6)*	HJ Kim

General Information

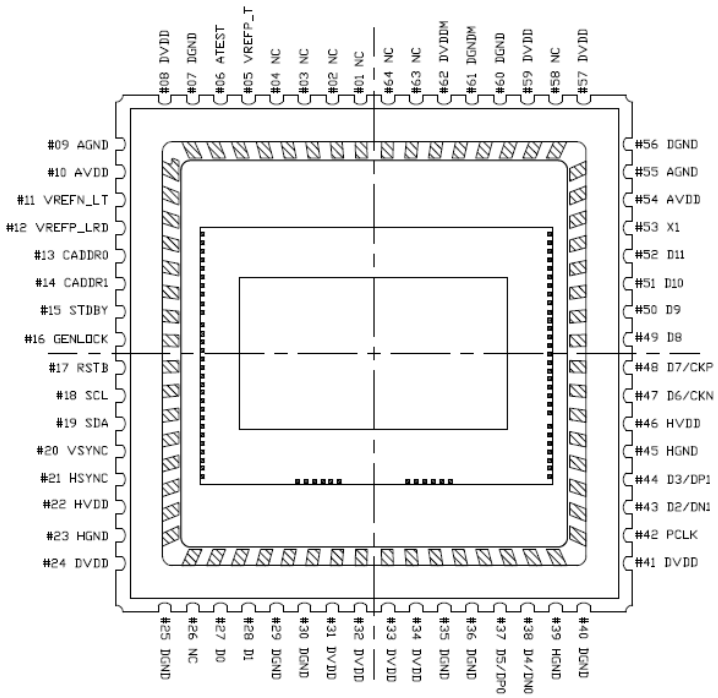
Product Name	PK5210N
Device Type	CMOS Mixed device
Product Package Type	64CLCC

Caution : This information can be changed without prior notice !! If you want to get up-to-date version, please send a mail to support@pixelplus.com

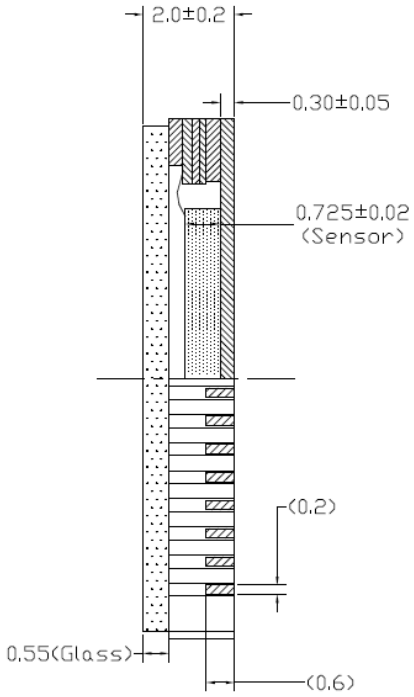
Package Mechanical Drawing (64CLCC)

IMAGE DIRECTION

TOP VIEW



SIDE VIEW



※Remark : Package Center = Image Center

BOTTOM VIEW

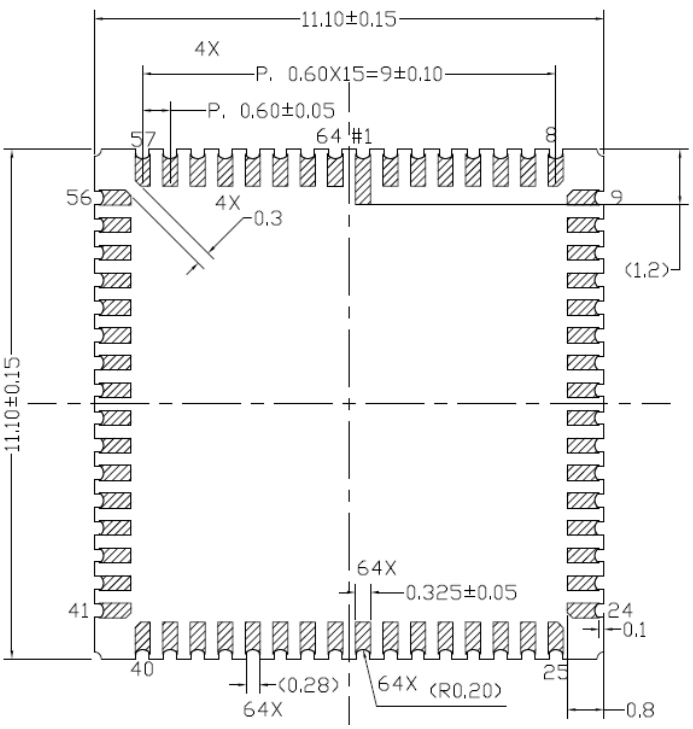
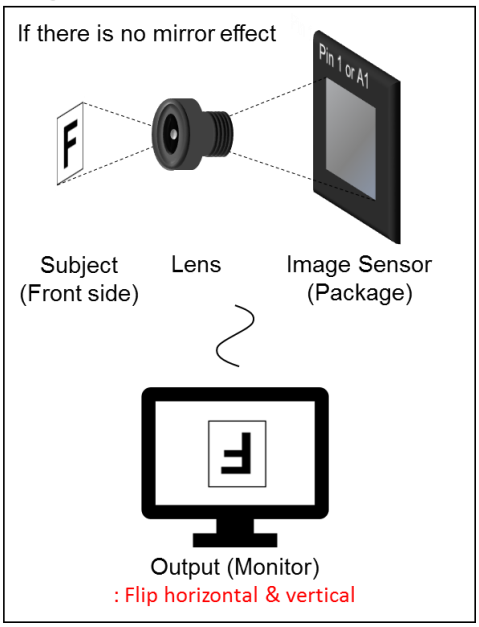


Image direction



Package Pin Assignment Table (1/2)

Num	NAME	I/O Type	pullup/ pulldown	PAD Description
1	NC	-	-	No connection
2	NC	-	-	No connection
3	NC	-	-	No connection
4	NC	-	-	No connection
5	VREFP_T	O	-	PCP output. It should be tied with nearby AGND by both 1uF bypass capacitors.
6	ATEST	O	-	Analog TEST PAD
7	DGND	P	-	Digital(Core) GND
8	DVDD	P	-	Digital(Core) VDD 1.3V DC
9	AGND	P	-	Analog GND
10	AVDD	P	-	Analog VDD 3.3V
11	VREFN_LT	O	-	NCP output. It should be tied with nearby AGND by both 1uF bypass capacitors.
12	VREFP_LRD	O	-	PCP output. It should be tied with nearby AGND by both 1uF bypass capacitors.
13	CADDR0	I	pullup	Chip Address0 selection bit
14	CADDR1	I	pullup	Chip Address1 selection bit
15	STDBY	I	pulldown	Power stdby mode. When Stdby ='1', there's no current flow in any analog circuit branch, neither any beat of digital clock.
16	GENLOCK	BIO	Pulldown	External Frame sync input. Slave chip can receive the external frame sync signal from master chip/External Frame sync output. Master chip can output the external frame sync signal through this pad to synchronize all digital outputs of two or more chips.
17	RSTB	I	Pullup	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
18	SCL	I	Pullup	2-wire serial interface clock, SCL line is pulled up to HVDD by off-chip resistor.
19	SDA	BIO	Pullup	2-wire serial interface data, SDA line is pulled up to HVDD by off-chip resistor.
20	VSYNC	O	Pulldown	Vertical sync : Indicates the start of a new frame
21	HSYNC	O	Pulldown	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
22	HVDD	P	-	IO VDD 3.3V DC
23	HGND	P	-	IO GND
24	DVDD	P	-	Digital(Core) VDD 1.3V DC
25	DGND	P	-	Digital(Core) GND
26	NC	-	-	No connection
27	D0	O	pulldown	Digital Output bit 0
28	D1	O	pulldown	Digital Output bit 1
29	DGND	P	-	Digital(Core) GND
30	DGND	P	-	Digital(Core) GND
31	DVDD	P	-	Digital(Core) VDD 1.3V DC
32	DVDD	P	-	Digital(Core) VDD 1.3V DC
33	DVDD	P	-	Digital(Core) VDD 1.3V DC
34	DVDD	P	-	Digital(Core) VDD 1.3V DC
35	DGND	P	-	Digital(Core) GND
36	DGND	P	-	Digital(Core) GND
37	D5 / DP0	O	pulldown	Digital Output bit 5 & MIPI DP0 Output (When in MIPI mode, HVDD is put the voltage for 3.3V)
38	D4 / DN0	O	pulldown	Digital Output bit 4 & MIPI DN0 Output (When in MIPI mode, HVDD is put the voltage for 3.3V)
39	HGND	P	-	IO GND
40	DGND	P	-	Digital(Core) GND

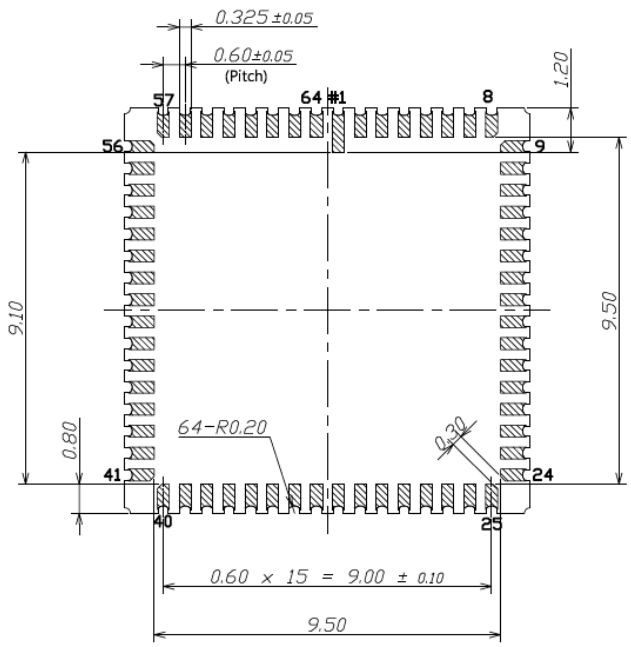
Package Pin Assignment Table (2/2)

Num	NAME	I/O Type	pullup/ pulldown	PAD Description
41	DVDD	P	-	Digital(Core) VDD 1.3V DC
42	PCLK	O	pulldown	Pixel clock Data can be latched by external devices at the rising or falling edge of PCLK.
43	D2 / DN1	O	pulldown	Digital Output bit 2 & MIPI DN1 Output (When in MIPI mode, HVDD is put the voltage for 3.3V)
44	D3 / DP1	O	pulldown	Digital Output bit 3 & MIPI DP1 Output (When in MIPI mode, HVDD is put the voltage for 3.3V)
45	HGND	P	-	IO GND
46	HVDD	P	-	IO VDD 3.3V DC
47	D6 / CKN	O	pulldown	Digital Output bit 6 & MIPI CKN Output (When in MIPI mode, HVDD is put the voltage for 3.3V)
48	D7 / CKP	O	pulldown	Digital Output bit 7 & MIPI CKP Output (When in MIPI mode, HVDD is put the voltage for 3.3V)
49	D8	O	pulldown	Digital Output bit 8
50	D9	O	pulldown	Digital Output bit 9
51	D10	O	pulldown	Digital Output bit 10
52	D11	O	pulldown	Digital Output bit 11
53	X1	I	-	Master clock input pad
54	AVDD	P	-	Analog VDD 3.3V
55	AGND	P	-	Analog GND
56	DGND	P	-	Digital(Core) GND
57	DVDD	P	-	Digital(Core) VDD 1.3V DC
58	NC	-	-	No connection
59	DVDD	P	-	Digital(Core) VDD 1.3V DC
60	DGND	P	-	Digital(Core) GND
61	DGNDM	P	-	MIPI GND
62	DVDDM	P	-	MIPI VDD 1.3V DC
63	NC	-	-	No connection
64	NC	-	-	No connection

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	NC	14	CADDR1	27	D0	40	DGND	53	X1
2	NC	15	STDBY	28	D1	41	DVDD	54	AVDD
3	NC	16	GENLOCK	29	DGND	42	PCLK	55	AGND
4	NC	17	RSTB	30	DGND	43	D2/DN1	56	DGND
5	VREFP_T	18	SCL	31	DVDD	44	D3/DP1	57	DVDD
6	ATEST	19	SDA	32	DVDD	45	HGND	58	NC
7	DGND	20	VSYNC	33	DVDD	46	HVDD	59	DVDD
8	DVDD	21	HSYNC	34	DVDD	47	D6/CKN	60	DGND
9	AGND	22	HVDD	35	DGND	48	D7/CKP	61	DGNDM
10	AVDD	23	HGND	36	DGND	49	D8	62	DVDDM
11	VREFN_LT	24	DVDD	37	D5/DP0	50	D9	63	NC
12	VREFP_LRD	25	DGND	38	D4/DN0	51	D10	64	NC
13	CADDR0	26	NC	39	HGND	52	D11		

Recommended PCB PAD Size for SMT

64 CLCC
BOTTOM VIEW



Recommended a Foot pattern of
64 CLCC