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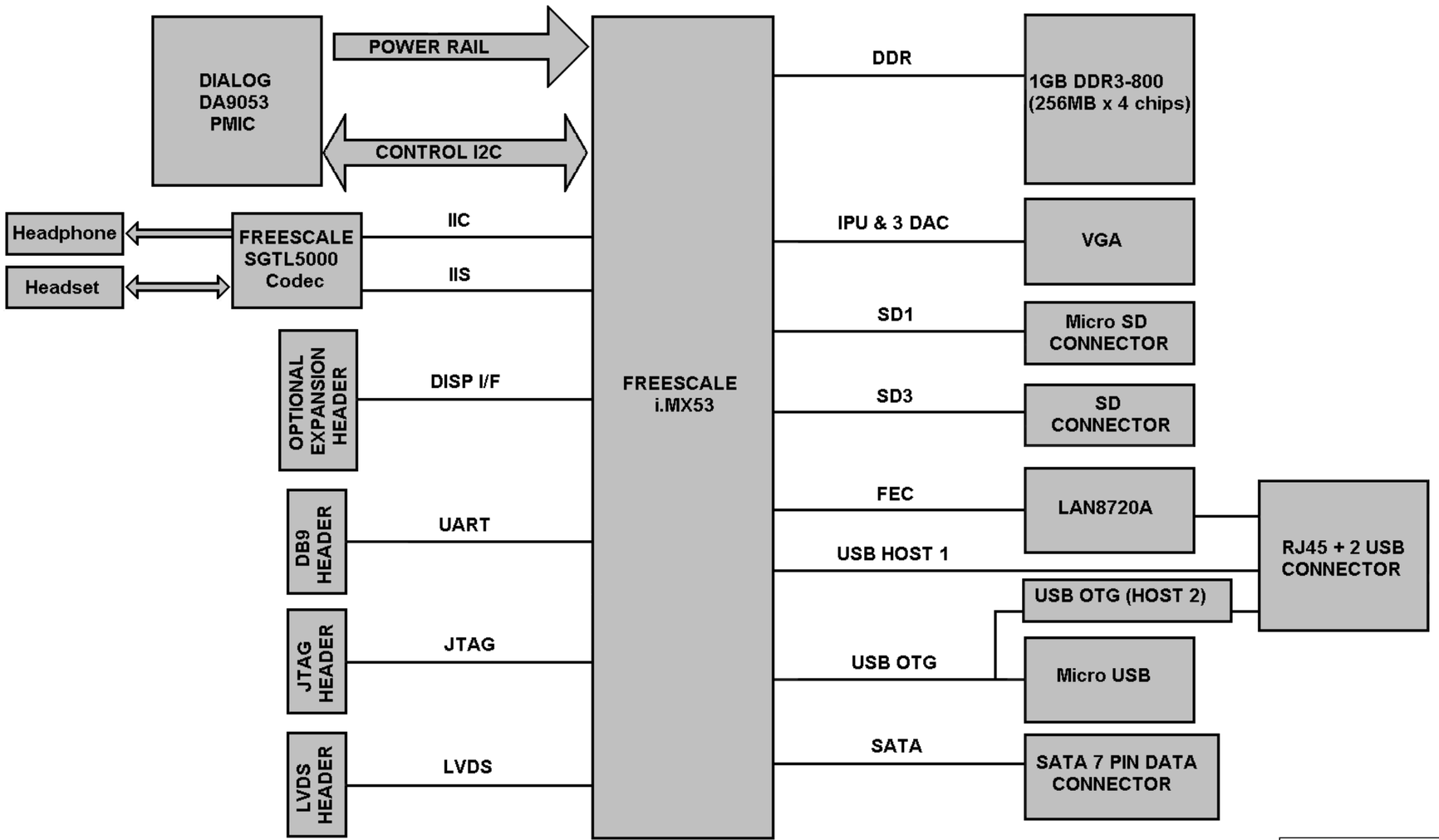
Revisions

Rev	Description	Date	Approved
A	Release to Inital Prototype	05/13/10	Mark Midddleton
B	Release to Pilot Build	10/15/10	Mark Midddleton
C	Parts U11, C163, C168, C169, and R111 now DNP. SATA clock reference now generated internally to i.MX53 processor. Input to Q13 pin 3 changed to VBUCKPRO. LVDS connector J9 pin 30 NO CONNECT. R151 now populated to support Touch Screen. Added 5V_MAIN power to J13 pins 11,13 to provide power to optional LCD display module.	01/11/11	Mark Midddleton
D	Parts Q13, and R203 are now DNP	03/11/11	Mark Midddleton

MCIMX53-QUICKSTART



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Multimedia Application Division, Wireless & Mobile System Group

 ICAP Classification: FCP: ___ FIUO: ___ PUBI: X ___

Designer: Mark Middleton	Drawing Title: MCIMX53-QUICKSTART		
Drawn by: DRAWN_BY	Page Title: COVER		
Approved: <Approver>	Size C	Document Number SOURCE:SCH-26565 PDF:SPF-26565	Rev D
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GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC
Current Output: > 1A (depending on application)
Polarity: 
Inner Diameter: 2.1mm
Outer Diameter: 5.5mm

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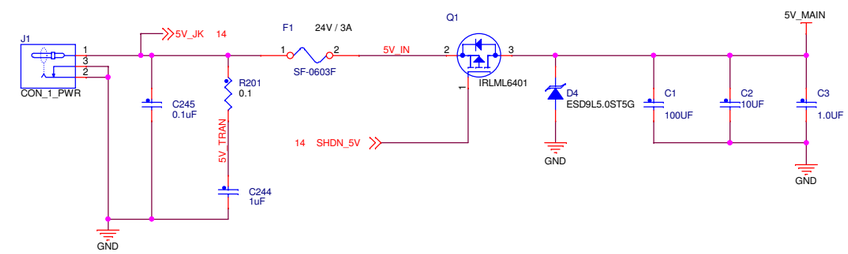
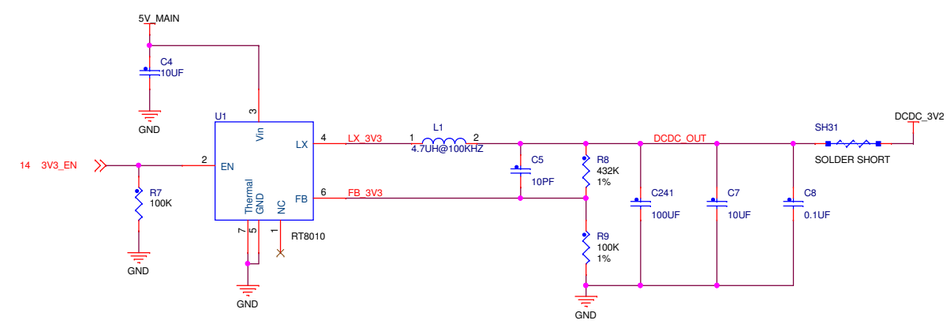
Power Table

DOMAIN	VOLTAGE	MODULE	SUBSYSTEM	BOOT TIMING
MAIN_5V	5V		PMIC DCDC_3V3 DISPLAY LEDS USB_HOST_PWR VGA_OUTPUT	ALWAYS ON
VLDO1	1V3	NVCC_SRTC		ALWAYS ON
VBUCKPRO	1V3	VCC		19 mSEC
VBUCKPERI	2V5	VDD_REG NVCC_XTAL		23 mSEC
VLDO6	1V3	VDDAL		23 mSEC
VLDO8	1V8	NVCC_RESET NVCC_JTAG NVCC_CKIH NVCC_NANDF NVCC_CSI VDD_ANA_PLL	BOOT_SEL	23 mSEC
VLDO10	1V3	VDDA		23 mSEC
VBUCKCORE	1V1	VDDGP		27 mSEC
VBUCKMEM	1V5	NVCC_EMI_DRAM	DDR3	31 mSEC
VBUCKPERI /SW	2V5		LVDS_2V5 SATA_PHY_2V5 USB_2V5	31 mSEC
VLDO2	1V3	VDD_DIG_PLL		31 mSEC
VLDO5	1V3		SATA_1V3	31 mSEC
VLDO4	2V775	NVCC_LCD1&2 VIOHI		35 mSEC
VLDO7	2V75	TVDAC	VGA	35 mSEC
VLDO3	3V3	NVCC_EIM_MAIN NVCC_EIM_SEC NVCC_SD1&2 NVCC_PATA NVCC_FEC NVCC_GPIO NVCC_KEYPAD	SD1 I2C1&2 BOOT_SEL	64 mSEC
VLDO9	1V5		EXP HDR	64 mSEC
DCDC_3V2	3V2	VDD_FUSE	FEC SD3 LCD_PORT USB_3V3 VGA_IO AUDIO	64 mSEC

5V@2A DC IN



3.3V@1A DC2DC



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Drawing Title: **MCIMX53-QUICKSTART**

Page Title: **MAIN 5V INPUT**

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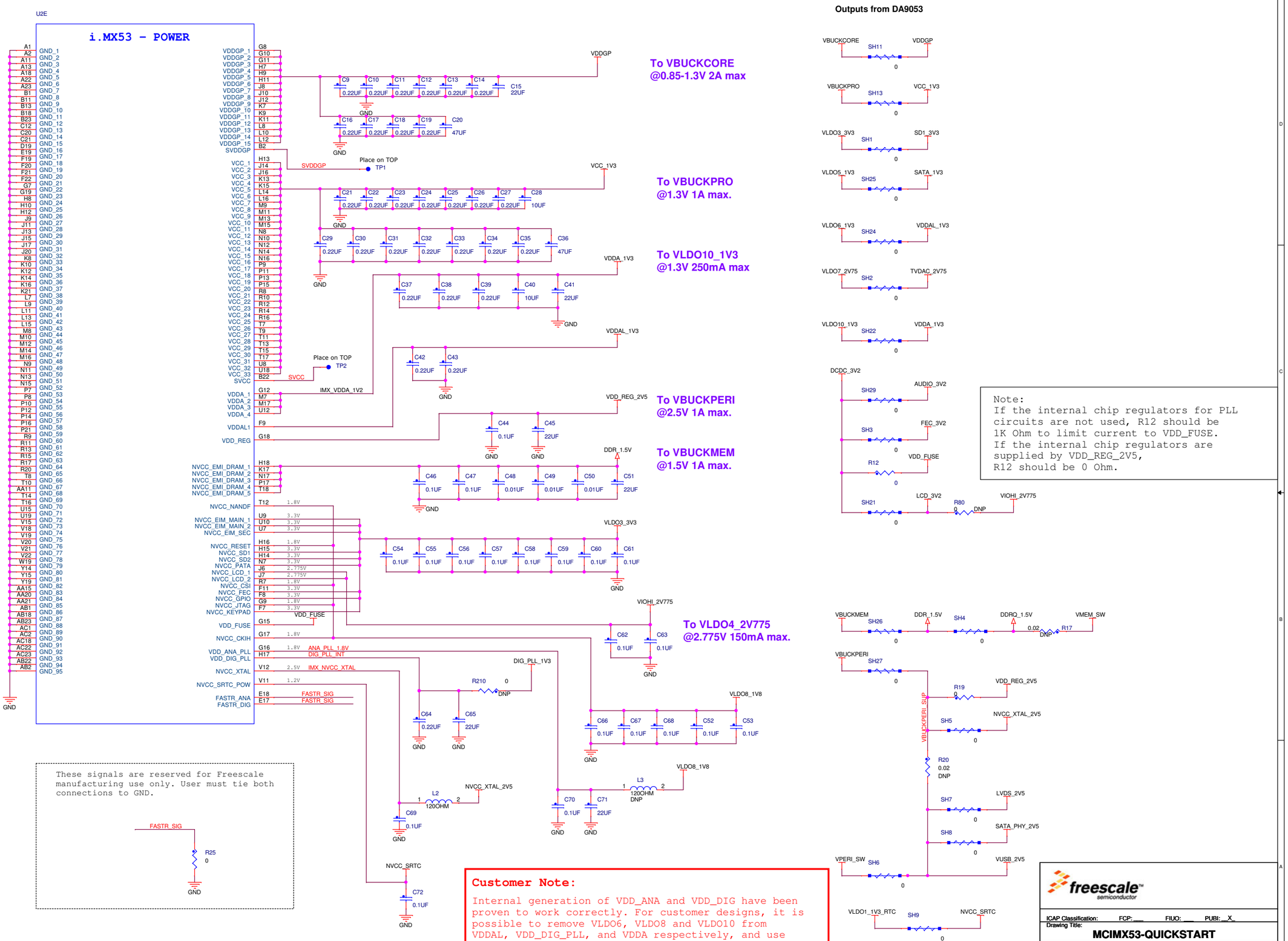
Outputs from DA9053
U2E
i.MX53 - POWER
To VBUCKCORE
@0.85-1.3V 2A max
To VBUCKPRO
@1.3V 1A max.
To VLDO10_1V3
@1.3V 250mA max
To VBUCKPERI
@2.5V 1A max.
To VBUCKMEM
@1.5V 1A max.
To VLDO4_2V775
@2.775V 150mA max.
Note:
If the internal chip regulators for PLL circuits are not used, R12 should be 1K Ohm to limit current to VDD_FUSE.
If the internal chip regulators are supplied by VDD_REG_2V5, R12 should be 0 Ohm.
These signals are reserved for Freescale manufacturing use only. User must tie both connections to GND.
Customer Note:
Internal generation of VDD_ANA and VDD_DIG have been proven to work correctly. For customer designs, it is possible to remove VLDO6, VLDO8 and VLDO10 from VDDAL, VDD_DIG_PLL, and VDDA respectively, and use those LDO regulators for other purposes. VDDA and VDDAL need to be connected to VDD_DIG_PLL externally in that case.
THIS MUST BE POWERED UP FIRST
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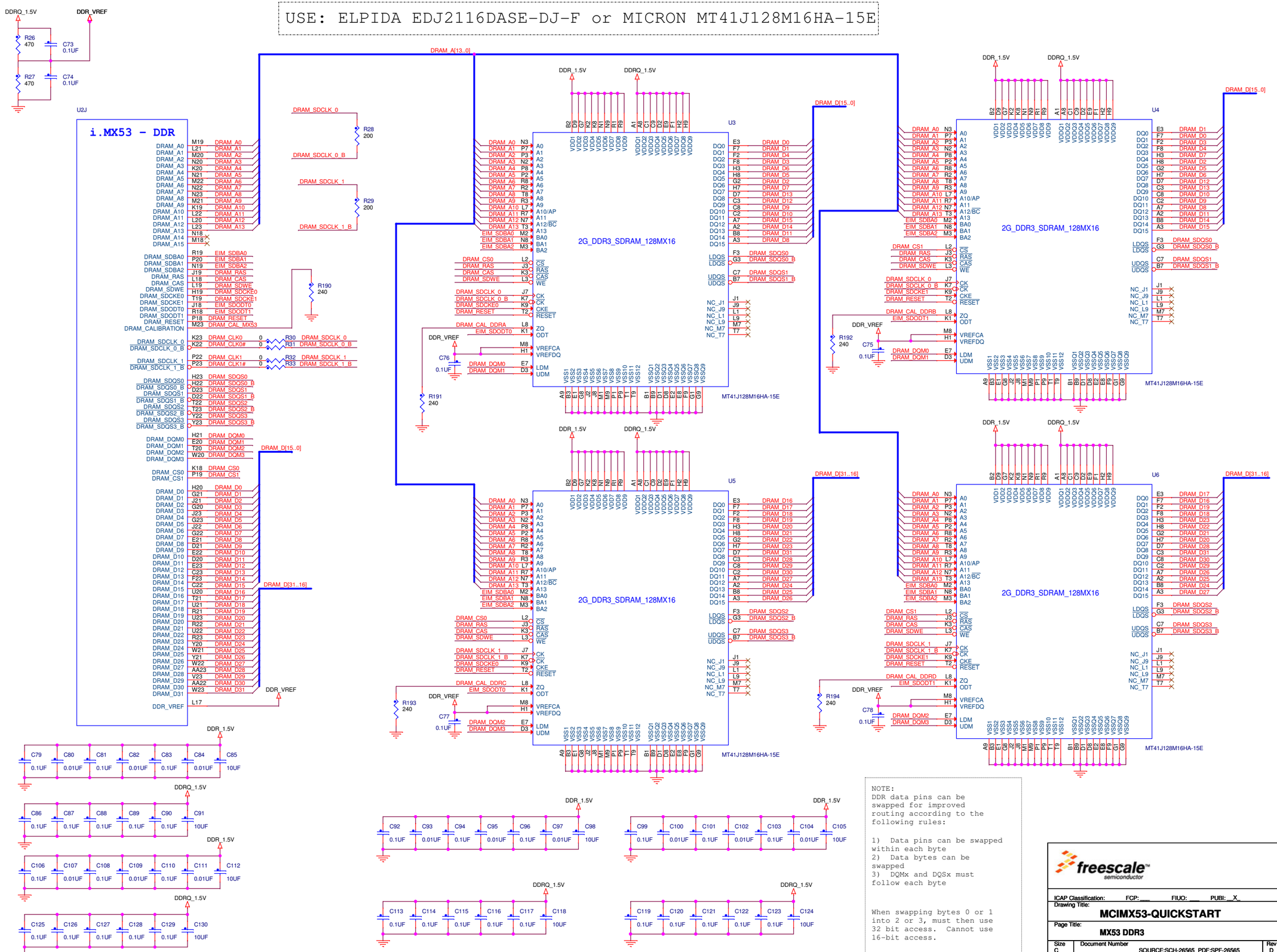
USE: ELPIDA EDJ2116DASE-DJ-F or MICRON MT41J128M16HA-15E



NOTE:
DDR data pins can be swapped for improved routing according to the following rules:

1) Data pins can be swapped within each byte
2) Data bytes can be swapped
3) DQMx and DQSx must follow each byte

When swapping bytes 0 or 1 into 2 or 3, must then use 32 bit access. Cannot use 16-bit access.

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Page Title: **MX53 DDR3**

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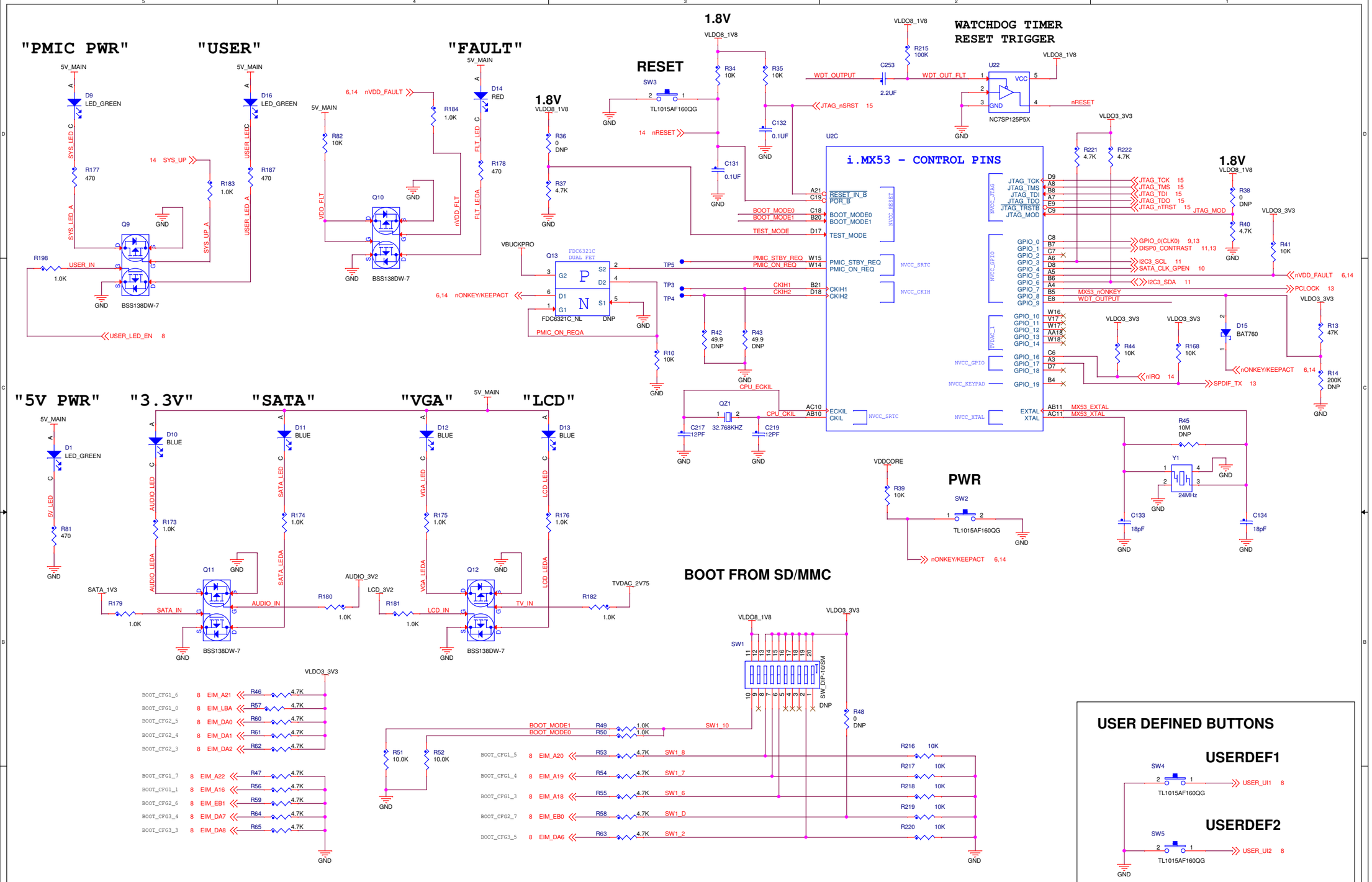

BOOT OPTION TABLE

SW1									
10	9	8	7	6	5	4	3	2	1
BOOT MODE	Not Used	Card Type:	Fast Boot:	sSD/MMC Speed	Not Used	Not Used	Not Used	Port Select	Not Used
0 - Internal Boot (default)		0 - SD/eSD	0 - Regular	0 - High				0 - eSDHC1	
1 - Serial Download		1 - MMC/eMMC	1- Fast Boot	1 - Normal				1 - eSDHC3	

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Drawing Title: **MCIMX53-QUICKSTART**

Page Title: **MX53 CONTROL**

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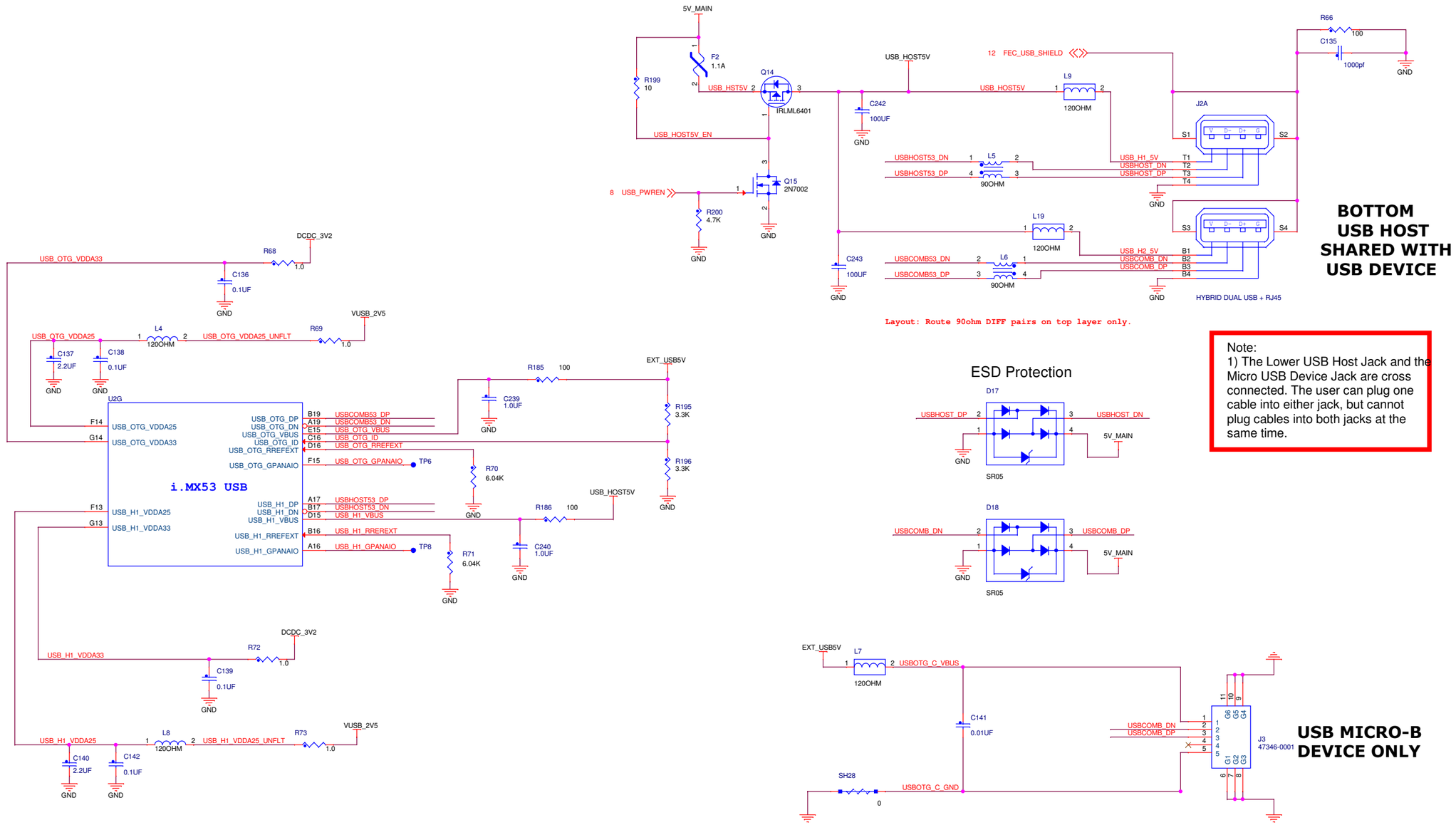

Note:
1) The Lower USB Host Jack and the Micro USB Device Jack are cross connected. The user can plug one cable into either jack, but cannot plug cables into both jacks at the same time.

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Drawing Title: **MCIMX53-QUICKSTART**

Page Title: **MX53 USB**

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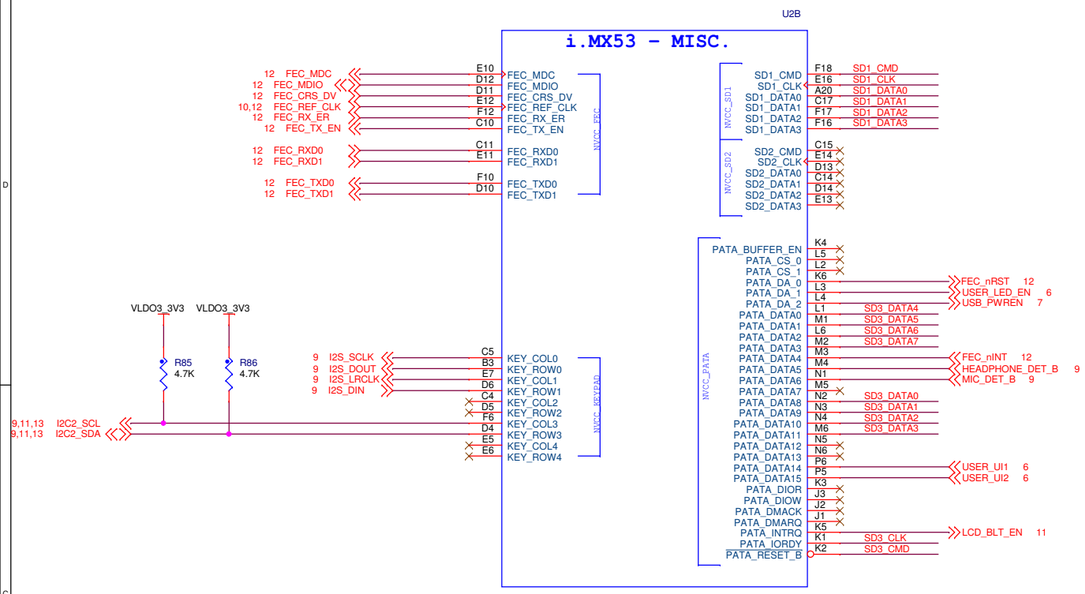
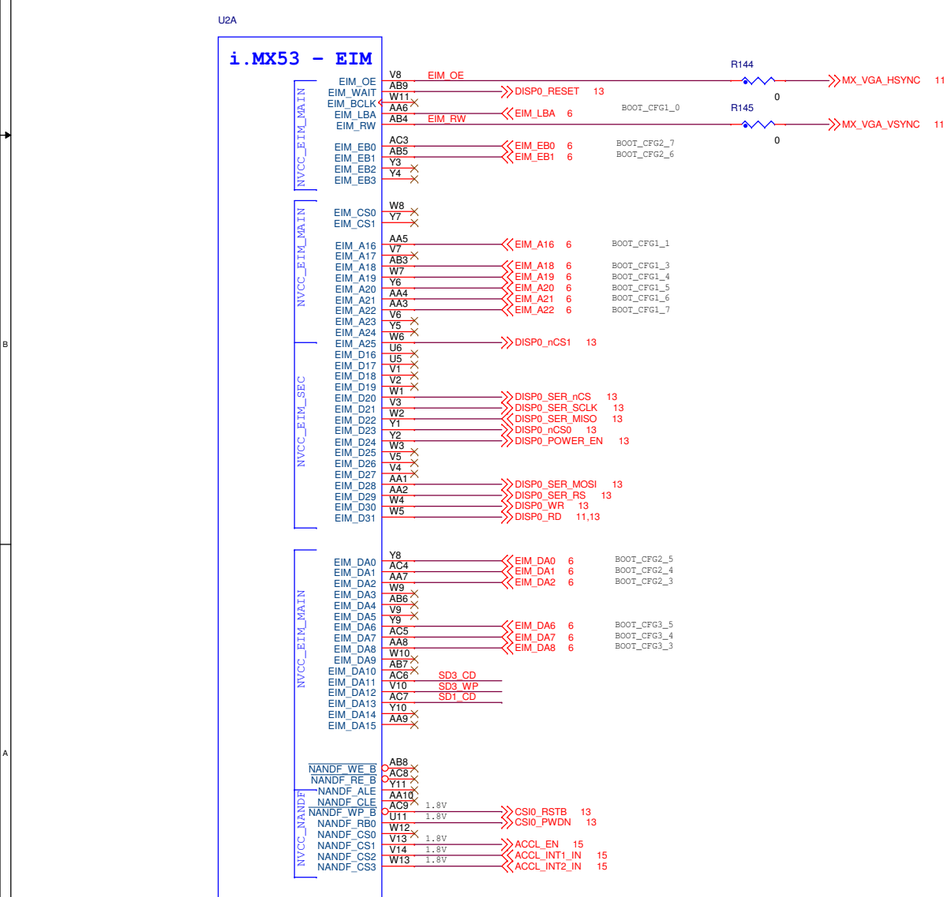
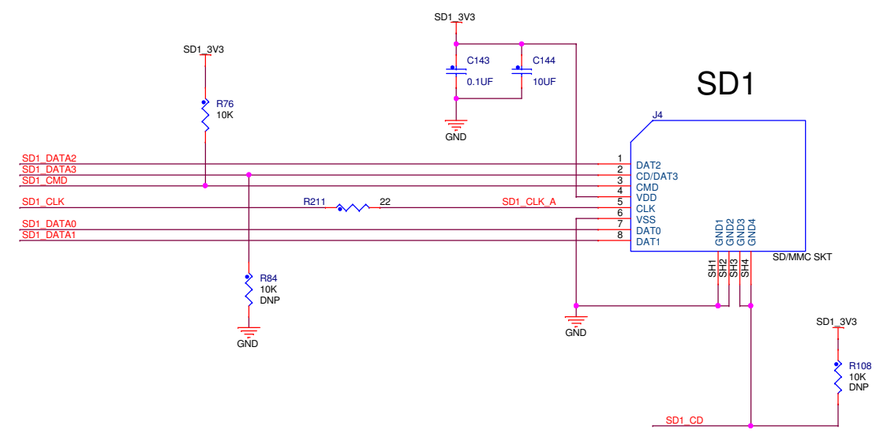
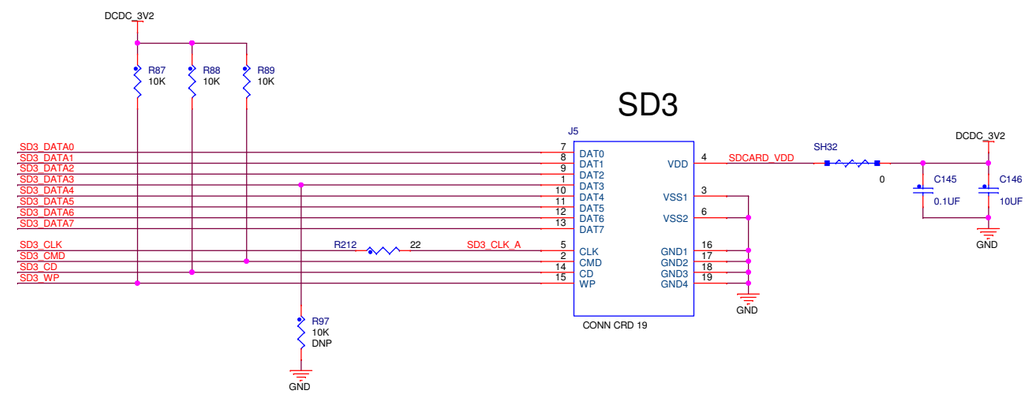
SD INTERFACES









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Drawing Title: **MCIMX53-QUICKSTART**

Page Title: **MX53 SD INTERFACE**

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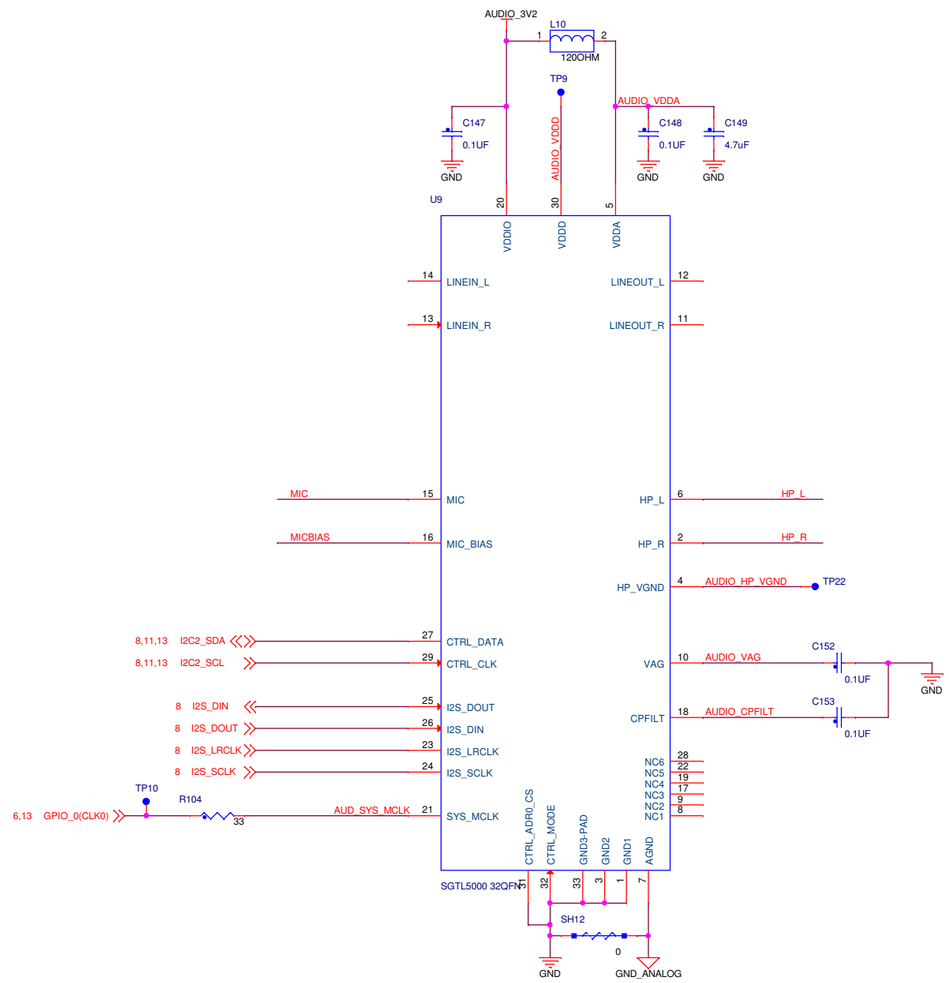
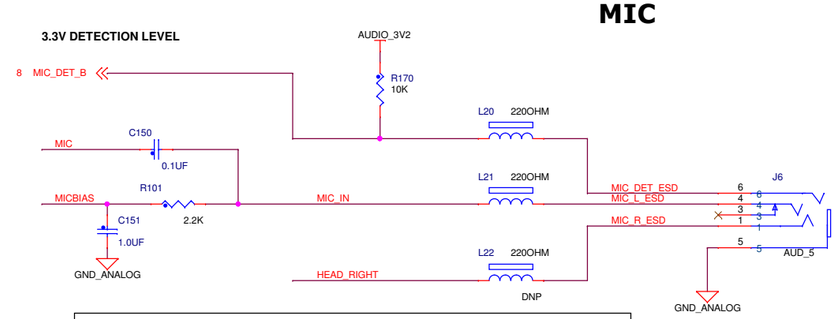
Audio CODEC

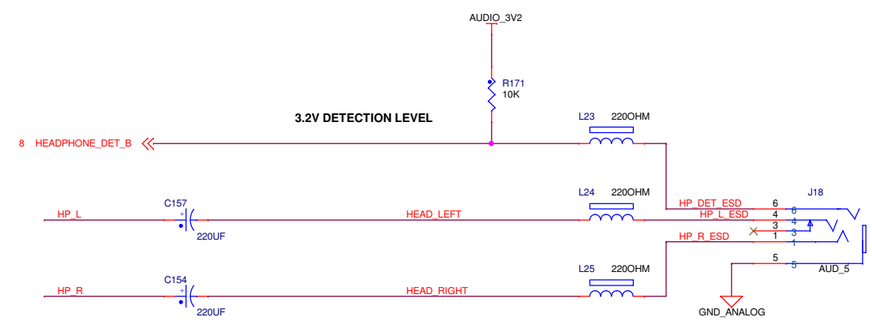


MIC



Note:
To support a MONO Headset with MIC, populate L22

Headphone



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Drawing Title: **MCIMX53-QUICKSTART**

Page Title: **MX53 AUDIO**

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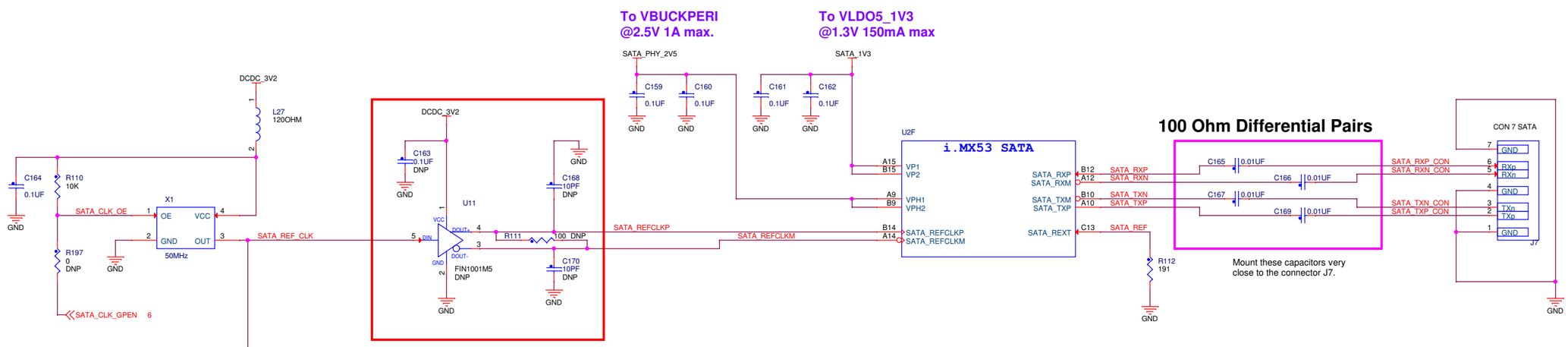
SATA



NOTE: Internal SATA clock reference was confirmed on tapeout T02.0. Optional parts have been removed from further production runs.

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Drawing Title: **MCIMX53-QUICKSTART**

Page Title: **MX53 SATA**

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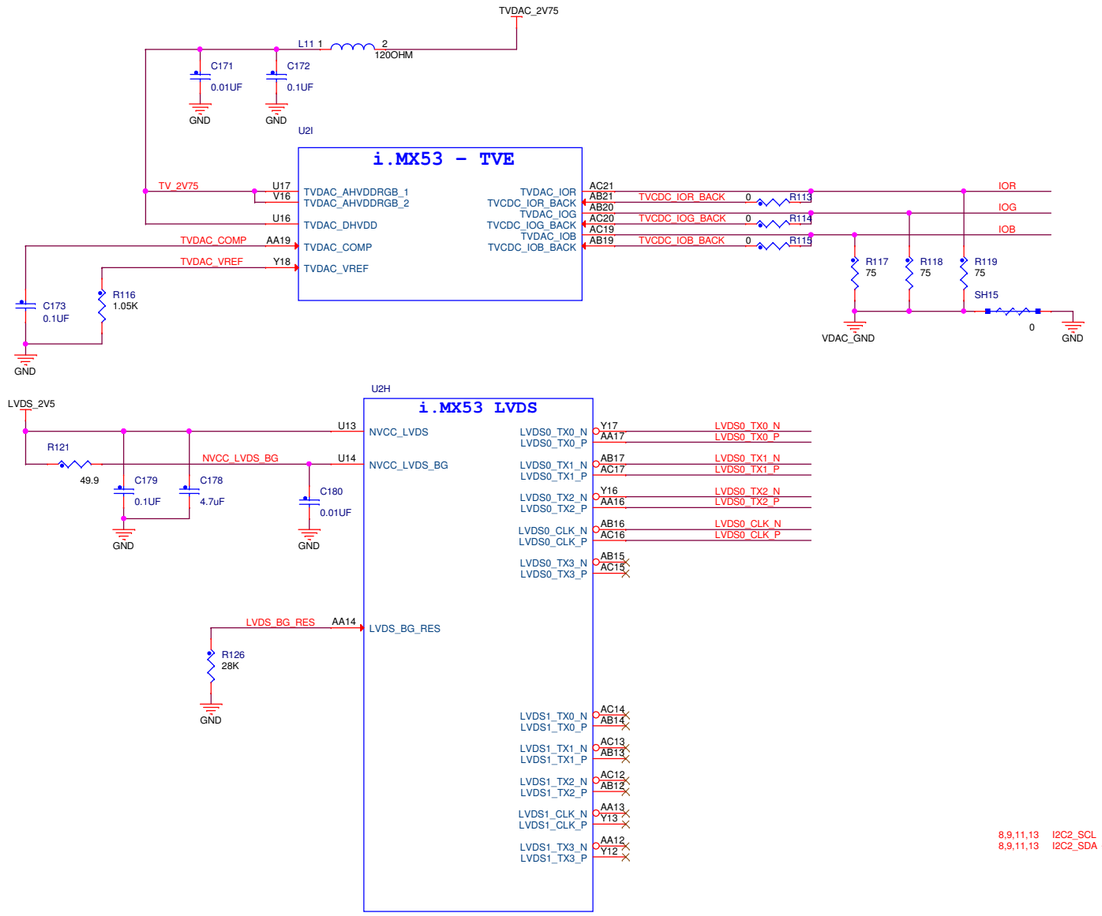
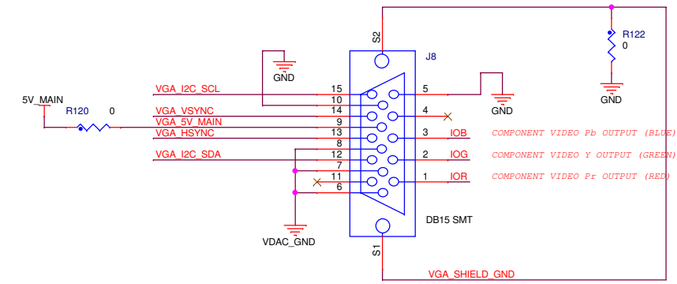
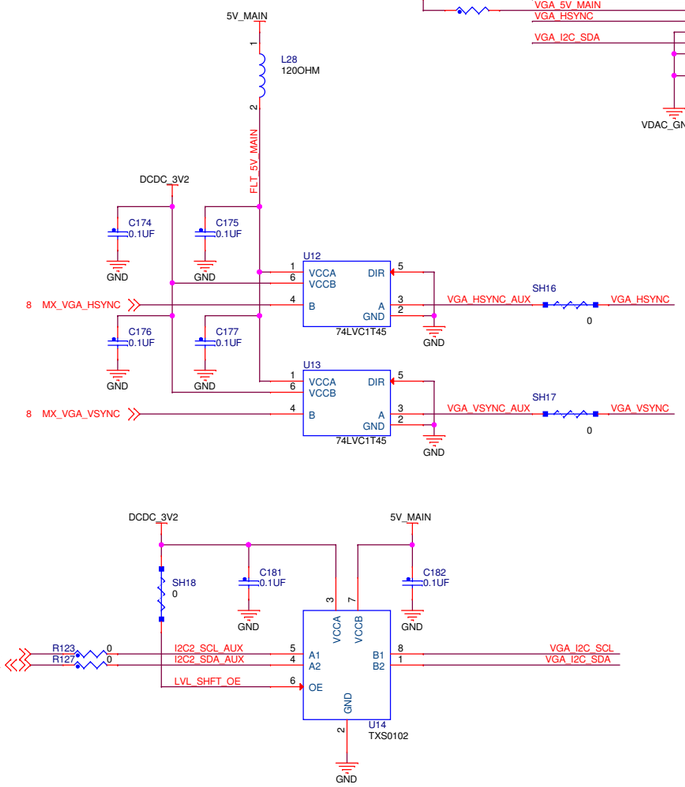
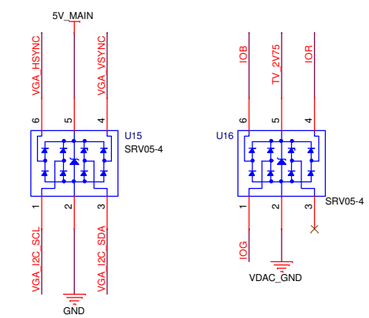
VGA



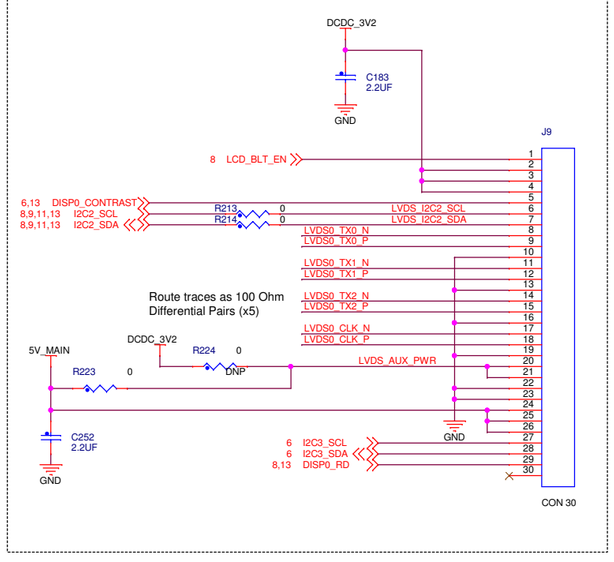
VGA VIDEO CONNECTOR







OPTIONAL LVDS0 DISPLAY OUTPUT



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Drawing Title: **MCIMX53-QUICKSTART**

Page Title: **MX53 VGA**

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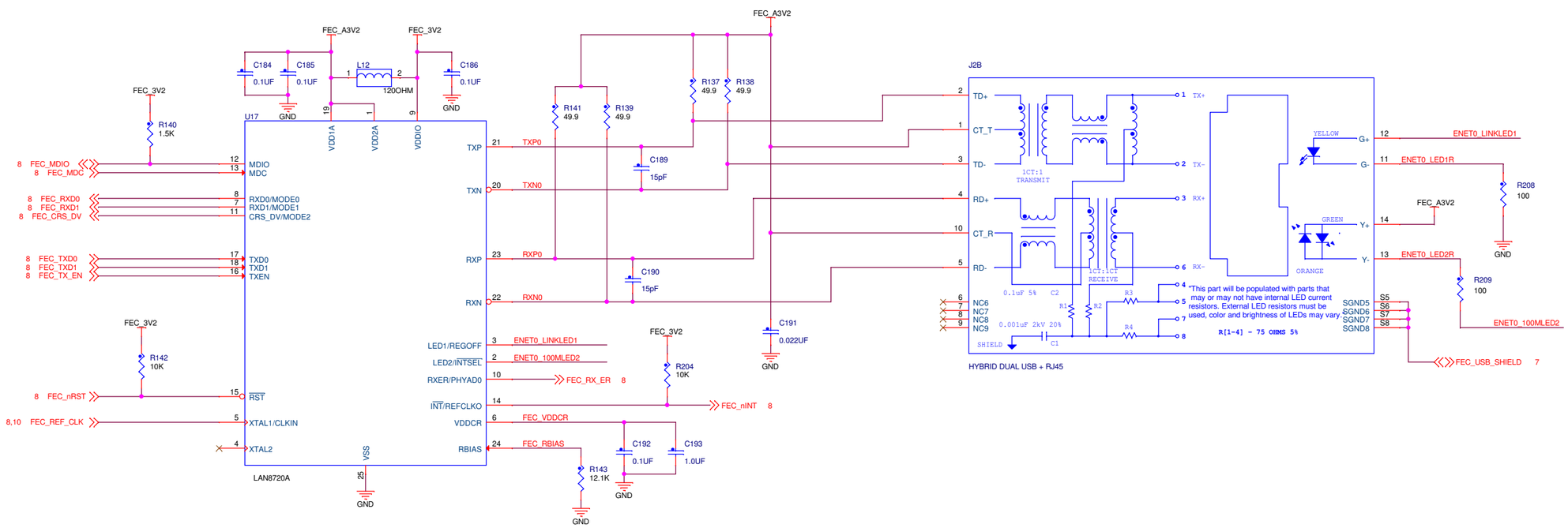
FAST ETHERNET PHY



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Drawing Title: **MCIMX53-QUICKSTART**

Page Title: **MX53 FEC**

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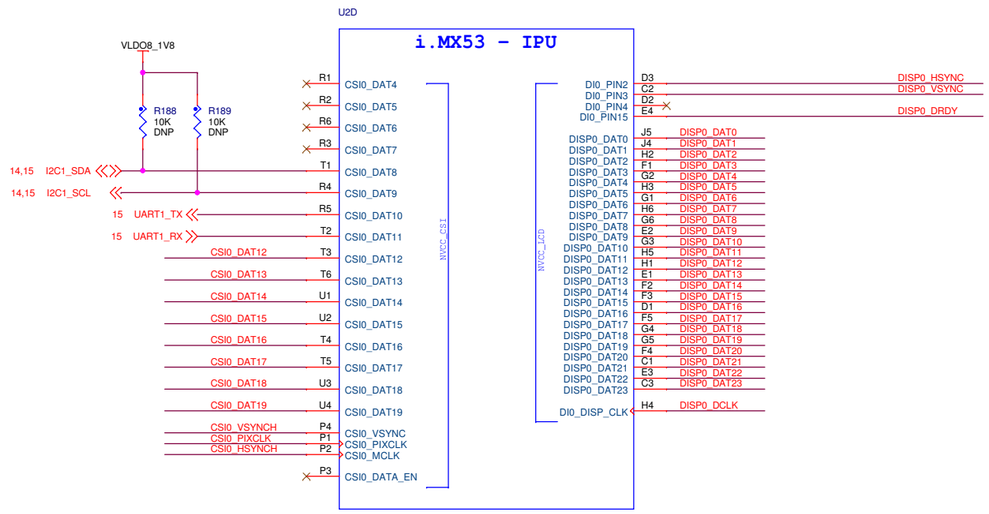
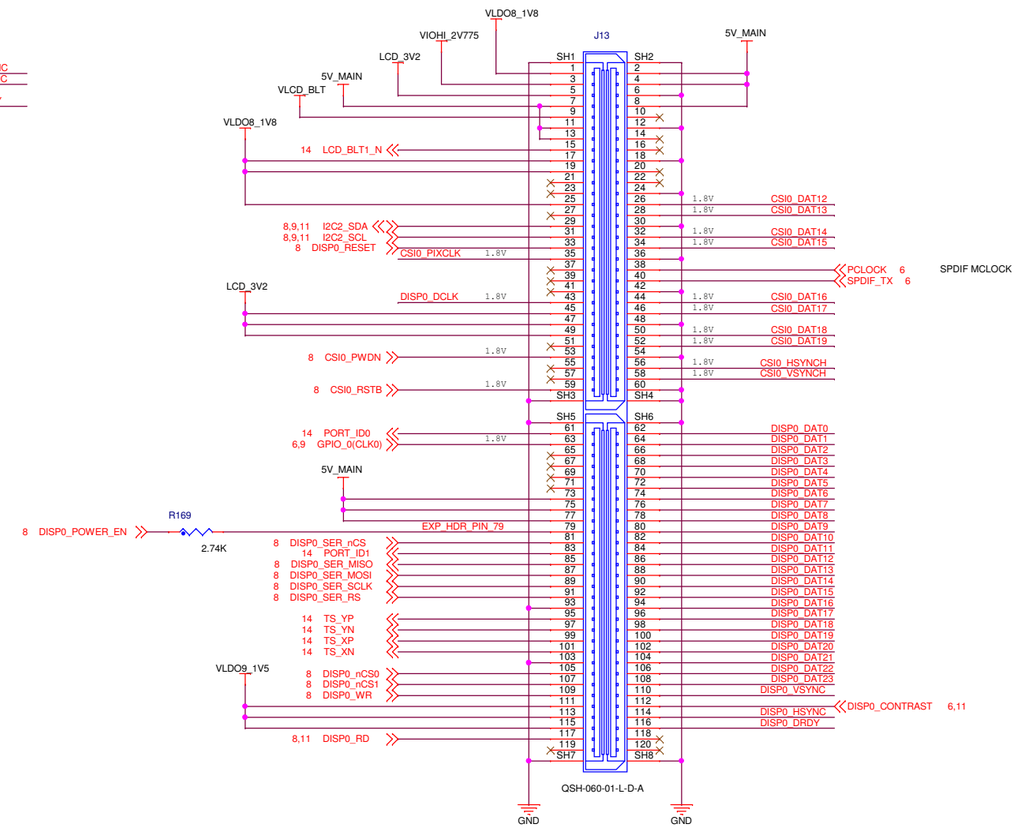
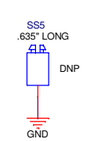
EXPANSION HEADER FOR DEBUG AND LCD I/F





EXP HDR STANDOFF



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Drawing Title: **MCIMX53-QUICKSTART**

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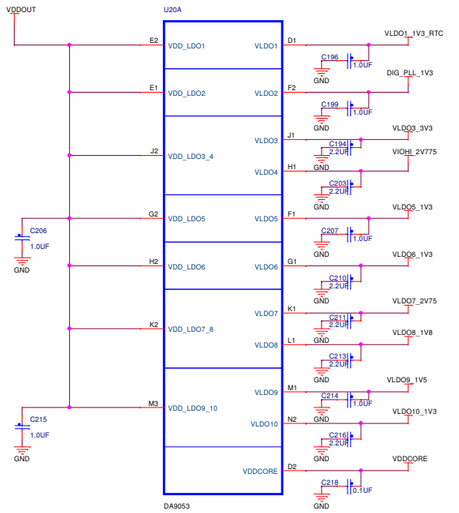
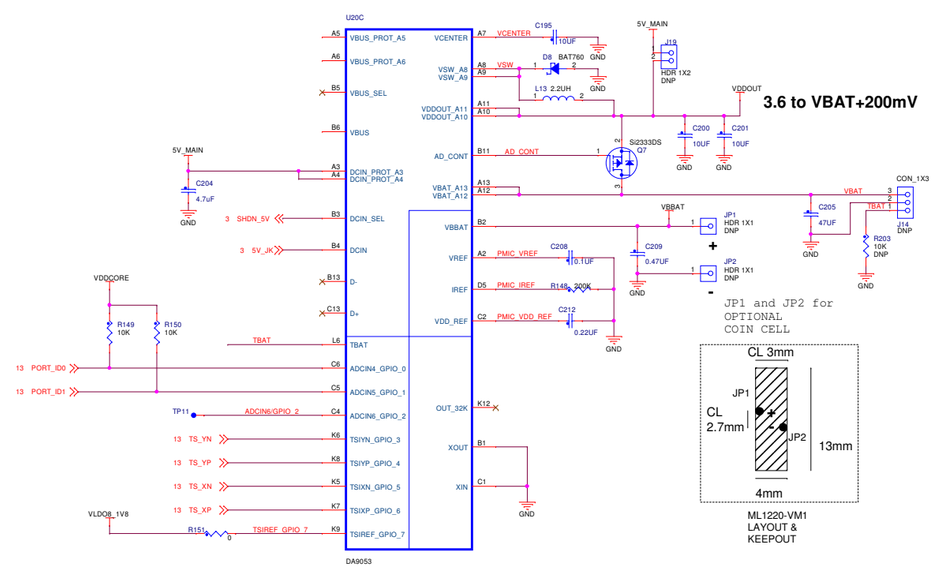
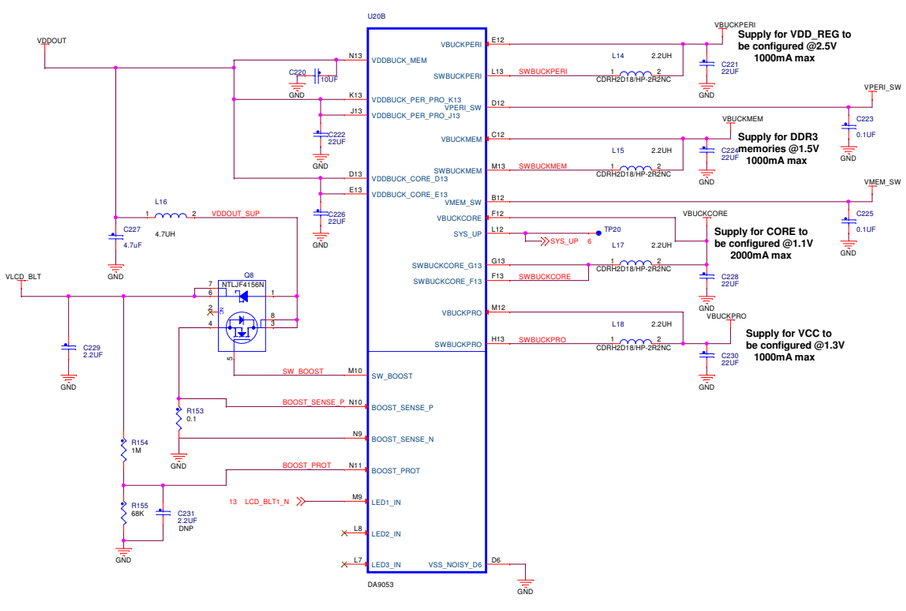
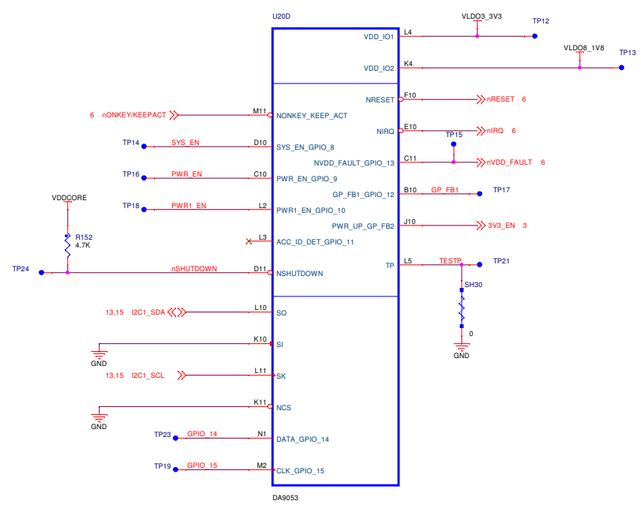
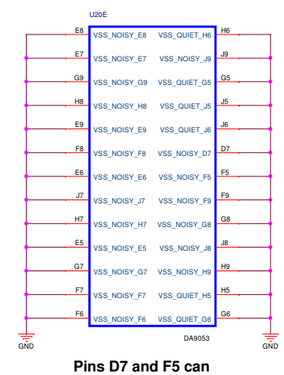




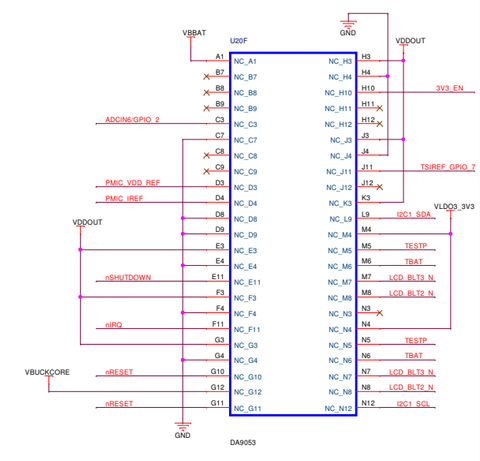
Regulator	Supplied pins	Supplied voltage	Supplied max. current	External Component	Notes
BUCKCORE	VBUCKCORE	0.5 – 2.075V ±3% accuracy default 1.8V	2000mA	2.2/1.0uH	DVC, 2MHz, 25mV steps, DVC ramp with controlled slew rate; pull-down resistor switch off
BUCKPRO	VBUCKPRO	0.5 – 2.075V ±3% accuracy default 1.2V	1000mA	2.2/1.0uH	DVC, 2MHz, 25mV steps, DVC ramp with controlled slew rate, , pull-down resistor switch off,
BUCKMEM	VBUCKMEM; VMEM_SW	0.925 – 2.5V ±3% accuracy default 2.0V	1000mA	2.2/1.0uH	DVC, 2MHz, 25mV steps, DVC ramp with controlled slew rate; 2nd output with sequencer controllable switch, pull-down resistor switch off,
BUCKPERI	VBUCKPERI VPERI_SW	0.925-2.475V ±3% accuracy default tbd	1000mA	2.2/1.0uH	2MHz, 25mV steps 2nd output with sequencer controllable switch
BOOST	Ext. FET	5 to 25V, regulated via current feedback	50mA	4.7uH	Current controlled boost converter for 3 strings of up to 6 serial white LEDs. Over voltage protection via a voltage feedback pin.
LDO1	VLDO1	0.6 – 1.8V ±3% accuracy default 1.2V	40mA	1.0uF	High PSSR, low noise LDO, 50mV steps, pull-down resistor switch off
LDO2	VLDO2	0.6 – 1.8V ±3% accuracy default 1.2V	100mA	1.0uF	DVC, digital LDO, 25mV steps, DVC ramp with controlled slew rate, pull-down resistor switch off
LDO3	VLDO3	1.725 – 3.3V ±3% accuracy default 2.85V	200mA	2.2uF	DVC, digital LDO, 25mV steps, DVC with controlled slew rate, common supply with LDO4
LDO4	VLDO4	1.725 – 3.3V ±3% accuracy default 2.85V	150mA	2.2uF	Digital LDO, 25mV steps, optional HW control from GPI1, common supply with LDO3
LDO5	VLDO5	1.2 – 3.6V ±3% accuracy default 3.1V	100mA	1.0uF	Digital LDO, 50mV steps, pull-down resistor switch off, optional HW control from GPI2,
LDO6	VLDO6	1.2 – 3.6V ±3% accuracy default 1.2V	150mA	2.2uF	High PSRR, low noise, 50mV steps
LDO7	VLDO7	1.2 – 3.6V ±3% accuracy default 3.1V	200mA	2.2uF	High PSRR, low noise, 50mV steps, common supply with LDO8
LDO8	VLDO8	1.2 – 3.6V ±3% accuracy default 2.85V	200mA	2.2uF	High PSRR, low noise, 50mV steps, common supply with LDO7
LDO9	VLDO9	1.25 – 3.6V ±1% accuracy default 2.5V	100mA	1.0uF	High PSRR, low noise, 50mV steps, OTP trimmed, optional HW control from GPI12, common supply with LDO10
LDO10	VLDO10	1.2 – 3.6V ±3% accuracy default 1.8V	250mA	2.2uF	High PSRR, low noise, 50mV steps, common supply with LDO9
BACKUP	VBBAT	1.1 – 3.1V default 3.0V	6mA	470nF	100/200mV steps, configurable current limit between 100 and 6000uA, reverse current protection
LDOCORE	Internal PMIC supply	2.5V ±2% accuracy	4mA	100nF	Not for external use







Pins D7 and F5 can be left open as they are "NC" pins.



Note:
Traces are routed to NC pins for layout purposes only.
This allows signals to route out of chip via NC pins on the top layer. NC pins are not connected to any pad internal to the PMIC.

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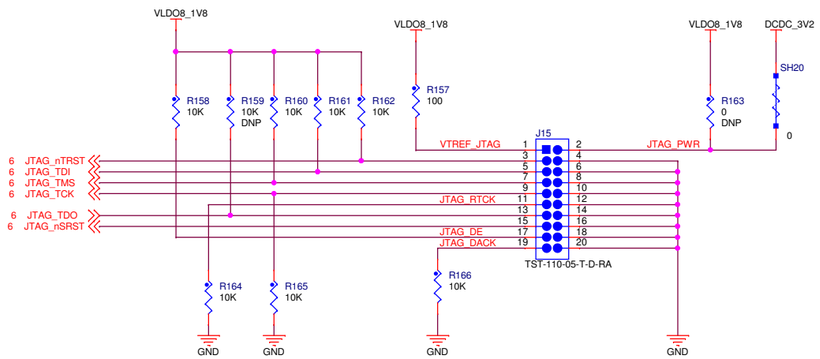
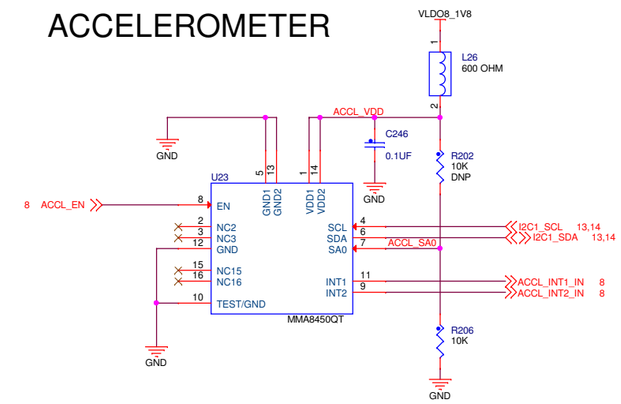
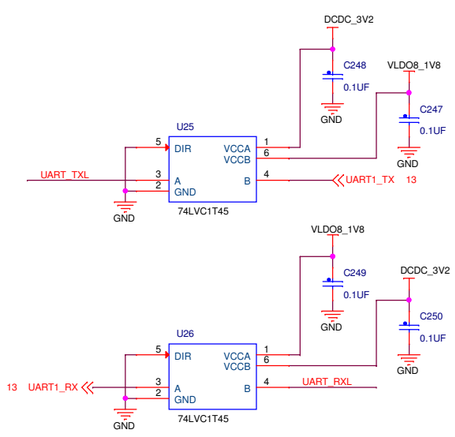
JTAG THROUGH HOLE CONNECTOR

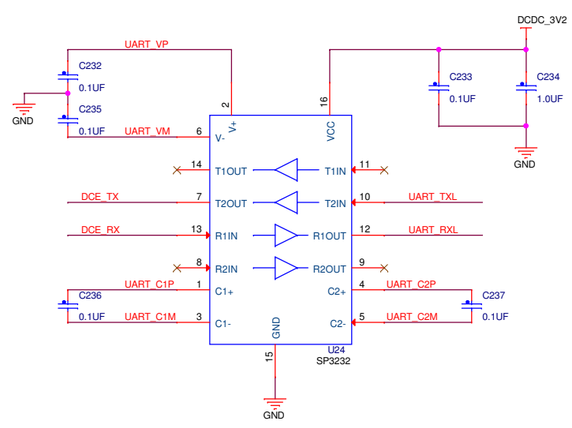


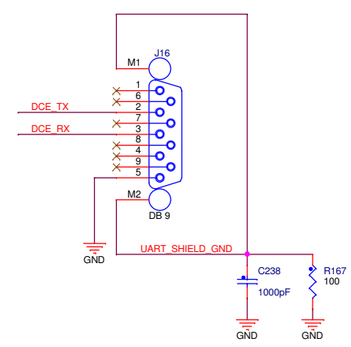
ACCELEROMETER



UART DB9 SMT CONNECTOR







DCE		
1	CD	O
2	TX	O
3	RX	I
4	DTR	I
5	GND	
6	DSR	O
7	RTS	I
8	CTS	O
9	RI	O

Female DB-9 Connector

freescale semiconductor

ICAP Classification: FCP: ___ FIUO: ___ PUBI: _X_

Drawing Title: **MCIMX53-QUICKSTART**

Page Title: **DEBUG, ACCELEROMETER**

Size	Document Number	Rev
C	SOURCE:SCH-26565 PDF:SPF-26565	D

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