SJA1110

Rev. 0.7 — 11 August 2021 Objective Datasheet

1 General description

SJA1110 is a family of automotive Ethernet switches offering a rich set of security, safety and TSN capabilities.

SJA1110 devices integrate:

- Up to six IEEE 100BASE-T1 PHYs
- A single IEEE 100BASE-TX PHY
- Up to two MII/RMII/RGMII interfaces
- Up to four SGMII interfaces
- An Arm Cortex-M7 ® based host controller

IEEE Audio Video Bridging (AVB) and the latest Time-Sensitive Networking (TSN) standards are supported.

The device comes in four variants, each capable of supporting a flexible and modular ECU design for Gateway, ADAS and Infotainment applications.

Flexible boot options allow for configuration via a selection of external NVMs or via an external host controller. Advanced security features allow for a secure boot mode to authenticate firmware before execution.

Innovative features such as frame inspection with a width of up to 128 bytes and two SGMII interfaces that can operate at up to 2.5 Gbit/s enable efficient cascading and uplinking to a host controller.

The SJA1110 is a purpose-built automotive switch that is AEC-Q100 qualified and compliant with ISO26262 ASIL B. All variants come in a 256-pin, 14 mm x 14 mm LFBGA package.

2 Features and benefits

2.1 General

- 10-port store-and-forward architecture for switch core with integrated 100BASE-T1 and 100BASE-TX transceivers
- Integrated Arm Cortex-M7 ® processor for autonomous and secure operation
- Selectable I/O voltages (1.8 V, 2.5 V and 3.3 V) offer design flexibility
- Small footprint
  - LFBGA256 (14 mm x 14 mm) package with 0.8 mm pitch
- Maximum junction temperature: +150 °C
- Automotive Grade 2 (ambient temperature: -40 °C to +105 °C)[1]
  - Variants A, B and C
- Automotive Grade 1 (ambient temperature: -40 °C to +125 °C)[1]
  - Variant D[2]
  - All variants are Grade 1 where total power dissipation does not exceed 1 W
- Automotive product qualification in accordance with AEC-Q100 Rev-H
- ISO 26262, ASIL-B compliant
- Sleep current <100 µA

2.2 Data interfaces

- Up to 10 data ports with integrated and external PHYs [3]
  - 6x integrated 100BASE-T1 PHYs
  - 1x 100BASE-TX or SGMII
  - 2x MII/RMII/RGMII or SGMII
  - 1x SGMII
- MII/RMII – 10/100 Mbit/s: 1.8 V/2.5 V/3.3 V selectable I/O operating voltage and programmable drive strength
- RGMII – 10/100/1000 Mbit/s; optional integrated delay (RGMII-ID), 1.8 V/2.5 V/3.3 V configurable I/O operating voltage with programmable drive strength
- SGMII – 10/100/1000 Mbit/s or 2500 Mbit/s[4] operation with 3.3 V I/O supply; programmable swing

2.3 100BASE-T1 PHYs

- Compliant with IEEE 802.3bw-2015 (100BASE-T1)
- Fully integrated MDI pin filtering
- Remote wake-up detection and forwarding according to OPEN Alliance TC10
- Up to 15 m cable length, including 110 ns propagation delay
- Dedicated PHY enable/disable input pin to support ISO 26262
- Local wake-up via dedicated wake pin

1 Automotive grade rating determined under conditions defined in JEDEC JESD51-6.
2 With 1.8 V xMII supply.
3 Number of interfaces depends on variant; highest number of ports (10) on variant A.
4 2500 Mbit/s operation supported for two dedicated ports.

- Enhanced link diagnosis
  - Diagnosis of cable errors
  - Signal Quality Index
  - Link training time
  - Link failure and link losses
- ESD robustness
  - MDI balls protected against ±4 kV HBM; ±2 kV HBM and 500 V CDM at any ball
  - MDI connector pins protected against ±6 kV IEC 61000-4-2 and ±8 kV(contact)/ ±15 kV(air) ISO 10605 with standard MDI circuitry
  - Link robustness for powered ESD Class-A1 up to 3 kV; prevents unwanted wake-up according to ESD Class-A3 up to 3 kV

2.4 L2 switch features

- IEEE802.3 and 802.1D compliant
- 256 kB frame buffer
- 1024 collision-free L2 lookup based on TCAM
- 2 kB frame length handling
- IEEE 802.1Q defined tag support
- 4096 VLANs
- Egress tagging/untagging on a per-VLAN basis per port
- QoS handling based on L2 (PCP bits) or L3 (IP TOS)
- Per-port policing based on PCP
- Per-port policing for multicast and broadcast traffic
- Per-port priority remapping and 8 configurable egress queues per port
- QinQ tag (double tag) support
- Configurable shapers (leaky bucket/credit based) and schedulers (strict priority, Weighted Round Robin (WRR), weighted fair queuing) per egress queue
- Frame replication, retagging and mirroring of traffic for enhanced diagnostics
- Extensive support for statistic counters, status flags and interrupt generation

2.5 Advanced traffic engineering features

- Additional configurable TCAM-based filter (bytes x depth): 16 x 1024/32 x 512/64 x 256/128 x128 for look-up and filtering capability up to L5 header
- Up to 1024 streams, each with IEEE 802.1Qci based policing capabilities
- Up to 4096 policers for L2 based streams (DA/SA/VID)
- Replication of frames toward a host and simultaneous forwarding for real-time traffic monitoring
- Timestamp capturing on filtered frames
- Support for static routing for L2 header replacement (SA or DA fields)

2.6 AVB and TSN features

- Hardware support for IEEE 802.1AS-2020 and IEEE 802.1Q AVB handling
- Ingress and egress timestamping per port
- Transit time in device measurement
- Credit-based shapers available according to IEEE 802.1Qav; shapers can be freely allocated to any priority queue on a per port basis

- Support for SR Class A, Class B and Class C traffic
- Free run and rate-corrected clock counters
- Software configurable PTP/media clock output
- IEEE 1588v2 E2E transparent operation in hardware
- IEEE 802.1Qci Per-stream Filtering and Policing (PSFP)
  - Up to 1024 streams based on configurable TCAM lookup
  - Up to 1024 Two Rate, Three Color (2R3C) policers with up to 8 input gates
- IEEE 802.1Qbv enhancements for scheduled traffic (time aware shaper)
  - Up to 256 schedule entries with 25 byte-time granularity for gate events
- IEEE 802.1CB frame replication and elimination for reliability
  - Stream selection based on either L2 TCAM or extended TCAM lookup
  - Operation as a talker end system, relay system or listener end system for every stream
  - Up to 64 streams for stream generation and recovery with L2 header modification

2.7 Integrated microcontroller features

- Arm Cortex-M7 ® core @ 200 MHz
  - 512 kB integrated SRAM as Instruction Tightly Coupled Memory (ITCM)
  - 256 kB integrated SRAM as Data Tightly Coupled Memory (DTCM)
  - Double-precision floating-point unit
  - Memory Protection Unit
- Boot time of less than 100 ms with a 512 kB firmware with authentication[5]
- Configurable boot options: from NVM (Flash/EEPROM) or external host
- Peripherals
  - SW Watchdog
  - 16-channel eDMA
  - 4-channel low-power interrupt timer (LPIT)
  - Cryptographic Acceleration and Assurance Module (CAAM)
- Communication peripherals
  - 1x 100 Mbit/s internal Ethernet MAC to switch core
  - 1x QSPI for external flash (quad lane or single lane) or serial EEPROM (single lane) for firmware and device configuration
  - 1x SPI for communication with peripherals (e.g. SBC)
  - 1x SPI for communication from external host
  - 1x SMI output for controlling external PHYs

2.8 External host interface

- SPI host interface to external microcontroller (direct register access to switch and PHY cores or proxied through internal microcontroller) for operation with a trusted host or when the integrated microcontroller is not used
- Access point SMI slave for configuration of internal 100BASE-T1 PHYs
- Separate reset inputs for the entire device and for the core only to enable Wake/Sleep operation
- Interrupt output

5 Using QSPI at 25 MHz.

2.9 Safety features

- Fail-safe shutdown inputs for integrated 100BASE-T1 PHYs
- Integrated system integrity unit monitoring health of device with an error indication output
- Memory with ECC
- Temperature sensors

2.10 Security features

- Ethernet security
  - IEEE 802.1X support for setting port reachability and disabling address learning
  - Extensive filtering rules for frame forwarding - retagging/tunneling/double tagging
  - Address learning space can be configured for static and learned addresses
  - Enhanced support for address learning restrictions for security
  - Ingress rate-limiting on a per-port basis for unicast/multicast and broadcast traffic
    - Broadcast storm protection
- Microcontroller security
  - Support for secure boot based on RSASSA-PSS 2048 and SHA-256 asymmetric signature verification
  - Firmware update via internal controller or external host
  - Firmware and key versioning for rollback prevention
  - Option to boot from an NVM (flash over QSPI, EEPROM over SPI) or from an external host controller via SPI

2.11 Clocks

- 25 MHz oscillator or clock reference input
- Four 25 MHz reference clock outputs
- Software configurable PTP clock output

2.12 Manufacturing and debug

- IEEE1149.1 and 1149.6 compliant JTAG and boundary scan interface
- Serial wire debug interface multiplexed with JTAG for software debugging

2.13 Supply voltage

- 3.3 V and 1.1 V supply
- 2.5 V supply: external or internal from integrated regulator
- Selectable IO voltage (1.8 V, 2.5 V, 3.3 V)

2.14 Other features

- 16 GPIOs
- Sync input/output
- Pinstrap options for boot configuration
- Pinstrap options for PHY configuration

3 Product family overview

Table 1. Feature overview of the SJA1110X family

Variant	Total No. of Ports[1]	100BASE-T1 PHYs	100BASE-TX PHYs	10/100/1000 SGMII	10/100/1000/2500 SGMII	MII/RMII/RGMII	AEC-Q100 Temp Grade[2]	LFBGA256 14 x 14 mm^2
SJA1110A	10	6	1	2	2	2	2	•
SJA1110B	9	5	1	0	2	2	2	•
SJA1110C	7	3	1	0	1	2	2	•
SJA1110D	7	3	0	2	2	2	1[3]	•

[1] Note that some interfaces are multiplexed and cannot be used at the same time.
[2] All variants are Grade 1 when total dissipation does not exceed 1 W.
[3] With 1.8 V xMII supply

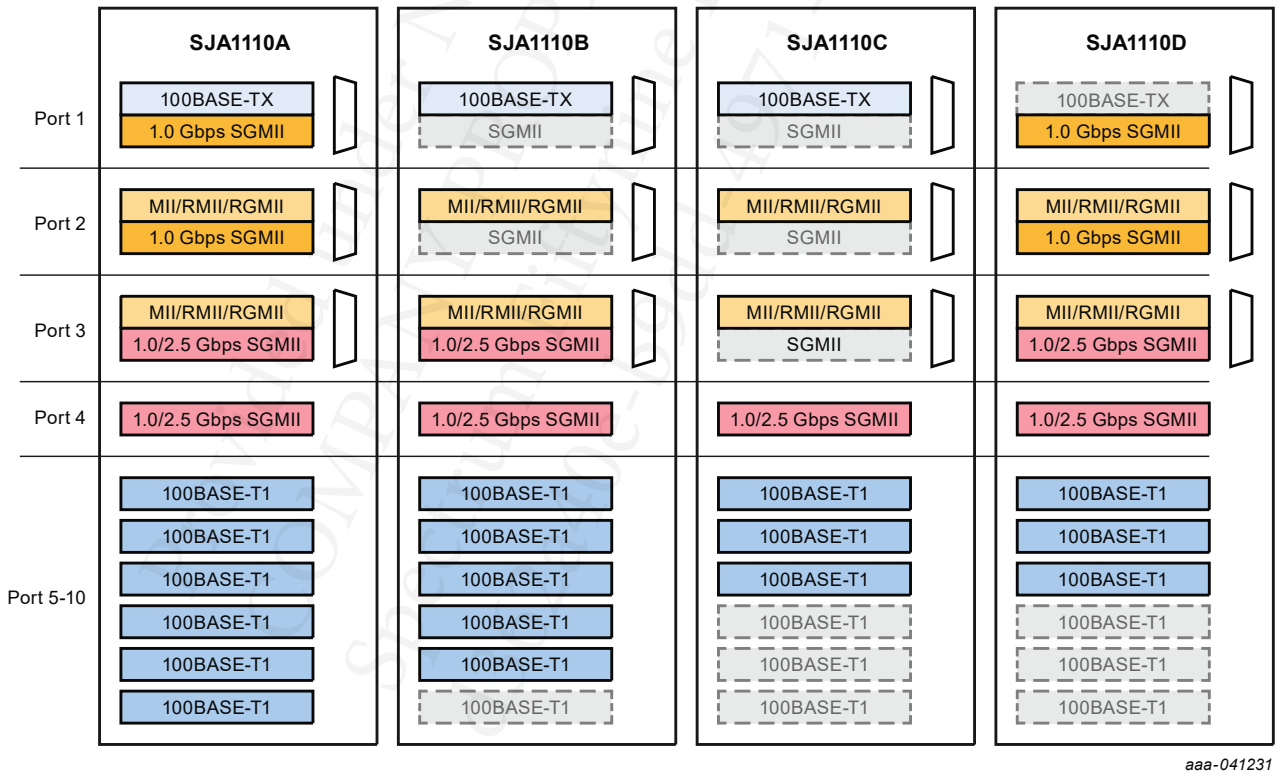


Figure 1. Overview of SJA1110 variants

4 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SJA1110AEL	LFBGA256	plastic low profile fine-pitch ball grid array package; 256 balls	SOT1020-3
SJA1110BEL			
SJA1110CEL			
SJA1110DEL			

5 Block diagram

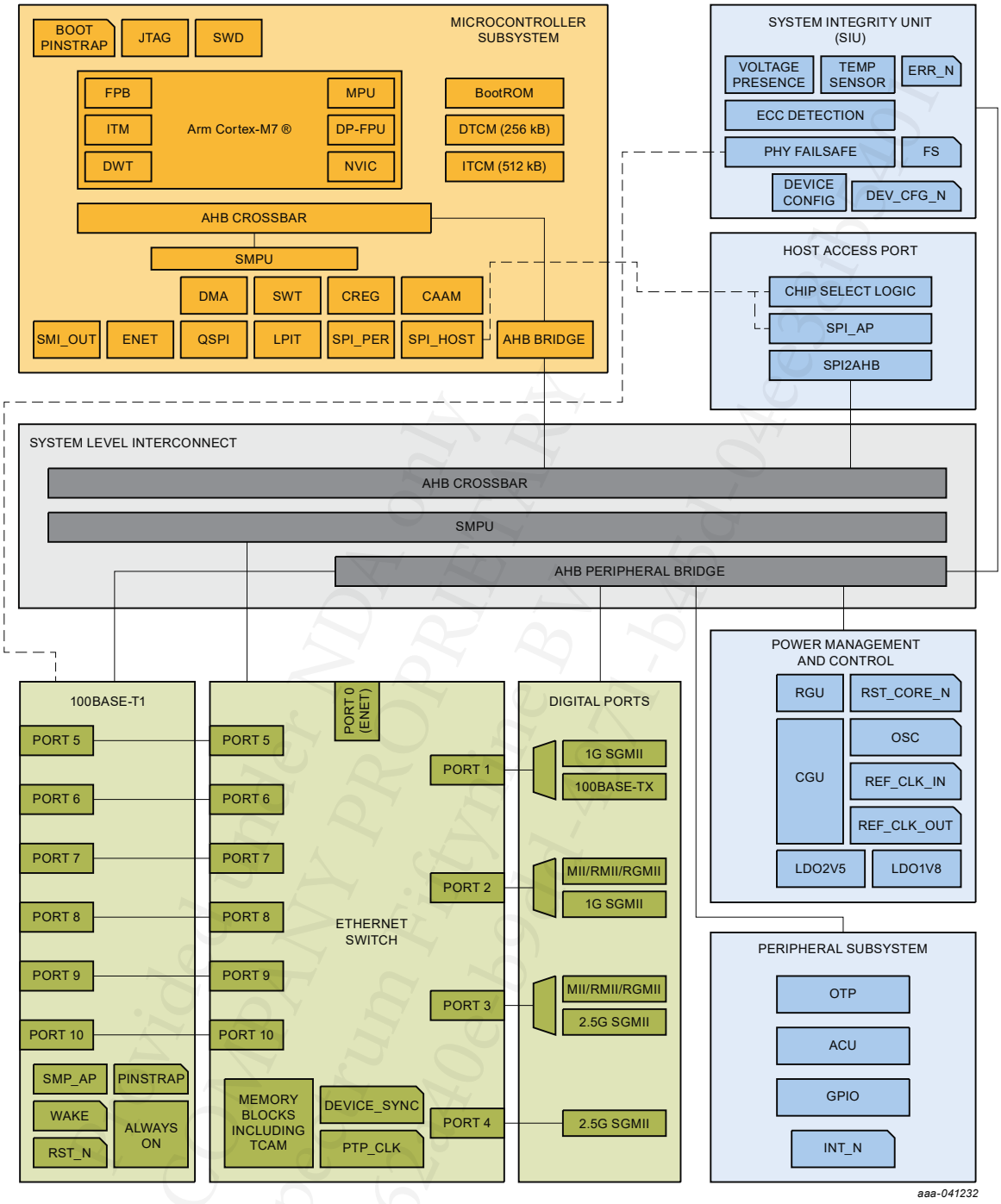


Figure 2. Block Diagram

6 Pinning information

6.1 Pinning

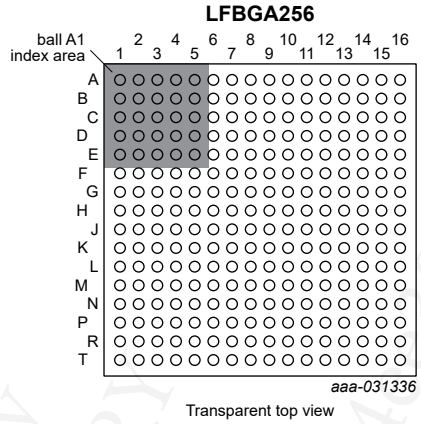


Figure 3. Pin configuration diagram

Table 3. Pin description

Pinning is for SJA1110A variant; some ports might be disabled depending on the variant.

	1	2	3	4	5	6	7	8
A	VSS	FSI1	MII2_RX_DV	MII2_RXD2	MII2_RXD0	MII2_TX_EN	MII2_TXD2	MII2_TXD0
B	ERR_N	FSI2	MII2_RXD3	MII2_RXD1	MII2_RX_CLK	MII2_TX_CLK	MII2_TXD3	MII2_TXD1
C	OSC_IN	VDDA11_OSC	VDDIO_FUSA	VSSIO_MII2	VDDIO_MII2	VSSIO_MII2	VDDIO_MII2	GPIO1
D	OSC_OUT	VSSA_OSC	VSS	SPI_HAP_ SDO	INT_N	MII2_RX_ER	MII2_TX_ER	GPIO2
E	VSSA_PLL	VDDA11_PLL	VDDIO_HOST	SPI_HAP_ SCLK	SPI_HAP_SDI	VDD11_CORE	GPIO0	GPIO3
F	VDDIO_SYNC	DEVICE_ SYNC	VSS	SPI_HAP_ SS0_N	SPI_HAP_ SS1_N	VDD11_CORE	VSS	VDDIO_GPIO1
G	VDDIO_ REFCLK_ OUT1	REFCLK_ OUT1	VSSIO_ REFCLK12	RST_CORE_N	DEVICE_ CFG_N	VSS	VSS	VSS
H	VDDIO_ REFCLK_ OUT2	REFCLK_ OUT2	VDDA18_ OTP_IN	VDDA18_ OTP_OUT	VDDA25_ VREG_OUT	VDDA33_ VREG_IN	VSS	VSS
J	VSS	VSS	VSS	GPIO8	GPIO10	VDDIO_GPIO3	VSS	VSS
K	SGMII4_TXP	SGMII4_TXN	VDDA33_ SGMII4	GPIO9	GPIO11	VDD11_CORE	VSS	VSS
L	SGMII4_RXP	SGMII4_RXN	VDDA11_ SGMII4	GPIO12	GPIO14	VDD11_CORE	VSS	VSS
M	VSS	VSS	VSS	GPIO13	GPIO15	VDDIO_GPIO4	VDDIO_HOST	VDD33_AO
N	SGMII2_TXP	SGMII2_TXN	VDDA11_ SGMII2	WAKE_IN_ OUT	LOC_WAKE_ IN	SMI_AP_MDC	BOOT_ OPTION0	PHY_ADDR3
P	SGMII2_RXP	SGMII2_RXN	VDDA33_ SGMII2	RST_N	INH	SMI_AP_ MDIO	BOOT_ OPTION1	VDDA25_RX_ 100BT1
R	VSS	VSS	VSSA25_ 100BT1_TXM5	VDDA25_ 100BT1_TXM5	VSSA25_ 100BT1_TXM6	VDDA25_ 100BT1_TXM6	VSSA25_ 100BT1_TXM7	VDDA25_ 100BT1_TXM7

Table 3. Pin description*...continued*

Pinning is for SJA1110A variant; some ports might be disabled depending on the variant.

	1	2	3	4	5	6	7	8
T	VSS	VSS	100BT1_TRX_P5	100BT1_TRX_M5	100BT1_TRX_P6	100BT1_TRX_M6	100BT1_TRX_P7	100BT1_TRX_M7

	9	10	11	12	13	14	15	16
A	MII3_RX_DV	MII3_RXD2	MII3_RXD0	MII3_TX_EN	MII3_TXD2	MII3_TXD0	VSS	VSS
B	MII3_RXD3	MII3_RXD1	MII3_RX_CLK	MII3_TX_CLK	MII3_TXD3	MII3_TXD1	PTP_CLK	VDDIO_PTP_CLK
C	GPIO4	VDDIO_MII3	VSSIO_MII3	VDDIO_MII3	VSSIO_MII3	VDDIO_SMI_OUT	SMI_OUT_MDC	SMI_OUT_MDIO
D	GPIO5	MII3_RX_ER	MII3_TX_ER	QSPI_SS_N	QSPI_IO2	VSS	REFCLK_OUT3	VDDIO_REFCLK_OUT3
E	GPIO6	GPIO7	VDD11_CORE	QSPI_IO0	QSPI_IO1	VSSIO_REFCLK34	REFCLK_OUT4	VDDIO_REFCLK_OUT4
F	VDDIO_GPIO2	VSS	VDD11_CORE	QSPI_SCLK	QSPI_IO3	VSSA11_100BTX	VSSA11_100BTX	VSSA11_100BTX
G	VSS	VSS	VDDIO_FLASH	SPI_PER_MOSI	SPI_PER_MISO	VDDA33_100BTX	100BTX_RX_P	100BTX_RX_M
H	VSS	VSS	VDDIO_SPI_PER	SPI_PER_SCLK	SPI_PER_SS0_N	VDDA11_100BTX	100BTX_TX_P	100BTX_TX_M
J	VSS	VSS	VDDIO_DEBUG	TCK	SPI_PER_SS1_N	VSSA11_100BTX	100BTX_EXTRES	VSSA11_100BTX
K	VSS	VSS	VDD11_CORE	TDI	TMS	VDDA33_SGMII3	SGMII3_RXN	SGMII3_RXP
L	VSSA11_100BT1	VSS	VDD11_CORE	TDO	TRST_N	VDDA11_SGMII3	SGMII3_TXN	SGMII3_TXP
M	VDDA11_100BT1	PHY_ADDR2	VDD11_CORE	PHY_M_S10	PHY_M_S9	VSS	VSS	VSS
N	PHY_ADDR0	PHY_ADDR1	PHY_M_S5	PHY_AUTO_MODE	PHY_M_S7	VDDA11_SGMII1	SGMII1_RXN	SGMII1_RXP
P	VSSA25_100BT1_RXM	PHY_ADDR4	PHY_M_S6	PHY_AUTO_POL_DET	PHY_M_S8	VDDA33_SGMII1	SGMII1_TXN	SGMII1_TXP
R	VSSA25_100BT1_TXM8	VDDA25_100BT1_TXM8	VSSA25_100BT1_TXM9	VDDA25_100BT1_TXM9	VSSA25_100BT1_TXM10	VDDA25_100BT1_TXM10	VSS	VSS
T	100BT1_TRX_P8	100BT1_TRX_M8	100BT1_TRX_P9	100BT1_TRX_M9	100BT1_TRX_P10	100BT1_TRX_M10	VSS	VSS

6.2 Pin description

6.2.1 Digital supply and ground

Table 4. Digital supply and ground

Symbol	Pin	Type [1]	Description
VDD11_CORE	E11, E6, F11, F6, K11, K6, L11, L6, M11	P	1.1 V digital core supply voltage
VSS	A1, A15, A16, D14, D3, F10, F3, F7, G10, G6, G7, G8, G9, H10, H7, H8, H9, J1, J10, J2, J3, J7, J8, J9, K10, K7, K8, K9, L10, L7, L8, M1, M14, M15, M16, M2, M3, R1, R15, R16, R2, T1, T15, T16, T2	P	digital supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.2 Power supply management

Table 5. Power supply management

Symbol	Pin	Type [1]	Description
INH	P5	O	inhibit output for voltage regulator control (active-HIGH, plain output (prog), low, VDD33_AO)
LOC_WAKE_IN	N5	I	local wake input (active-HIGH, plain output (prog), low, VDD33_AO)
VDD33_AO	M8	P	3.3 V always-on supply voltage
VDDA25_VREG_OUT	H5	AO	2.5 V analog regulator output voltage
VDDA33_VREG_IN	H6	P	3.3 V analog regulator supply voltage
WAKE_IN_OUT	N4	IO	wake in-out (open-drain) (active-HIGH, plain output (prog), low, VDD33_AO)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.3 Resets

Table 6. Resets

Symbol	Pin	Type [1]	Description
RST_CORE_N	G4	I	digital core reset (not including always-on domain) (active-LOW, pull-up (prog), low, VDDIO_HOST)
RST_N	P4	I	device reset (including always-on domain) (active-LOW, pull-up (prog), low, VDD33_AO)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.4 SGMII

6.2.4.1 SGMII Port 1

Table 7. SGMII Port 1

Symbol	Pin	Type [1]	Description
SGMII1_RXN	N15	AI	SGMII negative receiver terminal
SGMII1_RXP	N16	AI	SGMII positive receiver terminal
SGMII1_TXN	P15	AO	SGMII negative transmit terminal
SGMII1_TXP	P16	AO	SGMII positive transmit terminal
VDDA11_SGMII1	N14	P	1.1 V SGMII transceiver analog supply voltage
VDDA33_SGMII1	P14	P	3.3 V SGMII transceiver analog supply voltage

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.4.2 SGMII Port 2

Table 8. SGMII Port 2

Symbol	Pin	Type [1]	Description
SGMII2_RXN	P2	AI	SGMII negative receiver terminal
SGMII2_RXP	P1	AI	SGMII positive receiver terminal
SGMII2_TXN	N2	AO	SGMII negative transmit terminal
SGMII2_TXP	N1	AO	SGMII positive transmit terminal
VDDA11_SGMII2	N3	P	1.1 V SGMII transceiver analog supply voltage
VDDA33_SGMII2	P3	P	3.3 V SGMII transceiver analog supply voltage

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.4.3 SGMII Port 3

Table 9. SGMII Port 3

Symbol	Pin	Type [1]	Description
SGMII3_RXN	K15	AI	SGMII negative receiver terminal
SGMII3_RXP	K16	AI	SGMII positive receiver terminal
SGMII3_TXN	L15	AO	SGMII negative transmit terminal
SGMII3_TXP	L16	AO	SGMII positive transmit terminal
VDDA11_SGMII3	L14	P	1.1 V SGMII transceiver analog supply voltage
VDDA33_SGMII3	K14	P	3.3 V SGMII transceiver analog supply voltage

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.4.4 SGMII Port 4

Table 10. SGMII Port 4

Symbol	Pin	Type [1]	Description
SGMII4_RXN	L2	AI	SGMII negative receiver terminal

Table 10. SGMII Port 4*...continued*

Symbol	Pin	Type [1]	Description
SGMII4_RXP	L1	AI	SGMII positive receiver terminal
SGMII4_TXN	K2	AO	SGMII negative transmit terminal
SGMII4_TXP	K1	AO	SGMII positive transmit terminal
VDDA11_SGMII4	L3	P	1.1 V SGMII transceiver analog supply voltage
VDDA33_SGMII4	K3	P	3.3 V SGMII transceiver analog supply voltage

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.5 xMII

6.2.5.1 xMII Port 2

Table 11. xMII Port 2

Symbol	Pin	Type [1]	Description
MII2_RXD0	A5	I	MII/RMII/RGMII interface receive data input, bit 0 (active-HIGH, plain input (prog), high, VDDIO_MII2)
MII2_RXD1	B4	I	MII/RMII/RGMII interface receive data input, bit 1 (active-HIGH, plain input (prog), high, VDDIO_MII2)
MII2_RXD2	A4	I	MII/RGMII interface receive data input, bit 2 (active-HIGH, plain input (prog), high, VDDIO_MII2)
MII2_RXD3	B3	I	MII/RGMII interface receive data input, bit 3 (active-HIGH, plain input (prog), high, VDDIO_MII2)
MII2_RX_CLK	B5	IO	RX_CLK: MII interface receive clock (also configurable as output) REF_CLK: RMII interface reference clock (also configurable as input) RXC: RGMII interface receive clock (active-HIGH, plain input (prog), high (prog), VDDIO_MII2)
MII2_RX_DV	A3	I	RX_DV: MII interface receive data valid input CRS_DV: RMII interface carrier sense/data valid input RX_CTL: RGMII interface receive control input (active-HIGH, plain input (prog), high, VDDIO_MII2)
MII2_RX_ER	D6	I	MII/RMII interface receive error input (active-HIGH, plain input (prog), high, VDDIO_ MII2)
MII2_TXD0	A8	O	MII/RMII/RGMII interface transmit data output, bit 0 (active-HIGH, plain output (prog), fast (prog), VDDIO_MII2)
MII2_TXD1	B8	O	MII/RMII/RGMII interface transmit data output, bit 1 (active-HIGH, plain output (prog), fast (prog), VDDIO_MII2)
MII2_TXD2	A7	O	MII/RGMII interface transmit data output, bit 2 (active-HIGH, plain output (prog), fast (prog), VDDIO_MII2)
MII2_TXD3	B7	O	MII/RGMII interface transmit data output, bit 3 (active-HIGH, plain output (prog), fast (prog), VDDIO_MII2)
MII2_TX_CLK	B6	IO	TX_CLK: MII interface transmit clock (also configurable as output) REF_CLK: RMII interface reference clock (also configurable as input) TXC: RGMII interface transmit clock (active-HIGH, plain output (prog), fast (prog), VDDIO_MII2)

Table 11. xMII Port 2*...continued*

Symbol	Pin	Type [1]	Description
MII2_TX_EN	A6	O	TX_EN: MII/RMII interface transmit enable output TX_CTL: RGMII interface transmit control output (active-HIGH, plain output (prog), fast (prog), VDDIO_MII2)
MII2_TX_ER	D7	O	Port 2 MII/RMII interface transmit coding error output (active-HIGH, plain output (prog), fast (prog), VDDIO_MII2)
VDDIO_MII2	C5, C7	P	MII/RMII/RGMII I/O supply voltage port 2 (1.8 V, 2.5 V, 3.3 V)
VSSIO_MII2	C4, C6	P	MII2 supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.5.2 xMII Port 3

Table 12. xMII Port 3

Symbol	Pin	Type [1]	Description
MII3_RXD0	A11	I	MII/RMII/RGMII interface receive data input, bit 0 (active-HIGH, plain input (prog), high, VDDIO_MII3)
MII3_RXD1	B10	I	MII/RMII/RGMII interface receive data input, bit 1 (active-HIGH, plain input (prog), high, VDDIO_MII3)
MII3_RXD2	A10	I	MII/RGMII interface receive data input, bit 2 (active-HIGH, plain input (prog), high, VDDIO_MII3)
MII3_RXD3	B9	I	MII/RGMII interface receive data input, bit 3 (active-HIGH, plain input (prog), high, VDDIO_MII3)
MII3_RX_CLK	B11	IO	RX_CLK: MII interface receive clock (also configurable as output) REF_CLK: RMII interface reference clock (also configurable as input) RXC: RGMII interface receive clock (active-HIGH, plain input (prog), fast (prog), VDDIO_MII3)
MII3_RX_DV	A9	I	RX_DV: MII interface receive data valid input CRS_DV: RMII interface carrier sense/data valid input RX_CTL: RGMII interface receive control input (active-HIGH, plain input (prog), high, VDDIO_MII3)
MII3_RX_ER	D10	I	MII/RMII interface receive error input (active-HIGH, plain input (prog), high, VDDIO_MII3)
MII3_TXD0	A14	O	MII/RMII/RGMII interface transmit data output, bit 0 (active-HIGH, plain output (prog), fast (prog), VDDIO_MII3)
MII3_TXD1	B14	O	MII/RMII/RGMII interface transmit data output, bit 1 (active-HIGH, plain output (prog), fast (prog), VDDIO_MII3)
MII3_TXD2	A13	O	MII/RGMII interface transmit data output, bit 2 (active-HIGH, plain output (prog), fast (prog), VDDIO_MII3)
MII3_TXD3	B13	O	MII/RGMII interface transmit data output, bit 3 (active-HIGH, plain output (prog), fast (prog), VDDIO_MII3)
MII3_TX_CLK	B12	IO	TX_CLK: MII interface transmit clock (also configurable as output) REF_CLK: RMII interface reference clock (also configurable as input) TXC: RGMII interface transmit clock (active-HIGH, plain output (prog), fast (prog), VDDIO_MII3)

Table 12. xMII Port 3*...continued*

Symbol	Pin	Type [1]	Description
MII3_TX_EN	A12	O	TX_EN: MII/RMII interface transmit enable output TX_CTL: RGMII interface transmit control output (active-HIGH, plain output (prog), fast (prog), VDDIO_MII3)
MII3_TX_ER	D11	O	MII/RMII interface transmit coding error output (active-HIGH, plain output (prog), fast (prog), VDDIO_MII3)
VDDIO_MII3	C10, C12	P	MII/RMII/RGMII I/O supply voltage port 3 (1.8 V, 2.5 V, 3.3 V)
VSSIO_MII3	C11, C13	P	MII3 supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.6 100BASE-T1

6.2.6.1 100BASE-T1 common

Table 13. 100BASE-T1 common

Symbol	Pin	Type [1]	Description
VDDA11_100BT1	M9	P	1.1 V 100BASE-T1 analog supply voltage
VDDA25_RX_100BT1	P8	P	2.5 V receiver analog supply voltage; connect to VDDA25_VREG_OUT
VSSA11_100BT1	L9	P	digital 100BASE-T1 supply ground
VSSA25_100BT1_RXM	P9	P	analog 100BASE-T1 receiver supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.6.2 100BASE-T1 pinstrap options

Table 14. 100BASE-T1 pinstrap options

Symbol	Pin	Type [1]	Description
PHY_ADDR0	N9	I	PHY Address Bit 0 (active-HIGH, low, VDDIO_HOST)
PHY_ADDR1	N10	I	PHY Address Bit 1 (active-HIGH, low, VDDIO_HOST)
PHY_ADDR2	M10	I	PHY Address Bit 2 (active-HIGH, low, VDDIO_HOST)
PHY_ADDR3	N8	I	PHY Address Bit 3 (active-HIGH, low, VDDIO_HOST)
PHY_ADDR4	P10	I	PHY Address Bit 4 (active-HIGH, low, VDDIO_HOST)
PHY_AUTO_MODE	N12	I	PHY Autonomous mode selection (active-HIGH, low, VDDIO_HOST)
PHY_AUTO_POL_DET	P12	I	PHY automatic polarity detection and correction (active-HIGH, low, VDDIO_HOST)
PHY_M_S5	N11	I	PHY 5 Master/Slave setting (active-HIGH, low, VDDIO_HOST)
PHY_M_S6	P11	I	PHY 6 Master/Slave setting (active-HIGH, low, VDDIO_HOST)
PHY_M_S7	N13	I	PHY 7 Master/Slave setting (active-HIGH, low, VDDIO_HOST)
PHY_M_S8	P13	I	PHY 8 Master/Slave setting (active-HIGH, low, VDDIO_HOST)
PHY_M_S9	M13	I	PHY 9 Master/Slave setting (active-HIGH, low, VDDIO_HOST)
PHY_M_S10	M12	I	PHY 10 Master/Slave setting (active-HIGH, low, VDDIO_HOST)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.6.3 100BASE-T1 Port 5

Table 15. 100BASE-T1 Port 5

Symbol	Pin	Type [1]	Description
100BT1_TRX_M5	T4	AIO	negative MDI terminal
100BT1_TRX_P5	T3	AIO	positive MDI terminal
VDDA25_100BT1_TXM5	R4	P	2.5 V transmitter analog supply voltage; connect to VDDA25_VREG_OUT
VSSA25_100BT1_TXM5	R3	P	analog transmitter supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.6.4 100BASE-T1 Port 6

Table 16. 100BASE-T1 Port 6

Symbol	Pin	Type [1]	Description
100BT1_TRX_M6	T6	AIO	negative MDI terminal
100BT1_TRX_P6	T5	AIO	positive MDI terminal
VDDA25_100BT1_TXM6	R6	P	2.5 V transmitter analog supply voltage; connect to VDDA25_VREG_OUT
VSSA25_100BT1_TXM6	R5	P	analog transmitter supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.6.5 100BASE-T1 Port 7

Table 17. 100BASE-T1 Port 7

Symbol	Pin	Type [1]	Description
100BT1_TRX_M7	T8	AIO	negative MDI terminal
100BT1_TRX_P7	T7	AIO	positive MDI terminal
VDDA25_100BT1_TXM7	R8	P	2.5 V transmitter analog supply voltage; connect to VDDA25_VREG_OUT
VSSA25_100BT1_TXM7	R7	P	analog transmitter supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.6.6 100BASE-T1 Port 8

Table 18. 100BASE-T1 Port 8

Symbol	Pin	Type [1]	Description
100BT1_TRX_M8	T10	AIO	negative MDI terminal
100BT1_TRX_P8	T9	AIO	positive MDI terminal
VDDA25_100BT1_TXM8	R10	P	2.5 V transmitter analog supply voltage; connect to VDDA25_VREG_OUT
VSSA25_100BT1_TXM8	R9	P	analog transmitter supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.6.7 100BASE-T1 Port 9

Table 19. 100BASE-T1 Port 9

Symbol	Pin	Type [1]	Description
100BT1_TRX_M9	T12	AIO	negative MDI terminal
100BT1_TRX_P9	T11	AIO	positive MDI terminal
VDDA25_100BT1_TXM9	R12	P	2.5 V transmitter analog supply voltage; connect to VDDA25_VREG_OUT
VSSA25_100BT1_TXM9	R11	P	analog transmitter supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.6.8 100BASE-T1 Port 10

Table 20. 100BASE-T1 Port 10

Symbol	Pin	Type [1]	Description
100BT1_TRX_M10	T14	AIO	negative MDI terminal
100BT1_TRX_P10	T13	AIO	positive MDI terminal
VDDA25_100BT1_TXM10	R14	P	2.5 V transmitter analog supply voltage, connect to VDDA25_VREG_OUT
VSSA25_100BT1_TXM10	R13	P	analog transmitter supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.7 100BASE-TX

Table 21. 100BASE-TX

Symbol	Pin	Type [1]	Description
100BTX_EXTRES	J15	P	external calibration resistor (6.5k, 1%) to ground
100BTX_RX_M	G16	AIO	100BASE-TX negative receiver terminal
100BTX_RX_P	G15	AIO	100BASE-TX positive receiver terminal
100BTX_TX_M	H16	AIO	100BASE-TX negative transmit terminal
100BTX_TX_P	H15	AIO	100BASE-TX positive transmit terminal
VDDA11_100BTX	H14	P	1.1 V 100BASE-TX analog supply voltage
VDDA33_100BTX	G14	P	3.3 V 100BASE-TX analog transceiver supply voltage
VSSA11_100BTX	F14, F15, F16, J14, J16	P	100BASE-TX analog supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.8 Clock Interfaces

6.2.8.1 Analog clock interface

Table 22. Analog clock interface

Symbol	Pin	Type [1]	Description
OSC_IN	C1	AIO	crystal oscillator input
OSC_OUT	D1	AIO	crystal oscillator feedback

Table 22. Analog clock interface*...continued*

Symbol	Pin	Type [1]	Description
VDDA11_OSC	C2	P	1.1 V analog oscillator supply voltage
VDDA11_PLL	E2	P	1.1 V analog PLL supply voltage
VSSA_OSC	D2	P	analog oscillator ground
VSSA_PLL	E1	P	analog PLL ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.8.2 Digital clock interface 1

Table 23. Digital clock interface 1

Symbol	Pin	Type [1]	Description
REFCLK_OUT1	G2	O	digital 25 MHz reference clock 1 output (active-HIGH, plain output (prog), high (prog), VDDIO_REFCLK_OUT1)
VDDIO_REFCLK_OUT1	G1	P	reference clock 1 I/O supply voltage (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.8.3 Digital clock interface 2

Table 24. Digital clock interface 2

Symbol	Pin	Type [1]	Description
REFCLK_OUT2	H2	O	digital 25 MHz reference clock 2 output (active-HIGH, plain output (prog), high (prog), VDDIO_REFCLK_OUT2)
VDDIO_REFCLK_OUT2	H1	P	reference clock 2 I/O supply voltage (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.8.4 Digital clock interface 3

Table 25. Digital clock interface 3

Symbol	Pin	Type [1]	Description
REFCLK_OUT3	D15	O	digital 25 MHz REFCLK_OUT3 output (active-HIGH, plain output (prog), high (prog), VDDIO_REFCLK_OUT3)
VDDIO_REFCLK_OUT3	D16	P	reference clock 3 I/O voltage supply (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.8.5 Digital clock interface 4

Table 26. Digital clock interface 4

Symbol	Pin	Type [1]	Description
REFCLK_OUT4	E15	O	digital 25 MHz REFCLK_OUT4 output (active-HIGH, plain output (prog), high (prog), VDDIO_REFCLK_OUT4)
VDDIO_REFCLK_OUT4	E16	P	reference clock 4 I/O voltage supply (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.8.6 Digital clock interface common

Table 27. Digital clock interface common

Symbol	Pin	Type [1]	Description
VSSIO_REFCLK12	G3	P	reference clock 1 and 2 supply ground
VSSIO_REFCLK34	E14	P	reference clock 3 and 4 supply ground

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.9 Microcontroller

6.2.9.1 Boot pinstrap options

Table 28. Boot pinstrap options

Symbol	Pin	Type [1]	Description
BOOT_OPTION0	N7	I	pinstrap boot option selection, bit 0 (active-HIGH, low, VDDIO_HOST)
BOOT_OPTION1	P7	I	pinstrap boot option pin 1 (active-HIGH, low, VDDIO_HOST)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.9.2 Quad SPI Flash Interface

Table 29. Quad SPI Flash Interface

Symbol	Pin	Type [1]	Description
QSPI_IO0	E12	IO	QSPI IO pin 0 (active-HIGH, high (prog), VDDIO_FLASH)
QSPI_IO1	E13	IO	QSPI IO pin 1 (active-HIGH, high (prog), VDDIO_FLASH)
QSPI_IO2	D13	IO	QSPI IO pin 2 (active-HIGH, high (prog), VDDIO_FLASH)
QSPI_IO3	F13	IO	QSPI IO pin 3 (active-HIGH, high (prog), VDDIO_FLASH)
QSPI_SCLK	F12	O	QSPI SCLK (active-HIGH, high (prog), VDDIO_FLASH)
QSPI_SS_N	D12	O	QSPI chip select (active-LOW, high (prog), VDDIO_FLASH)
VDDIO_FLASH	G11	P	QSPI I/O voltage supply (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.9.3 SMI peripheral interface

Table 30. SMI peripheral interface

Symbol	Pin	Type [1]	Description
SMI_OUT_MDC	C15	O	SMI_OUT (Master SMI) MDC (active-HIGH, plain output (prog), high (prog), VDDIO_SMI_OUT)
SMI_OUT_MDIO	C16	I	SMI_OUT (Master SMI) MDIO (active-HIGH, plain output (prog), high (prog), VDDIO_SMI_OUT)
VDDIO_SMI_OUT	C14	P	SMI_OUT I/O voltage supply (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.9.4 SPI peripheral interface

Table 31. SPI peripheral interface

Symbol	Pin	Type [1]	Description
SPI_PER_MISO	G13	IO	SPI_PER MISO (active-HIGH, plain output (prog), high (prog), VDDIO_SPI_PER)
SPI_PER_MOSI	G12	IO	SPI_PER MOSI (active-HIGH, plain output (prog), high (prog), VDDIO_SPI_PER)
SPI_PER_SCLK	H12	IO	SPI_PER SCLK (active-HIGH, pull-up (prog), high (prog), VDDIO_SPI_PER)
SPI_PER_SS0_N	H13	IO	SPI_PER general purpose chip select 0 (active-LOW, pull-up (prog), high (prog), VDDIO_SPI_PER)
SPI_PER_SS1_N	J13	IO	SPI_PER general purpose chip select 1 (active-LOW, pull-up (prog), high (prog), VDDIO_SPI_PER)
VDDIO_SPI_PER	H11	P	SPI_PER I/O voltage supply (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.9.5 GPIO Interface 1

Table 32. GPIO Interface 1

Symbol	Pin	Type [1]	Description
GPIO0	E7	IO	GPIO pin 0 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO1)
GPIO1	C8	IO	GPIO pin 1 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO1)
GPIO2	D8	IO	GPIO pin 2 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO1)
GPIO3	E8	IO	GPIO pin 3 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO1)
VDDIO_GPIO1	F8	P	GPIO Group 1 I/O supply voltage (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.9.6 GPIO Interface 2

Table 33. GPIO Interface 2

Symbol	Pin	Type [1]	Description
GPIO4	C9	IO	GPIO pin 4 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO2)
GPIO5	D9	IO	GPIO pin 5 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO2)
GPIO6	E9	IO	GPIO pin 6 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO2)
GPIO7	E10	IO	GPIO pin 7 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO2)
VDDIO_GPIO2	F9	P	GPIO Group 2 I/O supply voltage (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.9.7 GPIO Interface 3

Table 34. GPIO Interface 3

Symbol	Pin	Type [1]	Description
GPIO8	J4	IO	GPIO pin 8 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO3)
GPIO9	K4	IO	GPIO pin 9 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO3)
GPIO10	J5	IO	GPIO pin 10 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO3)

Table 34. GPIO Interface 3*...continued*

Symbol	Pin	Type [1]	Description
GPIO11	K5	IO	GPIO pin 11 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO3)
VDDIO_GPIO3	J6	P	GPIO Group 3 I/O supply voltage (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.9.8 GPIO Interface 4

Table 35. GPIO Interface 4

Symbol	Pin	Type [1]	Description
GPIO12	L4	IO	GPIO pin 12 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO4)
GPIO13	M4	IO	GPIO pin 13 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO4)
GPIO14	L5	IO	GPIO pin 14 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO4)
GPIO15	M5	IO	GPIO pin 15 (active-HIGH, pull-up (prog), high (prog), VDDIO_GPIO4)
VDDIO_GPIO4	M6	P	GPIO Group 4 I/O supply voltage (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.10 Functional safety interface

Table 36. Functional safety interface

Symbol	Pin	Type [1]	Description
ERR_N	B1	O	fail-safe error output (active-LOW, low, VDDIO_FUSA)
FSI1	A2	I	fail-safe input 1 (active-HIGH, pull-down, low, VDDIO_FUSA)
FSI2	B2	I	fail-safe input 2 (active-HIGH, pull-down, low, VDDIO_FUSA)
VDDIO_FUSA	C3	P	FUSA I/O supply voltage (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.11 General

6.2.11.1 OTP

Table 37. OTP

Symbol	Pin	Type [1]	Description
VDDA18_OTP_IN	H3	P	1.8 V analog supply voltage. Connect to VDDA18_OTP_OUT and filter externally. Connect to ground, if in-field OTP programming not needed.
VDDA18_OTP_OUT	H4	AO	1.8 V analog OTP supply output

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.11.2 PTP interface

Table 38. PTP interface

Symbol	Pin	Type [1]	Description
PTP_CLK	B15	O	programmable PTP clock output (active-HIGH, plain output (prog), high (prog), VDDIO_PTP_CLK)

Table 38. PTP interface*...continued*

Symbol	Pin	Type [1]	Description
VDDIO_PTP_CLK	B16	P	PTP_CLK I/O supply voltage (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.11.3 Sync interface

Table 39. Sync interface

Symbol	Pin	Type [1]	Description
DEVICE_SYNC	F2	I	cascading time synchronization (active-HIGH, plain output (prog), high (prog), VDDIO_SYNC)
VDDIO_SYNC	F1	P	sync I/O supply voltage (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.12 External host

6.2.12.1 SMI access point

Table 40. SMI access point

Symbol	Pin	Type [1]	Description
SMI_AP_MDC	N6	I	MDC of the SMI_AP slave interface (active-HIGH, plain input, low, VDDIO_HOST)
SMI_AP_MDIO	P6	IO	MDIO of the SMI_AP slave interface (active-HIGH, plain input/output, high (prog), VDDIO_HOST)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.12.2 Host access point

Table 41. Host access point

Symbol	Pin	Type [1]	Description
DEVICE_CFG_N	G5	O	device completed configuration (active-LOW, plain output (prog), high (prog), VDDIO_HOST)
INT_N	D5	O	interrupt output open-drain (active-LOW, plain output (prog), high (prog), VDDIO_HOST)
SPI_HAP_SCLK	E4	I	serial clock (active-HIGH, pull-up (prog), low, VDDIO_HOST)
SPI_HAP_SDI	E5	I	serial data in (active-HIGH, pull-up (prog), low, VDDIO_HOST)
SPI_HAP_SDO	D4	T	serial data out (plain output (prog), high (prog), VDDIO_HOST)
SPI_HAP_SS0_N	F4	I	chip select to select SPI_AP (active-LOW, pull-up (prog), low, VDDIO_HOST)
SPI_HAP_SS1_N	F5	I	chip select to select SPI_HOST (active-LOW, pull-up (prog), low, VDDIO_HOST)
VDDIO_HOST	E3, M7	P	host supply voltage (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.13 Test and debug interface

Table 42. Test and debug interface

Symbol	Pin	Type [1]	Description
TCK	J12	I	JTAG TCK/Serial Wire Debug SWCLK (active-HIGH, pull-up, low, VDDIO_DEBUG)
TDI	K12	I	JTAG TDI (active-HIGH, pull-up, low, VDDIO_DEBUG)
TDO	L12	O	JTAG TDO/Single Wire Debug SWO (active-HIGH, plain output (prog), high (prog), VDDIO_DEBUG)
TMS	K13	I	JTAG TMS/Single Wire Debug SWDIO (active-HIGH, pull-up, high (prog), VDDIO_ DEBUG)
TRST_N	L13	I	JTAG TRST_N (active-LOW, pull-up, low, VDDIO_DEBUG)
VDDIO_DEBUG	J11	P	DEBUG I/O supply voltage (1.8 V, 2.5 V, 3.3 V)

[1] IO: digital input/output; I: digital input; O: digital output; AIO: analog input/output; AI: analog input; AO: analog output; P: power; G: ground.

6.2.14 Pinning Legend

Table 43. Digital pin legend

Qualifier	Description
plain output (prog)	default at plain output, pull-up/down configurable
plain input (prog)	default at plain input, pull-up/down configurable
pull-up	fixed at weak pull-up
pull-down	fixed at weak pull-down
pull-up (prog)	default weak pull-up, configurable
pull-down (prog)	default at weak pull-down, configurable

Table 44. Digital pin output speed

Qualifier	Description
low	fixed at very low noise/low speed
medium	fixed at low noise/medium speed
fast	fixed at medium noise/fast speed
high	fixed at high noise/igh speed
low (prog)	programmable with default at very low noise/low speed
medium (prog)	programmable with default at low noise/medium speed
fast (prog)	programmable with default at medium noise/fast speed
high (prog)	programmable with default at high noise/high speed

7 Functional description

7.1 100BASE-T1

The subsystem contains up to six IEEE 802.3bw compliant 100BASE-T1 PHYs. Each PHY module provides the functions needed to meet IEEE Std 802.3bw.

PHY configuration is managed via IEEE Std 802.3 Clause 45 register access.The registers can be accessed by the internal embedded processor via the internal APB or by an external processor via either the SPI_AP or a dedicated SMI_AP interface. The SMI interface supports Clause 45 transactions, as well as Clause 22 transactions. However, it does not support access to Clause 22 registers, except for accessing the Clause 45 register space using indirect addressing.

The 100BASE-T1 subsystem controller also includes an initialization controller that fetches configuration data from both pin-strapped IOs and one-time programmable (OTP) memory and applies it to the PHYs. This only occurs during the power-up boot process.

This subsystem handles support for OPEN Alliance TC-10 Wake/Sleep logic with the option to indicate via INH whether the device needs a power supply, or whether power supplies (except the always-on supply) can be switched off.

7.2 100BASE-TX

The 100BASE-TX is an Ethernet PHY transceiver compliant to IEEE 802.3 standard. The typical use case of this interface in automotive applications is to connect to an external diagnostic port with 100 Mb/s fast Ethernet connection.

7.3 Quad Serial Peripheral Interface (QuadSPI)

QuadSPI is a 6-signal interface used to connect a single serial NOR-flash or EEPROM to the SJA1110. QuadSPI supports SDR serial NOR-flash devices to a maximum size of 1 Gbit (128 Mbyte). This enables the user to select from a wide range of flash types and vendors. QuadSPI supports the following features:

- Support for a serial clock frequency of 5 MHz (default), 10 MHz, 25 MHz or 50 MHz
- Execute in Place (XiP) not supported
- On-the-fly decryption not supported
- Single Data Rate (SDR) mode of operation (DDR mode not supported)
- Internally generated sampling (Data Strobe Sampling (DQS) supported)
- SDR half-speed access mode not supported

Note: *An external pull-up is required on $\overline{CS}$.*

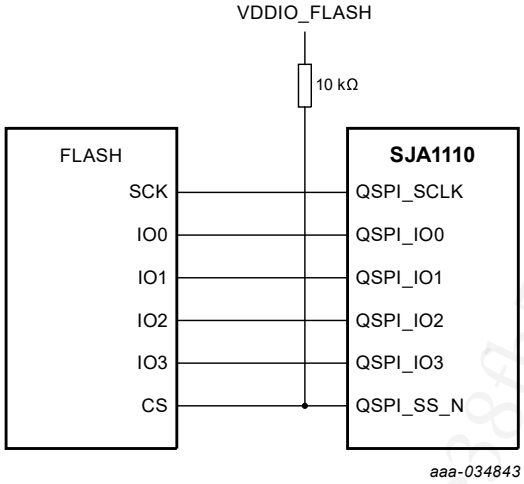


Figure 4. QuadSPI application

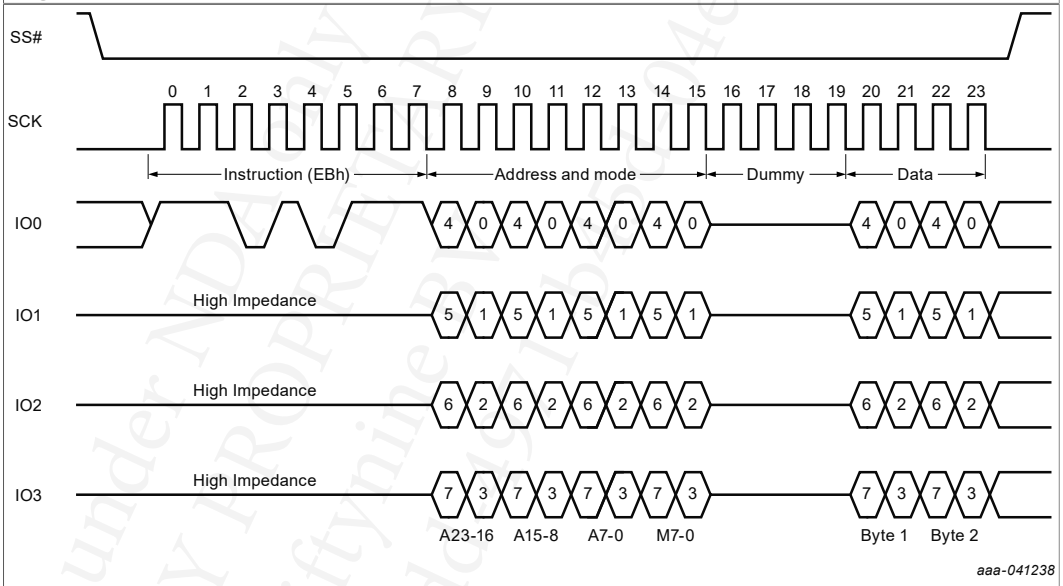


Figure 5. QuadSPI timing diagram

Table 45. External (QSPI) Flash and EEPROM chip requirements

	QuadSPI flash	SPI flash	EEPROM
Speed (MHz)[1]	≥ 25	≥ 25	≥ 5
Addressing	3-byte	3-byte	3-byte
Supply	1.8 V, 2.5 V or 3.3 V	1.8 V ,2.5 V or 3.3 V	1.8 V, 2.5 V or 3.3 V
SFDP support[2]	read in 4-4-4 or 1-1-1 mode	—	—
SFDP revisions	1.0, 1.5 or 1.6	—	—

[1] The bootstrap pins determine the type of NVM connected at startup. The default operating speed of the interface is 25 MHz for a flash (QuadSPI or SPI flash) and 5 MHz for an EEPROM. The NVM needs to support the minimum operating speed. If desired, the speed can be lowered or increased after booting up.

[2] opcode – address – data

7.4 Host Access Point (SPI_HAP)

The SPI_HAP can be used to interface with and control the SJA1110 over the SPI at a maximum frequency of 25 MHz. This interface multiplexes the SPI Access Point (SPI_AP) and the SPI Host Access (SPI_HOST) with shared SDI, SDO and SCK signal lines but dedicated chip select lines.

SPI_AP is an SPI slave device used to control internal device registers such as switch core, SGMII, internal PHYs and other peripherals. Internally, the AP acts as an AHB master.

SPI_HOST is an SPI slave interface that enables communication between an external host and the internal host. It can be used to allow an external host to selectively access internal blocks. It can also be used by the external host to download firmware for execution by the internal host. In this configuration, a dedicated external NVM may be optional.

SPI_HAP provides access to either SPI_AP or SPI_HOST, depending on the levels on pins SPI_HAP_SSx_N (see Table 41).

Pin SPI_HAP_SS1_N maps to SPI_HOST and pin SPI_HAP_SS0_N to SPI_AP.

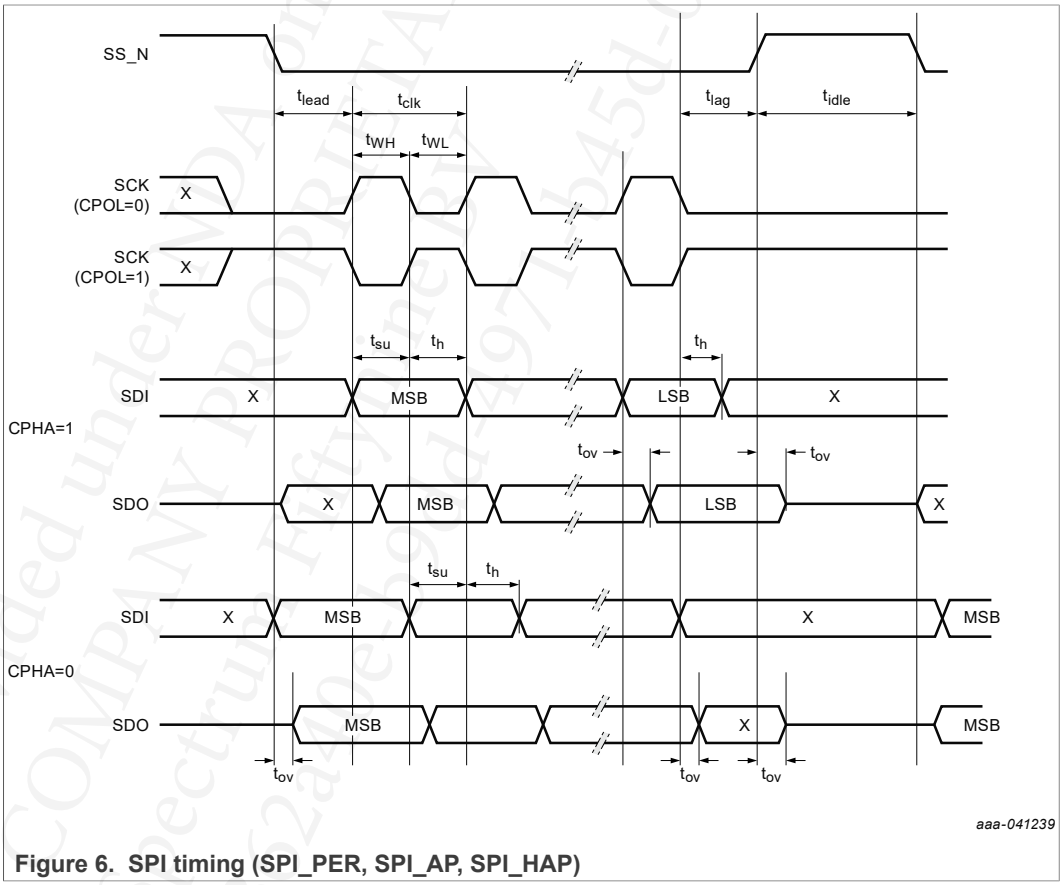


Figure 6. SPI timing (SPI_PER, SPI_AP, SPI_HAP)

7.5 SPI_PER

The SPI_PER interface is connected to the internal low-power SPI (LPSPI) core, which can operate in master or slave configuration. The interface can operate at up to 50 MHz in master mode and up to 25 MHz in slave mode.

Two active-LOW chip select pins are provided for controlling peripheral devices (SPI_PER configured as master). The chip select pins are inputs in slave mode.

Note: *External pull-ups to the chip select pins are advised to prevent unintended activation.*

This block is designed to reduce CPU overhead with DMA offloading of FIFO register access.

Peripheral devices connected can communicate in full duplex mode with the SJA1110. This allows for connections to external managed switches such as the SJA1105x and a cascaded SJA1110 operating in managed mode.

7.6 SMI_AP

A dedicated SMI slave interface is provided for accessing the 100BASE-T1 subsystem.

Note: *The 100BASE-TX and SGMII registers are not accessible via the SMI_AP interface*

The SJA1110 supports IEEE limited Clause 22 as well as IEEE Clause 45.

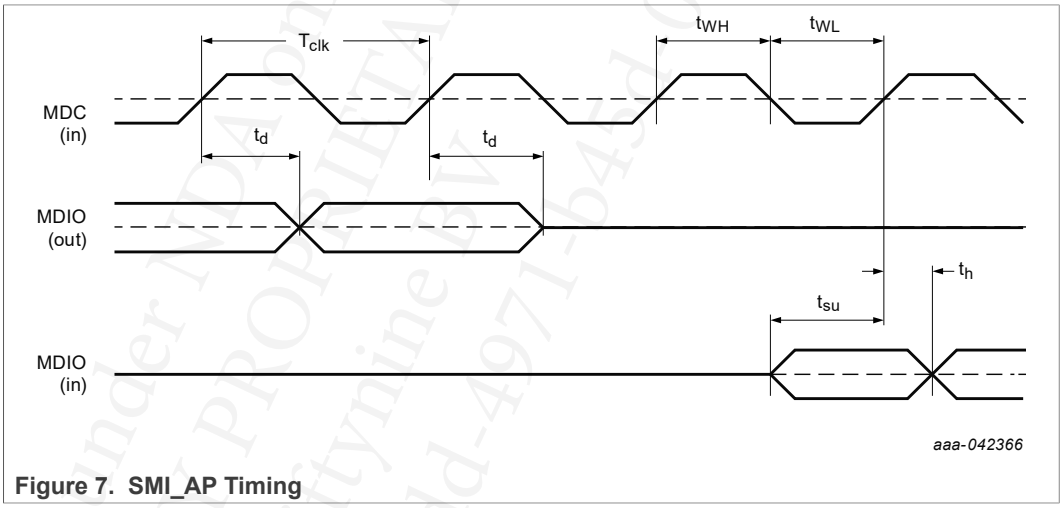


Figure 7. SMI_AP Timing

7.7 SMI_OUT

The SMI_OUT interface is an SMI master interface used to configure external PHYs from the internal Arm core.

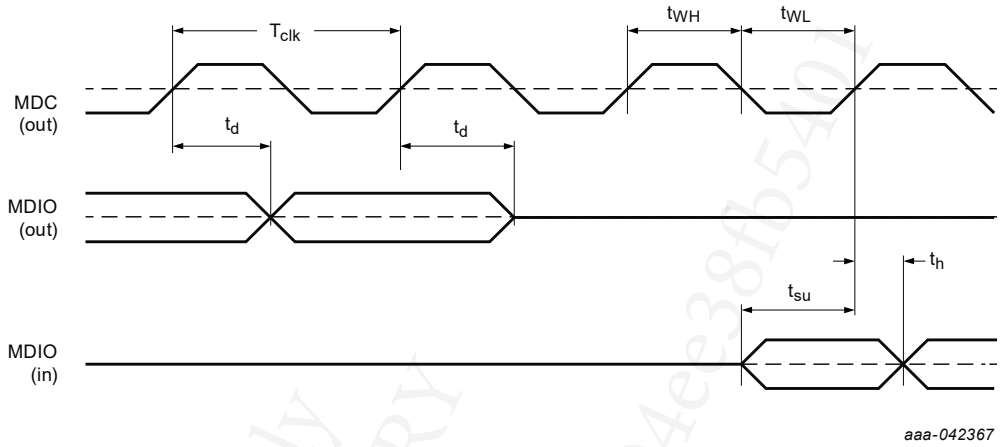


Figure 8. SMI_OUT Timing

7.8 xMII Interfaces

The device has 4 ports which support the following xMII variants for PHY/MAC connectivity:

- MII
- RMII
- RGMII
- SGMII 1.0 Gbit/s
- SGMII 2.5 Gbit/s

The CMOS level interfaces MII/RMII/RGMII support IO voltages of 1.8 V, 2.5 V or 3.3 V, provided by the respective VDDIO supply.

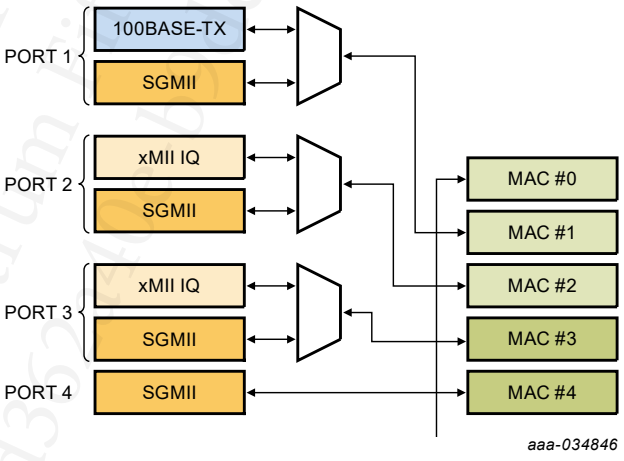


Figure 9. xMII

7.8.1 MII

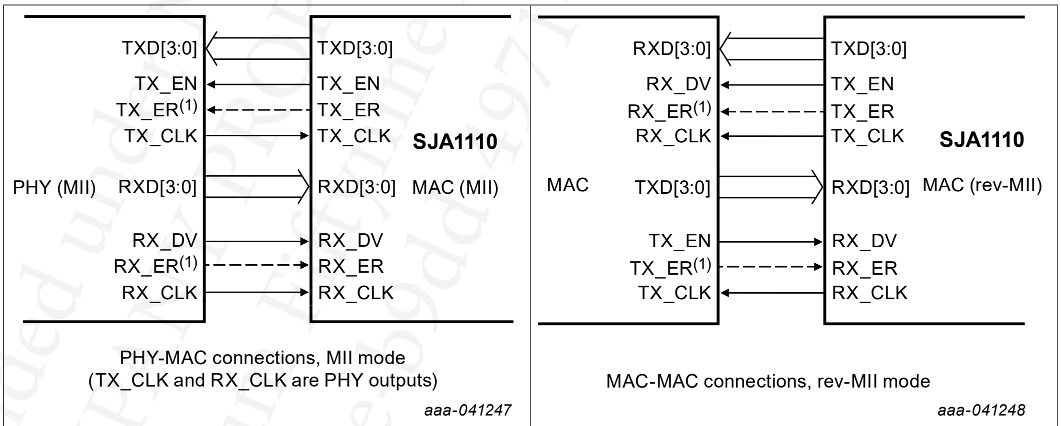
MII connectivity is depicted in Figure 10. Data is exchanged via 4-bit wide data nibbles on TXD[3:0] and RXD[3:0]. Transmit and receive data is synchronized, respectively, with the transmit (TX_CLK) and receive (RX_CLK) clocks. In MII operation, the clock signals are provided by the PHY and are typically derived from an external clock or crystal (MASTER) or recovered from the MDI (SLAVE). Both clocks have a nominal frequency of 25 MHz (± 100 ppm) for 100 Mbit/s operation or 2.5 MHz for 10 Mbit/s operation. Normal data transmission from MAC to PHY is initiated by asserting TX_EN, while data reception from PHY to MAC is indicated by asserting RX_DV.

In addition to MII mode, the device supports Reverse MII mode (rev-MII). In rev-MII mode, the MAC's MII interface acts like a PHY. In this mode TX_CLK and RX_CLK are inputs to the PHY, while the roles of TX_EN, TX_ER, TXD, RX_DV, RXD an RX_ER are unchanged.

Table 46. MII modes

MII mode	Description
MII	In this mode, the device behaves as a MAC per the IEEE 802.3 MII spec and TX_ CLK and RX_CLK are inputs
rev-MII[1]	In this mode, the device behaves like a PHY interface as described in IEEE 802.3 MII. TX_CLK and RX_CLK are outputs. As in MII mode, RXD, RX_DV and RX_ER are inputs and TXD, TX_EN and TX_ER are outputs to the SJA1110.

[1] Also referred to as MII-PHY mode



(1) external or internal pull-down may be needed.

Figure 10. MII interface connections

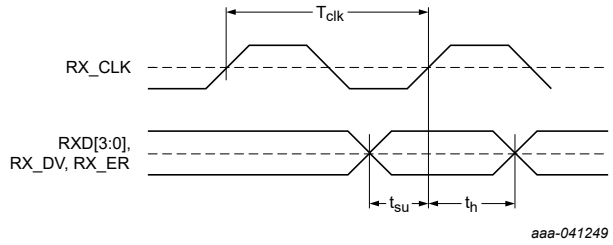


Figure 11. MII receive timing

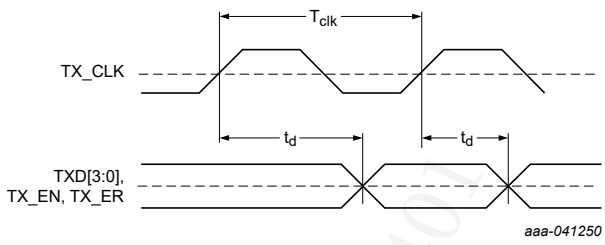


Figure 12. MII transmit timing

7.8.2 RMII

RMII connectivity is depicted in Figure 13. RMII data is exchanged via 2-bit wide dibits on TXD[1:0] and RXD[1:0]. To achieve 100 Mbit/s, the data is clocked at 50 MHz. In 10 Mbit/s mode of operation, REF_CLK is clocked at 5 MHz.

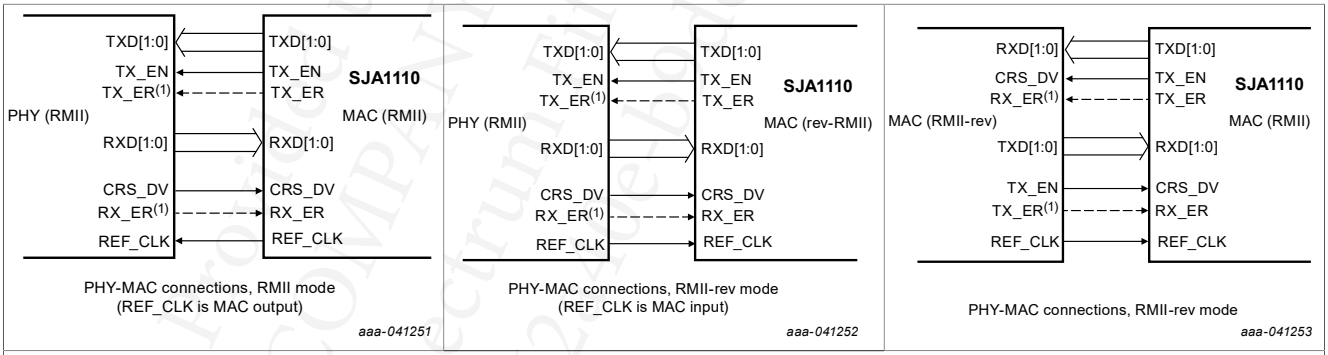
Data and control signals are synchronized with a single clock signal, REF_CLK. This 50 MHz (± 50 ppm) clock is typically generated by the MAC and input to the PHY (RMII mode). Alternatively the MAC can sink a 50 MHz REF_CLK (RMII-rev mode). This mode can be used in MAC back-to-back configurations.

RMII REF_CLK functonallity is available on pins MIIx_RX_CLK or MIIx_TX_CLK and can be software selected for flexibility.

The SJA1110 supports the following RMII modes:

Table 47. RMII modes

RMII mode	Description
RMII	In RMII mode, the REF_CLK is configured as an output and outputs a 50 MHz clock.
RMII-rev	In RMII mode the REF_CLK is configured as an input and expects a 50 MHz clock.



(1) external or internal pull-down may be needed; REF_CLK can be also input to both MAC and PHY.

Figure 13. RMII interface connections

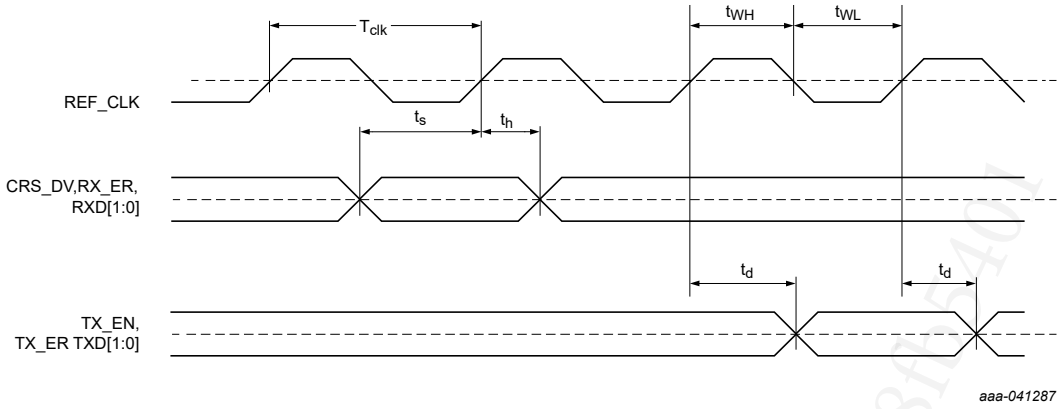


Figure 14. RMII timing diagram

7.8.3 RGMII

RGMII connectivity is depicted in Figure 15. Control signals are multiplexed together and transmitted data is synchronized with both clock edges (double data rate). The interface is intended for 1000 Mbit/s operation, but can also be used for 100 Mbit/s and 10 Mbit/s operation.

RGMII is a symmetrical interface and TXC is always generated by the MAC and RXC by the PHY. For 100 Mbit/s operation, the clock operates at 25 MHz (+/- 50 ppm) and data is duplicated on the falling edge of the appropriate clock.

RX_CTL and TX_CTL encode the RX_DV/RX_ER and TX_EN/TX_ER signals, respectively. To reduce power consumption in the interface, TXERR and RXERR are encoded in a manner that minimized transitions during nominal data transmission (see Figure 16 and Figure 17)..

TXERR <= TX_ER xor TX_EN

RXERR <= RX_ER xor RX_DV

The device is compliant with ISO21111-2:2020. This extends support for 1.8 V and 3.3 V operation of the CMOS interface in addition to the 2.5 V operation specified in RGMII v1.3. The internal delay setting on TXC and RXC (RGMII-ID) as per RGMII v2.0 is also incorporated into the specification. These delays can be independently configured for both TXC or RXC at source (Delay on Source) and at destination (Delay on Destination).

Note: *The maximum interconnect delay is limited to 1 ns, so the maximum supported trace length is approximately 15 cm in FR4.*

Table 48. RGMII modes

RMII mode[1]	Description
RGMII	RXC/TXC delays not enabled
RGMII-ID	TXC delay enabled
RGMII-ID (hybrid TX/RX)	RXC and TXC delays enabled
RGMII-ID (hybrid RX)	RXC delay enabled

[1] All possible TX/RX combinations for internal delay can be selected via software.

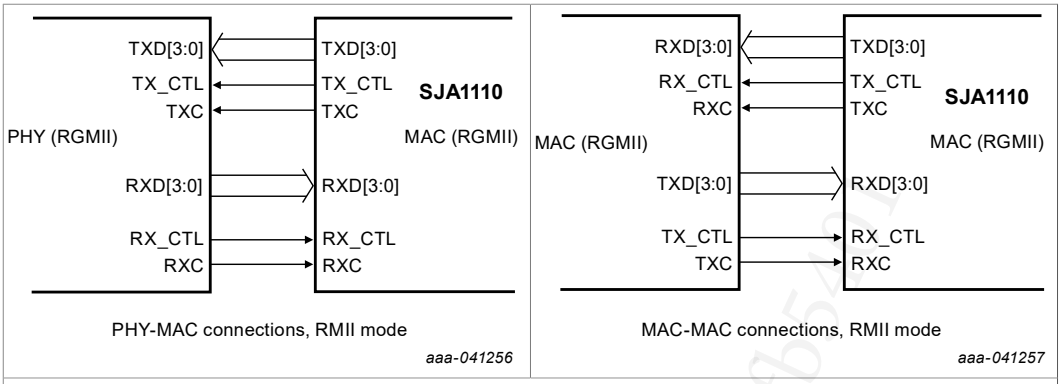


Figure 15. RGMII interface connections

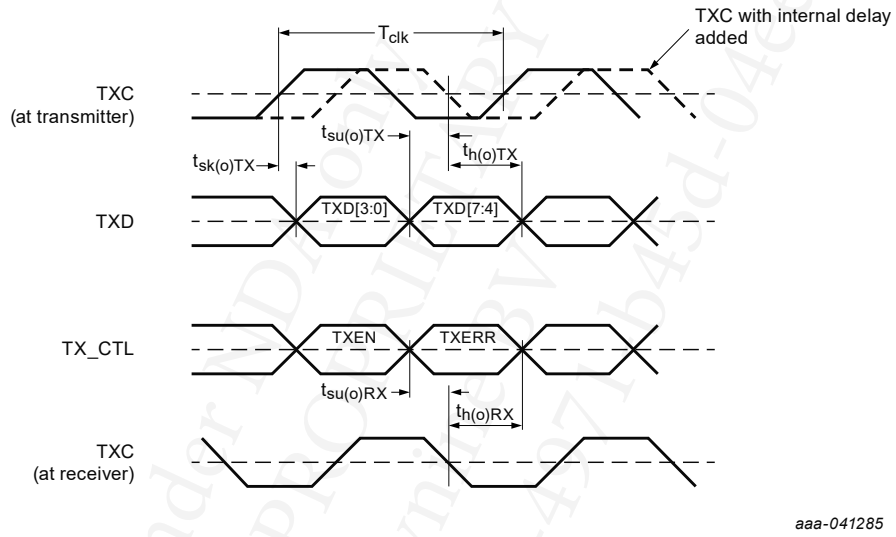


Figure 16. RGMII transmit timing diagram

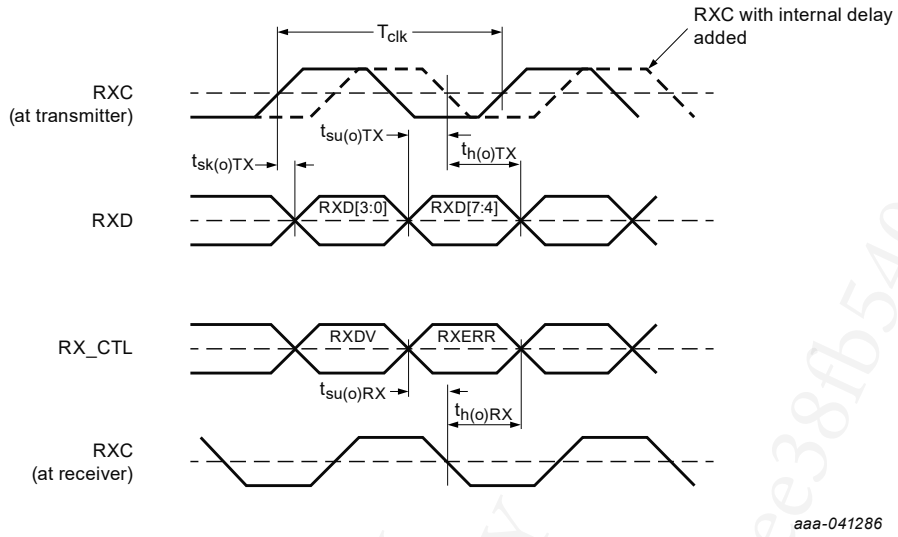


Figure 17. RGMII receive timing diagram

7.8.4 SGMII

The device supports a 4 wire Serial-GMII (SGMII) SerDes interface as depicted in Figure 18[6]. The SGMII protocol is intended as an alternative to the RGMII standard. It uses fewer interface signals and provides better EMC performance by using differential signaling.

The SGMII's transfer rate for 1 Gbit/s, 100 Mbit/s and 10 Mbit/s is fixed at 1.25 Gbaud. For 100 Mbit/s (and 10 Mbit/s) operation the interface 'elongates' the frame by replicating each octet 10 times (100 for 10 Mbit/s). For 2.5 Gbit/s operation, the interface transfer rate is increased to 3.125 Gbaud.

SGMII must always be AC coupled with a 100 nF capacitor. The SJA1110 is AC-compliant to the SGMII 1.8 specification. The SGMII interface implements (optional) Auto-Negotation. In this mode, PHY and MAC handshake the supported interface capabilities to find the optimal operating conditions.

Note: *When the interface operates in 2.5 Gbit/s overclocked mode, 1 Gbit/s, 100 Mbit/s and 10 Mb/s are not supported. Also, the autonegotiation feature is not available.*

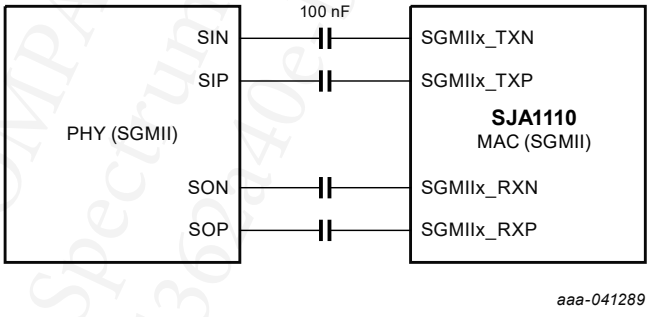


Figure 18. SGMII signaling

A block diagram of the SGMII subsystem is shown in Figure 19.

6 The SGMII 8-wire interface is not supported. The 4-wire interface implements clock and data recovery.

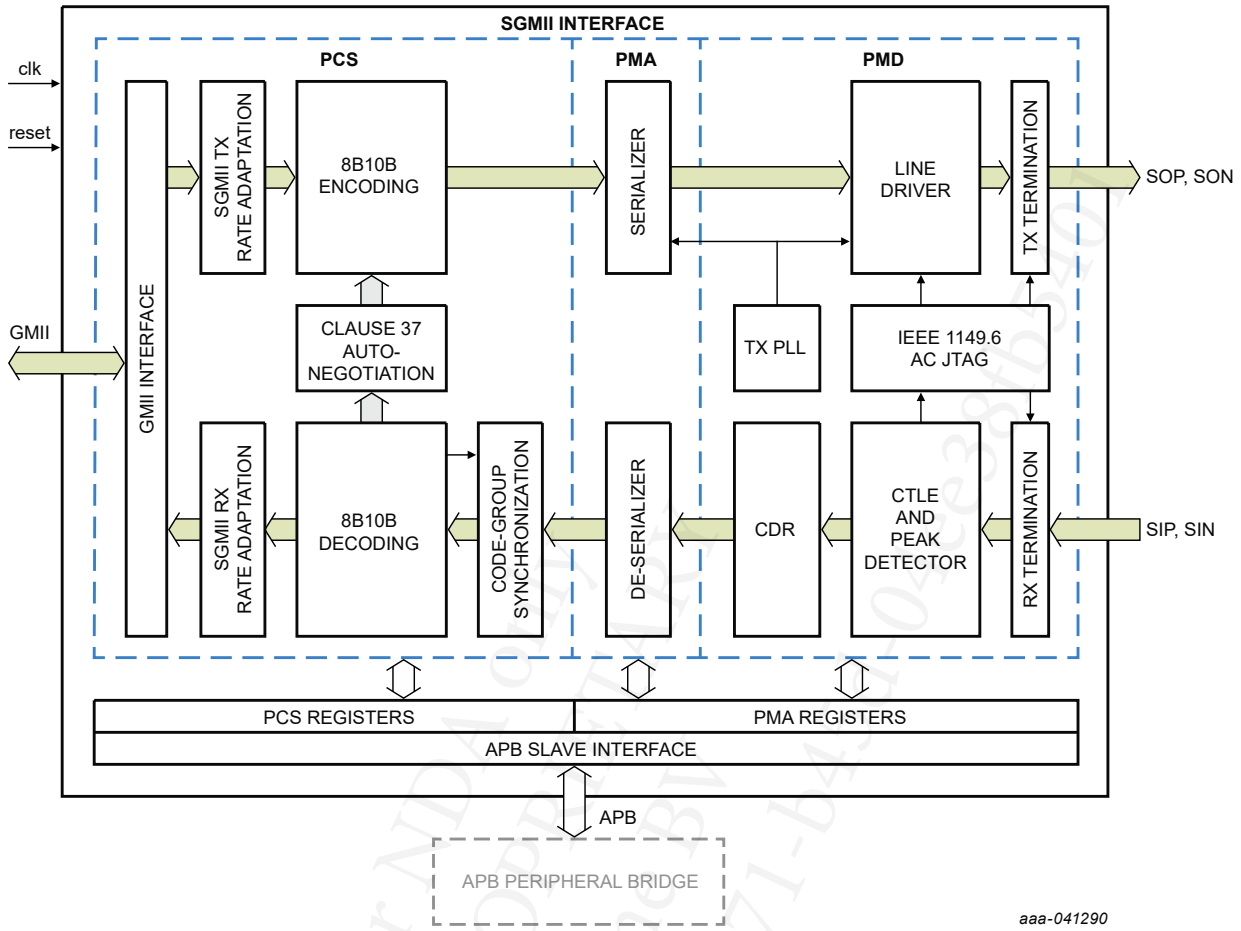


Figure 19. SGMII block diagram

7.9 Resets

The device has two reset inputs, RST_N and RST_CORE_N.

RST_N is the functional reset for the entire device. When this pin is asserted (active-LOW), the entire device is reset including all sleep preserving functions.

RST_CORE_N is the chip-level functional reset. In context of a wakeup-triggered, power-supply ramp-up, the RST_CORE_N pin is used to reset all blocks on the device, excluding the always-on functions.In case RST_CORE_N is asserted at a other moment then the device hardware wake-up, it will reset the entire drive including the sleep-preserving functions, identical to RST_N.

Note: *Only assert RST_CORE_N during a board wake-up event. Make sure RST_N pin is* ***not*** *asserted during board wake-up events. Otherwise, all wake-up relevant registers will be cleared.*

Please consult application note AN13225 *'SJA1110 hardware application notes*'.

7.10 Clocks

In crystal oscillator mode, the OSC_IN and OSC_OUT pins are connected to an external 25 MHz crystal.

In oscillator slave mode, an external clock is connected to input terminal OSC_IN with OSC_OUT left open.

Note: *The clock signal must be AC coupled. The input peak-to-peak voltage must be limited to VDDA11_OSC.*

The device outputs 25 MHz digital clock signals on REFCLK_OUT1 to REFCLK_OUT4. These signals can be used to provide a clock signal to an external Ethernet PHY, another switch or a clock buffer for further distribution.

The digital clock signals can be disabled in software if not needed.

7.11 Pin strapping

The 100BASE-T1 PHYs and the integrated processor can be configured via pin strapping. The following table provides an overview of the available settings.

Table 49. SJA1110 Pin strapping

Pins	Function	Description
PHY_ADDR[4:0]	PHY address of the 100BASE-T1 PHYs	This setting controls the base PHY address of all 100BASE-T1 PHYs. pull-up: 1; pull-down: 0 Setting PHY_ADDR = 19h (10011b) assigns this address to port 5, 1Ah to port 6, 1Bh to port 7 and so on.
PHY_AUTO_POL_DET	Automatic polarity detection on 100BASE-T1 PHYs	0: if polarity is wrong, link training is blocked 1: fully automated polarity detection and correction
PHY_AUTO_MODE	Autonomous mode select	0: managed mode select 1: autonomous mode select: PHY starts link training automatically
PHY_M_Sx	MASTER / SLAVE select at port x	0: SLAVE 1: MASTER
BOOT_OPTION[0:1]	Boot option selection	00: Boot from QSPI_FLASH 01: Boot from SPI_FLASH 10: Boot from SPI EEPROM 11: Serial boot (SPI)

7.12 Miscellaneous

7.12.1 Wake-up/Sleep related signals

The WAKE_IN_OUT pin is an open-drain active-HIGH pin. It is used to forward wake-up events to other devices that support this interface. In addition, other devices can assert this pin in order to forward a wake-up request to this device.

The LOC_WAKE_IN pin is a general purpose local wake input. It can be connected to the wake-up terminal in the wiring harness in order to wake up the ECU. This pin is also used to output the recovered clock in 100BASE-T1 compliance tests.

The INH pin is used to control an external voltage regulator or PMIC. INH is a high-side switch that is pulled to VDDA_AO in situations where the device requests power. If the device enters sleep mode (TC10 sleep), INH is set to tri-state.

7.12.2 PTP related signals

The recovered PTP clock, which is derived from the internal 125 MHz clock and the local time sychronization settings (rate-correction, offset), can be output on pin PTP_CLK. A toggeling signal is output on PTP_CLK when it is configured as PTP clock master.

DEVICE_SYNC pin is used to synchronize the local clocks on the device in cascaded switch setups. When the DEVICE SYNC master switch toggles this signal, all connected devices including the master take a snapshot of the current time. Pin functionality is configured in software.

7.12.3 Device config done, IRQ and JTAG

The active-LOW DEVICE_CFG_N pin signals when device (switch subsysterm) configuration has been completed (static configuration is loaded).

INT_N is an open drain IRQ output. If required, the pin can be shared by multiple devices. It is recommended to connect an external pull-up.

The JTAG interface provides a boundary scan interface for production testing. In debugging mode, it can be used for flash download or for a connecting a debugger.

8 Thermal characteristics

Table 50. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board[1].

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		20	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	[2]	11	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		1	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm)

[2] Case temperature refers to the center of the heat sink at the bottom of the package.

9 Limiting values

Table 51. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_x	Voltage on pin x	on pins VDD_CORE	-0.3	-	1.6	V
		on pins VDD_SGMIIx	-0.3	-	1.6	V
		on pins VDDA33_SGMIIx	-0.3	-	4	V
		on pins VDDA11_SGMIIx	-0.3	-	1.6	V
		on pins VDDA11_100BT1	-0.3	-	1.6	V
		on pins VDDA11_100BTX	-0.3	-	1.6	V
		on pins 100BT1_TRX_M/Px	-0.3	-	4	V
		on pins VDDA33_100BTX	-0.3	-	4	V
		on pins VDDA25_RX_100BT1, VDDA25_100BT1_TXMx	-0.3	-	4	V
		on pins VDDA33_VREG_IN	-0.3	-	4	V
		on pins VDD33_AO	-0.3	-	4	V
		on pins VDDIO_x	-0.3	-	4	V
		on pin VDDA18_OTP_OUT	-0.3	-	4	V
		on pin VDDA25_VREG_OUT	-0.3	-	4	V
		on pin VDDA18_OTP_IN [1]	-0.3	-	1.6	V
		on pins SGMIIx_TRXP/N SGMIIx_RXP/N	-0.3	-	1.6	V
		on pins 100BTX_EXTRES, 100BTX_RX_P/M, 100BTX_TX_P/M	-0.3	-	4	V
		on other pins	-0.3	-	4	V
V_{trt}	transient voltage	on pins TRX_P, TRX_M [2]				
		pulse 1	-100	-	-	V
		pulse 2a	-	-	+75	V
		pulse 3a	-150	-	-	V
		pulse 3b	-	-	100	V
V_{ESD}	electrostatic discharge voltage	according to IEC 61000-4-2; 150 pF, 330Ω, on pins TRX_P, TRX_M to GND [2]	-6.0	-	6	kV
		according to Human Body Model (HBM); 100 pF, 1.5 kΩ [3]				
		pins TRX_P, TRX_M to GND	-4.0	-	+4.0	kV
		all other pins	-2	-	+2	kV
		according to Charge Device Model (CDM) [4]				
		corner balls	-750	-	+750	V
		other balls	-500	-	+500	V

Table 51. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_j	junction temperature		-40	-	+150	°C
T_{stg}	storage temperature	[5]	-55	-	+150	°C
T_{amb}	ambient temperature	Variant SJA1110D in 1.8 V xMII supply voltage	-40	-	+125	°C
		Variants SJA1110A, SJA1110B, SJA1110C in operating conditions not exceeding total power at 125 °C of 1 W	-40	-	+125	°C
		Variants SJA1110A, SJA1110B, SJA1110C	-40	-	+105	°C

[1] The voltage on pin VDDA18_OTP_IN is allowed to exceed the specified maximum rating during OTP programming only. The programming voltage and timings are controlled by the device.
[2] Verified by an external test house according to IEC 62228-5
[3] According to AEC-Q100-002
[4] According to AEC-Q100-011
[5] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

10 Static characteristics

Table 52. Static characteristics

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply						
V_{DD}	supply voltage	pin VDD11_CORE	1.045	1.1	1.155	V
		pin VDDIO_x, 3.3 V signaling	3.0	3.3	3.6	V
		pin VDDIO_x, 2.5 V signaling	2.375	2.5	2.625	V
		pin VDDIO_x, 1.8 V signaling	1.65	1.8	1.95	V
		pin VDDA_AO	3.0	3.3	3.6	V
		pin VDDA33_VREG_IN	3.0	3.3	3.6	V
		pin VDDA11_SGMIIx	1.045	1.1	1.155	V
		pin VDDA33_SGMIIx	3.0	3.3	3.6	V
		pin VDDA11_100BT1	1.045	1.1	1.155	V
		pin VDDA25_100BT1_RXM	2.375	2.5	2.625	V
		pin VDDA25_100BT1_TXMx	2.375	2.5	2.625	V
		pin VDDA11_100BTX	1.045	1.1	1.155	V
		pin VDDA33_100BTX	3.135	3.3	3.465	V
		pin VDDA11_PLL, VDDA11_OSC	1.045	1.1	1.155	V
		pin VDDA18_OTP_IN [1]	1.755	1.8	1.845	V
Digital I/O pins[2]						
V_{IH}	HIGH-level input voltage	3.3, 2.5, 1.8 V signaling	0.65 × V_{DDIO}	-	-	V
V_{IL}	LOW-level input voltage	3.3, 2.5, 1.8 V signaling	-	-	0.35 × V_{DDIO}	V
V_{OH}	HIGH-level output voltage	3.3, 2.5, 1.8 V signaling I_{OH} = -2 mA	V_{DDIO} - 0.4	-	-	V
V_{OL}	LOW-level output voltage	3.3, 2.5, 1.8 V signaling I_{OH} = 2 mA	-	-	0.4	V
C_i	input capacitance	[3]	-	-	5.0	pF
$V_{hys(i)}$	input hysteresis voltage	[3]	0.1V × V_{DDIO}	-	-	V
I_{OSH}	HIGH-level short-circuit output current	[3]	-	-	155	mA
I_{OSL}	LOW-level short-circuit output current	[3]	-	-	165	mA
R_{pd}	pull-down resistance		40	50	62	kΩ
R_{pu}	pull-up resistance		40	50	62	kΩ
R	output impedance	[3]	-	50	-	Ω

Table 52. Static characteristics*...continued*

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SGMII[3]						
$\lvert V_{o(dif)} \rvert$	differential output voltage (absolute value)	R_L = 100 Ω	150	-	400	mV
$R_{term(se)}$	single-ended termination resistance		-	100	-	Ω
$V_{ring(o)}$	ringing voltage		-	-	0.1 × Vo(dif)	V
$Z_{o(se)}$	single-ended output impedance		40	-	140	Ω
$\Delta Z_{o(se)}$	single-ended output impedance mismatch		-	-	10	%
$\lvert \Delta_{Vo(dif)\lvert}$	differential output voltage difference	change in differential output voltage between complementary output states R_L = 100 Ω	-	-	25	mV
ΔV_{cm}	common-mode voltage difference	change in output offset voltage between complementary output states R_L = 100 Ω	-	-	25	mV
$V_{th(i)dif}$	differential input threshold voltage		-50	-	50	mV
$Z_{i(dif)RX}$	receiver differential input impedance		80	100	120	Ω
100BASE-T1[3]						
$\lvert V_{o(dif)} \rvert$	differential output voltage (absolute value)	load 100 Ω measured at MDI	-	-	2.2	V
R_{term}	termination resistance		-	100	-	Ω
100BASE-TX[3]						
$\lvert V_{o(dif)} \rvert$	differential output voltage (absolute value)	load 100 Ω measured at MDI	-	1	-	V
R_{term}	termination resistance		-	100	-	Ω
Oscillator[3]						
C_i	input capacitance	on pin XI	-	2	-	pF
C_L	load capacitance		-	8	-	pF
$V_{i(p-p)}$	input voltage	on pin XI	0.8	-	$V_{DDA(OSC)}$	Vpp
Current consumption[3]						
$I_{DD(RMS)}$	RMS supply current[4]	on pin VDDA11_OSC, oscillation mode, 25MHz crystal	-	150	350	µA
		on pin VDDA11_OSC startup current, oscillation mode, 25MHz crystal	-	1.1	3.5	mA
		on pin VDDA11_OSC, slave mode, 25MHz	-	200	450	µA

Table 52. Static characteristics*...continued*

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		on pin VDDA11_PLL, per PLL	-	0.52	0.76	mA
		pins VDDA11_100BT1, per PHY	-	8.5	10	mA
		pins VDDA11_100BTX	-	32	33	mA
		pins VDDA11_SGMIIx , 1 Gbps, per PHY	-	13	21	mA
		pins VDDA11_SGMIIx , 2.5 Gbps, per PHY	-	25	39	mA
		pins VDD11_CORE	-	100	700	mA
		pins VDDA33_AO	-	1	1.5	mA
		pins VDDA33_VREG_IN, all PHYs enabled	-	100	108	mA
		pins VDDA33_100BTX, 100 Mbs mode	-	39	55	mA
		pins VDDA33_SGMIIx, per PHY, 1 GBps	-	2.5	5	mA
		pins VDDA33_SGMIIx, per PHY, 2.5 Gbps	-	6.5	13	mA
		pins VDDA25_100BT1_RXM, per PHY	-	1	1	mA
		pins VDDA25_100BT1_TXMx, per PHY	-	18	18	mA
		pin VDDIO_xMII 1.8V. MII Mode(MAC) 100Mb/s worst-case pattern	-	6	9	mA
		pin VDDIO_xMII 1.8V. RMII Mode(MAC) 100Mb/s worst-case pattern	-	9	12	mA
		pin VDDIO_xMII 1.8V. RGMII Mode 1000Mb/s worst-case pattern	-	17	50	mA
		pin VDDIO_xMII 2.5V. MII Mode(MAC) 100Mb/s worst-case pattern	-	8	13	mA
		pin VDDIO_xMII 2.5V. RMII Mode(MAC) 100Mb/s worst-case pattern	-	12	17	mA
		pin VDDIO_xMII 2.5V. RGMII Mode 1000Mb/s worst-case pattern	-	25	72	mA
		pin VDDIO_xMII 3.3V. MII Mode(MAC) 100Mb/s worst-case pattern	-	10	16	mA

Table 52. Static characteristics*...continued*

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		pin VDDIO_xMII 3.3V. RMII Mode(MAC) 100Mb/s worst-case pattern	-	16	29	mA
		pin VDDIO_xMII 3.3V. RGMII Mode 1000Mb/s worst-case pattern	-	32	88	mA
		pin VDDIO_GPIO, 3.3V, Cl = 29 pF, f = 2 MHz per toggeling pin	-	-	1	mA
		pin VDDIO_HOST, 3.3V, Cl = 29 pF, f = 25 MHz	-	-	4	mA
		pin VDDIO_SPI_PER 3.3V, Cl=29 pF, f = 25 MHz SPI master mode	-	-	6	mA
		pin VDDIO_SPI_PER 3.3V, Cl=29 pF, f = 50 MHz SPI master mode	-	-	12	mA
		pin VDDIO_FLASH 3.3V, Cl = 29 pF, f = 50 MHz	-	-	24	mA
		pin VDDIO_DEBUG, 3.3V Cl = 29 pF, f = 25 MHz	-	-	2	mA
		pin VDDIO_PTP_CLK, 3.3V, Cl = 29 pF, f = 31.25 Mhz	-	-	5	mA
		pin VDDIO_REFCLK_OUT, 3.3V, Cl = 29 pF, f = 31.25 Mhz, per REFCLK_OUT pin	-	-	4	mA
		pin VDDIO_SYNC, 3.3V, Cl = 29 pF	-	-	1	mA
		pin VDDIO_FUSA 3.3V, 1 simultaneous outputs.	-	-	1	mA
I_q	quiescent current	1× 100BASE-T1 PHYs enabled	-	27.1	-	μA
		2× 100BASE-T1 PHYs enabled	-	29.2	-	μA
		3× 100BASE-T1 PHYs enabled	-	31.3	-	μA
		4× 100BASE-T1 PHYs enabled	-	33.4	-	μA
		5× 100BASE-T1 PHYs enabled	-	35.5	-	μA
		6× 100BASE-T1 PHYs enabled	-	37.6	-	μA

[1] This pin must be connected to VDDA18_OTP_OUT only. Do not supply this pin directly
[2] Some pins are input-only or output-only. In this case only the relevant information applies
[3] Not measured in production, guaranteed by design.
[4] Does not include leakage current of disabled PHYs.

11 Dynamic characteristics

Table 53. Dynamic characteristics

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital I/Os (non-MII/RMII/RGMII pins)[1][2]						
t_r	rise time	10 cm PCB transmission line: 50 Ω; 5 pF far-end load. 20% - 80%				
		1.8 V, low drive, low speed mode	2.5	-	5.3	ns
		1.8 V, high drive, low speed mode	2.6	-	5.2	ns
		1.8 V, low drive, high speed mode	1.4	-	4.0	ns
		1.8 V, high drive, high speed mode	1.3	-	3.2	ns
		2.5 V, low drive, low speed mode	2.5	-	5.3	ns
		2.5 V, high drive, low speed mode	2.6	-	5.2	ns
		2.5 V, low drive, high speed mode	0.9	-	2.2	ns
		2.5 V, high drive, high speed mode	0.9	-	2.2	ns
		3.3V, low drive, low speed mode	1.7	-	3.3	ns
		3.3 V, high drive, low speed mode	1.7	-	3.2	ns
		3.3 V, low drive, high speed mode	0.9	-	2.2	ns
		3.3 V, high drive, high speed mode	0.8	-	1.8	ns
t_f	fall time	10 cm PCB transmission line: 50 Ω; 5 pF far-end load. 20% - 80%				
		1.8 V, low drive, low speed mode	2.4	-	5.4	ns
		1.8 V, high drive, low speed mode	2.5	-	5.1	ns
		1.8 V, low drive, high speed mode	1.5	-	4.1	ns
		1.8 V, high drive, high speed mode	1.2	-	3.2	ns
		2.5 V, low drive, low speed mode	2.4	-	5.4	ns
		2.5 V, high drive, low speed mode	2.5	-	5.1	ns
		2.5 V, low drive, high speed mode	0.9	-	2.4	ns
		2.5 V, high drive, high speed mode	0.9	-	2.3	ns
		3.3V, low drive, low speed mode	1.8	-	3.5	ns
		3.3 V, high drive, low speed mode	1.6	-	3.4	ns
		3.3 V, low drive, high speed mode	0.9	-	2.4	ns
		3.3 V, high drive, high speed mode	0.8	-	1.9	ns
Digital I/Os (MII/RMII/RGMII pins)[1][2]						

Table 53. Dynamic characteristics*...continued*

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	15 cm PCB transmission line: 50 Ω; 5 pF far-end load. 20% - 80% [3]				
		1.8 V, Low speed mode	1.4	-	3.6	ns
		1.8 V, Medium speed mode	0.8	-	2.8	ns
		1.8 V, Fast speed mode	0.3	-	1.4	ns
		1.8 V, High speed mode	0.25	-	0.75	ns
		2.5 V, Low speed mode	1.2	-	2.9	ns
		2.5 V, Medium speed mode	0.5	-	2.1	ns
		2.5 V, Fast speed mode	0.25	-	0.75	ns
		2.5 V, High speed mode	0.2	-	0.5	ns
		3.3 V, Low speed mode	0.8	-	2.6	ns
		3.3 V, Medium speed mode	0.4	-	1.4	ns
		3.3 V, Fast speed mode	0.23	-	0.55	ns
		3.3 V, High speed mode	0.2	-	0.4	ns
t_f	fall time	15 cm PCB transmission line: 50 Ω; 5 pF far-end load. 20% - 80% [3]				
		1.8 V, Low speed mode	1.5	-	3.4	ns
		1.8 V, Medium speed mode	0.8	-	2.8	ns
		1.8 V, Fast speed mode	0.3	-	1.4	ns
		1.8 V, High speed mode	0.25	-	0.75	ns
		2.5 V, Low speed mode	0.9	-	2.4	ns
		2.5 V, Medium speed mode	0.5	-	2.1	ns
		2.5 V, Fast speed mode	0.25	-	0.75	ns
		2.5 V, High speed mode	0.2	-	0.5	ns
		3.3 V, Low speed mode	0.6	-	2.4	ns
		3.3 V, Medium speed mode	0.38	-	1.45	ns
		3.3 V, Fast speed mode	0.23	-	0.55	ns
		3.3 V, High speed mode	0.2	-	0.4	ns
MII timing[1][4]						
T_{clk}	clock period	100 Mbit	-	40	-	ns
		10 Mbit	-	400	-	ns
δ	duty cycle	on pin TX_CLK, RX_CLK	35	-	65	%
Δf	frequency deviation	on pin TX_CLK, RX_CLK	-100	-	+100	ppm

Table 53. Dynamic characteristics*...continued*

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	set-up time	from pin RX_CLK to RXD[3:0], RX_DV				
		MII-MAC mode	10	-	-	ns
		MII-PHY mode	10	-	-	ns
t_h	hold time	from pin RX_CLK to RXD[3:0], RX_DV				
		MII-MAC mode	10	-	-	ns
		MII-PHY mode	0	-	-	ns
t_d	delay time	from pin TX_CLK to TXD[3:0], TX_EN				
		MII-MAC mode	0	-	25	ns
		MII-PHY mode, 10 Mbit	12	-	300	ns
		MII-PHY mode, 100 Mbit	12	-	25	ns
RMII timing[1][5]						
T_{clk}	clock period	100 Mbps	-	20	-	ns
		10 Mbps	-	200	-	ns
δ	duty cycle	on pin REF_CLK	35	-	65	%
t_{su}	set-up time	from pins RXD[1:0], CRSDV, RX_ER to REF_CLK	4	-	-	ns
t_h	hold time	from pin REF_CLK to RXD[1:0], CRSDV, RX_ER	2	-	-	ns
t_d	delay time	from pin REF_CLK to TXD[1:0], TX_EN, TX_ER,	2	-	10	ns
RGMII transmit/receive timing[1][6]						
T_{clk}	clock period	on pins TXC, RXC				
		1 Gbps	-	8	-	ns
		100 Mbps	-	40	-	ns
δ	duty cycle	on pins TXC, RXC				
		1 GBps	45	50	55	%
		pin TXC for 100 MBps, 10 Mbps	40	50	60	%
$t_{sk(o)TX}$	transmitter output skew time	RGMII mode, from TXC to TXD[3:0], TX_CTL	-500	-	+500	ps
$t_{sk(i)RX}$	receiver input skew time	RGMII mode, RXC to RXD[3:0], RX_CTL	1	-	2.6	ns
$t_{su(o)TX}$	transmitter output setup time	RGMII-ID mode, from pins TXD[3:0], TX_CTL to TXC	1.2	-	-	ns
$t_{h(o)TX}$	transmitter output hold time	RGMII-ID mode, from pin TXC to TXD[3:0], TX_CTL	1.2	-	-	ns
$t_{su(o)RX}$	receiver output setup time	RGMII-ID mode, from pins RXD[3:0], RX_CTL to RXC	1	-	-	ns

Table 53. Dynamic characteristics...*continued*

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(o)RX}$	receiver output hold time	RGMII-ID mode, from RXC to RXD[3:0], RX_CTL	1	-	-	ns
SGMII[1]						
t_r	rise time	20% - 80%	40	-	200	ps
t_f	fall time	20% - 80%	40	-	200	ps
t_{jit}	jitter time	Baudrate 1.25 Gbps	-	7.7	10	ps
		Baudrate 3.125 Gbps	-	2.3	4.5	ps
100BASE-T1[1]						
$t_{TX\_latency}$	transmitter latency	internal MII from TX_EN to SSD on MDI	145	-	190	ns
$t_{RX\_latency}$	receiver latency	SSD on MDI to RX_DV on internal MII	730	-	800	ns
SMI_AP timing[1]						
T_{clk}	clock period	pin MDC	400	-	-	ns
δ	duty cycle	pin MDC	-	50	-	%
t_{su}	set-up time	MDC to MDIO	10	-	-	ns
t_h	hold time	MDC to MDIO	10	-	-	ns
t_d	delay time	MDC to MDIO	0	-	300	ns
SMI_OUT timing[1]						
T_{clk}	clock period	pin MDC	400	-	-	ns
δ	duty cycle	pin MDC	-	50	-	%
t_{su}	set-up time	MDC to MDIO	30	-	-	ns
t_h	hold time	MDC to MDIO	0	-	-	ns
t_d	delay time	MDC to MDIO	-10	-	25	ns
JTAG[1]						
f_{clk}	clock frequency	pin TCK, 3.3 V signaling, fast-speed mode	0.1	-	25	MHz
δ	duty cycle	pin TCK	40	50	60	%
$t_{det(rst)}$	reset detection time	pin TRST_N	100	-	-	ns
t_{su}	set-up time		4	-	-	ns
t_h	hold time		25	-	-	ns
t_{ov}	output valid time		-	-	20	ns
SPI_AP[1][7]						
f_{clk}	clock frequency		0.1	-	20	MHz
δ	duty cycle		45	50	55	%
t_L	slave-select lead time	fast speed mode	32	-	-	ns

Table 53. Dynamic characteristics*...continued*

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_T	slave-select trailing time	fast speed mode	32	-	-	ns
t_I	idling time	fast speed mode	25	-	-	ns
t_{su}	data input setup time	SCK to SDI	12.4	-	-	ns
t_h	data input hold time	SCK to SDI	18	-	-	ns
t_{ov}	output valid time	SCK to SDO 3.3 V or 2.5 V signaling Fast speed mode	0	-	14	ns
SPI_HOST[1][8]						
f_{clk}	clock frequency	Fast speed mode 3.3 V, 2.5 V signaling	0.1	-	25	MHz
		Fast speed mode 1.8 V signaling	0.1	-	20	MHz
t_L	slave-select lead time		0.5 × TCLK	-	-	ns
t_T	slave-select trailing time		0.5 × TCLK	-	-	ns
t_I	idling time	Deasserting of SPI_HAP_SS1 to asserting SPI_HAP_SS1	0.5 × TCLK	-	-	ns
δ	duty cycle		45	50	55	%
t_{su}	data input setup time	SCK to SDI	12.4	-	-	ns
t_h	data input hold time	SCK to SDI	18	-	-	ns
t_{ov}	output valid time	SCK to SDO 3.3 V or 2.5 V signaling Fast speed mode	0	-	14	ns
		SCK to SDO 1.8 V signaling High speed mode	0	-	19	ns
QSPI[1]						
f_{clk}	clock frequency	Drivestrength setting PIN_CFG_QSPI.XXXX_ODS=Fast. MCR.DQS_EN=0, SMPR.FSPHS=0, SMPR.FSDLY=0.	5	25	50	MHz
Δf	frequency deviation		-100	-	100	ppm
δ	duty cycle		45	50	55	%
t_{lag}	slave-select lead time		3 × TCLK	-	-	ns
t_{lead}	slave-select trailing time		3 × TCLK	-	-	ns

Table 53. Dynamic characteristics...*continued*

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{idle}	idling time		3 × TCLK	-	-	ns
t_{su}	data input setup time	W.r.t. SCLK falling edge. Drivestrength setting PIN_CFG_QSPI.XXXX_ODS=Fast. MCR.DQS_EN=0, SMPR.FSPHS=0, SMPR.FSDLY=0.	15.4	-	-	ns
t_h	data input hold time	W.r.t. SCK falling edge.	0	-	-	ns
t_{ov}	data output valid time	W.r.t. SCK failing edge.	-	-	4	ns
t_{oh}	data output hold time	W.r.t. SCK failing edge.	-4	-	-	ns
SPI_PER[1]						
f_{clk}	clock frequency	Master mode sample mode disabled Fast speed mode	0.1	16	20	MHz
		Master mode sample mode enabled. Fast speed mode	0.1	25	50	MHz
δ	duty cycle	For Slave and Master mode	45	50	55	%
t_{lag}	slave-select lead time	Slave mode	0.5 × TCLK	-	-	ns
t_{lead}	slave-select trailing time	Slave mode	0.5 × TCLK	-	-	ns
t_{idle}	idling time	Slave mode	0.5 × TCLK	-	-	ns
t_{su}	set-up time	Slave mode 1.8 V signaling High-speed mode	12.4	-	-	ns
		Slave mode 2.5 V, 3.3 V signaling Fast-speed mode	18	-	-	ns
		Master mode Sample mode disabled 2.5 or 3.3 V signaling Fast-speed mode	9	-	-	ns
		Master mode Sample mode disabled 1.8V signaling Fast-speed mode	12	-	-	ns

Table 53. Dynamic characteristics*...continued*

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Master mode Sample mode enabled Fast-speed mode	4	-	-	ns
t_h	hold time	Slave mode 1.8 V signaling High-speed mode	18	-	-	ns
		Slave mode 2.5 V, 3.3 V signaling Fast-speed mode	18	-	-	ns
		Master mode Sample mode disabled Fast-speed mode	0	-	-	ns
		Master mode Sample mode enabled Fast-speed mode	3	-	-	ns
t_{ov}	output valid time	Slave mode 1.8 V signaling High-speed mode	0	-	18	ns
		Slave mode 2.5 V, 3.3 V signaling Fast-Speed mode	0	-	14	ns
		Master mode	0	-	5	ns
CLK_OUT[1]						
f_{clk}	clock frequency	pins REFCLK_OUT[0:3]	-	25	-	MHz
Δf	frequency deviation	pins REFCLK_OUT[0:3]	-50	-	50	ppm
$t_{jit(per)}$	period jitter time	with external crystal. Measured over 10000 cycles.	-	-	10	ps
		running in slave mode. Clock source has the maximum allowed amount of jitter. Measured over 10000 cycles.	-	-	16	ps
Oscillator[1]						
f_{osc}	oscillator frequency		-	25	-	MHz
Δf	frequency deviation	over lifetime and temperature range	-50	-	50	ppm
Oscillator Slave Mode (external clock)[1]						
$V_{i(osc)}$	oscillator input voltage	pin XI for externally connected AC-coupled clock. C_{AC}=100 pF	0.6	-	1.21	V_{pp}
δ	duty cycle	pin XI	45	50	55	%
$t_{jit(per)}$	period jitter time	pin XI	-	1	10	ps

Table 53. Dynamic characteristics...*continued*

T_j = -40 °C to + 150 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC. Not measured in production, guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reset and startup[1]						
$t_{det(rst)}$	reset detection time	pins RST_N, RST_CORE_N V_{AO} 3.3 V	1	-	-	ms
dV_{ru}/dt	rate of change of ramp-up voltage	20 % - 80 %; all supply pins	0.001	-	10	V/ms

[1] Not measured in production, guaranteed by design.
[2] For reference only. Run simulations with the IBIS model and your custom board for accurate results.
[3] Not all IO speed modes are available in any MII/RMII/RGMII mode, consult the SJA1110 Usermanual
[4] MII configuration as per Usermanual
[5] RMII configuration as per Usermanual
[6] RGMII configuration as per Usermanual
[7] SPI_HAP with SPI_HAP_SS0 asserted
[8] SPI_HAP with SPI_HAP_SS1 asserted

12 Application information

12.1 100BASE-T1

A typical MDI application is shown in Figure 20. It consists of 100 nF AC-coupling capacitors, a common mode choke, a common mode termination network and optional ESD diodes. External ESD protection is required if more than 6 kV robustness is required.

It is recommended to use CMC and ESD components that are OPEN Alliance compatible.

The analog line driver and receiver of the 100BASE-T1 PHYs are supplied with 2.5 V via pins VDDA25_RX_100BT1 and VDDA25_100BT1_TXMx. The integrated VDDA25_VREG_OUT regulator can be used to generate 2.5 V specifically for this use case.

Note: *Do not supply any external loads from VDDA25_REG_OUT.*

The digital and analog core voltage common to all PHYs is supplied via pins VDDA11_100BT1.

The recoved clock (TX_TCLK 66.666 MHz) used for the PMA conformance test is output on pin LOC_WAKE_IN.

Further information on the application of the SJA1110 can be found in AN13225 *'SJA1110 hardware application notes'*.

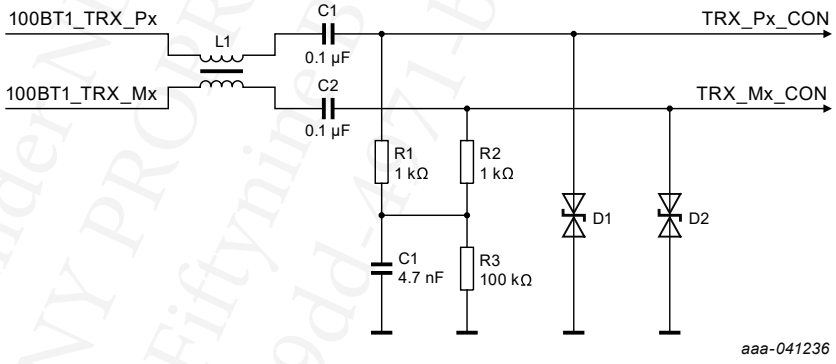


Figure 20. MDI schematic diagram

12.2 Single SJA1110

Figure 21 shows a typical application with a single SJA1110A connected to an external host controller over a 2.5 Gbit/s SGMII link. The high-speed uplink allows for additional traffic filtering and routing on the external host.

In such a configuration, a 100BASE-TX interface and all six integrated 100BASE-T1 PHYs are available.

External 1000BASE-T1 PHYs can be connected over SGMII and RGMII interfaces for backbone communication.

The integrated Arm core boots from the externally connected flash IC and takes care of running 802.1AS (gPTP) and other management tasks.

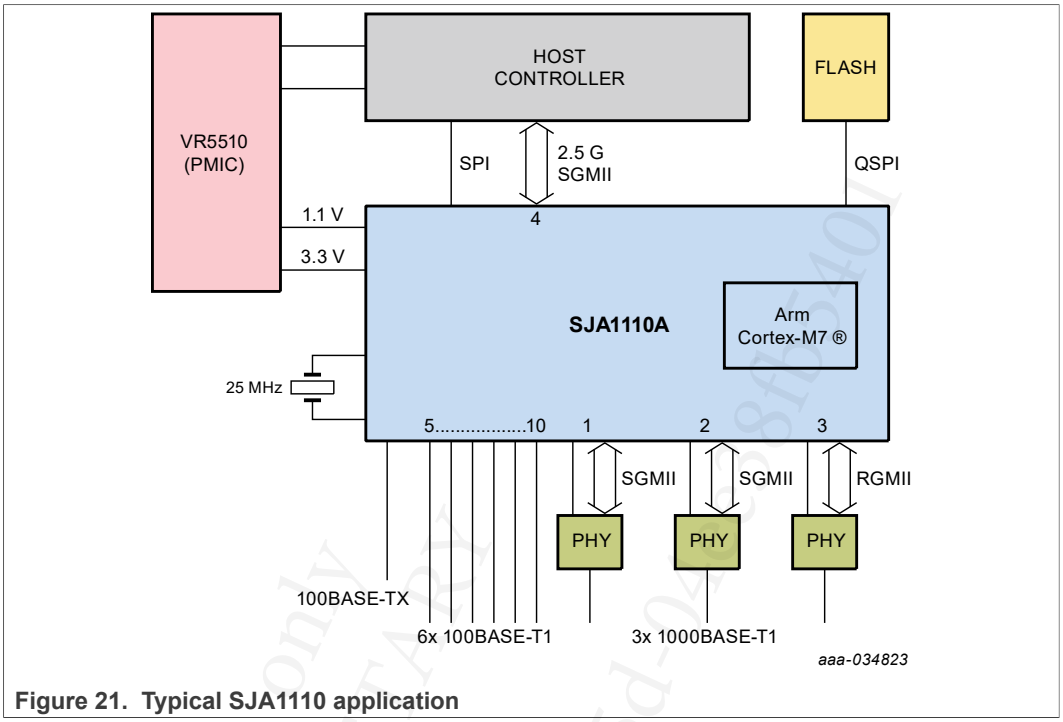


Figure 21. Typical SJA1110 application

12.3 Power supply

The device requires the following suppy voltages and it is advisable to use an integrated PMIC (for example VR5510) to generate the voltages.

- 1.1 V supply for core, oscillator, PLL and 100BASE-T1, 100BASE-TX and SGMII PHYs
- 2.5 V supply for 100BASE-T1 PHY, typically supplied by the integrated 2.5 V regulator.
- 3.3 V for on-chip 1.8 V/2.5 V regulators,100BASE-TX and SGMII PHYs
- 3.3 V (always-on domain) for Wake-up/Sleep support
- 1.8 V, 2.5 V or 3.3 V IO supply, depending on the connected devices

No special sequencing is needed during supply ramp-up. RST_CORE_N should be released when all supplies are within specified values.

It is recommended to use PI type filtering circuits on each main functional block supply, see Figure 22. Note that the IR drop across the ferrit beads is critical and must be selected to meet the operating conditions of each rail (especially digital core supply). It is recommended to use max. 330 Ω @100 MHz, for example BLM18PG331. Addition information can be found in AN13225 *'SJA1110 hardware application notes'*.

Note: *VDDIO_MII2 and VDDIO_MII3 must also be supplied, even when an interface is unused. The xMII2 and xMII3 pins must be connected to ground.*

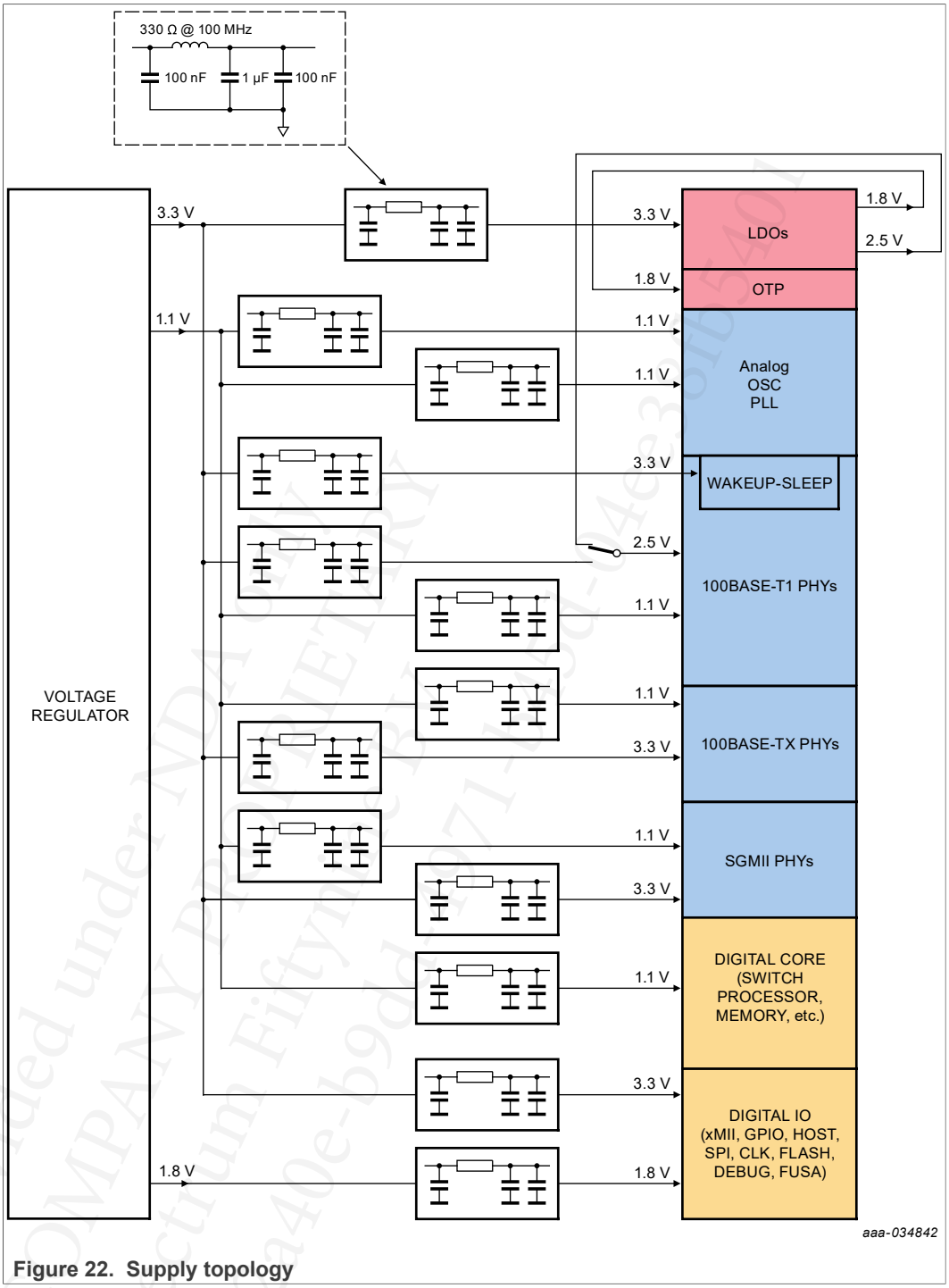


Figure 22. Supply topology

Note: *VDDA11_SGMII[1:4] must be supplied from the same supply source as the VDD11_CORE. If a variant does not support an SGMII port or if an SGMII port is unused, supply pins VDDA11_SGMII[n] and VDDA_SGMII[n] of the unused SGMII port [n] should be grounded.*

13 Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-H - *Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14 Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 23) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 54 and Table 55

Table 54. SnPb eutectic process (from J-STD-020D)

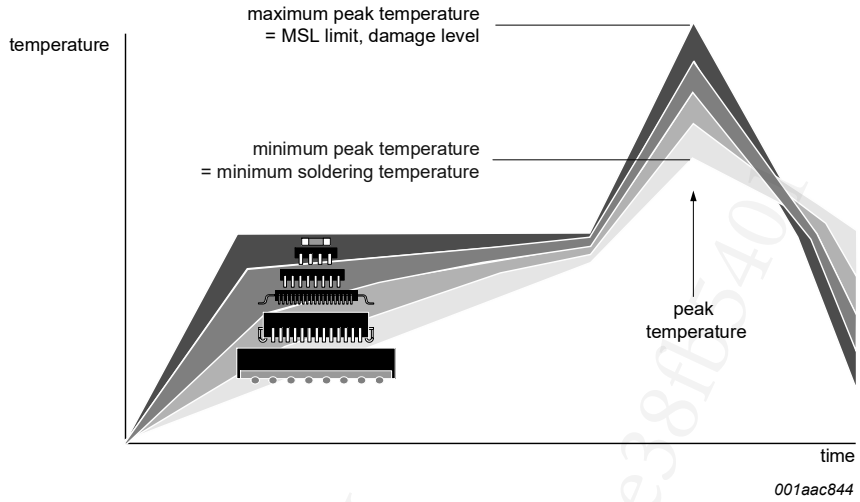
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 55. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 23.



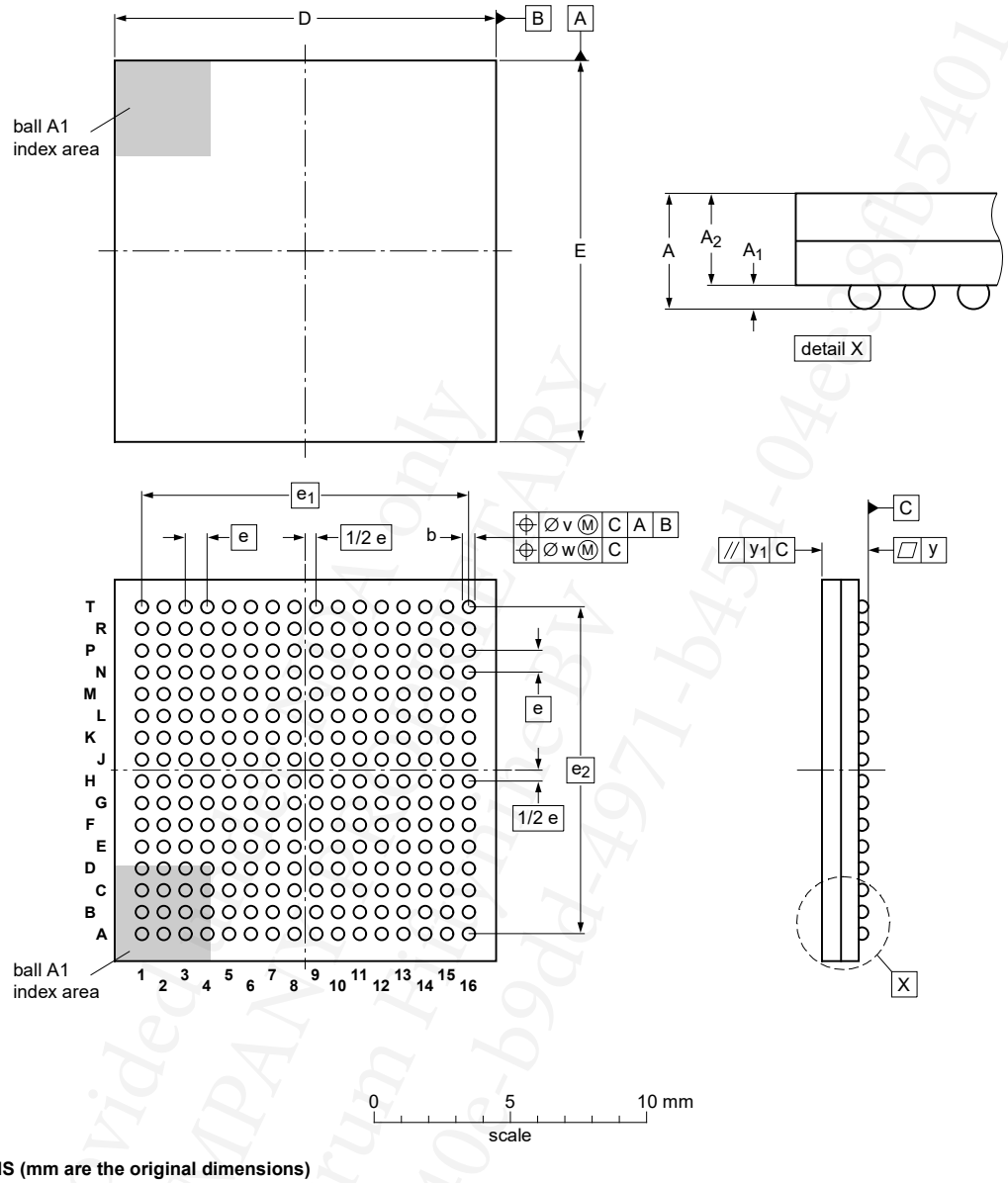
MSL: Moisture Sensitivity Level

Figure 23. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15 Package outline

LFBGA256: plastic low profile fine-pitch ball grid array package; 256 balls **SOT1020-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.7	0.4 0.3	1.35 1.15	0.5 0.4	14.1 13.9	14.1 13.9	0.8	12	12	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1020-1						~~07-07-11~~ 07-08-20

Figure 24. Package outline SJA1110A, SJA1110B, SJA1110C, SJA1110D

16 Revision history

Table 56. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SJA1110 v.0.1	25.07.2018	Objective Datasheet	-	-
SJA1110 v.0.2	17.10.2018	Objective Datasheet • Fixed some supply pin descriptions which stated wrong voltages • New block diagram • Updated default pin states as defined in pinning sheet • Reworked µC section in Features list.	-	v.0.1
SJA1110 v.0.3	10.12.2018	Objective Datasheet • Added missing pins to power management table	-	v.0.2
SJA1110 v.0.4	04.26.2019	Objective Datasheet • Removed LFBGA196 throughout document • Table 1 "Feature overview of the SJA1110X family" – Changed bullets to values in multiple cells • Added the following sections – Limiting values – Thermal characteristics – Static charactersitics – Dynamic charactersitics	-	v.0.3
SJA1110 v.0.5	30.08.2020	Objective Datasheet • Added block diagram as in Usermanual • Added support for ASIL-B • Added functional descriptions • Added application section with power supply network • Added 2.5 V support on all VDDIOx • Revised marking: Preliminary marking changed to Objective. • Revised variant D: second MII/RMII/RGMII port enabled • Revision of all characteristics • Revised Grade 1 / Grade 2 ratings	-	v0.4

Table 56. Revision history...*continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
SJA1110 v.0.6	07.05.2021	Objective Datasheet • Added missing 2.5 V statements in pinning list • Spelling and editorial rework • Added more description to reset section • Fixed incorrect descriptions in the pinning sheet – MDIO, MDC and MII pins were incorrectly described • Updated figures • Updated characteristics – Changed symbols to NXP conventions – Added missing SPI lead, lag, idle times – Added missing SPI_PER mode (Slave mode, 2.5/3.3V mode) – Fixed 3.3V CMOS levels. Previous revision stated TTL compatible level – Added missing supply level for pin VDDA33_100BTX – Completed thermal section – Completed HBM ESD data – Revised SGMII characteristics • Added test information section • Added soldering section	-	v0.5
SJA1110 v.0.7	11.08.2021	Objective Datasheet • Text corrections and <tbd> items updated	-	v0.6

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Date of release: 11 August 2021
Document identifier: SJA1110