Freescale Semiconductor
Application Note

Document Number:
Rev. #, 10/2011

Migrating between MX6DQ, 6DL and 6S

The i.MX6D, i.MX6Q, i.MX6DL and i.MX6S multimedia applications processors represent there of Freescale Semiconductor's ARM Cortex-A9 based multimedia-focused products; offering high performance processing with a high degree of functional integration and optimized for low power consumption.

The i.MX6D, MX6Q, i.MX6DL and i.MX6S processors have similar features. Their similar implementation allows a natural migration from i.MX6D, MX6Q, i.MX6DL and i.MX6S. The flexibility of these four processors allows them to be used in a wide variety of applications such as the following:

- Automotive navigation and entertainment
- Graphics rendering for HMI
- High performance speech processing with large databases
- Audio playback
- Video processing and display
- Netbooks (web tablets)
- Nettops (Internet desktop devices)
- PDAs
- PMP (Portable Media players) with HD video capability
- Gaming consoles
- Portable Navigation Devices (PND)
- Color &Monochrome eReaders

Contents

1. Overview

i.MX6D, i.MX6Q, i.MX6DL and i.MX6S feature Freescale's advanced implementation of the Quad/Dual/Sole ARM™ Cortex-A9 core, which operates at speeds up to 1 GHz. They include 2D and 3D graphics processors, 3D 1080p video processing, and integrated power management. Each processor provides a DDR3/LVDDR3/LPDDR2 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, Hard drive, displays, and camera sensors.

Note that each processor has a part family, meaning that there are multiple versions of each part with the possibility of different features/modules enabled or disabled in each. Each part in the family targets a specific market segment (consumer, automotive or industrial). For a complete list of currently available part versions and their included features/modules, refer to the latest chip-specific datasheet.

2. Common Features Summary

The i.MX6D, i.MX6Q, i.MX6DL and i.MX6S contain a large number of digital and analog modules. For a more detailed description of all of the modules and features for each, refer to the product datasheet and/or reference manual for the four silicons. Table 1shows the common features of them.

The Board Design of the common features should be same.

Table 1 Common Features Summary of i.MX6x processors

Features	Description
Nand Flash	8 bit, support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
Nor Flash	16 bit, all WEIMv2 pins are muxed on other interfaces
PSRAM	16 bit, Cellular RAM
Parallel Display Port	24 bit, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
HDMI	Support HDMI 1.4
Parallel Camera Port	Support up to 20 bit and up to 240MHz peak

MMC/SD/SDIO	Four MMC/SD/SDIO card ports all supporting: • bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
USB	High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy Three USB 2.0 (480 Mbps) hosts: • One HS host with integrated High Speed Phy • Two HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
PCIe	Support V2.0 one lane • PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
I2S/SSI/AC97	Up to 1.4Mbps each
ESAI	Up to 1.4Mbps per channel
UART	Five UARTs, up to 4.0 Mbps each: • Providing RS232 interface • Supporting 9-bit RS485 multidrop mode • One of the five UARTs (UART1) supports 8-wire while others four support 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
Gigabit Ethernet Controller	IEEE1588 compliant, 10/100/1000Mbps
PWM	Four Pulse Width Modulators
SJC	System JTAG Controller
GPIO	With interrupt capabilities
KPP	8x8 Key Pad Port
SPDIF	Sony Philips Digital Interface, Rx and Tx
FlexCAN	Two Controller Area Network (FlexCAN), 1 Mbps each
WDOG	Two Watchdog timers (WDOG)
AUDMUX	Audio MUX

3. Comparative Features

Table 2 shows the key feature differences of i.MX6D, i.MX6Q, i.MX6DL and i.MX6S that will be discussed in this application note.

Table 2 Comparative Features Summary of the i.MX6D, i.MX6Q, i.MX6DL and i.MX6S

Features	i.MX6D	i.MX6Q	i.MX6DL	i.MX6S
Core	Dual Cortex-A9 1GHz	Qual Cortex-A9 1GHz	Dual Cortex-A9 1GHz	Sole Cortex-A9 1GHz
Memory	4 GB, x16/x32/x64 DDR3-1066 LV-DDR3-1066 1/2 LPDDR2-1066 Supporting DDR interleaving mode, for 2x32 LPDDR2-1066	4 GB, x16/x32/x64 DDR3-1066 LV-DDR3-1066 1/2 LPDDR2-1066 Supporting DDR interleaving mode, for 2x32 LPDDR2-1066	4 GB, x16/x32/x64 DDR3-800 LV-DDR3-800 1/2 LPDDR2-800 Supporting DDR interleaving mode, for 2x32 LPDDR2-800	4 GB, x16/x32 DDR3-800 LV-DDR3-800 LPDDR2-800
RAM	256KB	256KB	128KB	128KB
L2 Cache	1MB unified I/D L2 Cache shared by dual core	1MB unified I/D L2 Cache shared by Qual core	512KB unified I/D L2 Cache shared by dual core	512KB unified I/D L2 Cache
IPU	2 Antonomous and independent IPU	2 Antonomous and independent IPU	An IPU	An IPU
Graphics Acceleration	Three independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with four shaders (up to 200 MT/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator	Three independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with four shaders (up to 200 MT/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator	Two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with one shader and a 2D graphics accelerator	Two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with one shader and a 2D graphics accelerator
EPD Controller	N/A	N/A	Supports E-INK color and monochrome with up to 1650x2332 resolution and 5-bit grayscale (32-levels per color channel)	Supports E-INK color and monochrome with up to 1650x2332 resolution and 5-bit grayscale (32-levels per color channel)
Displays	Support up to 4 displays including parallel display, HDMI1.4, MIPI display, and LVDS display	Support up to 4 displays including parallel display, HDMI1.4, MIPI display, and LVDS display	Up to 2 displays	Up to 2 displays
Video input	Support 3 video inputs	Support 3 video inputs	Support 2 video inputs	Support 2 video inputs
MIPI Camera	Support 4 lanes	Support 4 lanes	Support 2 lanes	Support 2 lanes
SATA	SATAII, 3.0Gbps	SATAII, 3.0Gbps	N/A	N/A
I2C	3 I2C, supporting 400 kbps	3 I2C, supporting 400 kbps	4 I2C, supporting 400 kbps	4 I2C, supporting 400 kbps

eCSPI	5 eCSPI, up to 52Mbps each	5 eCSPI, up to 52Mbps each	4 eCSPI, up to 52Mbps each	4 eCSPI, up to 52Mbps each

4. Power

4.1. Connection difference

The pin out of the MX6D, 6Q, 6DL and 6S devices is the same in all of them. The only difference is on how to connect the VDDARM23_xx and VDDARM1_xx power domains. Figure 1 show where these domains are located and Table 3 specifies how to connect them for each one of the devices. As can be seen in the table, the ADDARM_IN and VDDARM_CAP domains have the same connection for all the devices.

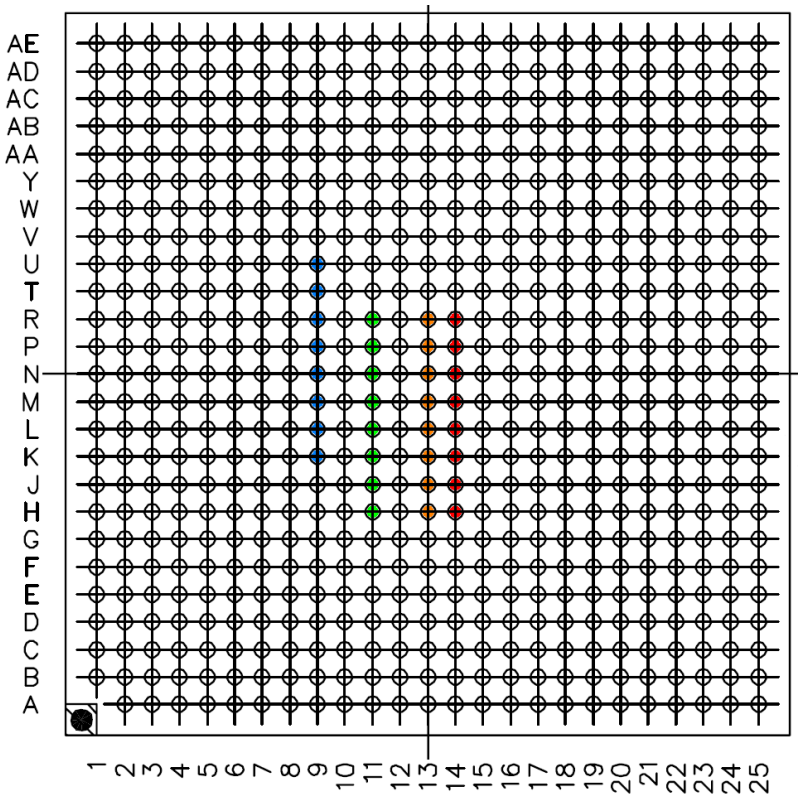

Figure 1 MX6x VDDARMxx_xx locations (Bottom view)

Table 3 VDDARMxx_xx connections

	MX6 Quad		MX6 Dual		MX6 Dual Lite		MX6 Solo	
	Domain Name	**Connection**	**Domain Name**	**Connection**	**Domain Name**	**Connection**	**Domain Name**	**Connection**
	VDDARM23_IN	Connect to VDDARM_IN	VDDARM23_IN	Connect to GND	VDDARM1_IN	Connect to VDDARM_IN	VDDARM1_IN	Connect to VDDARM_IN
	VDDARM23_CAP	Connect to VDDARM_CAP	VDDARM23_CAP	Connect to GND	VDDARM1_CAP	Connect to VDDARM_CAP	VDDARM1_CAP	Connect to VDDARM_CAP
	VDDARM_IN	Connect to power supply	VDDARM_IN	Connect to power supply	VDDARM_IN	Connect to power supply	VDDARM_IN	Connect to power supply
	VDDARM_CAP	Place external capacitors	VDDARM_CAP	Place external capacitors	VDDARM_CAP	Place external capacitors	VDDARM_CAP	Place external capacitors

4.2. All-in-one Circuit

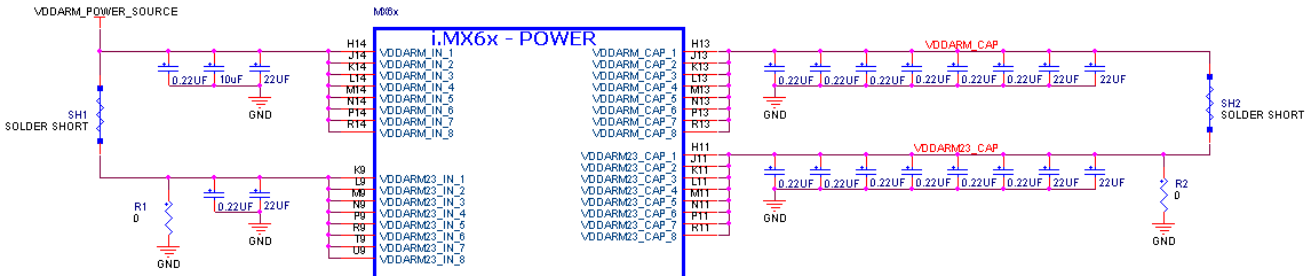

Figure 6 All-in-one Circuit

Table 4 ARM Power Pins connection

	MX6 Quad	MX6 Dual	MX6 Dual Lite	MX6 Solo
SH1	Shorted	Open	Shorted	Shorted
SH2	Shorted	Open	Shorted	Shorted
R1	Open	Shorted	Open	Open
R2	Open	Shorted	Open	Open

4.3. Layout Guidelines

4.3.1. Capacitor Placement

It is highly recommended to place the decoupling capacitors of the power domains on the bottom layer of the board, right next to their respective pins. Figure 7 shows the recommended placement for the VDDARMxx_xx domains. The highlighted pins correspond to the VDDARM23_IN and VDDARM23_CAP nets and their respective capacitors in the case of the MX6Q and MX6D devices and VDDARM1_IN and VDDARM1_CAP in the case of the MX6DL and MX6S. These capacitors can be removed in order to save space in the case when these pins are connected to GND.

Legend:

Red: i.MX6x on Top layer

Blue: Capacitors footprints at Bottom layer

Green: VDDARMxx_IN

Yellow: VDDARMxx_CAP

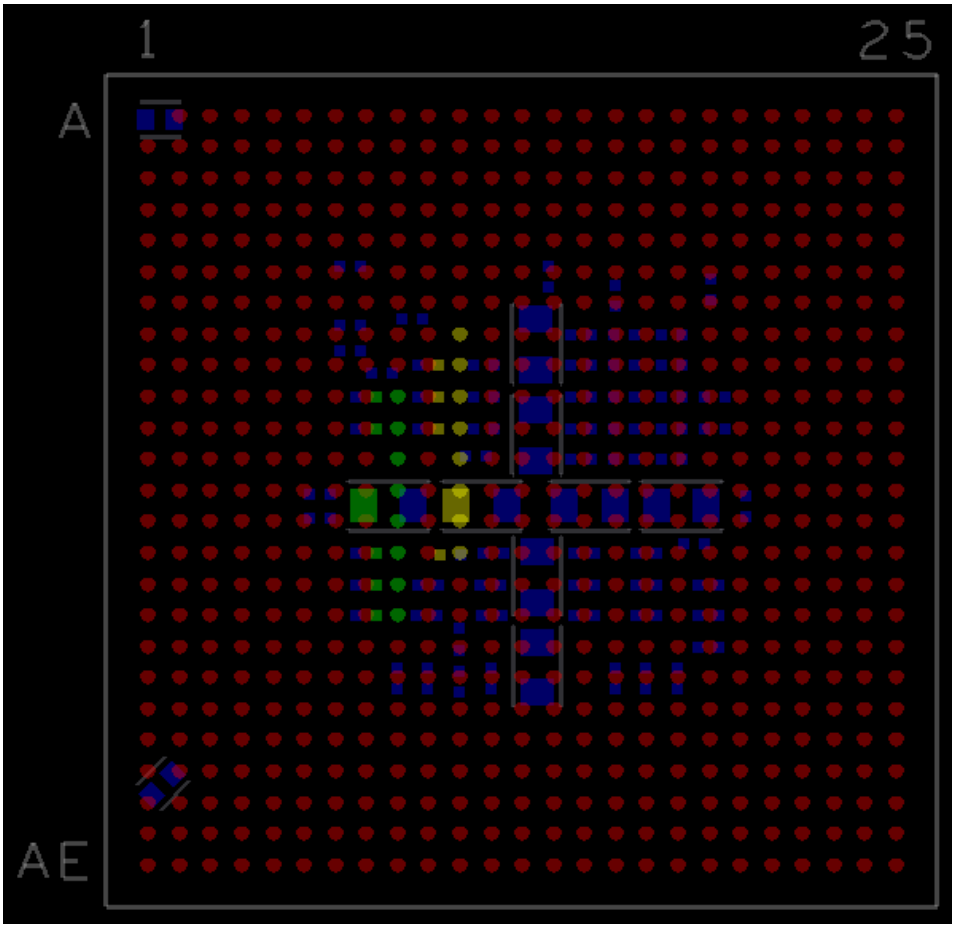

Figure 7 Decoupling Capacitor Placement

5. DRAM Interface

i.MX6x series processors support up to 4Gbyte DDR memory space.

As MX6D, 6Q, 6DL have same ball map, the DRAM PCB layout routing should be no much difference. MX6S only support 32 bit DRAM, the D32~D63, DQM4~7 and SDQS4~7(_B) should be empty.

5.1. DDR3 Connection

i.MX6D and i.MX6Q support 16/32/64 bit DDR3-1066 and LV-DDR3-1066.

i.MX6DL supports 16/32/64 bit DDR3-800 and LV-DDR3-800.

i.MX6S supports 16/32 bit DDR3-800 and LV-DDR3-800

5.1.1. 64 bit, 2CS DDR3 use case

In 64bit, 2CS use case, when migrating MX6Q and MX6D board to MX6DL, no HW change need, except the memory access speed will be reduced. When migrating MX6Q and MX6D board to MX6S in 64bit use case, the 4 pcs DDR3 in higher 32bit should be DNP.

Address Space: Take 2GB space as example
Basic memory Chip: 256MB x8
64bit bus, 2 CSs

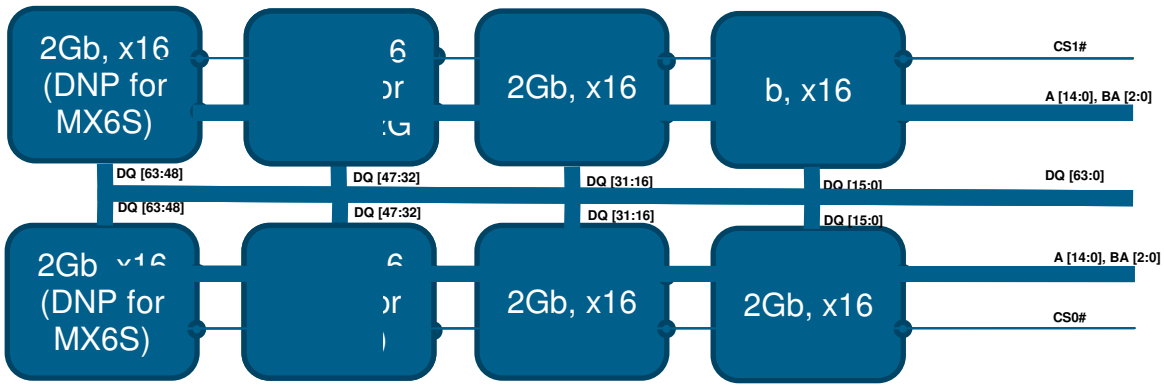

Figure 8 64 bit, 2 CS DDR3 use case

5.1.2. 64 bit, 1CS DDR3 use case

In 64bit, 1 CS use case, when migrating MX6Q and MX6D board to MX6DL, no HW change need, except the memory access speed will be reduced. When migrating MX6Q and MX6D board to MX6S in 64bit use case, the 4 pcs DDR3 in higher 32bit should be DNP.

Address Space: Take 1GB space as example
Basic memory Chip: 2Gb, x8 (256M x8)
64bit bus, 1 CS

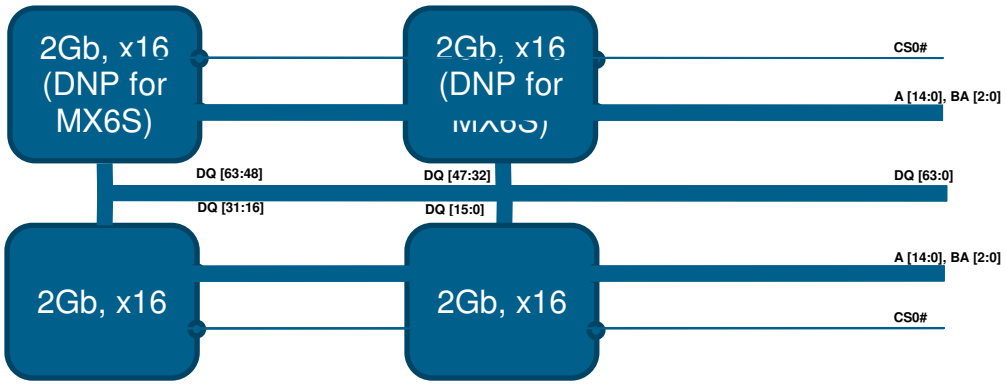

Figure 9 64 bit, 1 CS DDR3 use case

5.1.3. 32 bit, 2CS DDR3 use case

In 32bit, 2 CS use case, when migrating MX6Q and MX6D board to MX6DL or MX6S, no HW change need, except the memory access speed will be reduced.

Address Space: Take 1GB space as example
Basic memory Chip: 2Gb, x8 (256M x8)
32bit bus, 2 CSs

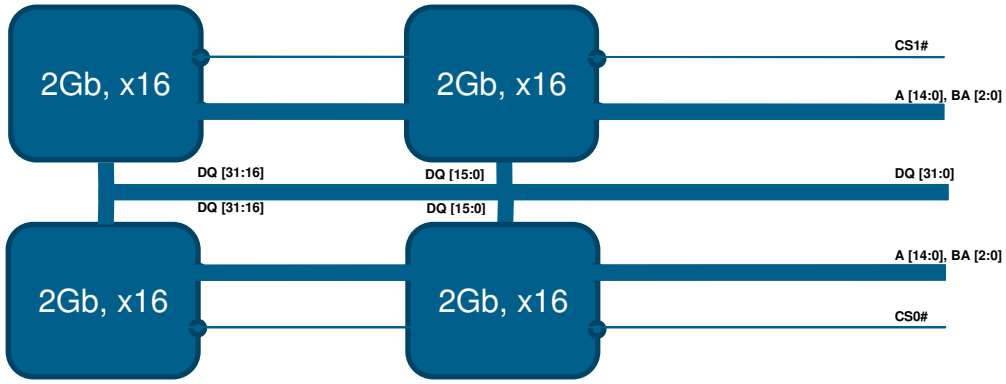

Figure 10 32 bit, 2 CS DDR3 use case

Note: In each use cases, designer can adjust the data lines sequence in same byte for PCB layout convenience, except the lowest bit which will be used for memory calibration.

5.2. LPDDR2

i.MX6D and 6Q can support 2x32 or 64 bit configuration LPDDR2-1066.

i.MX6DL supports 2x32 or 64 bit configuration bit LPDDR2-800.

i.MX6S supports 32bit LPDDR2-800.

MX6D, MX6Q and MX6DL POP packages have same top ball map and can support 14x14mm, 0.5 mm pitch, 240 balls POP LPDDR2.

i.MX6S POP package is not finalized yet when the doc is editing.

5.2.1. 64 bit dual LPDDR2 use case

Address Space: Up to 1GB
Basic memory Chip: 4Gb x2, 2CS

Figure 12 64 bit LPDDR2 connection for MX6D, MX6Q and MX6DL

The 64 bit, dual LPDDR2 (Interleave) use case can only work on the three devices.

6. EPD

As MX6D and MX6Q do not have EPD controller, designer has to reserve the EPD related pins if the board will migrate to MX6DL and MX6S for e-Reader application.

MX6DL and MX6S EPD muxed pins are muxed with EIM signals and listed as followed:

Table 6 EPD muxed pins

PAD (451)	Alt8
EIM_DA14	epdc.SDDO[14]
EIM_DA15	epdc.SDDO[9]
EIM_BCLK	epdc.SDCE[9]
EIM_DA13	epdc.SDDO[13]
EIM_DA10	epdc.SDDO[1]
EIM_DA12	epdc.SDDO[2]
EIM_DA9	epdc.SDCE[5]
EIM_DA11	epdc.SDDO[3]
EIM_DA7	epdc.SDCE[3]
EIM_DA5	epdc.SDCE[1]
EIM_DA8	epdc.SDCE[4]
EIM_DA4	epdc.SDCE[0]
EIM_DA2	epdc.BDR[0]
EIM_DA6	epdc.SDCE[2]
EIM_DA0	epdc.SDCLKN
EIM_DA3	epdc.BDR[1]
EIM_EB1	epdc.SDSHR
EIM_EB0	epdc.PWRCOM
EIM_DA1	epdc.SDLE
EIM_LBA	epdc.SDDO[4]
EIM_OE	epdc.PWRIRQ
EIM_RW	epdc.SDDO[7]
EIM_CS1	epdc.SDDO[8]
EIM_A16	epdc.SDDO[0]
EIM_A18	epdc.PWRCTRL[0]
EIM_CS0	epdc.SDDO[6]
EIM_A23	epdc.GDOE
EIM_A21	epdc.GDCLK
EIM_A19	epdc.PWRCTRL[1]
EIM_A20	epdc.PWRCTRL[2]
EIM_A24	epdc.GDRL
EIM_A17	epdc.PWRSTAT
EIM_A22	epdc.GDSP
EIM_D26	epdc.SDOED
EIM_D28	epdc.PWRCTRL[3]
EIM_D30	epdc.SDOEZ
EIM_D23	epdc.SDDO[11]
EIM_D31	epdc.SDCLK
EIM_D18	epdc.VCOM[1]
EIM_D25	epdc.SDCE[8]
EIM_EB3	epdc.SDCE[0]

EIM_D16	epdc.SDDO[10]
EIM_D29	epdc.PWRWAKE
EIM_D27	epdc.SDOE
EIM_D19	epdc.SDDO[12]
EIM_A25	epdc.SDDO[15]
EIM_D24	epdc.SDCE[7]
EIM_D22	epdc.SDCE[6]
EIM_D17	epdc.VCOM[0]
EIM_EB2	epdc.SDDO[5]

7. Displays

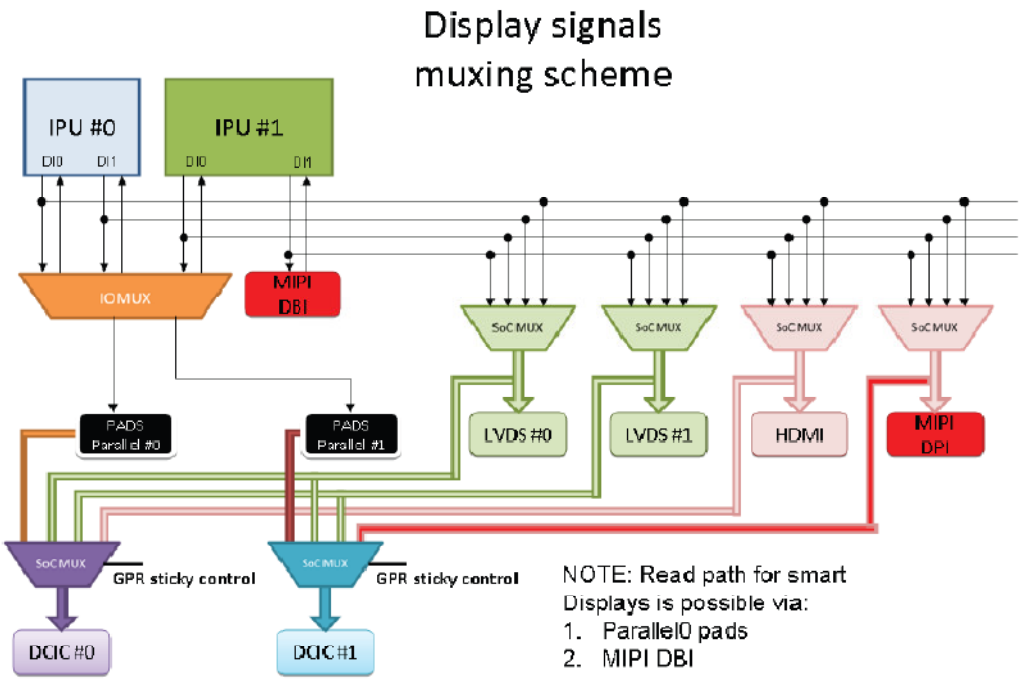

Figure 13 MX6D and MX6Q Display Ports muxing scheme

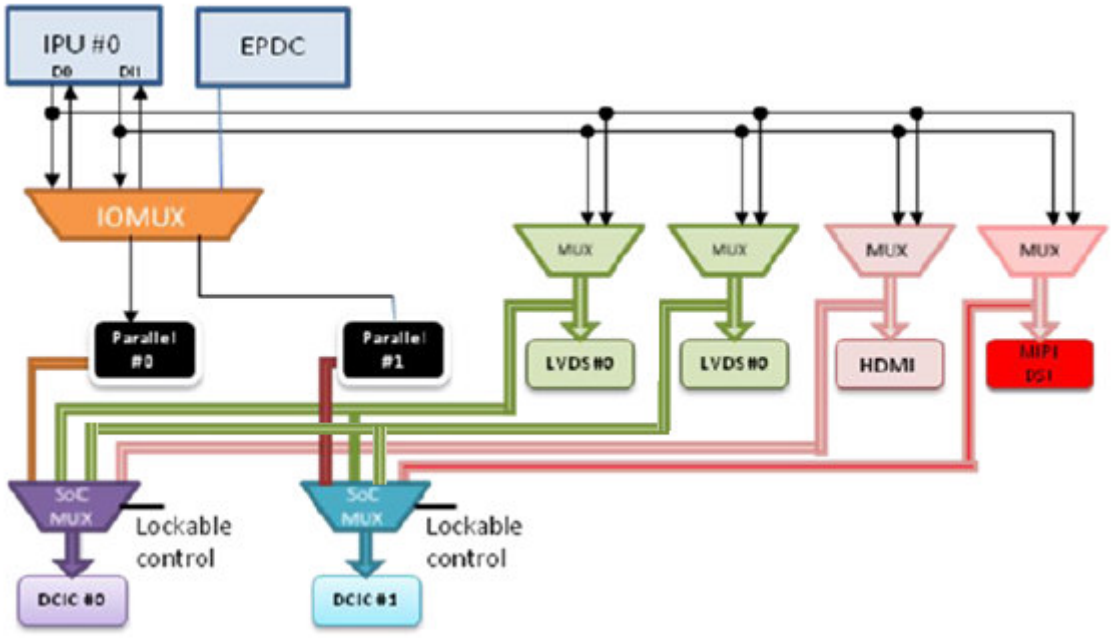

Figure 14 MX6DL and MX6S Display Port muxing scheme (to be update)

MX6D and MX6Q have 2 independent IPU (Image Process Unit), and each IPU has 2 display ports. There are up to four external ports can be active at any given time.

MX6DL and MX6S have 1 IPU, so they can only support two display ports at one time.

8. Video input

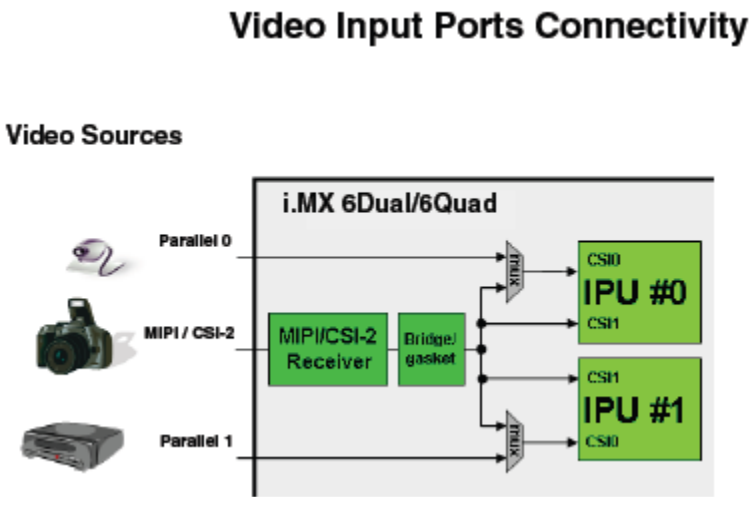

Figure 15 MX6D and MX6Q Video Input Ports

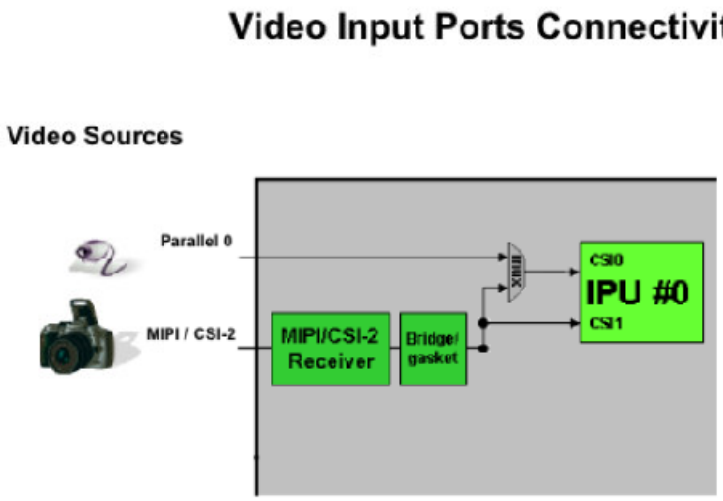

Figure 16 MX6DL and MX6S Video Input Ports

Pls do not use Parallel 1 port as the Video input if the board will be migrated to MX6DL or MX6S

9. SATA

All SATA pins can be left open when migrating MX6D, MX6Q board to MX6DL or MX6S

10. eCSPI

MX6D and MX6Q have 5 eCSPI (eCSPI1~5) interfaces, support up to 52Mbps each. While MX6DL and MX6S have 4 eCSPI (eCSPI1~4) interfaces, and each of them can support up to 53Mbps.

Pls note that do not use SD1 and SD2 signals as CSPI5 if the board will be migrated to MX6DL or MX6S, because MX6DL and MX6S will have no eCSPI5 muxing function in SD1 and SD2 signals.

Table 7 eCSPI5 muxed pins in MX6D and MX6Q

Pad	Power Group	ALT1 Mode	
		Instance	Port
SD2_DAT1	SD2	ecspi5	SS0
SD2_DAT2	SD2	ecspi5	SS1
SD2_DAT0	SD2	ecspi5	MISO
SD1_DAT1	SD1	ecspi5	SS0
SD1_DAT0	SD1	ecspi5	MISO
SD1_DAT3	SD1	ecspi5	SS2
SD1_CMD	SD1	ecspi5	MOSI

SD1_DAT2	SD1	ecspi5	SS1
SD1_CLK	SD1	ecspi5	SCLK
SD2_CLK	SD2	ecspi5	SCLK
SD2_CMD	SD2	ecspi5	MOSI
SD2_DAT3	SD2	ecspi5	SS3

11. I2C

Compared with MX6D and MX6Q, MX6DL and MX6S have an extra I2C (I2C4).

Table 8 I2C4 muxing in MX6DL and MX6S

PAD (451)	Alt8
GPIO_8	i2c4.SDA
GPIO_7	i2c4.SCL

Pls reserve GPIO_8 and GPIO_7 for I2C4 in MX6D and MX6Q board if I2C4 will be used after migrating to MX6DL and MX6S

12. MIPI Camera

MX6D and MX6Q support up to 4 D-PHY Rx Data lanes, but MX6DL and MX6S only support 2 D-PHY Rx Data lanes. CSI_D2 and CSI_D3 related pins will not present in MX6DL and MX6S. Pls use MIPI Camera with two data lanes and connect them with CSI_D0 and CSI_D1 pins if the board will be migrated to MX6DL and MX6S.

Table 9 Extra MIPI CSI Pins in MX6D and MX6Q

CSI_D3P	MIPI
CSI_D3M	MIPI
CSI_D2P	MIPI
CSI_D2M	MIPI

13. References

i.MX 6Dual_6Quad Automotive and Infotainment Applications Processors Datasheet (REV A).pdf

i.MX 6Dual_6Quad Multimedia Applications Processor Reference Manual (REV B).pdf

iMX61_pins_integration_110226.xls

Rigel-pinmux.xlsx

IMX6SDLCEC_RevA.pdf

i.MX6SDLRM_RevA.pdf

14. Revision History

0summarizes revisions to this document since the release of the previous version (Rev. A).

Table 9 Migrating between MX6DQ, 6DL and 6S Rev.A		
Rev. Number	**Date**	**Substantive Changes**
Rev A	10/2011	Initial NDA release

Appendix A

NOTES

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