NXP Semiconductors
User's Guide

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Hardware Development Guide for the MIMXRT1010 Processor

Contents

Chapter 1
Introduction

This document guides hardware engineers to design and test their MIMXRT1010 processor-based designs. It provides information about board layout recommendations and design checklists to ensure first-pass success and avoid any board bring-up problems.

This guide is released with the relevant device-specific hardware documentation such as data sheets, reference manuals, and application notes available on www.nxp.com.

Chapter 2
Background

The MIMXRT1010 processors are the latest additions to the growing family of real-time processing products from NXP, offering high-performance processing optimized for lowest power consumption and best real-time response. The MIMXRT1010 processors feature advanced implementation of the Arm® Cortex®-M7 core, which operates at speeds of up to 500/400 MHz.

The MIMXRT1010 processors are useful for applications such as:

- Audio device
- Industrial control
- IoT node

Chapter 3
Power supply

See Table 1 for the power domains and power supply decoupling recommendations.

Table 1. Power domains

Power rail	MIN (V)	TYP (V)	MAX (V)	Description
VDD_SOC_IN	0.925	—	1.3[1]	Power for the core supply
VDD_HIGH_IN	3	3.3	3.6	VDD_HIGH_IN supply voltage
DCDC_IN	3	3.3	3.6	Power for the DCDC
VDD_SNVS_IN	2.4	3.0	3.6	Power for the SNVS and RTC
USB_OTG1_VBUS	4.4	5.0	5.5	Power for the USB VBUS
VDDA_ADC_3P3	3	3.3	3.6	Power for the 12-bit ADC
NVCC_GPIO	3	3.3	3.6	IO power for the GPIO

1. Max is 1.26 V for the industrial part numbers.

Table 2. Power supply decoupling recommendations

Power rail	Decoupling and bulk capacitors (min qty)	Description
VDD_SOC_IN	3 × 0.22 µF[2] + 1 × 4.7 µF[1]	Place at least one 4.7 µF capacitor and three 0.22 µF capacitors next to PIN 53, 77, 14, and so on.
VDD_HIGH_IN	1 × 0.22 µF[2] + 1 × 4.7 µF[1]	Place at least one 4.7 µF capacitor and one 0.22 µF capacitors next to PIN 39.
VDD_HIGH_CAP	1 × 0.22 µF[2] + 1 × 4.7 µF[1]	VDD_HIGH_CAP is restricted to the RT1010. loads.
DCDC_IN	1 × 0.22 µF[2] + 1 × 4.7 µF[1]	Place at least one 4.7 µF capacitor and one 0.22 µF capacitor next to PIN 18.
VDD_SNVS_IN	1 × 0.22 µF[2]	—
VDD_SNVS_CAP	1 × 0.22 µF[2] + 1 × 4.7 µF[1]	Select a small capacitor with a low ESR. Do not connect any loads to VDD_SNVS_CAP.
USB_OTG1_VBUS	1 × 1 µF[1]	10 V rated.
VDDA_ADC_3P3	1 × 0.22 µF[2] + 1 × 1 µF[1]	Place the bypass capacitors next to PIN 42.

Table continues on the next page...

Table 2. Power supply decoupling recommendations (continued)

Power rail	Decoupling and bulk capacitors (min qty)	Description
NVCC_GPIO	4 × 0.1 µF + 3 × 4.7 µF[1]	Place at least four 4.7 µF capacitor and four 0.22 µF capacitors next to PIN 7, 50, 63, 71.

1. For the 4.7-µF capacitors, use the 0402 package.

2. For the 0.22-µF capacitors, use the 0402 package.

3. For the 22-µF capacitors, the 0603 package is preferred; the 0805 and 1206 packages are acceptable.

Table 3. Power sequence and recommendations

Item	Recommendation	Description
Power sequence	Comply with the power-up/power-down sequence guidelines (as described in the data sheet) to guarantee a reliable operation of the device.	Any deviation from these sequences may result in these situations: • Excessive current during the power-up phase • Prevention of the device from booting • Irreversible damage to the processor (worst-case scenario)
SNVS domain signals	Do not overload the coin cell backup power rail VDD_SNVS_IN. These I/Os are associated with VDD_SNVS_IN (most inputs have on-chip pull resistors and do not require external resistors): • PMIC_ON_REQ—push-pull output • TEST_MODE—on-chip pull down	Concerning i.MX RT1010: • When VDD_SNVS_IN = VDD_HIGH_IN in the SNVS domain, the current is drawn from both equally. • When VDD_HIGH_IN > VDD_SNVS_IN, VDD_HIGH_IN supplies all the SNVS domain current and the current flows into VDD_SNVS_IN to charge the coin cell battery. • When VDD_SNVS_IN > VDD_HIGH_IN, • VDD_SNVS_IN supplies current to SNVS, and a small leakage current flows into VDD_HIGH_IN.
Power ripple	Maximum ripple voltage limitation.	The common limitation for the ripple noise shall be less than 5 % Vp-p of the supply voltage average value. The related power rails affected are VDD_xxx_IN and VDD_xxx_CAP.
VDD_SNVS_IN and VDD_HIGH_IN	If VDD_SNVS_IN is directly supplied by a coin cell battery, a Schottky diode is required between VDD_HIGH_IN and VDD_SNVS_IN. The cathode is connected to VDD_SNVS_IN. Alternately, VDD_HIGH_IN and VDD_SNVS_IN can be tied together if the real-time clock function is not needed during the system power-down.	When no power is supplied to VDD_SNVS_IN, the diode limits the voltage difference between the two on-chip SNVS power domains to approximately 0.3 V. The processor allows the current to flow between the two SNVS power domains, proportionally to the voltage difference.

Power-up sequence requirement:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- When internal DCDC is enabled, external delay circuit is required to delay the “DCDC_PSWITCH” signal at least 1 ms after DCDC_IN is stable.
- POR_B must be held low during the entire power-up sequence.

Power-down sequence requirement:

- VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off.

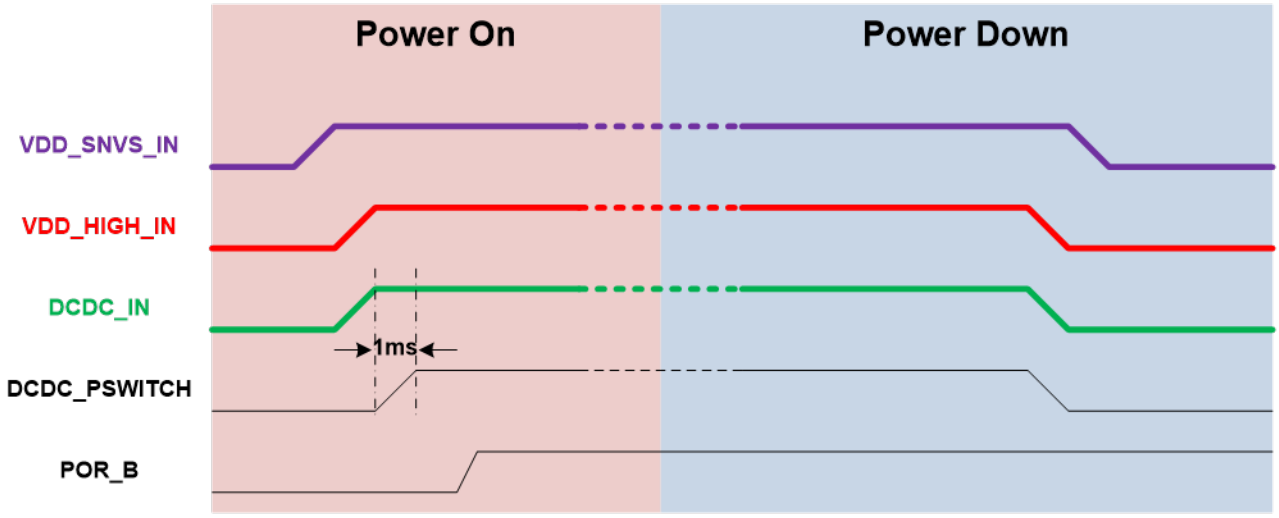

Figure 1. Power up and power down sequence

For RT1010-EVK, see Figure 2.

- First, it powers up SNVS
- PMIC_REQ_ON is then switched on to enable the external DC/DC to power up all other power domains.
- DCDC_PSWITCH is delayed more than 1 ms to switch on the internal DCDC.
- DCDC_OUT output powers the VDD_SOC_IN.
- The ON/OFF button is used to switch PMIC_REQ_ON on/off to control power modes.
- The RESET button and the WDOG output are used to reset the system power.

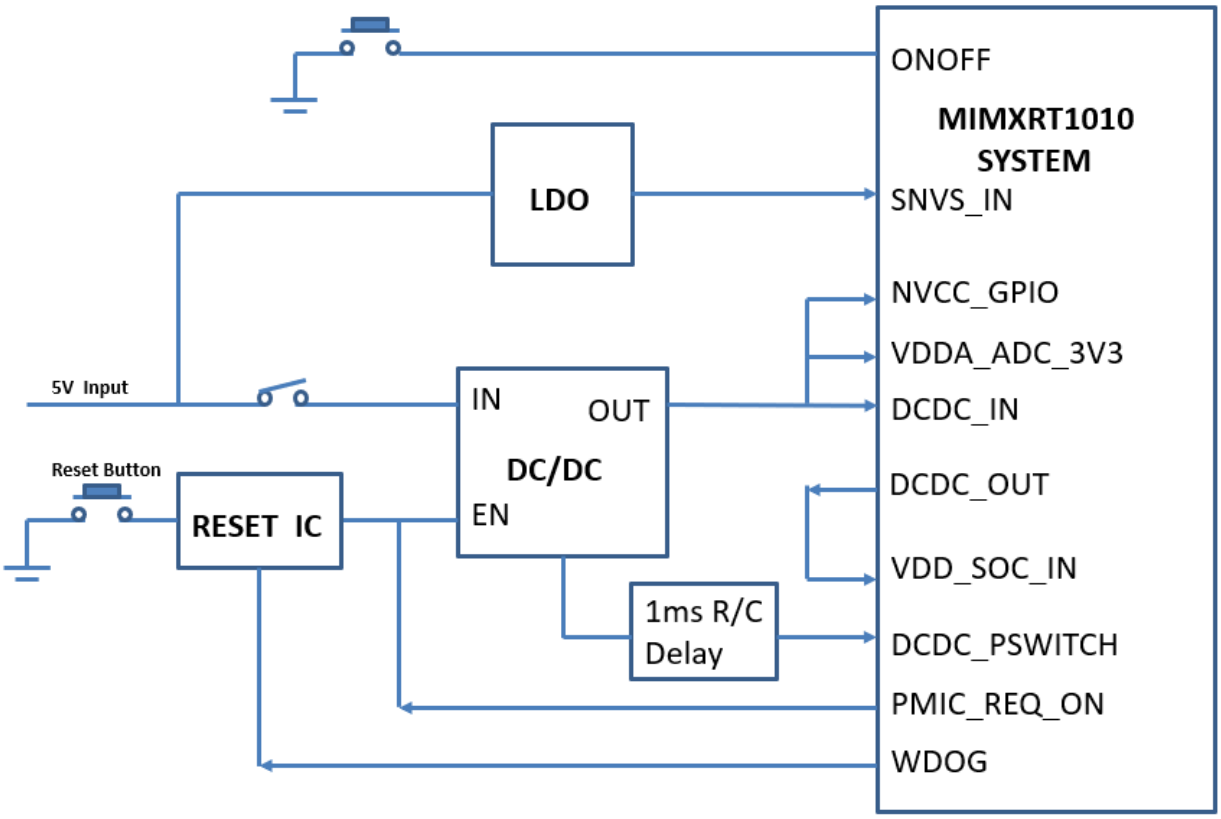

Figure 2. Power control diagram

The internal DC/DC switching frequency is about 1.5 MHz. The DC/DC requires external inductor and capacitors, the illustration is as below Figure 3, pay attention to below items:

- The recommended value for the external inductor is about 4.7μH ~10 μH, saturation current >1A, ESR < 0.2 Ohm.
- The external buck capacitor total is about 33 μF, this includes all the capacitors used on DCDC_OUT and VDD_SOC_IN.
- DCDC_PSWITCH should delay 1 ms regarding DCDC_IN to guarantee that DCDC_IN is stable before the DC/DC starts up.
- If you want to bypass internal DC/DC, you still must power DCDC_IN. DCDC_PSWITCH should be grounded to disable the DC/DC, and DCDC_LP should be left floating.
- Try to keep the DC/DC current loop as small as possible to avoid EMI issues.

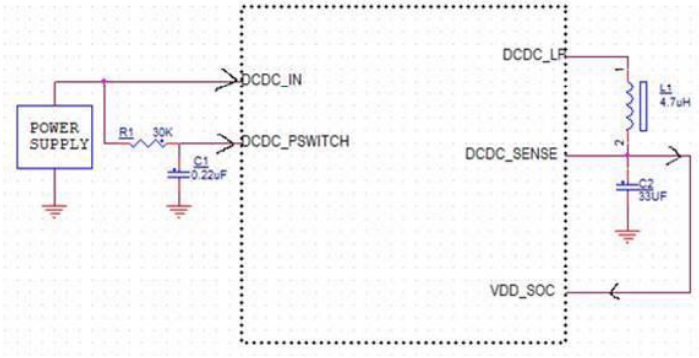

Figure 3. DC/DC function diagram

Chapter 4
Clocks

See Table 4 for the clock configuration. The 32.768 kHz and 24 MHz oscillators are used for the EVK

Design and it cannot be replaced with crystal with other frequency.

Table 4. Clock configurations

Signal name	Recommended connections	Description
RTC_XTALI/RTC_XTALO	For the precision 32.768 kHz oscillator, connect a crystal between RTC_XTALI and RTC_XTALO. Choose a crystal with a maximum ESR (Equivalent Series Resistance) of 100 k and follow the recommendation from manufacturer for the loading capacitance. Do not use an external biasing resistor because the bias circuit is on the chip.	To hit the exact oscillation frequency, the board capacitors must be reduced to account for the board and chip parasitic. The integrated oscillation amplifier is self-biasing, but relatively weak. Care must be taken to limit the parasitic leakage from RTC_XTALI and RTC_XTALO to either the power or the ground (>100 M). This de-bias the amplifier and reduces the start-up margin.
	For the external kHz source (if feeding an external clock into the device), RTC_XTALI can be driven DC-coupled with RTC_XTALO floating or driven by a complimentary signal.	If you want to feed an external low-frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The logic level of this forcing clock must not exceed the VDD_SNVS_CAP level and the frequency shall be <100 kHz under the typical conditions.
	An on-chip loose-tolerance ring oscillator of approximately 40 kHz is available. If RTC_XTALI is tied to GND and RTC_XTALO is floating, the on-chip oscillator is engaged automatically.	When a high-accuracy real-time clock is not required, the system may use the on-chip 40 kHz oscillator. The tolerance is ±50 %. The ring oscillator starts faster than the external crystal and is used until the external crystal reaches a stable oscillation. The ring oscillator also starts automatically if no clock is detected at RTC_XTALI at any time.

Table continues on the next page...

Table 4. Clock configurations (continued)

Signal name	Recommended connections	Description
XTALI/XTALO	For the precision 24 MHz oscillator, connect a fundamental-mode crystal between XTALI and XTALO. A typical 80 ESR crystal rated for a maximum drive level of 250 µW is acceptable. Alternately, a typical 50 ESR crystal rated for a maximum drive level of 200 µW may be used.	A 24.0 MHz crystal should be connected between XTALI and XTALO. External load capacitance value depends on the typical load capacitance of crystal used and PCB design. The crystal must be rated for a maximum drive level of 250 uW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. NXP SDK software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI mounted with 18 pF capacitor. The logic level of this forcing clock cannot exceed NVCC_PLL level. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details. If driving the chip with an external clock source, then a 24 MHz oscillator can be driven in one of three configurations using a nominal 1.1 V source. • A single ended external clock source can be used to overdrive the output of the amplifier (XTALO). Since the oscillation sensing amplifier is differential, the XTALI pin should be externally floating and capacitively loaded. The combination of the internal biasing resistor and the external capacitor will filter the signal applied to the XTALO pin and develop a rough reference for the sensing amplifier to compare. • A single ended external clock source can be used to drive XTALI. In this configuration, XTALO should be left externally floating. • A differential external clock source can be used to drive both XTALI and XTALO. Generally, second configuration is anticipated to be the most used configuration, but all three configurations may be utilized.

Chapter 5
Debugging and programming

See Table 5 for the JTAG interface summary and recommendation. The RT1010 EVK also features an OpenSDA, which makes it easier to debug without an external debugger.

NOTE

For RT1010 silicon, it defaults to SWD mode instead of JTAG.

Table 5. JTAG interface summary

JTAG signals	I/O type	On-chip termination	External termination
JTAG_TCK	Input	47 kΩ pull-up	Not required; can use 10 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up	Not required; can use 10 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up	Not required; can use 10 kΩ pull-up
JTAG_TDO	3-state output	No pull-up/pull-down	Do not use pull-up or pull-down
JTAG_TRSTB	Input	47 kΩ pull-up	Not required; can use 10 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up	Use 4.7 kΩ pull-down or tie to GND

Table 6. JTAG recommendation

Signals	Recommendation	Description
JTAG_TDO	Do not add external pull-up or pull-down resistors on JTAG_TDO.	JTAG_TDO is configured with an on-chip keeper circuit, such that the floating condition is actively eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental. See Table 5 for a summary of the JTAG interface.
ALL JTAG Signals	Ensure that the on-chip pull-up/pull-down configuration is followed if external resistors are used with the JTAG signals (except for JTAG_TDO). For example, do not use an external pull-down on an input that has an on-chip pull-up.	External resistors can be used with all JTAG signals except for JTAG_TDO, but they are not required. See Table 5 for a summary of the JTAG interface.
JTAG_MOD	JTAG_MOD is called SJC_MOD in some documents. Both names refer to the same signal. JTAG_MOD shall be externally connected to GND for normal operation in a system. The termination to GND through an external pull down resistor is allowed. Use a 4.7-kΩ resistor.	When JTAG_MOD is low, the JTAG interface is configured for a common software debug, adding all the system TAPs to the chain. When JTAG_MOD is high, the JTAG interface is configured to a mode compliant with the IEEE 1149.1 standard.

Table 7. OpenSDA recommendation

Signals	Recommendation	Description
SWD_DIO	Connect to the LPC4322 signal through a buffer	The OpenSDA in the EVK board is implemented as a debugger, which eliminates the cost for the users.
SWD_CLK	Connect to the LPC4322 signal through a buffer	
UART_TXD/UART_RXD	Connect to the LPC4322 signal through a buffer	The UART signals connected to LPC4322 realize a virtual COM port for the OpenSDA USB for debugging.

Table 8. Flashloader peripheral I/Os

Signals	Recommendation	Description
UART1	The Serial Downloader provides a means to download a program image to the chip over the USB and UART serial connections. In this mode, ROM programs WDOG1 for a timeout specified by the fuse WDOG Time-out Select (See the Fuse map chapter for details) if the WDOG_ENABLE eFuse is 1 and continuously polls for the USB and UART connection. If no activity is found on USB OTG1 and UART 1/2 and the watchdog timer expires, the Arm core is reset.	The ROM code first polls the UART1 signals from TXD1/RXD1. Add a 10-kΩ pull-up resistor to the TXD1/RXD1 pins to avoid an invalid trigger of the UART port in the serial download mode.
USB1		If there is no polling activity from UART1 in the serial download mode, the ROM code acts as an HID device for PC downloading.

Chapter 6
Boot, reset, and miscellaneous

See Table 9 for the boot, reset, and miscellaneous configurations, such as ON/OFF, TEST_MODE, NC pins, and other.

Table 9. Boot configuration

Item	Recommendation	Description
BOOT_CFG[2:0]	The BOOT_CFG signals are required for a proper functionality and operation and shall not be left floating during development if BOOT_CFG fuses and BT_FUSE_SEL are not configured.	See the “System Boot” chapter in your chip reference manual for the correct boot configuration. Note that an incorrect setting may result in an improper boot sequence.
BOOT_MODE[1:0]	For BOOT_MODE1 and BOOT_MODE0, use one of these options to achieve logic 0: • Tie to GND through any-value external resistor • Tie directly to GND. For logic 1, use one of these options: • Tie directly to the NVCC_GPIO_XX rail. • Tie to the NVCC_GPIO_XX rail through an external 10 kΩ resistor. A value of 4.7 kΩ is preferred for high-noise environments. If a switch control is desired, no external pull-down resistors are necessary. Simply connect the SPST switches directly to the NVCC_GPIO_XX rail.	BOOT_MODE1 and BOOT_MODE0 each has on-chip pull-down devices with a nominal value of 100 kΩ, a projected minimum of 60 kΩ, and a projected maximum of 140 kΩ. When the on-chip fuses determine the boot configuration, both boot mode inputs can be disconnected.
BOOT _CFG and B OOT _ MODE signals with FlexSPI_B signals	To reduce incorrect boot-up mode selections, do one of the following: • Use the FlexSPI_B interface lines only as processes or outputs. Ensure that the FlexSPI_B interface lines are not loaded down (such that the level is interpreted as low during the power-up) when the intent is to be at a high level, or the other way around. • If the FlexSPI_B boot signal must be configured as an input, isolate the SEMC signal from the target driving source with an analog switch and apply the logic value with a second analog switch. Alternately, the peripheral devices with 3-state outputs may be used. Ensure that the output is high-impedance.	Using the FlexSPI_B interface lines as inputs may result in a wrong boot because of the source overcoming the pull resistor value. A peripheral device may require the FlexSPI_B signal to have an external or on-chip resistor to minimize signal floating. If the usage of the FlexSPI_B signal affects the peripheral device, then an analog switch, an open collector buffer, or an equivalent shall isolate the path. A pull-up or pull-down resistor at the peripheral device may be required to maintain the desired logic level. See the switch or device data sheet for the operating specifications.

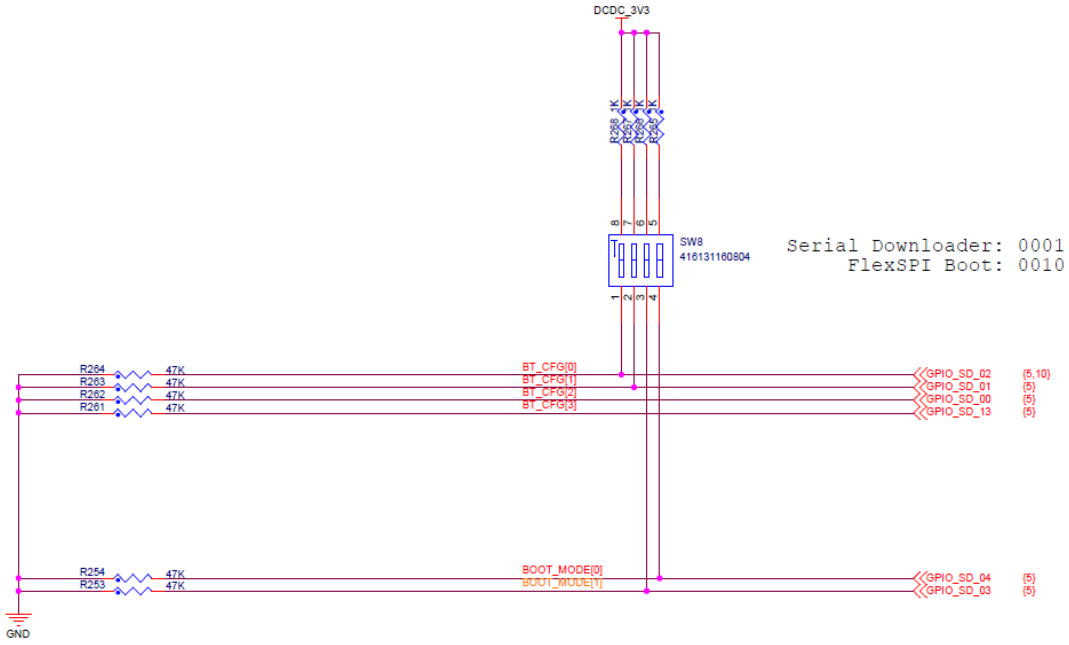

Figure 4. Boot mode setting

Table 10. Reset and miscellaneous recommendations

Item	Recommendation	Description
POR_B	If the external POR_B signal is used to control the processor POR, then POR_B must be immediately asserted at the power-up. and remain asserted until the VDD_HIGH_CAP and VDD_SNVS_CAP supplies are stable. VDD_SOC_IN may be applied in either order with no restrictions. In the absence of an external reset feeding the SRC_POR_B input, the internal POR module takes control.	See the “System Boot” chapter in your chip reference manual for the correct boot configuration. An incorrect setting may result from an improper boot sequence. POR_B signal has internal 100 K pull up to SNVS domain, should pull up to VDD_SNVS_IN if must add external pull-up resistor, otherwise it causes additional leakage during SNVS mode. It is recommended to add the external reset IC to the circuit to guarantee POR_B is properly processed during power up/down, refer to the EVK design for details. **Note**: As the Low DCDC_IN detection threshold is 2.6 V, the reset IC's reset threshold must be higher than 2.6 V, then the whole chip is reset before the internal DCDC module reset to guarantee the chip safety during power-down. For power-on reset, on any conditions ones must make sure the voltage on DCDC_PSWITCH PIN is below 0.5 V before power-up.
ON/OFF	For portable applications, the ON/OFF input may be connected to the ON/OFF SPST push button. The on-chip de-bouncing is provided, and this input has an on-chip pullup. If not used, ON/OFF can be a no-connect. A 4.7-kΩ to 10-kΩ series resistor can be used when the current drain is critical.	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF. Both boot mode inputs can be disconnected.
TEST_MODE	The TEST_MODE input is internally connected to an on-chip pull-down device. You may either float this signal or tie it to GND.	This input is reserved for NXP manufacturing use.
GPANAIO	GPANAIO must be a no-connect.	This output is reserved for NXP manufacturing use.
NC pin	The NC contacts are no-connected and shall float.	Depending on the feature set, some versions of ICs may have the NC contacts connected inside the LQFP.

Table 11. ROM Bootloader Peripheral PinMux

BT Device	IO Function	ALT	PAD
UART1	lpuart1.TX	0	GPIO_10
	lpuart1.RX	0	GPIO_09
	lpuart1.CTS_B	6	GPIO_08
	lpuart1.RTS_B	6	GPIO_07
FlexSPI	flexspi.B_DATA[3]	0	GPIO_SD_04
	flexspi.B_DATA[2]	0	GPIO_SD_02
	flexspi.B_DATA[1]	0	GPIO_SD_01
	flexspi.B_DATA[0]	0	GPIO_SD_03
	flexspi.B_SCLK	0	GPIO_SD_13
	flexspi.B_DQS	0	GPIO_00
	flexspi.B_SS0_B	0	GPIO_SD_00
	flexspi.A_DQS	0	GPIO_SD_12
	flexspi.A_SS0_B	0	GPIO_SD_06
	flexspi.A_SS1_B	0	GPIO_SD_05
	flexspi.A_SCLK	0	GPIO_SD_10
	flexspi.A_DATA[0]	0	GPIO_SD_09
	flexspi.A_DATA[1]	0	GPIO_SD_07
	flexspi.A_DATA[2]	0	GPIO_SD_08
	flexspi.A_DATA[3]	0	GPIO_SD_11
FlexSPI RESET	gpio*mux*.IO[*13*]	5	GPIO_13

Chapter 7
Layout recommendations

- Stackup
- Placement of bulk and decoupling capacitors"
- USB
- High-speed signal routing recommendations

7.1 Stackup

A high-speed design requires a good stackup to have the right impedance for the critical traces.

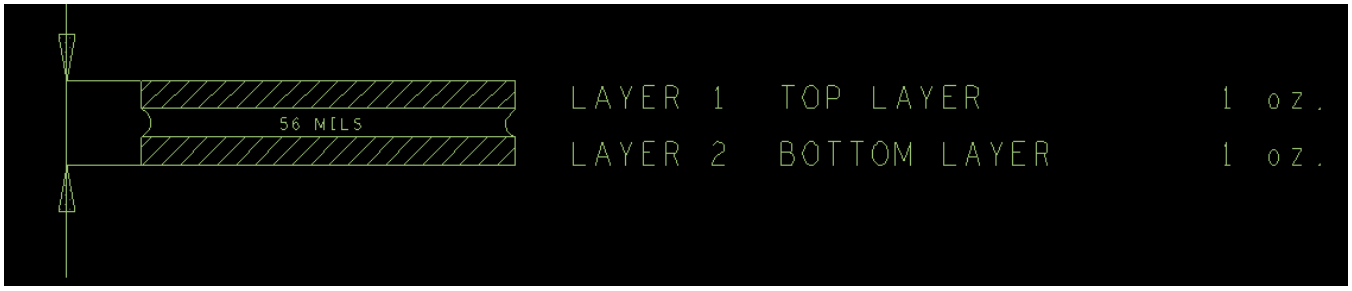

Figure 5. RT1010-EVK stackup

The constraints for the trace width depend on many factors, such as the board stackup and the associated dielectric and copper thickness, required impedance, and required current (for power traces).

The stackup also determines the constraints for routing and spacing. Consider the following when designing the stackup and selecting the material for your board:

- The board stackup is critical for the high-speed signal quality.
- Plan the impedance of the critical traces.
- The high-speed signals must have reference planes on adjacent layers to minimize crosstalk.
- The NXP reference design equals Isola FR4.
- The NXP validation boards equal Isola FR4.
- The recommended stackup is two layers, with the layer stack shown in Figure 5.

The left-hand image shows the detail provided by NXP inside the fabrication detail as a part of the Gerber files. The right-hand side shows that the solution suggested by the PCB fabrication company for the requirements. Figure 6 shows the RT1010-EVK PCB stackup implementation:

Layers	Single Ended		Differential			Differential		
	Trace Width (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)
L1	5.00	50	4.2	6.00	100	4.70	5.00	90
L2	5.00	50				4.70	5.00	90

Figure 6. RT1010-EVK stackup implementation

7.2 Placement of bulk and decoupling capacitors

Place the small decoupling capacitors and the larger bulk capacitors on the bottom side of the CPU. The 0402 decoupling capacitors and the 0603 bulk capacitors must be placed as close as possible to the power balls. Placing the decoupling capacitors close to the power pins is critical to minimize inductance and ensure the high-speed transient current demand of the processor. The correct via size, trace width, and trace space are critical to preserve the adequate routing space. The recommended geometry is as follows:

- Via type is 18/8 mils, the trace width is 5 mils, and the trace space is 7 mils.
- Use the NXP design strategy for power and decoupling.

7.3 USB

Use these recommendations for the USB:

- Route the high-speed clocks and the DP and DM differential pair first.
- Route the DP and DM signals on the top (or bottom) layer of the board.
- The trace width and spacing of the DP and DM signals must meet the differential impedance requirement of 90 Ω.
- Route the traces over the continuous planes (power and ground):
  - They must not pass over any power/GND plane slots or anti-etch.
  - When placing the connectors, make sure that the ground plane clear-outs around each pin have ground continuity between all pins.
- Maintain the parallelism (skew-matched) between DP and DM, and match the overall differential length difference to fewer than 5 mils.
- Maintain the symmetric routing for each differential pair.
- Do not route the DP and DM traces under the oscillators or parallel to the clock traces (and/or data buses).
- Minimize the lengths of the high-speed signals that run parallel to the DP and DM pair.
- Keep the DP and DM traces as short as possible.
- Route the DP and DM signals with a minimum number of corners. Use 45 degrees turns instead of 90 degrees turns.
- Avoid layer changes (vias) on the DP and DM signals. Do not create stubs or branches.
- Provide the ground return vias within a 50 mil distance from the signal layer-transition vias when transitioning between different reference ground planes.

7.4 FlexSPI

FlexSPI is a flexible SPI (Serial Peripheral Interface) host controller which supports two SPI channels and up to 4 external devices. Each channel supports Single/Dual/Quad/ Octal mode data transfer (1/2/4/8 bidirectional data lines). FlexSPI is the most commonly used external memory.

- Internal dummy read strobe and loopbacked internally(MCR0[RXCLKSRC]==0)

  Supporting legacy device with zero device output hold time.

  Saving one pad(DQS pad).

  Supporting low frequency clock for boot up usage.
- Internal dummy read strobe and loopbacked from DQS pad(MCR0[RXCLKSRC]==1)

  Supporting higher frequency than mode "MCR0[RXCLKSRC]==0".

  Supporting device doesn't provide read strobe.

- Flash provided read strobe(MCR0[RXCLKSRC]==3)

  Supporting the highest frequency.

  Supporting device provides read strobe.

7.5 High-speed signal routing recommendations

The following list provides recommendations for routing the traces for high-speed signals. The propagation delay and the impedance control must match to have a correct communication with the devices.

- The high-speed signals (SDRAM, USB, SD card) must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in the reference planes. Review the via voids to ensure that they do not create splits (space out vias).
- Provide the ground return vias within a 100 mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- A solid GND plane must be directly under the crystal-associated components, and traces.
- The clocks or strobes that are on the same layer need at least 2.5× spacing from the adjacent traces (2.5× height from the reference plane) to reduce crosstalk.
- Provide the ground return vias within a 100 mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- All synchronous modules must have the bus length matching and relative clock length control.

Chapter 8
Two-layer board design

8.1 MCU pinout

Form design phase, RT1010 pinout is adjusted properly to meet two-layer board design especially for some high-speed signals. For example, signals like USB must route at same length and do not across with each other, see Figure 7. RT1010-EVK signals for reference.

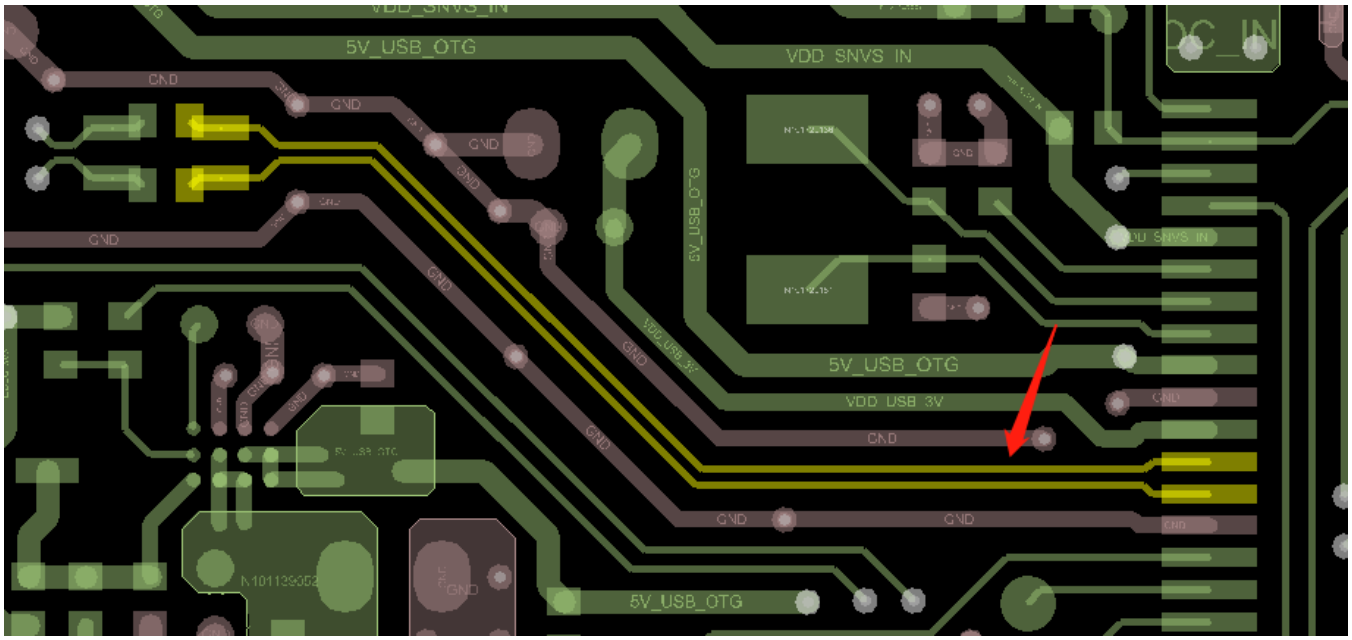

Figure 7. RT1010-EVK USB signals

8.2 Power supply

RT1010 power supply is designed with two-layer board, almost each power domain will have GND pad in parallel, see Figure 8. With such power pin design, it is easier for placing decoupling capacitor to the board.

At the same time, it needs to keep the bottom layer of MCU to have a somehow overall GND plane and make sure the board has a good current loop to the external power supply to improve the EMC performance, see Figure 9.

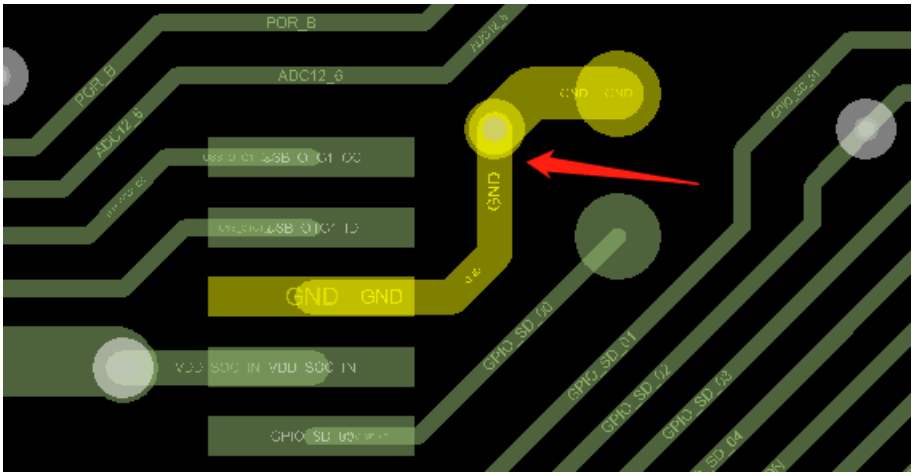

Figure 8. RT1010-EVK MCU power

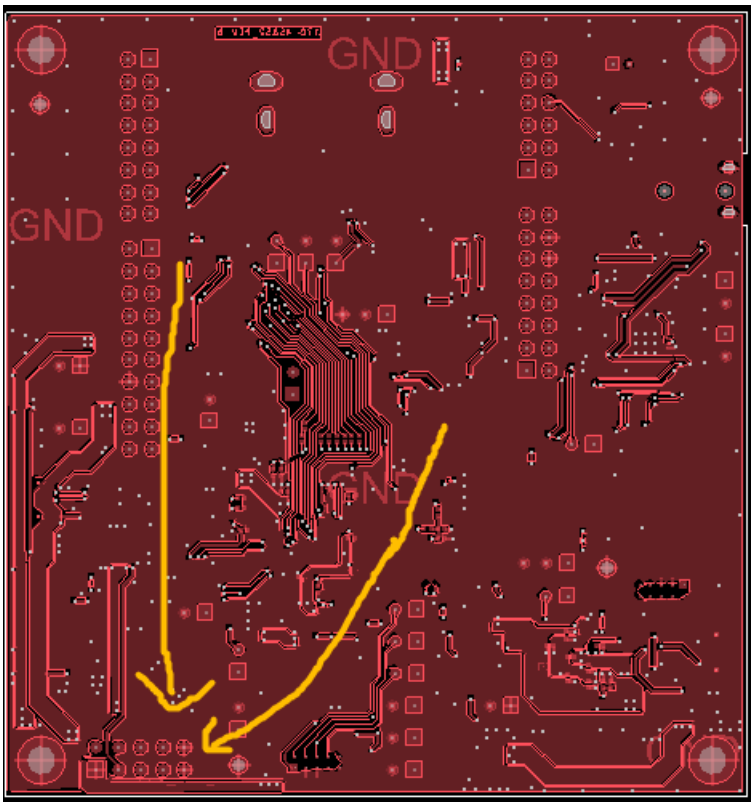

Figure 9. RT1010-EVK GND plane

8.3 Routing rule

There are some general high-speed layout guidelines which mentioned above. For two-layer board design, it is better to have each high-speed signal with GND in parallel helps impedance matching and improve the signal quality. For reference, see Figure 10.

For two-layer board design, make sure that at least one layer has a good GND plane (normally bottom layer), which means it must route most of the signals at the top layer. For reference, see Figure 11.

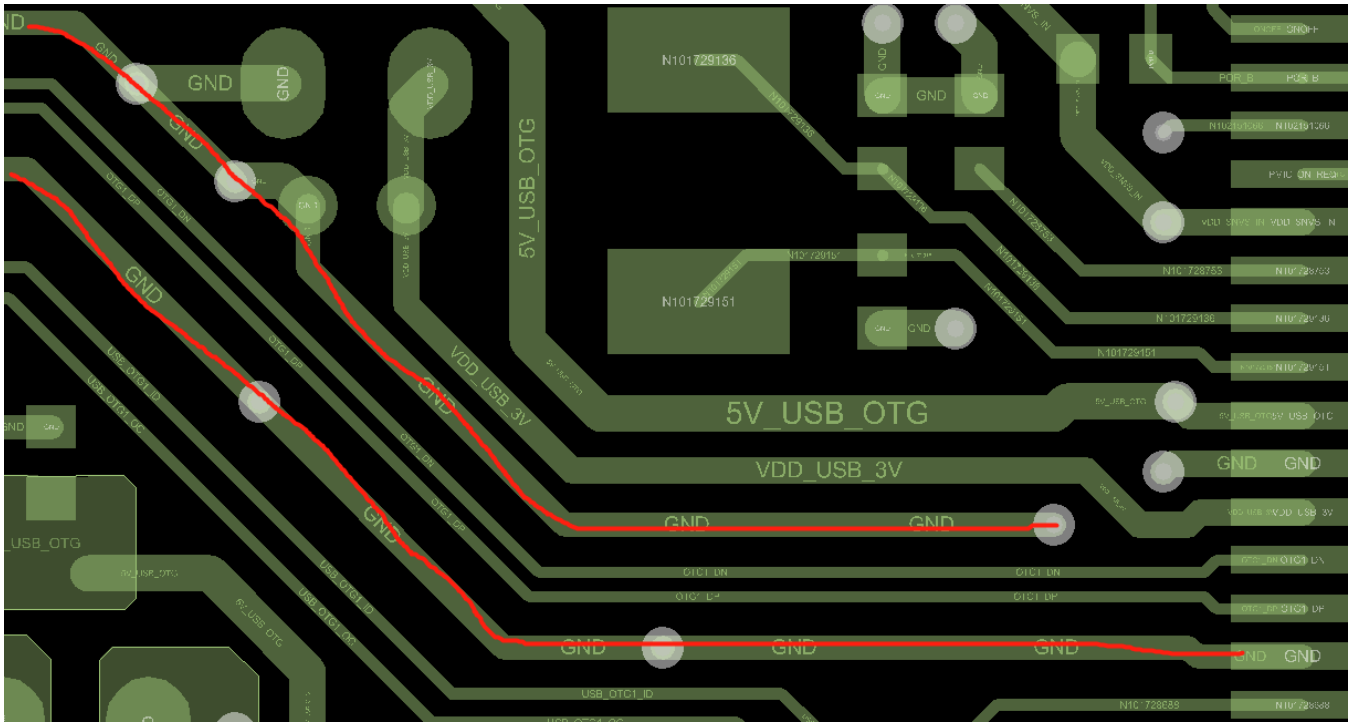

Figure 10. RT1010-EVK high speed signals

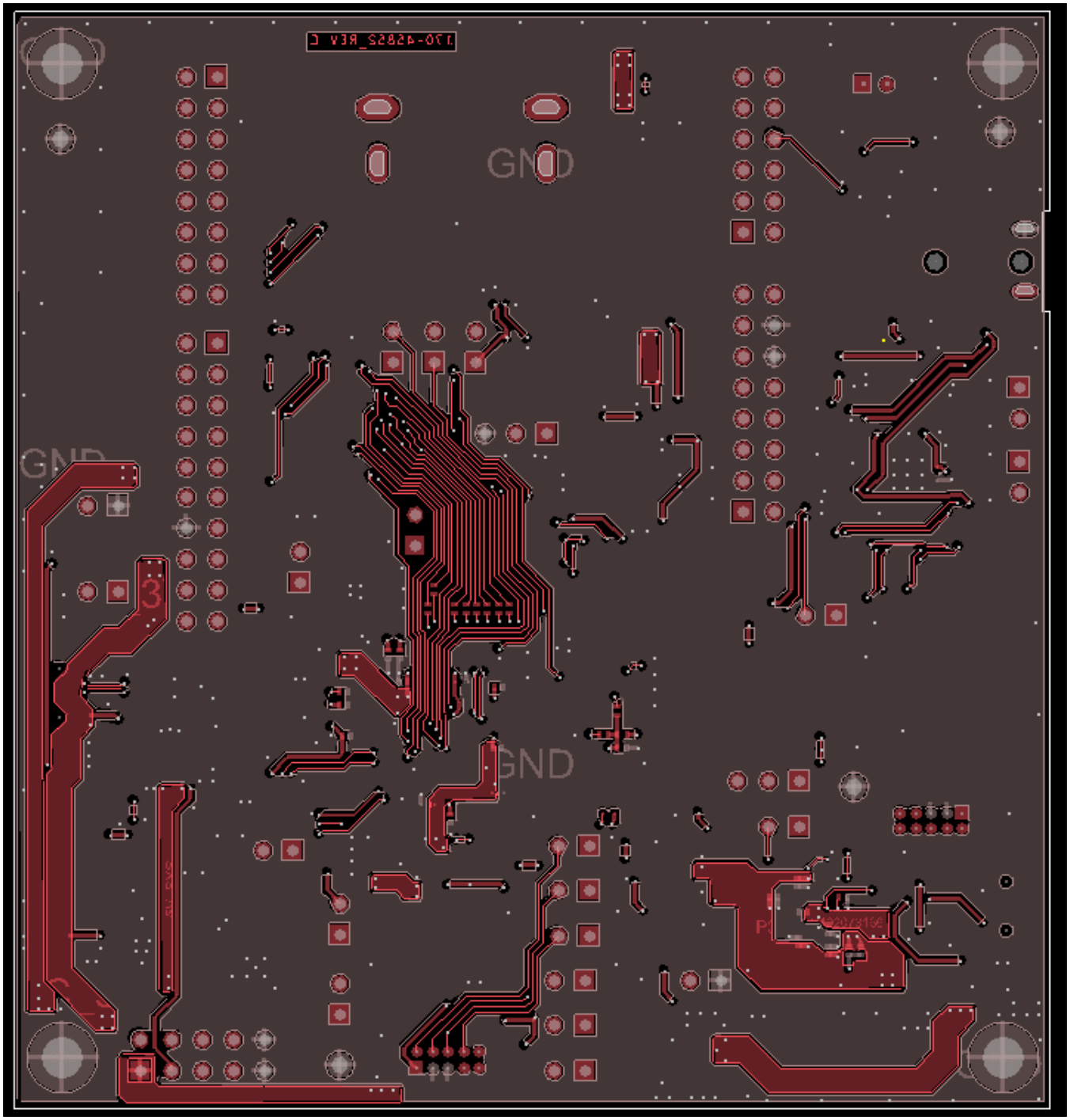

Figure 11. RT1010-EVK bottom layer

Chapter 9
Revision history

Table 12 summarizes the changes done to this document since the initial release.

Table 12. Revision history

Revision number	Date	Substantive changes
0	09/2019	Initial release

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