Summary of Results

Test Statistics	
Failed	3
Passed	3
Total	6

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	RootComplex Tests, Unit Interval (2.5 GT/s)	400.0110 ps	45.4 %	399.8800 ps <= VALUE <= 400.1200 ps
✗	1	1	RootComplex Tests, Template Tests (2.5 GT/s)	Fail	**-100.0 %**	VALUE = 0.000
✓	0	1	RootComplex Tests, Median to Max Jitter (2.5 GT/s)	12.79 ps	83.4 %	VALUE <= 77.00 ps
✓	0	1	RootComplex Tests, Eye-Width (2.5 GT/s)	379.91 ps	54.4 %	VALUE >= 246.00 ps
✗	1	1	RootComplex Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s)	1.2451 V	**-4.9 %**	274.0 mV <= VALUE <= 1.2000 V
✗	1	1	RootComplex Tests, Peak Differential Output Voltage (Non Transition) (2.5 GT/s)	1.3069 V	**-11.3 %**	253.0 mV <= VALUE <= 1.2000 V

Report Detail

Next

✓RootComplex Tests, Unit Interval (2.5 GT/s)

Reference: This test is not required. It is informative only.

Test Summary: Pass | Test Description: A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.

Pass Limits: [399.8800 ps to 400.1200 ps] | **Mean UI (PCIE1.1, RootComplex, 2.5GT/s)** 400.0110 ps

Result Details

DataLane Lane0 | **Note:** Non-SSC Limits Used: 2.5E9 +/-300ppm | **#3500 UI Blocks Measured** 996.469 k | **Min UI** 399.9850 ps | **Max UI** 400.0460 ps | **Mean UI** 400.0110 ps | **Worst Case Data Rate** 2.499712533059 Gbits/sec | **Mean Data Rate** 2.499931251891 Gbits/sec

Next

✗RootComplex Tests, Template Tests (2.5 GT/s)

Reference: PCI Express CEM Specification, Rev 1.1, Section 4.7.3, Figure 4-10

Test Summary: **FAIL** | Test Description: System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.3 of the PCI Express Card Electromechanical (CEM) Specification, Rev 1.1, as measured after the connector with an ideal load.

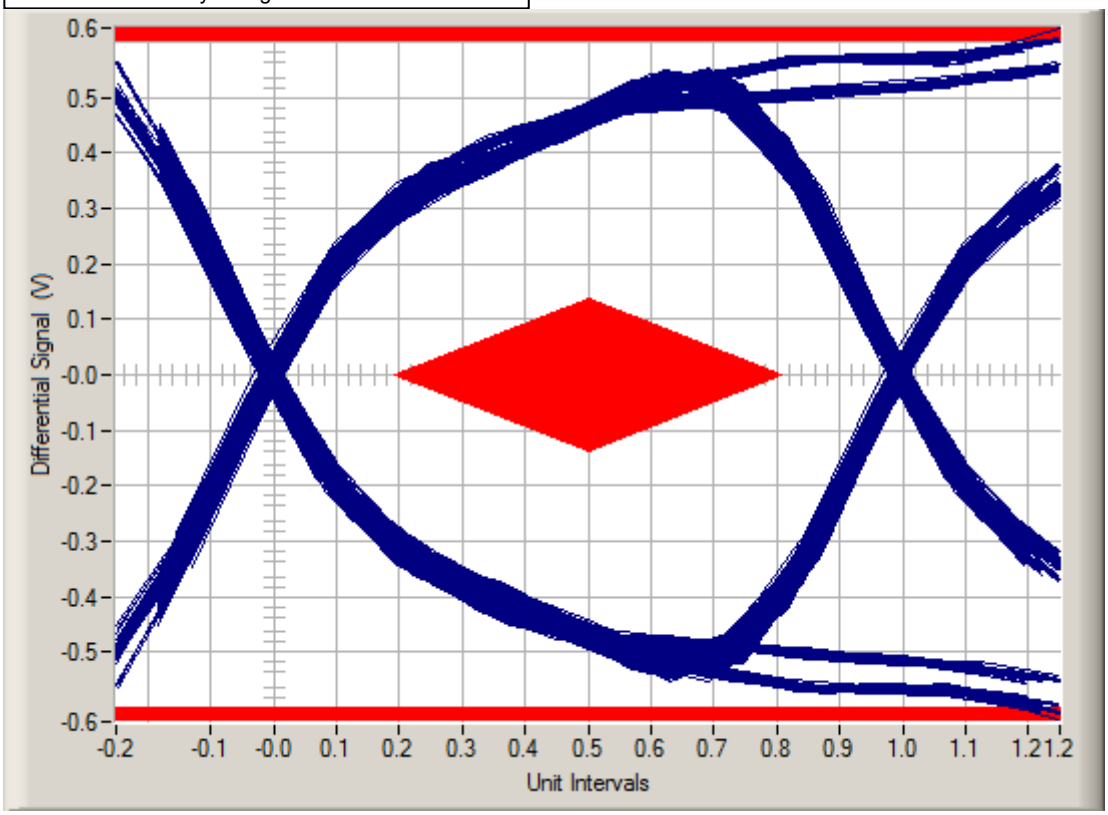
Pass Limits: = 0.000 | **Total # Failures (PCIE1.1, 2.5GT/s, RootComplex)** Fail

Result Details

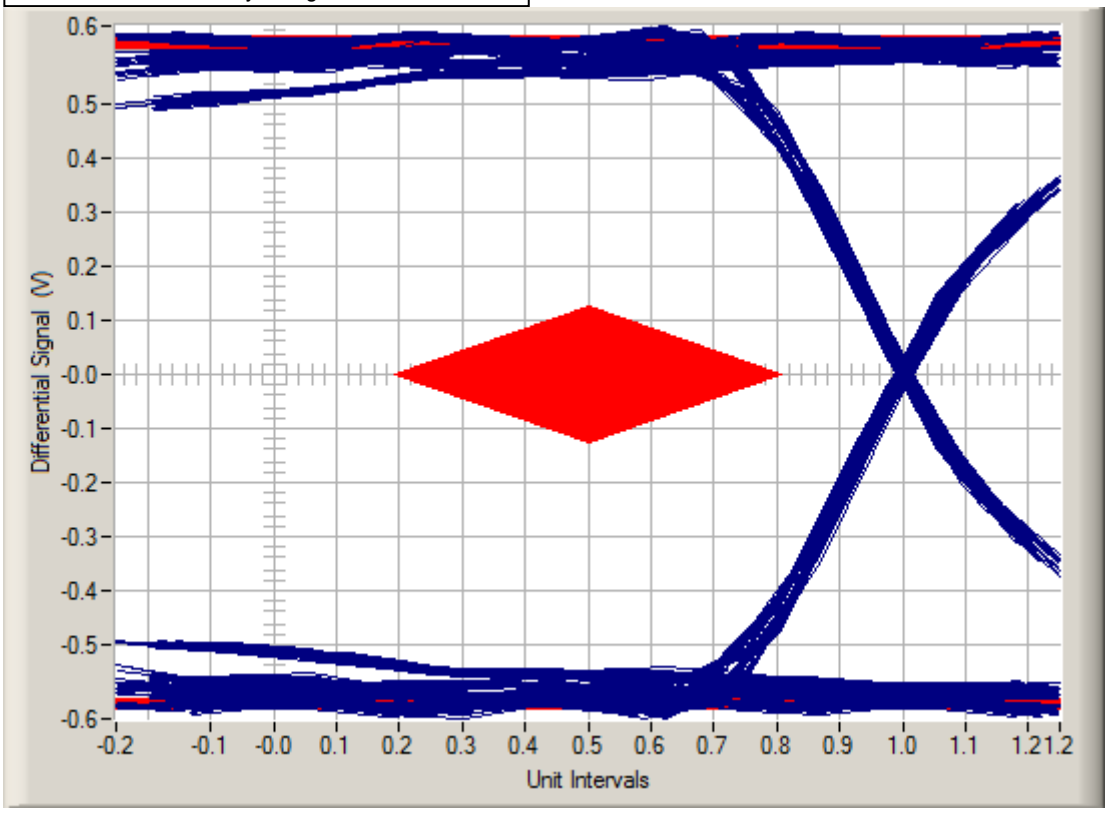
Transition Eye Diagram (See image) | **Non-Transition Eye Diagram** (See image) | **Total #UI Measured** 1.000000000 M | **Reference Clock** Not Clean or SSC | **Transition Min Voltage** -621.8 mV | **Transition Max Voltage** 623.2 mV | **Transition Eye Top Margin Value** 270 mV | **Transition Eye Top Margin** -3.87 % | **Transition Eye Bottom Margin Value** -270 mV | **Transition Eye Bottom Margin** -3.64 % | **Non Transition Min Voltage** -650.8 mV | **Non Transition Max Voltage** 656.1 mV | **Non Transition Eye Top Margin Value** 410 mV | **Non Transition Eye Top Margin** -9.35 % | **Non Transition Eye Bottom Margin Value** -400 mV | **Non Transition Eye Bottom Margin** -8.47 % | **Transition Minimum Eye Height** 815.1 mV | **Non Transition Minimum Eye Height** 1.0666 V | **DataLane** Lane0 | **Connection Type** Channel 1,Channel 3 - Direct Connect | **Selected SigTest Version** 3.2.0.3 | **Requested Sample Rate (GSa/s)** 20

Trial 1

Trial 1: Transition Eye Diagram



Trial 1: Non-Transition Eye Diagram



Next

✓RootComplex Tests, Median to Max Jitter (2.5 GT/s)

Reference: PCI Express CEM Specification, Rev 1.1, Table 4-9

Test Summary: Pass | Test Description: This test measures the maximum time between the jitter median and maximum deviation from the median.

Pass Limits: <= 77.00 ps | **Median-to-Max Jitter (PCIE1.1, RootComplex)** 12.79 ps

Result Details

DataLane Lane0	**Connection Type** Channel 1,Channel 3 - Direct Connect	**Selected SigTest Version** 3.2.0.3

Next

✓RootComplex Tests, Eye-Width (2.5 GT/s)

Reference: PCI Express CEM Specification, Rev 1.1, Table 4-9

Test Summary: Pass | Test Description: This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].

Pass Limits: >= 246.00 ps | **Eye-Width (PCIE1.1, RootComplex, 2.5GT/s)** 379.91 ps

Result Details

DataLane Lane0 | **Connection Type** Channel 1,Channel 3 - Direct Connect | **Selected SigTest Version** 3.2.0.3

Next

✗RootComplex Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s)

Reference: PCI Express CEM Specification, Rev 3.0, Section 4.8.7, Table 4-16

Test Summary: **FAIL** | Test Description: This test verifies that the Differential Peak Differential Output Voltage for transition bits is within the allowed range.

Pass Limits: [274.0 mV to 1.2000 V] | **PeakVoltage (G1.1, RootComplex, 2.5GT/s, Transition)** 1.2451 V

Result Details

Total #UI Measured 1.000000000 M | **Largest Transition Amplitude (Outer eye)** 623.2 mV

Smallest Transition Amplitude (Inner eye) -621.8 mV | **DataLane** Lane0 | **Connection Type** Channel 1,Channel 3 - Direct Connect

Selected SigTest Version 3.2.0.3

Next

✗RootComplex Tests, Peak Differential Output Voltage (Non Transition)(2.5 GT/s)

Reference: PCI Express CEM Specification, Rev 3.0, Section 4.8.7, Table 4-16

Test Summary: **FAIL** | Test Description: This test verifies that the Differential Peak Differential Output Voltage for non transition bits is within the allowed range.

Pass Limits: [253.0 mV to 1.2000 V] | **PeakVoltage (G2, RootComplex, 2.5GT/s, Non-Transition)** 1.3069 V

Result Details

Total #UI Measured 1.000000000 M | **Largest Non Transition Amplitude (Outer eye)** (no value)

Smallest Non Transition Amplitude (Inner eye) (no value) | **DataLane** Lane0 | **Connection Type** Channel 1,Channel 3 - Direct Connect

Selected SigTest Version 3.2.0.3