## Swapping CTS and RTS functions

3 🗄 :		5 5 7	2 P type	filter text						
Pin	Pin name	Label	Identifier	GPIO	UART ^	EIM	USDHC	CSI	MMDC	^
C5	NAND_CE0_B			gpio4_1013	uart3_RX[]	eim_DTACK_B	usdhc1_DAT			
H16	UART3_RX_D			gpio1_1025	uart3_RX[]			csi_DATA0		
A3	NAND_READ			gpio4_1012	uart3_TX[]	eim_CS1_B	usdhc1_DAT			
H17	UART3_TX_D			gpio1_1024	uart3_TX[]			csi_DATA1		
D9	LCD_HSYNC			gpio3_102	uart4_CTS_B[					
E17	ENET1_RX_D			gpio2_101	uart4_CTS_B[		usdhc2_LCTL	csi_DATA17		
C9	LCD_VSYNC			gpio3_103	uart4_RTS_B[					
F16	ENET1_RX_D			gpio2_100	uart4_RTS_B[		usdhc1_LCTL	csi_DATA16		
B8	LCD_ENABLE			gpio3_IO1	uart4_RX[]	eim_CS3_B				
G16	UART4_RX_D	1		gpio1_1029	uart4_RX[]			csi_DATA13		
<b>A</b> 8	LCD_CLK			gpio3_100	uart4_TX[]	eim_CS2_B				
G17	UART4_TX_D			gpio1_1028	uart4_TX[]			csi_DATA12		
E1	CSI_DATA03			gpio4_1024	uart5_CTS_B[	eim_AD3	usdhc2_DAT	csi_DATA5		
E15	ENET1_TX_D			gpio2_103	uart5_CTS_B[		usdhc2_VSEL	csi_DATA19		
M15	GPIO1_IO09			gpio1_109	uart5_CTS_B[		usdhc2_RESE	csi_HSYNC		
E2	CSI_DATA02			gpio4_1023	uart5_RTS_B[	eim_AD2	usdhc2_DAT	csi_DATA4		
E16	ENET1_RX_EN			gpio2_102	uart5_RTS_B[		usdhc1_VSEL	csi_DATA18		
N17	GPIO1_IO08			gpio1_108	uart5_RTS_B[		usdhc2_VSEL	csi_VSYNC		
E3	CSI_DATA01			gpio4_1022	uart5_RX[]	eim_AD1	usdhc2_DAT	csi_DATA3		
G13	UART5_RX_D			gpio1_1031	uart5_RX[]			csi_DATA15		

	Routing	Details
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Pins Signals & type filter text

#	Peripheral	Signal	Ar	Routed	Label	Identifier	Power gr	Direction	Software	Hysteres	Pull Up /	Pu
A8	UART4	uart_rx	<-	[A8] LC		n/a	NVCC_L	Input	Input Pa	CMOS in	100K Oh	Ke
DO	LIADTA	uart ty		[B8] LC		n/a	NVCC_L	Output	Input Pa	CMOS in	100K Oh	Ke
C9	UART4	uart_cts_b	->	[C9] LC,		n/a	NVCC_L	Output	Input Pa	CMOS in	100K Oh	Ke
D9	UART4	uart_rts_b	<-	[D9]								

Pin	Pin name	Label	Identifier	GPIO	UART	EIM	USDHC	CSI	MMDC	^
C5	NAND_CE0_B			gpio4_1013	uart3_RX[]	eim_DTACK_B	usdhc1_DAT			
H16	UART3_RX_D			gpio1_1025	uart3_RX[]			csi_DATA0		
A3	NAND_READ			gpio4_1012	uart3_TX[]	eim_CS1_B	usdhc1_DAT			
H17	UART3_TX_D			gpio1_IO24	uart3_TX[]			csi_DATA1		
<b>D</b> 9	LCD_HSYNC			gpio3_102	uart4_CTS_B[					
E17	ENET1_RX_D			gpio2_101	uart4_CTS_B[		usdhc2_LCTL	csi_DATA17		
✓C9	LCD_VSYNC			gpio3_103	uart4_RTS_B[					
F16	ENET1_RX_D			gpio2_100	uart4_RTS_B[		usdhc1_LCTL	csi_DATA16		
<mark>⊻</mark> 88	LCD_ENABLE			gpio3_101	uart4_RX[]	eim_CS3_B				
G16	UART4_RX_D			gpio1_1029	uart4_RX[]	1		csi_DATA13		
▲ A8	LCD_CLK			gpio3_100	uart4_TX[]	eim_CS2_B				
G17	UART4_TX_D			gpio1_IO28	uart4_TX[]			csi_DATA12		
E1	CSI_DATA03			gpio4_1024	uart5_CTS_B[	eim_AD3	usdhc2_DAT	csi_DATA5		
E15	ENET1_TX_D			gpio2_103	uart5_CTS_B[		usdhc2_VSEL	csi_DATA19		
M15	GPIO1_IO09			gpio1_109	uart5_CTS_B[		usdhc2_RESE	csi_HSYNC		
E2	CSI_DATA02			gpio4_1023	uart5_RTS_B[	eim_AD2	usdhc2_DAT	csi_DATA4		
E16	ENET1_RX_EN			gpio2_102	uart5_RTS_B[		usdhc1_VSEL	csi_DATA18		
N17	GPIO1_IO08			gpio1_IO8	uart5_RTS_B[		usdhc2_VSEL	csi_VSYNC		
E3	CSI_DATA01			gpio4_1022	uart5_RX[]	eim_AD1	usdhc2_DAT	csi_DATA3		
G13	UART5_RX_D			gpio1_1031	uart5_RX[]			csi_DATA15		~
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## Routing Details

Pins Sig	nals 🔎 type f	ilter text										
Routing D	Details for BOA	RD 4	0	3 ~ ~								
#	Peripheral	Signal	Ar	Routed	Label	Identifier	Power gr	Direction	Software	Hysteres	Pull Up /	Pull / I
A8	UART4	uart_rx	<-	[A8] LC		n/a	NVCC_L	Input	Input Pa	CMOS in	100K Oh	Keepe
bo	UAITH	uart_tx	->	[B8] LC		n/a	NVCC_L	Output	Input Pa	CMOS in	100K Oh	Keepe
D9	UART4	uart_cts_b	->	[D9] LC		n/a	NVCC_L	Output	Input Pa	CMOS in	100K Oh	Keepe
C9	UART4	uart_rts_b	<-	[C9] LC		n/a	NVCC_L	Input	Input Pa	CMOS in	100K Oh	Кеере