Comments on Thales i.MX8QXP power consumption questions (20201127):

Here are some comments on the questions:

1) No use case only changes the number of active cores, so current/core cannot be isolated (too many variables are changing). Moreover, "CoreMark only" results are confusing: VCC_CPU draws 447 mA when 4 cores are active whereas datasheet rather shows about 2500 mA for VDD_A35... I understand the app note was done at room temperature, but were are talking about a ~5.5 factor...

[Leo] The maximum supply currents in Table 11 are used to setup the potential inrush current limits for the companion regulator (PMIC) so that the system can startup and run stably and safely. It is not for the actual use cases power consumption. The power rails for the 4 A35 cores is VDD_A35 which is powered from VCC_CPU on the EVK board.

As it has described in AN12338, under KS2 use case, only one A35 is enabled in idle and the VCC_CPU consumption current is around 36mA.

4.1.3. KS2 – System idle

The use case is as follows:

- Linux is idle mostly waiting for interrupt.
- 1 CPU powered, no GPU powered.
- Screen is off so no significant I/O to DDR is occurring

Table 4. KS2 system idle with no screens — 25°C

Supply domain	Voltage (V)	L4.14.78 GA	
		I (mA)	P (mW)
VCC_CPU	1.00	36.27	36.27
VCC_MAIN	1.02	478.93	488.51
VCC_GPU	1.10	6.94	7.64
VCC_DDRIO	1.10	93.43	103.98
VCC_SCU_1V8	1.79	25.08	45.00
Total SoC	—	—	681.4
VCC_1V8	1.81	62.11	112.90
VCC_3V3	3.28	17.50	57.42
Total SoC W/ IOs+Peripheral	—	—	851.72

Under Kanzi only use case, 4 A35 cores are enabled, but no workload is executing on them, it looks like A35 cores in idle mode, the VCC_CPU consumption current is around 142mA (36mA x 4 = 144mA). The consumption current of 4 A35 cores is around 4 times of one A35 core (36mA).

4.2.2. Kanzi performance analyzer only

Kanzi Performance Analyzer (KPA) is a Human Machine Interface (HMI) benchmarking tool from RightWare.

It is primarily focused on automotive Human Machine Interfaces such as Cluster, Heads up Displays, Infotainment screens but is an excellent tool for measuring the performance and power consumption for any generic HMI tool.

Kanzi Performance Analyzer is available from Rightware (www.rightware.com)

In this use case only KPA is running on the GPU. No workloads are executing on the main Cortex A cores (or any other IP block). This emulates a heavy GPU-specific use case and associated power consumption.

Table 7. Kanzi only — 25 °C

Supply domain	Voltage (V)	L4.14.78 GA	
		I (mA)	P (mW)
VCC_CPU	1.10	141.70	155.86
VCC_MAIN	1.02	937.31	956.06
VCC_GPU	1.10	404.65	445.11
VCC_DDRIO	1.10	413.08	454.39
VCC_SCU_1V8	1.80	27.24	48.96
Total SoC	—	—	2060.38
VCC_1V8	1.83	113.64	208.10
VCC_3V3	3.28	16.29	53.42
Total SoC W/ IOs+Peripheral	—	—	2321.92

Under CoreMark only use case, 4 A35 cores are enabled and run in full workload and maximum performance, the VCC_CPU consumption current is around 447mA. Thus, the estimated consumption current for one A35 core in full workload and maximum performance is around 112mA (447mA / 4 = 112mA). If customers have doubt on it, they can just enable one A35 core and run CoreMark to measure the actual consumption current on VCC_CPU by referring to AN12338 on how to do that.

4.2.1. CoreMark only

CoreMark is a modern, sophisticated benchmark that lets you accurately measure processor performance and is intended to replace the older Dhrystone benchmark. Arm recommends using CoreMark in preference to Dhrystone.

Coremark is built with 4 threads, and running 1 instance of Coremark will fill up all 4 cores.

- CPU frequency is set to maximum value
- DDR frequency is set to 1200 MHz

Table 6 show the measurement results when this use case is applied on the i.MX 8QuadXPlus processor.

Table 6. CoreMark only — 25 °C

Supply domain	Voltage (V)	L4.14.78 GA	
		I (mA)	P (mW)
VCC_CPU	1.10	447.18	491.90
VCC_MAIN	1.02	477.14	486.68
VCC_GPU	1.10	7.25	7.99
VCC_DDRIO	1.11	93.82	104.40
VCC_SCU_1V8	1.79	25.10	45.05
Total SoC	—	—	1136.02
VCC_1V8	1.82	62.43	113.44
VCC_3V3	3.28	16.33	53.56
Total SoC W/ IOs+Peripheral	—	—	1303.01

2) No test case enables the DSP. Current per rail is not provided for VPU tests.

[Leo] Both HiFi4 DSP and VPU are powered from VCC_MAIN. Both HiFi4 DSP and VPU are powered from VCC_MAIN. Both HiiFi4 DSP and VPU are not enabled under all use cases in AN12338. NXP does not have Instance code for HiFi4 DSP application, customers have to run their own code on the HiFi4 DSP to measure the increasing current on VCC_MAIN.

3) No test case disables the User Cortex-M4.

[Leo] The User Cortex-M4 is powered from VCC_MAIN and it is not enabled under all use cases in AN12338. Normally, it will cause around 10mA creasing of consumption current on VCC_MAIN if the User Cortex-M4 is enabled and run at 264MHz.

4) Maybe the app note answers: what are the supply voltages associated with the Display Controller and Imaging Subsystem (MIPI DSI/LVDS/CSI, Parallel Capture, MJPEG) ?

My concern is that if I simply multiply the supplies operating voltage ranges with the maximum currents found in the datasheet, the power consumption goes over 10W even without a GPU! I would like to know how much I can save by disabling the User M4 core, 1xA35 core, the Imaging subsystem, Display Controller, VPU, DSP and Audio DMA subsystem.

[Leo] The estimated power consumption under this condition is roughly same as the one under CoreMark only (1303mW) minus 3 A35 cores power consumption in full workload and maximum performance (1.10V x 112mA x 3 = 369.6mW). That is (1301mW – 369.6mW = 933.4mW).

Table 6. CoreMark only — 25 °C

Supply domain	Voltage (V)	L4.14.78 GA	
		I (mA)	P (mW)
VCC_CPU	1.10	447.18	491.90
VCC_MAIN	1.02	477.14	486.68
VCC_GPU	1.10	7.25	7.99
VCC_DDRIO	1.11	93.82	104.40
VCC_SCU_1V8	1.79	25.10	45.05
Total SoC	—	—	1136.02
VCC_1V8	1.82	62.43	113.44
VCC_3V3	3.28	16.33	53.56
Total SoC W/ IOs+Peripheral	—	—	1303.01